μPD5753T7G

SiGe/CMOS Integrated Circuit
4 × 2 IF Switch Matrix with Tone/Voltage Controller

R09DS0014EJ0100
Rev.1.00
Feb 22, 2011

FEATURES

- 4 independent IF channels, integral switching to channel input to either channel output
- 4 × 2 switch matrix with integrated switch control - Tone/Voltage
  - Switch's Enable/Disable function is linked with POLA input voltage level
- Switch's Enable condition : V_{POLA} > 9.5 V
- Frequency range : f = 250 MHz to 2150 MHz
- High isolation : $ISL_{D/U}$ = 33 dB TYP. @Worst mode
- Insertion loss : L_{INS} = 7 dB TYP. @ $Z_S = Z_L$ = 50 Ω
- Insertion loss flatness : ΔL_{INS} = 1.0 dB TYP.
- 20-pin 4 × 4 mm square micro lead package (20-pin plastic QFN (0.5 mm pitch))

APPLICATIONS

- DBS IF switching
- Multiswitch, Switch box
- 4 × 2 switching application for microwave signal

ORDERING INFORMATION

Part Number	Order Number	Package	Marking	Supplying Form
μPD5753T7G-E1	μPD5753T7G-E1-A	20-pin plastic QFN (0.5 mm pitch) (Pb-Free)	D5753	• Embossed tape 12 mm wide • Pin 6 to 10 face the perforation side of the tape • Qty 5 kpcs/reel • Dry packing specification (MSL 3 Equivalent)

Remark To order evaluation samples, please contact your nearby sales office.
Part number for sample order: μPD5753T7G

CAUTION

Observe precautions when handling because these devices are sensitive to electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	+4.0	V
Logic mode Control Voltage (MO and M1)	V_{MO}, V_{M1}	+4.0	V
Power Dissipation Note	P_D	325	mW
Storage Temperature	T_{stg}	–55 to +125	°C
Operating Ambient Temperature	T_A	–40 to +85	°C
Input Power	P_{in}	+15	dBm
POLA Control Input Voltage (POLA1 and POLA2)	V_{POLA}	+25	V
TONE Signal Input Voltage	V_{TONE}	1	V_{p-p}

Note: Mounted on double-sided copper-clad 50 × 50 × 0.51 mm laminates PWB, T_A = +85°C

RECOMMENDED OPERATING RANGE (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}	+3.0	+3.3	+3.6	V
Operating Ambient Temperature	T_A	–40	+25	+85	°C
POLA Control Input Voltage	V_{POLA}	0	–	21	V
TONE Signal Frequency	f_{TONE}	18	22	26	kHz
TONE Signal Input Voltage	V_{TONE}	0.4	0.6	0.8	V_{p-p}

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{DD} = +3.3 V, Z_S = Z_L = 50 Ω for each port, Worst mode, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current	I_{DD}	Non–RF, Non control Signal/Voltage	–	1.9	3.0	mA
Insertion Loss 1	$L_{INS}1$	P_{in} = 0 dBm, f = 0.95 GHz	–	6.5	8.5	dB
Insertion Loss 2	$L_{INS}2$	P_{in} = 0 dBm, f = 2.15 GHz	–	7.5	9.5	dB
Isolation D/U Ratio 2 Note	$ISL_{D/U}2$	P_{in} = 0 dBm, f = 2.15 GHz	28	33	–	dB
Output Return Loss 1	$RL_{out}1$	P_{in} = 0 dBm, f = 0.95 GHz	15	25	–	dB
Output Return Loss 2	$RL_{out}2$	P_{in} = 0 dBm, f = 2.15 GHz	10	13	–	dB
POLA Control Threshold Voltage, Channel Selection	V_{th_POLA}	OFF to ON	14	14.75	15.5	V
TONE Signal Threshold Voltage, Channel Selection	V_{th_TONE}	f_{TONE} = 22 kHz, Duty Cycle = 50%, pulse wave, OFF to ON	0.1	0.15	0.35	V_{p-p}

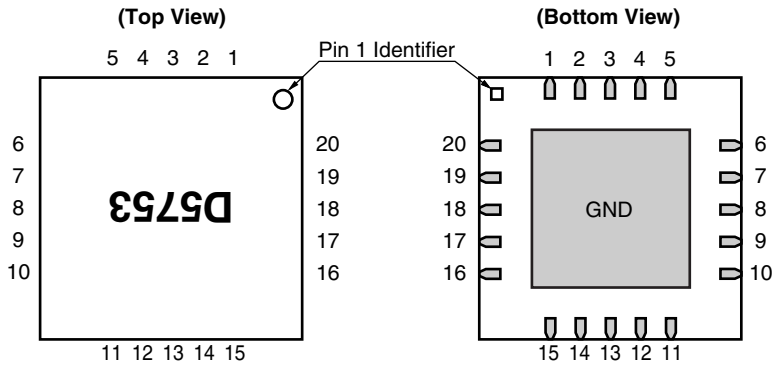
Note: Isolation D/U (Desire/Un-desire) ratio = |(Signal Leakage (off-state)) – (Insertion loss (on-state))| at Worst mode

STANDARD CHARACTERISTICS FOR REFERENCE (T_A = +25°C, V_{DD} = +3.3 V, Z_S = Z_L = 50 Ω for each port, Worst mode, unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference Value	Unit
Insertion Loss Flatness	ΔL_{INS}	$\lvert L_{INS}1-L_{INS}2\rvert$	1.0	dB
Isolation D/U Ratio 1 Note	$ISL_{D/U}1$	P_{in} = 0 dBm, f = 0.95 GHz	40	dB
Input Return Loss 1	$RL_{in}1$	P_{in} = 0 dBm, f = 0.95 GHz	20	dB
Input Return Loss 2	$RL_{in}2$	P_{in} = 0 dBm, f = 2.15 GHz	14	dB
POLA Control Current	I_{POLA}	V_{POLA} = 21 V	230	μA
POLA Switching Time	T_{POLA}	V_{POLA} = 18 V, OFF to ON	0.75	μs
TONE Switching Time	T_{TONE}	f_{TONE} = 22 kHz, Duty Cycle = 50%, pulse wave, V_{TONE} = 600 mV_{p-p}, OFF to ON	220	μs

Note: Isolation D/U (Desire/Un-desire) ratio = |(Signal Leakage (off-state)) – (Insertion loss (on-state))| at Worst mode

PIN CONNECTIONS



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TONE1	6	IN-B	11	GND	16	OUT2
2	POLA1	7	GND	12	IN-C	17	M1
3	GND	8	GND	13	GND	18	V_{DD}
4	IN-A	9	GND	14	POLA2	19	M0
5	GND	10	IN-D	15	TONE2	20	OUT1

Remark Heat Sink (Bottom side) : GND

TRUTH TABLE

SWITCHING CONTROL OF OUT1 SIGNAL PATH

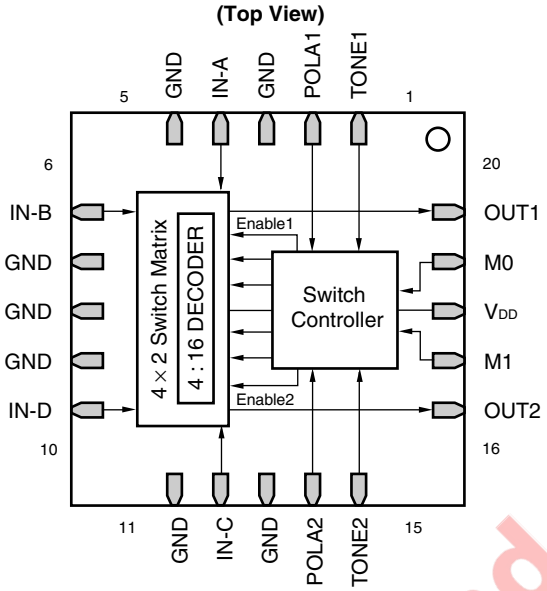
Logic Pattern Select		CONTROL PINS for OUT1		OUT1
M0	M1	POLA1	TONE1	Output Signal
0	0	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-C
		Low	0	IN-D
		High	0	IN-B
		High	22 kHz	IN-A
1	1	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-A
		Low	0	IN-B
		High	0	IN-D
		High	22 kHz	IN-C
0	1	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-D
		Low	0	IN-C
		High	0	IN-B
		High	22 kHz	IN-A
1	0	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-B
		Low	0	IN-A
		High	0	IN-D
		High	22 kHz	IN-C

SWITCHING CONTROL OF OUT2 SIGNAL PATH

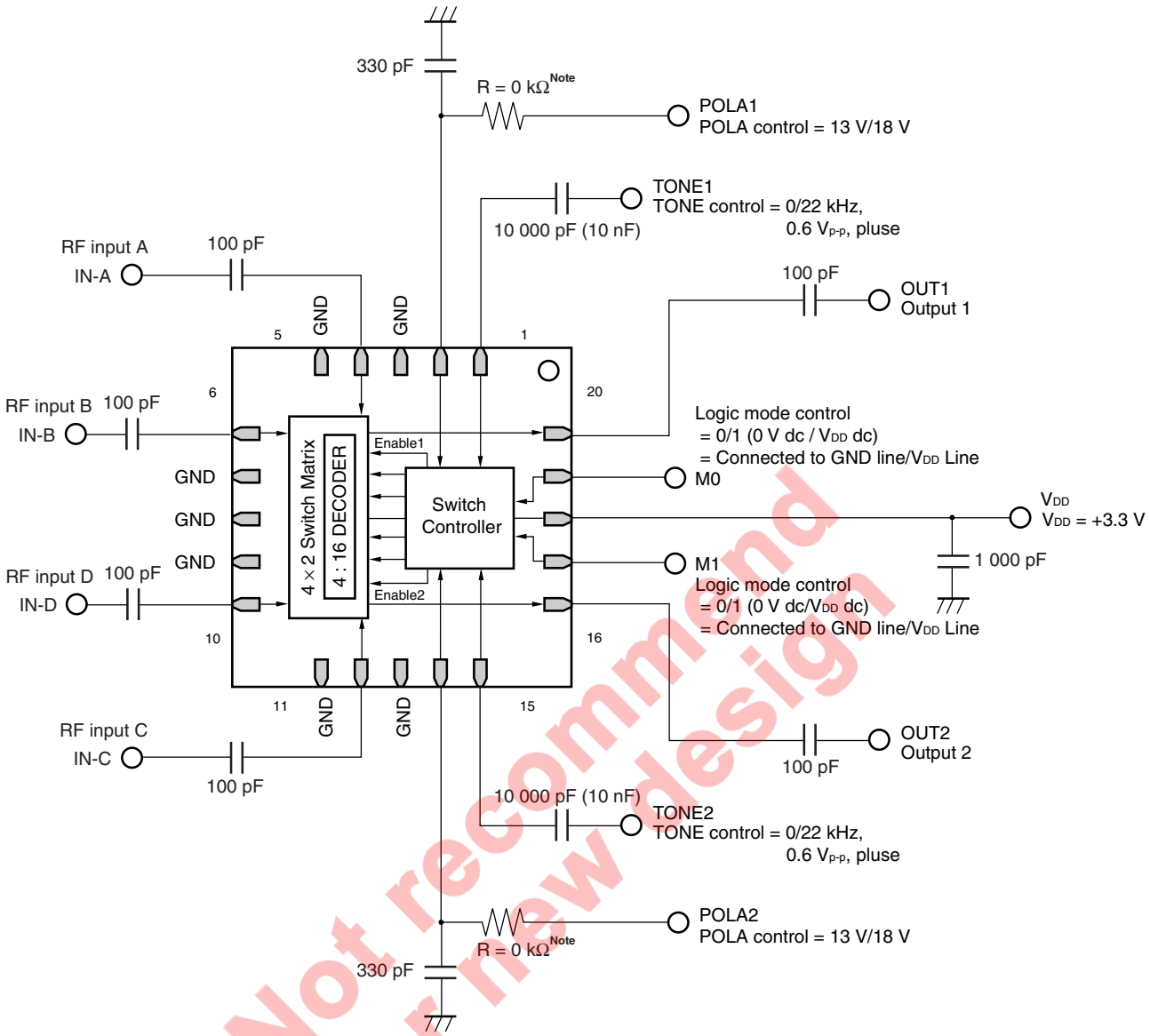
Logic Pattern Select		CONTROL PINS for OUT2		OUT2
M0	M1	POLA2	TONE2	Output Signal
0	0	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-C
		Low	0	IN-D
		High	0	IN-B
		High	22 kHz	IN-A
1	1	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-A
		Low	0	IN-B
		High	0	IN-D
		High	22 kHz	IN-C
0	1	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-D
		Low	0	IN-C
		High	0	IN-B
		High	22 kHz	IN-A
1	0	No Voltage	22 kHz	None
		No Voltage	0	None
		Low	22 kHz	IN-B
		Low	0	IN-A
		High	0	IN-D
		High	22 kHz	IN-C

Remarks M0, M1 : "0" : 0 V dc (Connected to GND line)
"1" : V_{DD} dc (Connected to V_{DD} line)
V_{DD} = + 3.3 V dc
POLA1, 2 : "Low" : 9.5 V to 14 V dc
"High" : 15.5 V to 19 V dc
"No Voltage" : 0 V dc (< 5 V dc) or Open
Switch's Enable/Disable function is linked with POLA input voltage level
Switch's Enable condition : V_{POLA} > 9.5 V

FUNCTIONAL DIAGRAM



EVALUATION CIRCUIT



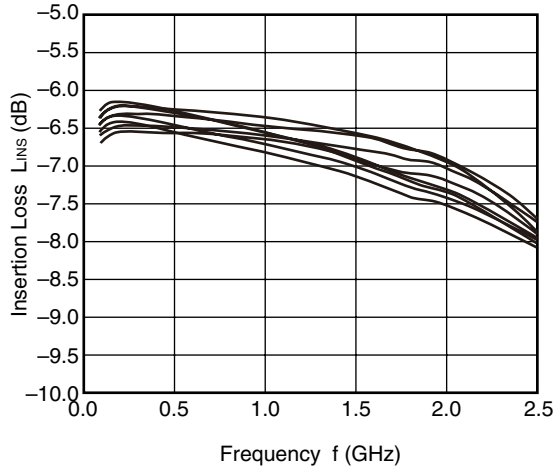
Note: R = 0 kΩ (at POLA control = 13 V/18 V)
= 5.6 kΩ (at POLA control = 14 V/18 V)

Remarks Heat Sink (Bottom Side): GND
$Z_S = Z_L = 50\ \Omega$
Switch's Enable/Disable function is linked with POLA input voltage level
Switch's Enable condition : $V_{POLA} > 9.5$ V

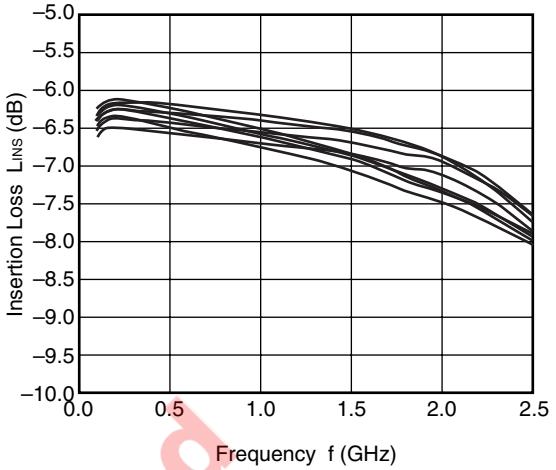
The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

TYPICAL CHARACTERISTICS
(T_A = +25°C, V_{DD} = +3.3 V, P_{in} = 0 dBm, Z_S = Z_L = 50 Ω for each port, unless otherwise specified)

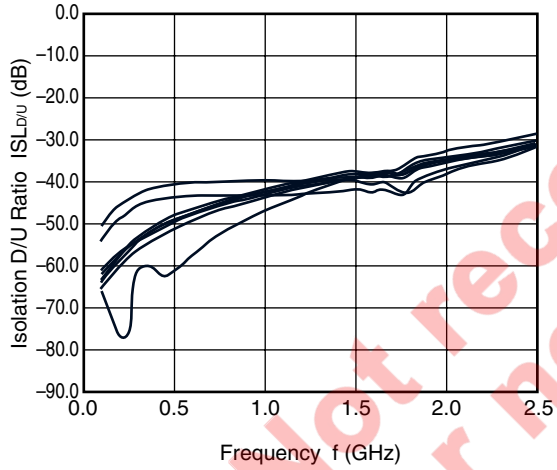
INSERTION LOSS vs. FREQUENCY
(IN-x - OUT1)



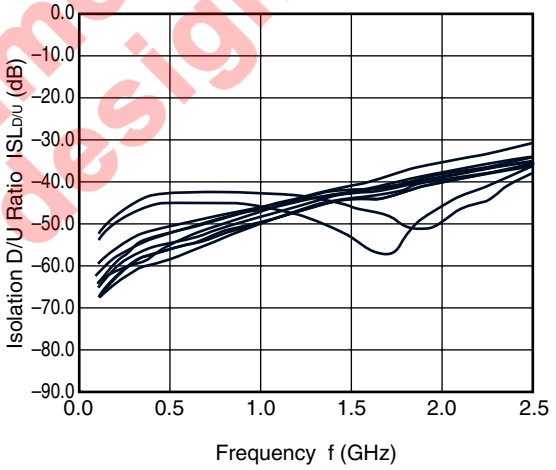
INSERTION LOSS vs. FREQUENCY
(IN-x - OUT2)



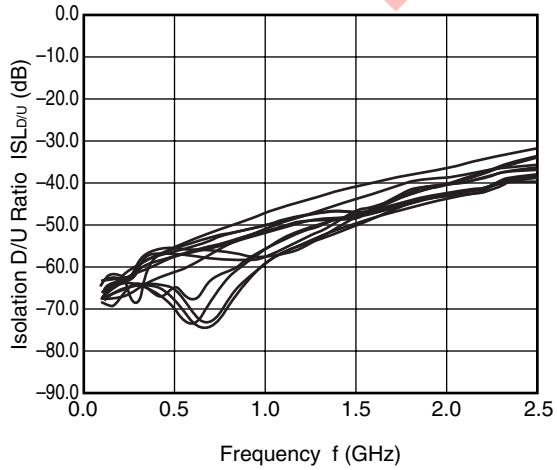
ISOLATION D/U RATIO vs. FREQUENCY
(IN-A - OUT1)



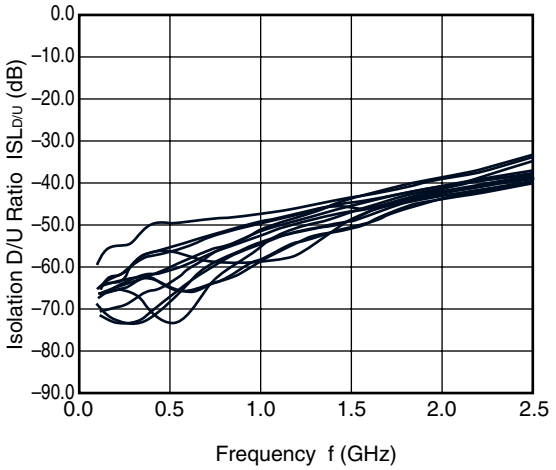
ISOLATION D/U RATIO vs. FREQUENCY
(IN-B - OUT1)



ISOLATION D/U RATIO vs. FREQUENCY
(IN-C - OUT1)

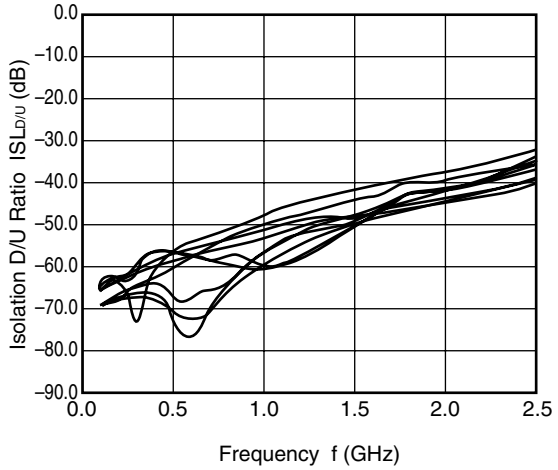


ISOLATION D/U RATIO vs. FREQUENCY
(IN-D - OUT1)

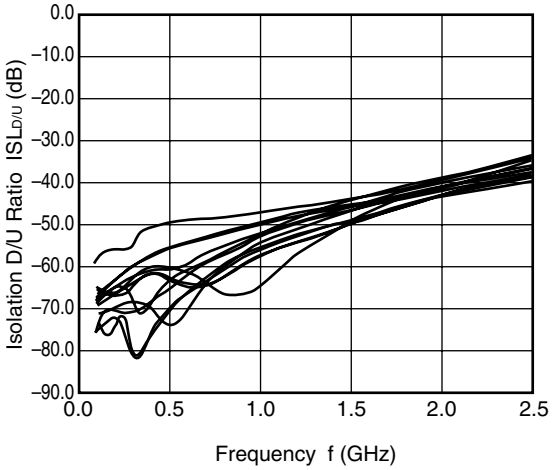


Remark The graphs indicate nominal characteristics.

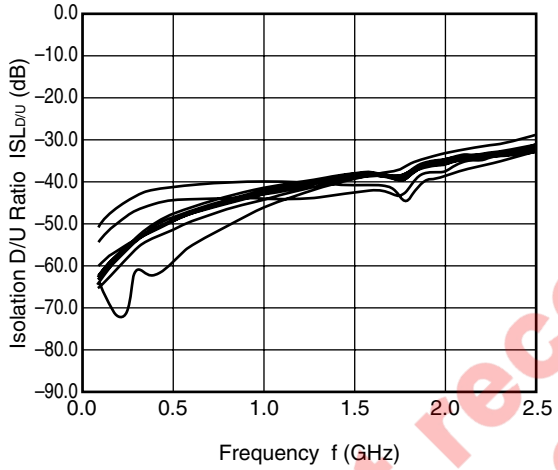
ISOLATION D/U RATIO vs. FREQUENCY
(IN-A - OUT2)



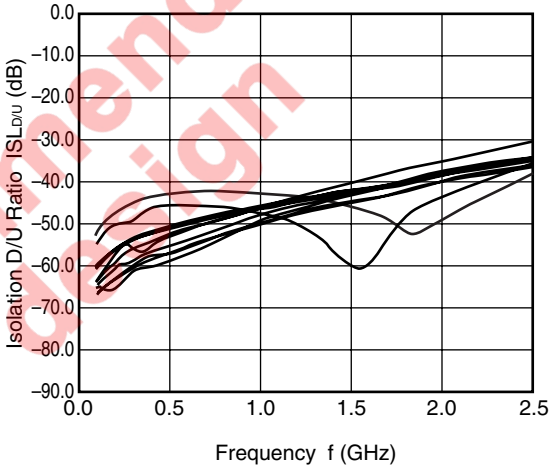
ISOLATION D/U RATIO vs. FREQUENCY
(IN-B - OUT2)



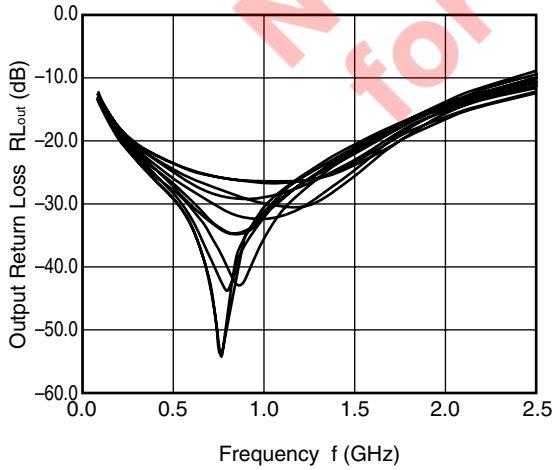
ISOLATION D/U RATIO vs. FREQUENCY
(IN-C - OUT2)



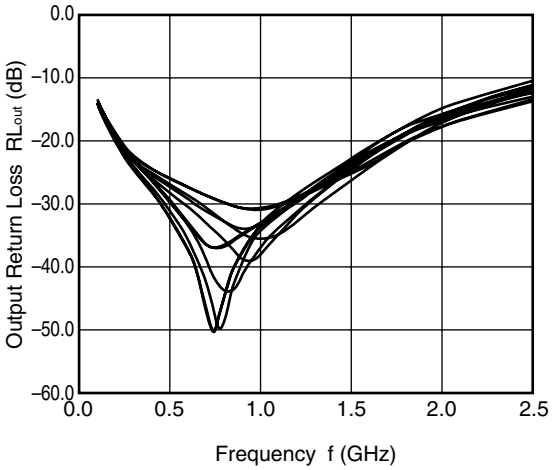
ISOLATION D/U RATIO vs. FREQUENCY
(IN-D - OUT2)



OUTPUT RETURN LOSS vs. FREQUENCY
(IN-x - OUT1)

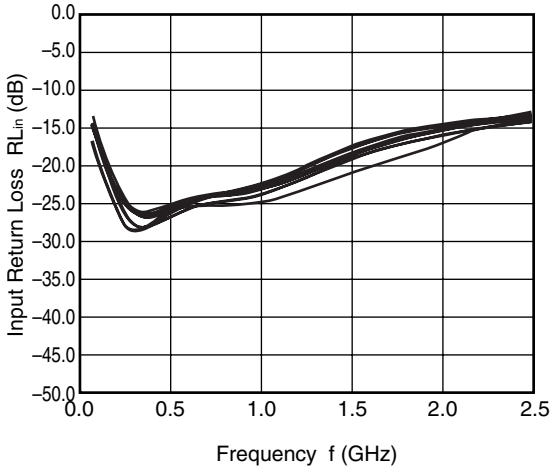


OUTPUT RETURN LOSS vs. FREQUENCY
(IN-x - OUT2)

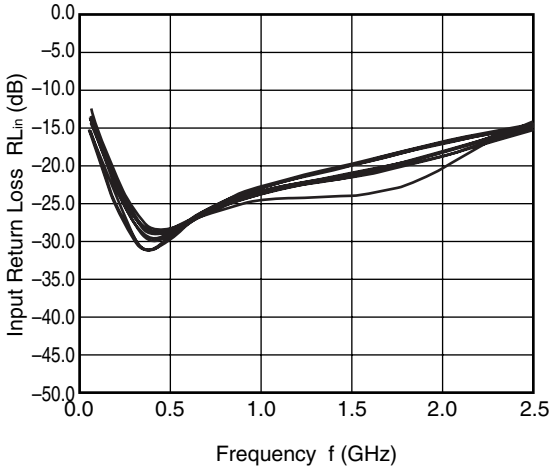


Remark The graphs indicate nominal characteristics.

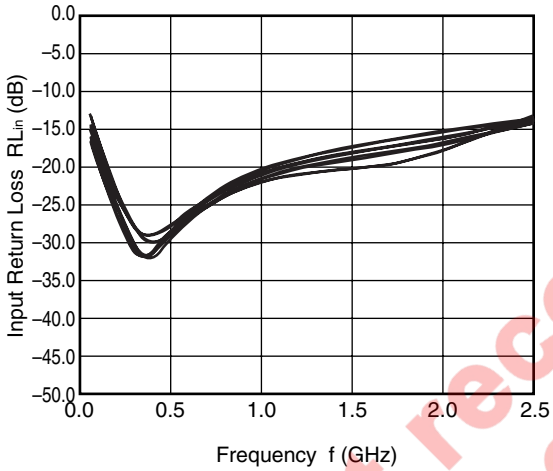
INPUT RETURN LOSS vs. FREQUENCY
(IN-A - OUTx)



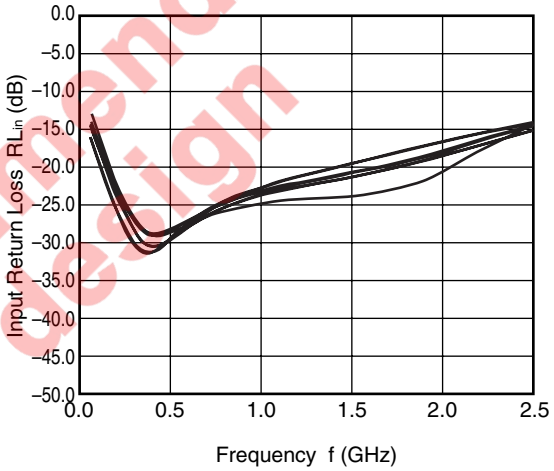
INPUT RETURN LOSS vs. FREQUENCY
(IN-B - OUTx)



INPUT RETURN LOSS vs. FREQUENCY
(IN-C - OUTx)



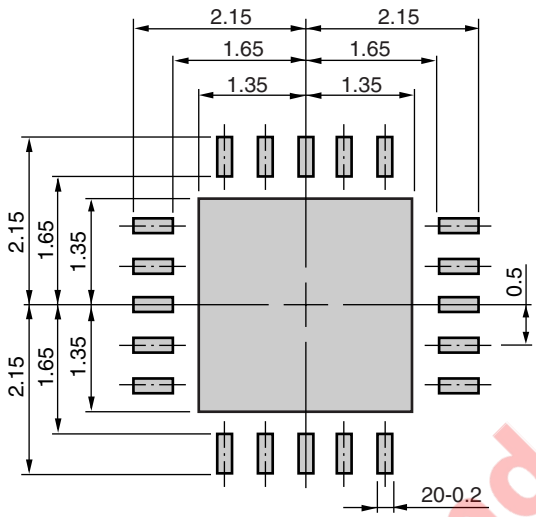
INPUT RETURN LOSS vs. FREQUENCY
(IN-D - OUTx)



Remark The graphs indicate nominal characteristics.

MOUNTING PAD LAYOUT DIMENSIONS

20-PIN 4 × 4 mm SQUARE MICRO LEAD PACKAGE (20-PIN PLASTIC QFN (0.5 mm pitch)) (UNIT: mm)



Remark The mounting pad layout in this document is for reference only.

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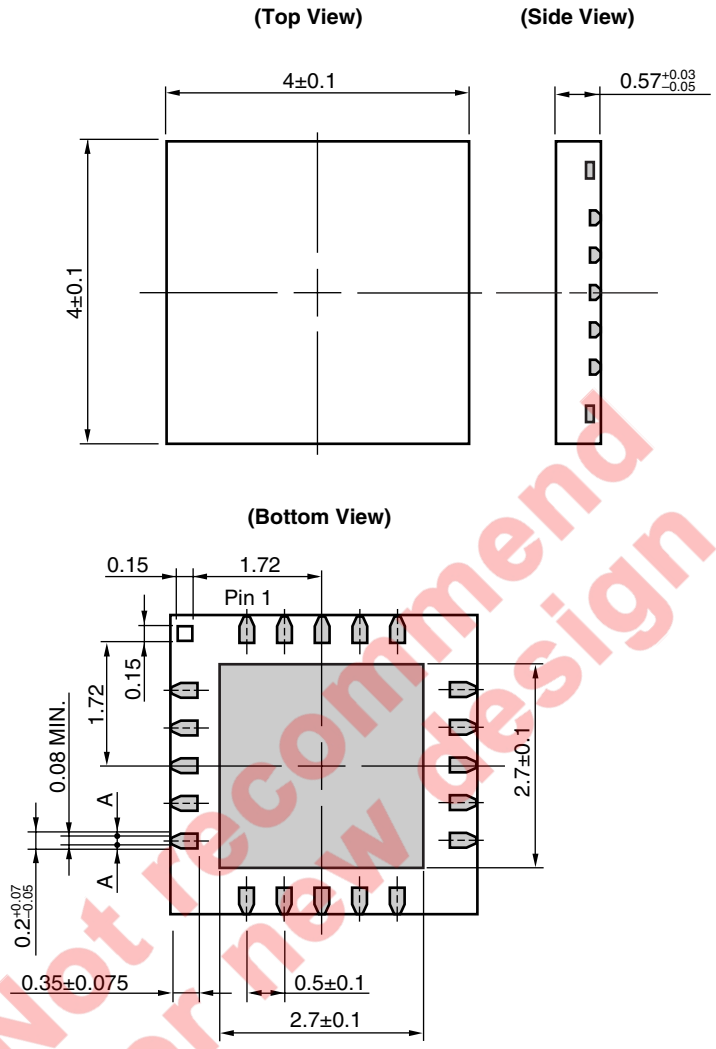
20-PIN 4 × 4 mm SQUARE MICRO LEAD PACKAGE (20-PIN PLASTIC QFN (0.5 mm pitch)) (UNIT: mm)



Remark A>0

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	IR260
Partial Heating	Peak temperature (package surface temperature) : 350°C or below Soldering time (per side of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	HS350

CAUTION

Do not use different soldering methods together (except for partial heating).

Revision History	μPD5753T7G Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb 22, 2011	–	First edition issued

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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