

SANYO**LB1649****Dual Bidirectional Motor Driver****Overview**

The LB1649 is a dual bidirectional motor driver. Since each channel has a 2-input logic circuit and performs bidirectional driving and braking functions, it is capable of direct driving 2pcs. of motor of various types rated at 6 to 24V.

The output voltage can be varied by using external zener diodes.

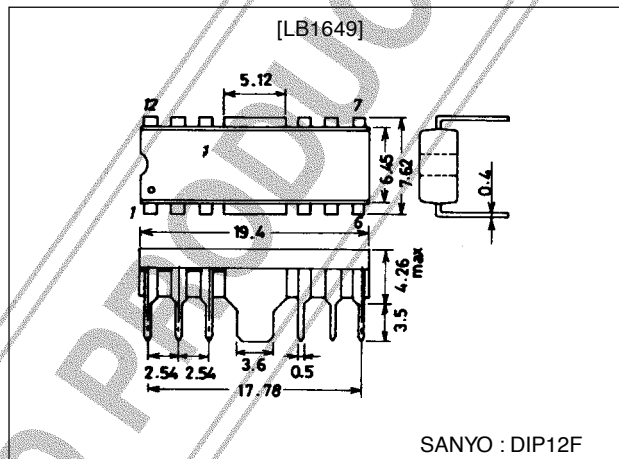
It is especially suited for dual motor drive (reel motor, loading motor, cassette motor in VCR) and for stepping motor drive.

Features

- With power transistor for motor drive contained, capable of withstanding dash current of 1A max.
- Performs braking function at the motor stop mode.
- Contains elements to absorb motor dash current.
- Input connectable direct to MOS LSI.
- Minimum number of external parts required.
- Wide operating voltage range.

Package Dimensions

unit:mm

3022A-DIP12F**Specifications****Absolute Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \text{ max}}$		25	V
Input voltage	V_{IN}		25	V
Output current	I_O		± 1	A
Allowable power dissipation	$P_d \text{ max}$		1.9	W
Operating temperature	T_{opr}		-25 to +75	°C
Storage temperature	T_{stg}		-55 to +125	°C

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		7 to +25	V

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82098HA (KT)/N3093TS/9074KI, TS No.1571-1/5

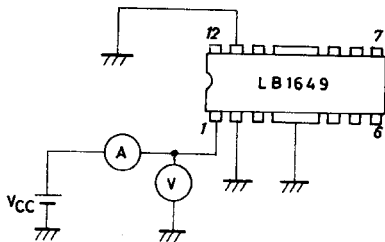
LB1649

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC}=12\text{V}$, per channel

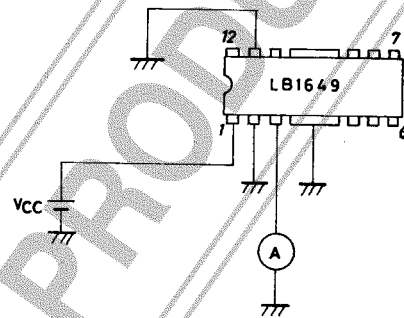
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	Braking mode, $R_L=\infty$, per channel		7.0	10.0	mA
Output leakage current	I_{OL}	Braking mode, $R_L=\infty$, per channel		40	120	μA
Input threshold voltage	V_{th}	$R_L=\infty$	0.9	1.05	1.20	V
Output voltage	V_O	$R_L=60\Omega$, $V_Z=7.4\text{V}$	6.5	7.2	7.5	V
Output transistor saturation voltage (upper)	V_{sat1}	$I_{OUT}=300\text{mA}$		1.9	2.3	V
		$I_{OUT}=500\text{mA}$		2.0	2.4	V
Output transistor saturation voltage (lower)	V_{sat2}	$I_{OUT}=300\text{mA}$		0.3	0.55	V
		$I_{OUT}=500\text{mA}$		0.5	0.7	V

Test Circuit (per channel)

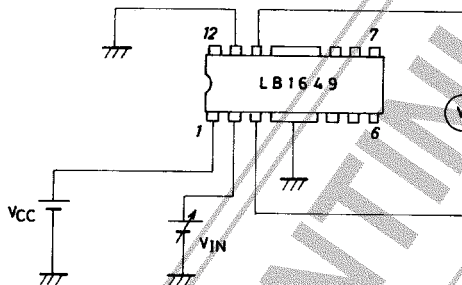
(1) I_{CC}



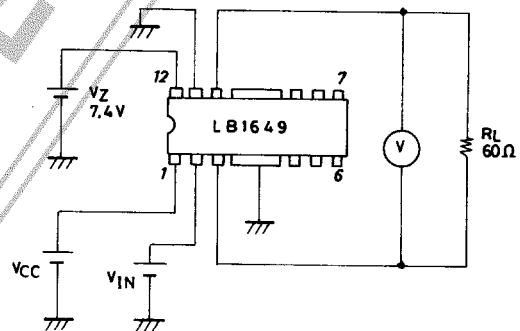
(2) I_{OL}



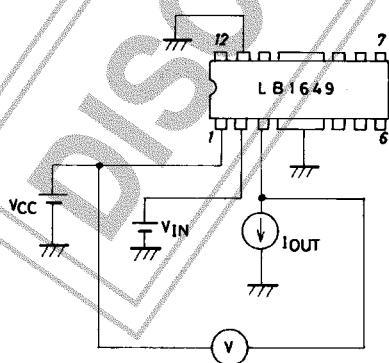
(3) V_{th}



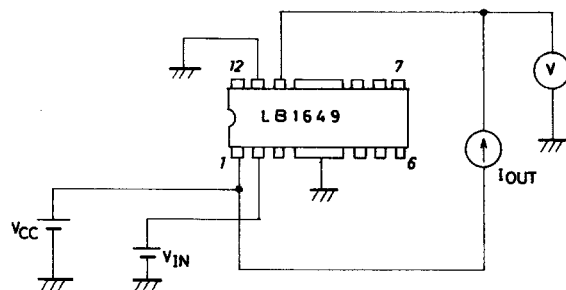
(4) V_O



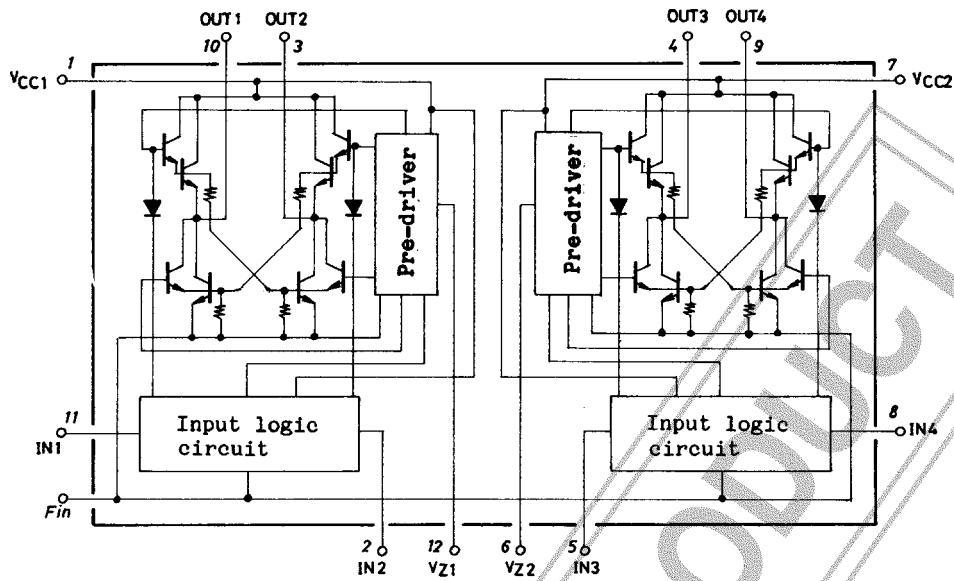
(5) V_{sat1}



(6) V_{sat2}



Equivalent Circuit Block Diagram



Truth Table of Logic Circuit

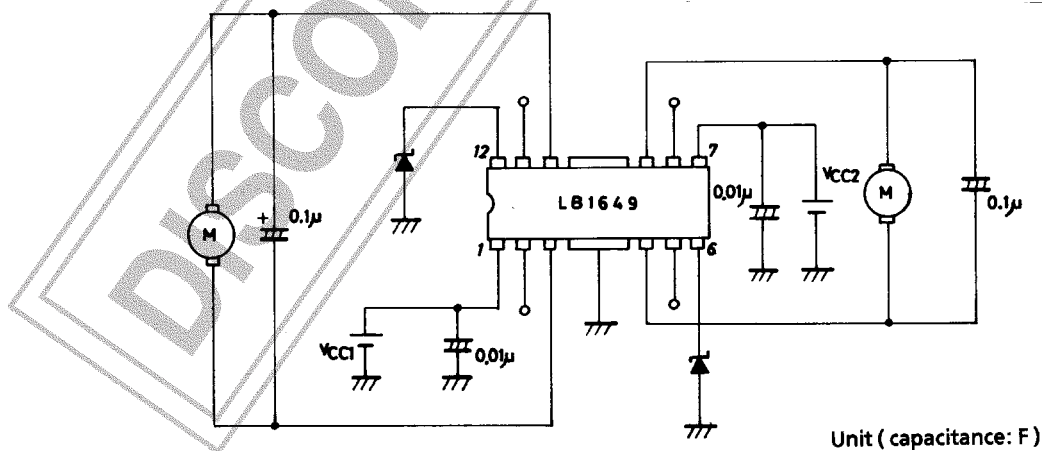
IN1	IN2	OUT1	OUT2	IN3	IN4	OUT3	OUT4
0	0	L	L	0	0	L	L
1	0	H	L	1	0	H	L
0	1	L	H	0	1	L	H
1	1	L	L	1	1	L	L

Note : A capacitor of 0.01 μ F or greater must be connected across V_{CC}1,2 and GND.

INPUT			OUTPUT				MODE	
IN1	IN2, 3	IN4	OUT1	OUT2	OUT3	OUT4	M1	M2
0	0	0	L	L	L	L	Brake	Brake
1	0	0	H	L	L	L	Forward/reverse	Brake
0	1	1	L	H	L	L	Reverse/forward	Brake
1	1	0	L	L	H	L	Brake	Forward/reverse
0	0	1	L	L	L	H	Brake	Reverse/forward
1	1	1	L	L	L	L	Brake	Brake

The remaining input states 1, 0, 1 and 0, 1, 0 are not inhibited.

Sample Application Circuit



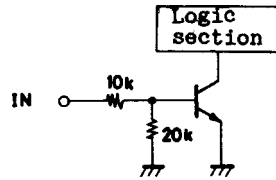
Input Circuit

The input circuit is shown right

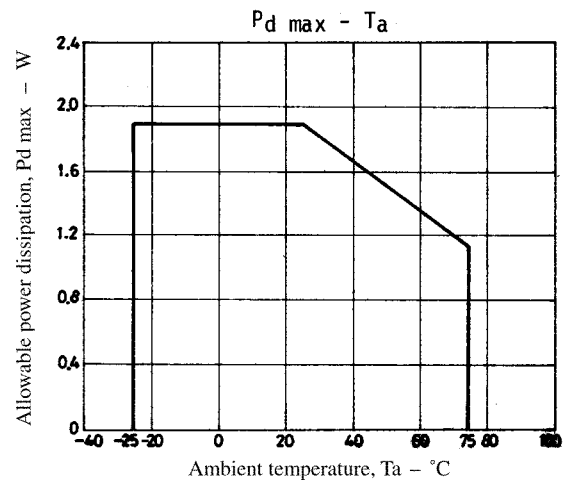
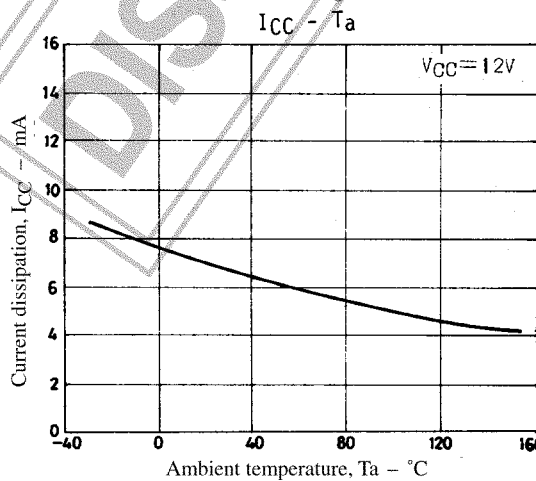
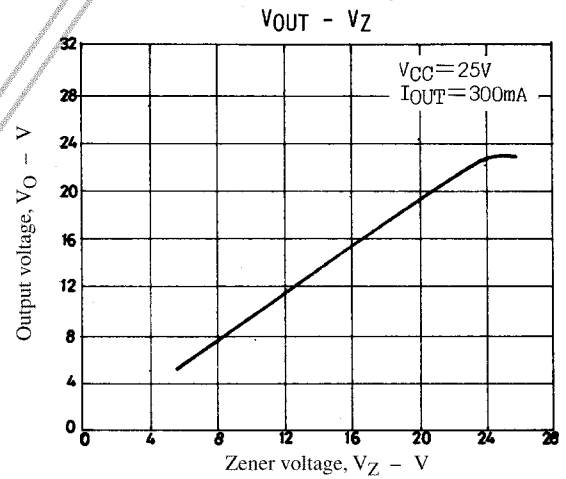
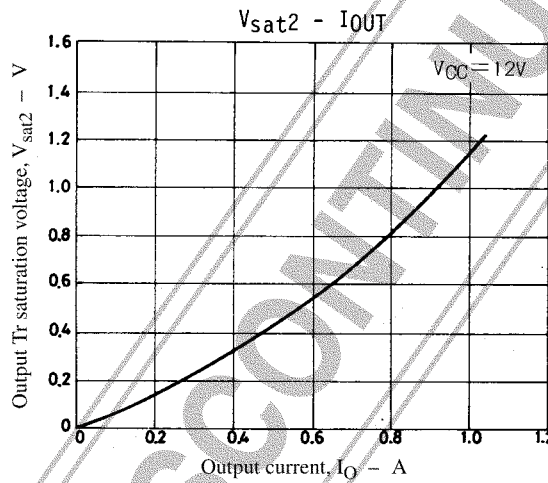
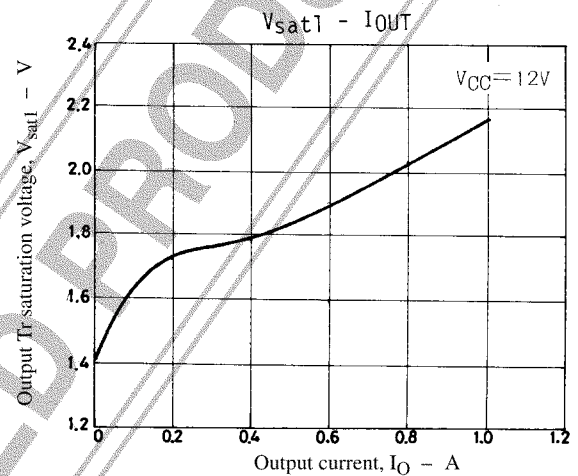
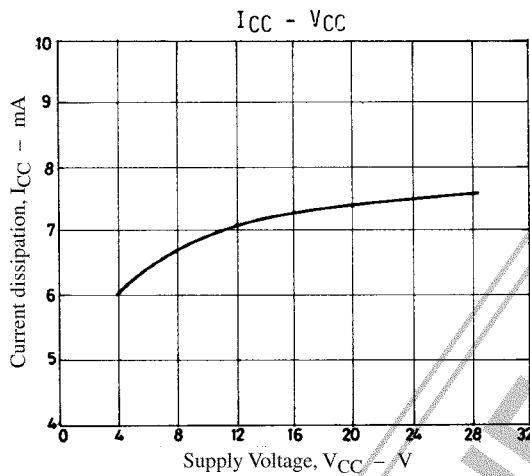
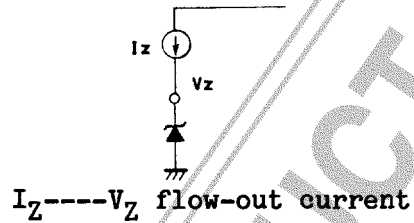
V_Z pin

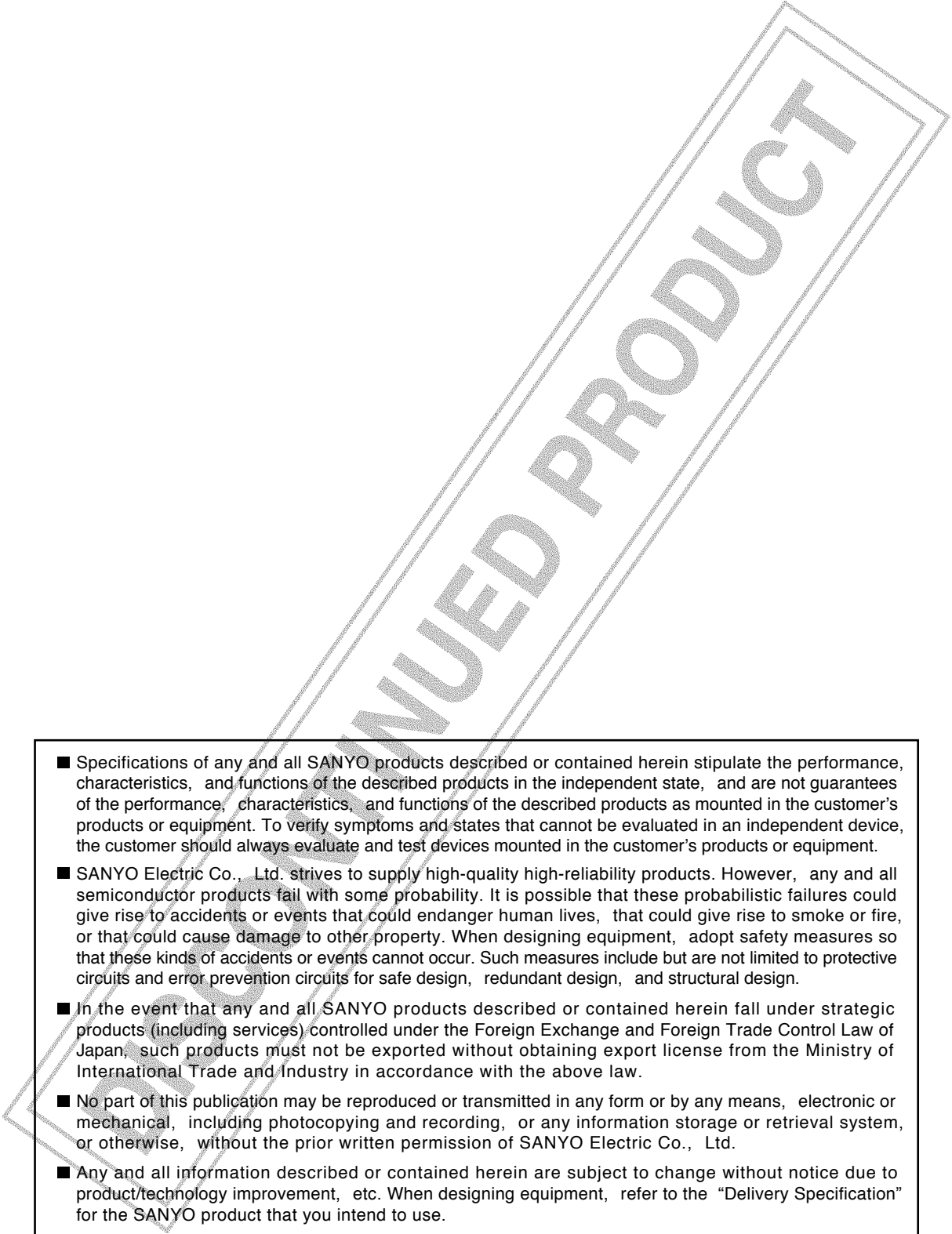
Zener voltage	V_Z pin voltage vaule
$\geq 5.6V$	small
$< 5.6V$	large*

* Susceptible to V_Z pin flow-out current change.



Unit (resistance: Ω)



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