



Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCIVER/ REGISTERS (3-STATE)

IDT54/74FCT646T/AT/CT/DT
IDT54/74FCT648T/AT/CT
IDT54/74FCT651T/AT/CT
IDT54/74FCT652T/AT/CT/DT

FEATURES:

- Fastest CMOS logic family available
- Std., A, C and D speed grades with 4.4ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of true and inverting data paths
- I_{OL} = 64mA (commercial), 48mA (military)
- CMOS power levels
- TTL input and output level compatible
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

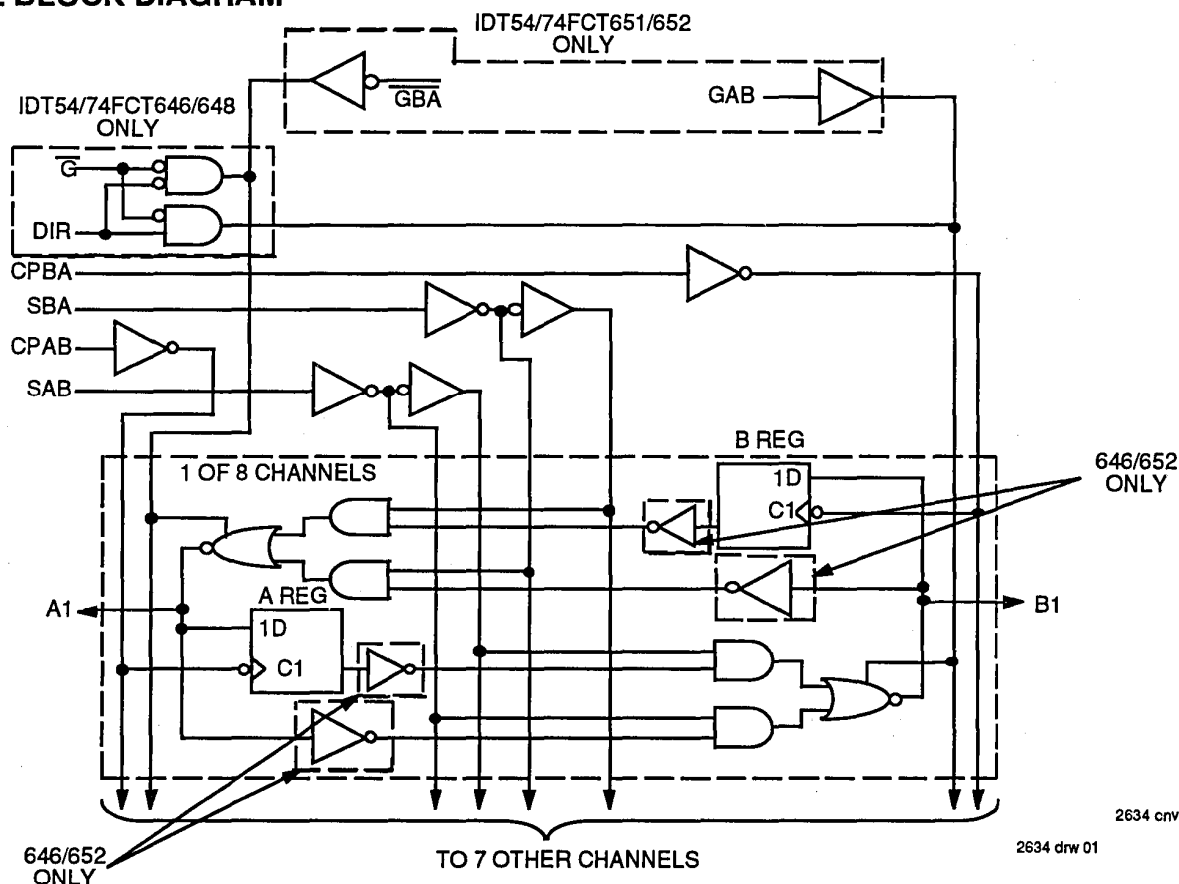
The IDT54/74FCT646/652T/AT/CT/DT and IDT54/74FCT648/651T/AT/CT consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

The '651/652 utilize GAB and $\overline{\text{GBA}}$ signals to control the transceiver functions. The '646/648 utilize the enable control ($\overline{\text{G}}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

FUNCTIONAL BLOCK DIAGRAM



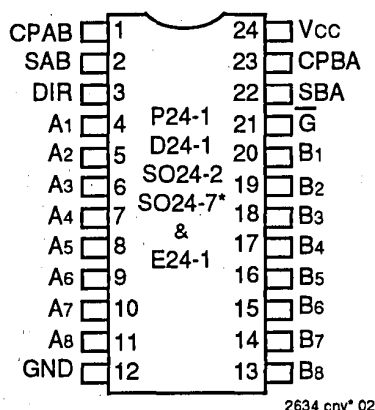
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

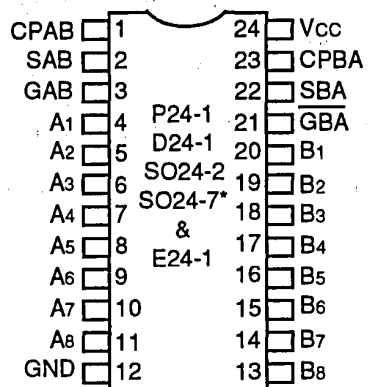
PIN CONFIGURATIONS



2634 cnv* 02

**DIP/SSOP/CERPACK
TOP VIEW**

* FCT646T/AT/CT/DT only

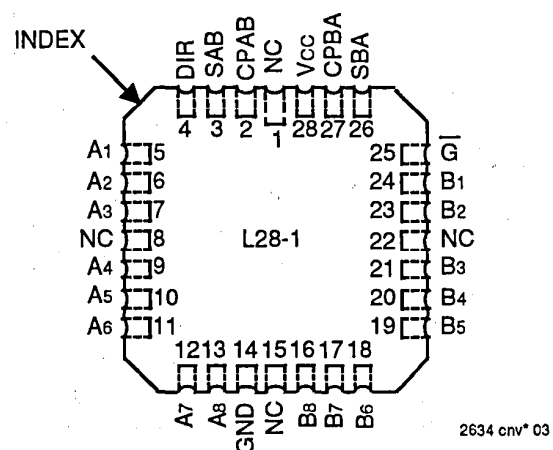


2634 cnv* 04

**DIP/SSOP/CERPACK
TOP VIEW**

* FCT652T/AT/CT/DT only

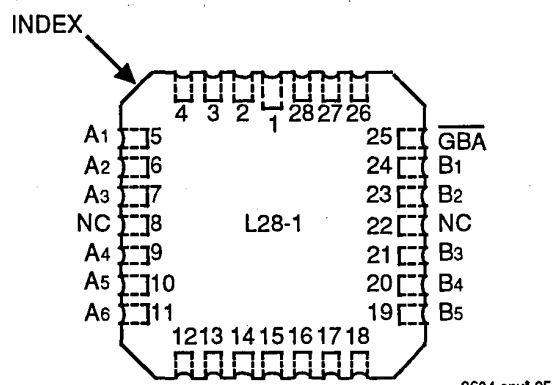
FCT646/648T



2634 cnv* 03

**LCC
TOP VIEW**

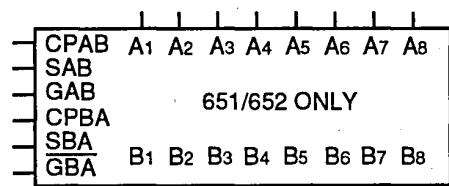
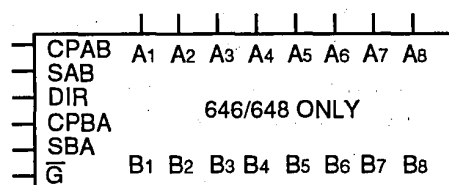
FCT651/652T



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**LCC
TOP VIEW**

LOGIC SYMBOLS



2634 cnv* 06

PIN DESCRIPTION

Pin Names	Description
A1 - A8	Data Register A Inputs Data Register B Outputs
B1 - B8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, G	Output Enable Inputs (646/648)
GAB, GBA	Output Enable Inputs (651/652)

2634 tbi 01

FUNCTION TABLE FCT646/648T

Inputs						Data I/O ⁽¹⁾		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A ₁ - A ₈	B ₁ - B ₈	IDT54/74FCT646T	IDT54/74FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

2634 tbl 02

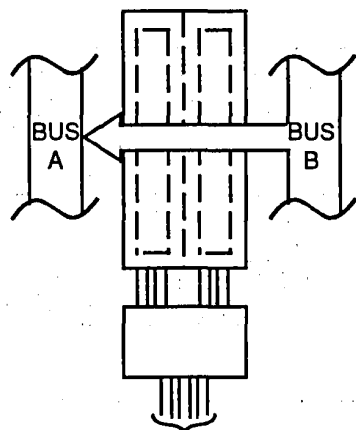
FUNCTION TABLE FCT651/652T

Inputs						Data I/O		Operation or Function	
GAB	GBA	CPAB	CPBA	SAB	SBA	A ₁ - A ₈	B ₁ - B ₈	IDT54/74FCT651T	IDT54/74FCT652T
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾ Output	Store A, Hold B Store A in Both Registers ⁽³⁾	Store A, Hold B Store A in Both Registers
H	H	↑	↑	X ⁽²⁾	X				
L	X	H or L	↑	X	X	Unspecified ⁽¹⁾ Output	Input	Hold A, Store B Store B in Both Registers ⁽⁴⁾	Hold A, Store B Store B in Both Registers
L	L	↑	↑	X	X ⁽²⁾				
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

2634 tbl 03

NOTES:

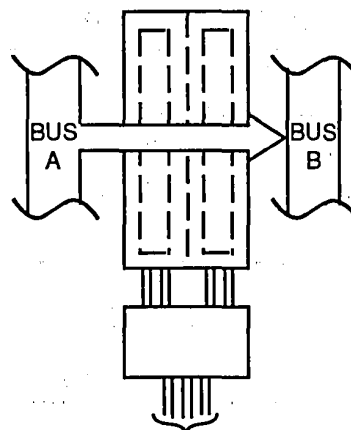
- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.
H = HIGH, L = LOW, X = Don't Care, ≠ = LOW-to-HIGH transition.
- $\overline{A}$ in B Register.
- $\overline{B}$ in A Register.



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO A

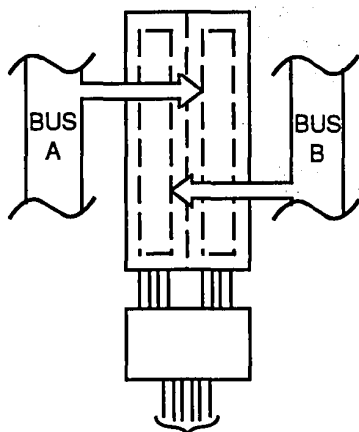
2634 cnv* 07



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO B

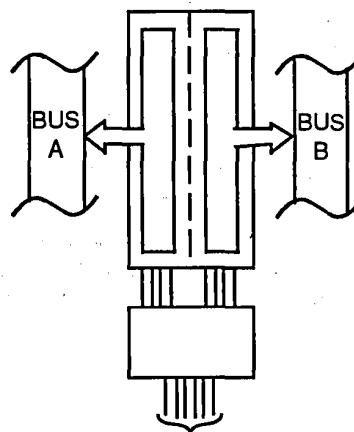
2634 cnv* 08



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM
A AND/OR B

2634 cnv* 09



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H
646/648 ⁽¹⁾	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X

TRANSFER STORES
DATA TO A AND/OR B

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NOTE:

1. 646/648 cannot transfer data to A bus and B bus simultaneously.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC}	−0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	−55 to +125	°C
T _{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T _{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

- NOTES:** 2634 tbl 04
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
 - Input and V_{CC} terminals only.
 - Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	8	12	pF

- NOTE:** 2634 tbl 05
- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Except I/O pins)	VCC = Max.	V _I = 2.7V	—	—	5	μA
I _{IL}	Input LOW Current (Except I/O pins)		V _I = 0.5V	—	—	-5	μA
I _{IH}	Input HIGH Current (I/O pins only)	VCC = Max.	V _I = 2.7V	—	—	15	μA
I _{IL}	Input LOW Current (I/O pins only)		V _I = 0.5V	—	—	-15	μA
I _I	Input HIGH Current	VCC = Max., V _I = VCC (Max.)		—	—	20	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _N = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max ⁽³⁾ , V _O = GND		-60	-120	-225	mA
I _{OFF}	Power Down Disable	VCC = GND V _O = 4.5V		—	—	100	μA
V _{OH}	Output HIGH Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.3	—	V
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA MIL.	—	0.3	0.55	V
			I _{OL} = 64mA COM'L. ⁽⁴⁾	—	0.3	0.55	V
V _H	Input Hysteresis	—		—	200	—	mV
I _{CC}	Quiescent Power Supply Current	VCC = Max. V _{IN} = GND or VCC		—	0.2	1.5	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- These are maximum I_{OL} values per output for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

2634 tbl 06

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{GAB} = \overline{GBA} = \text{GND}$ or $\overline{G} = \overline{DIR} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{GAB} = \overline{GBA} = \text{GND}$ or $\overline{G} = \overline{DIR} = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.7	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.2	6.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{GAB} = \overline{GBA} = \text{GND}$ or $\overline{G} = \overline{DIR} = \text{GND}$ Eight Bits Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	7.0	12.8 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	9.2	21.8 ⁽⁵⁾	

2634 tbl 07

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_{HNT} = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Outputs at } f_i$
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	646T/648T/651T/652T				646AT/648AT/651AT/652AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time, $\overline{G}$, DIR to Bus ⁽³⁾		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time, $\overline{G}$, DIR to Bus ⁽³⁾		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns

2634 tbl 08

Symbol	Parameter	Condition(1)	646CT/648CT/651CT/652CT				646DT/652DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	4.4	—	—	ns
tPZH tPZL	Output Enable Time, G, DIR to Bus(3)		1.5	7.8	1.5	8.9	1.5	5.0	—	—	ns
tPHZ tPLZ	Output Disable Time, G, DIR to Bus(3)		1.5	6.3	1.5	7.7	1.5	4.3	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	4.4	—	—	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		1.5	6.2	1.5	7.0	1.5	5.0	—	—	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.0	—	—	—	ns
tW	Clock Pulse Width, HIGH or LOW(4)		5.0	—	5.0	—	3.0	—	—	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. GAB, $\bar{G}$ BA to Bus for 651, 652.
4. This parameter is guaranteed but not tested.

2634 tbl 09