



















## Retriggerable Monostable Multivibrator (with Clear)

**ELECTRICALLY TESTED PER:**  
**MIL-M-38510/31403**

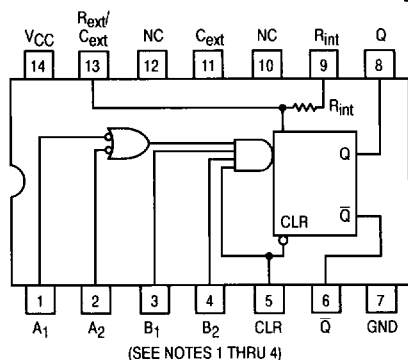
This DC triggered multivibrator features pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The  $\text{LS122}$  has an internal timing resistor that allows the circuit to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

The 'LS122 has a Schmitt trigger input to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

- Overriding Clear Terminates Output Pulse
- Compensated for  $V_{CC}$  and Temperature Variations
- DC Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Internal Timing Resistors

Inputs						Outputs	
CLEAR	A <sub>1</sub>	A <sub>2</sub>	B <sub>1</sub>	B <sub>2</sub>	Q	$\bar{Q}$	
L	X	X	X	X	L	H	
X	H	H	X	X	L	H	
X	X	X	L	X	L	H	
X	X	X	X	L	L	H	
H	L	X	↑	H			
H	L	X	H	↑			
H	X	L	↑	H			
H	X	L	H	↑			
H	H	↓	H	H			
H	↓	↓	H	H			
H	↓	H	H	H			
↑	L	X	H	H			
↑	X	L	H	H			

### LOGIC DIAGRAM



## Military 54LS122

**AVAILABLE AS:**

- 1) JAN: JM38510/31403BXA  
2) SMD: 7600301  
3) 883: 54LS122/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2

**THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.**

## PIN ASSIGNMENTS

PIN ASSIGNMENTS				
FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A <sub>1</sub>	1	1	2	VCC
A <sub>2</sub>	2	2	3	VCC
B <sub>1</sub>	3	3	4	VCC
B <sub>2</sub>	4	4	6	VCC
CLR	5	5	8	GND
Q̄	6	6	9	VCC
GND	7	7	10	GND
Q	8	8	12	OPEN
R <sub>int</sub>	9	9	13	VCC
NC	10	10	14	VCC
C <sub>ext</sub>	11	11	16	GND
NC	12	12	18	VCC
R <sub>ext</sub> /C <sub>ext</sub>	13	13	19	OPEN
VCC	14	14	20	VCC

**BURN-IN CONDITIONS:**

**V<sub>CC</sub> = 5.0 V MIN/6.0 V MAX**

**NOTES:**

1. An external timing capacitor may be connected between  $C_{ext}$  and  $R_{ext}/C_{ext}$  (positive).
2. To use the internal timing resistor of the 'LS122, connect  $R_{int}$  to  $V_{CC}$ .
3. For improved pulse width accuracy connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between  $R_{ext}/C_{ext}$  and  $V_{CC}$ .

## TYPICAL APPLICATION DATA

The output pulse  $t_p$  is a function of the external components,  $C_{ext}$  and  $R_{ext}$  or  $C_{ext}$  and  $R_{int}$  on the 'LS122. For values of  $C_{ext} \geq 1000$  pF, the output pulse at  $V_{CC} = 5.0$  V and  $V_{RC} = 5.0$  V is given by  $t_p = K R_{ext}/C_{ext}$  where  $K$  is nominally 0.45.

If  $C_{ext}$  is in pF and  $R_{ext}$  is in k $\Omega$  then  $t_p$  is in nanoseconds.

The  $C_{ext}$  terminal of the 'LS122 and 'LS123 is an internal connection to ground, however for the best system performance  $C_{ext}$  should be hardwired to ground.

Care should be taken to keep  $R_{ext}$  and  $C_{ext}$  as close to the monostable as possible with a minimum amount of inductance between the  $R_{ext}/C_{ext}$  junction and the  $R_{ext}/C_{ext}$  pin. Good groundplane and adequate bypassing should be designed into the system for optimum performance to ensure that no false triggering occurs.

It should be noted that the  $C_{ext}$  pin is internally connected to ground on the 'LS122 and 'LS123, but not on the 'LS221. Therefore, if  $C_{ext}$  is hardwired externally to ground, substitution of a 'LS221 onto a 'LS123 socket will cause the 'LS221 to become non-functional.

The switching diode is not needed for electrolytic capacitance application and should not be used on the 'LS122 and 'LS123.

To find the value of  $K$  for  $C_{ext} \geq 1000$  pF, refer to Figure 4. Variations on  $V_{CC}$  or  $V_{RC}$  can cause the value of  $K$  to change, as can the temperature of the 'LS123, 'LS122. Figures 5 and 6 show the behavior of the circuit shown in Figures 1 and 2 if separate power supplies are used for  $V_{CC}$  and  $V_{RC}$ . If  $V_{CC}$  is

tied to  $V_{RC}$ , Figure 7 shows how  $K$  will vary with  $V_{CC}$  and temperature. Remember, the changes in  $R_{ext}$  and  $C_{ext}$  with temperature are not calculated and included in the graph.

As long as  $C_{ext} \geq 1000$  pF and  $5.0 \text{ k} \leq R_{ext} \leq 160 \text{ k}$  (54LS122/123), the change in  $K$  with respect to  $R_{ext}$  is negligible.

If  $C_{ext} \leq 1000$  pF the graph shown on Figure 8 can be used to determine the output pulse width. Figure 9 shows how  $K$  will change for  $C_{ext} \leq 1000$  pF if  $V_{CC}$  and  $V_{RC}$  are connected to the same power supply. The pulse width  $t_p$  in nanoseconds is approximated by

$$t_p = 6.0 + 0.05 C_{ext} (\text{pF}) + 0.45 R_{ext} (\text{k}\Omega) \\ C_{ext} + 11.6 R_{ext}$$

In order to trim the output pulse width, it is necessary to include a variable resistor between  $V_{CC}$  and the  $R_{ext}/C_{ext}$  pin or between  $V_{CC}$  and the  $R_{ext}$  pin of the 'LS122. Figures 10, 11 and 12 show how it can be done.  $R_{ext}$  remote should be kept as close to the monostable as possible.

Retriggering of the part, as shown in Figure 3, must not occur before  $C_{ext}$  is discharged or the retrigger will not have any effect. The discharge time of  $C_{ext}$  in nanoseconds is guaranteed to be less than  $0.22 C_{ext}$  (pF) and is typically  $0.05 C_{ext}$  (pF).

For the smallest possible deviation in output pulse widths from various devices, it is suggested that  $C_{ext}$  be kept  $\geq 1000$  pF.

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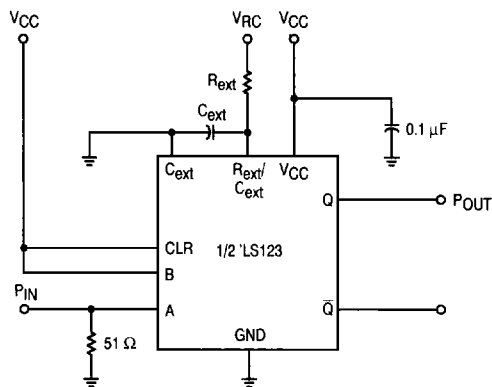


Figure 1

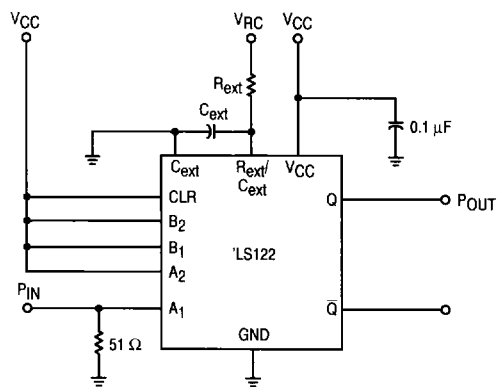
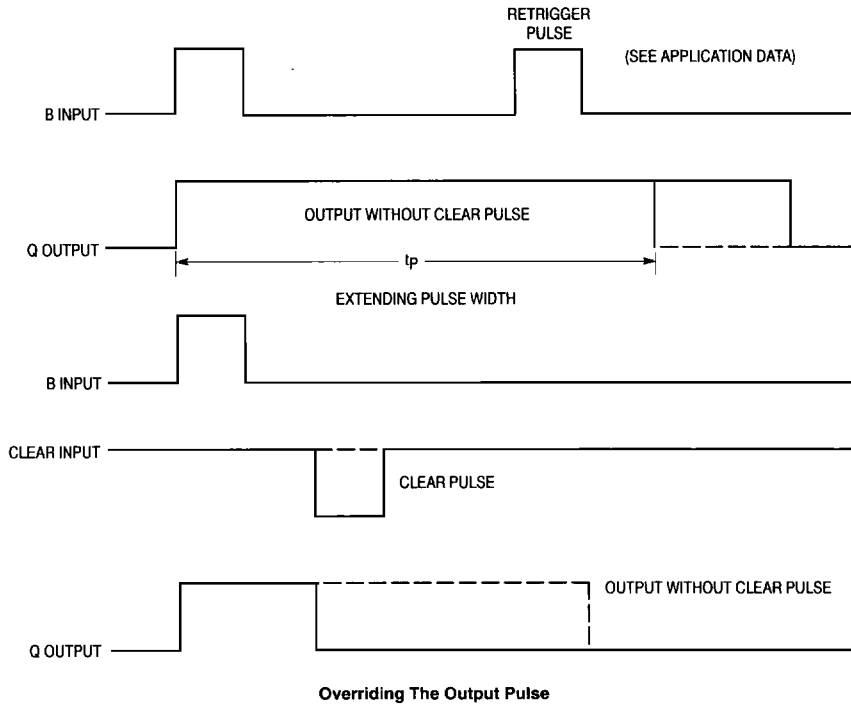


Figure 2

# 54LS122

## WAVEFORMS



Overriding The Output Pulse

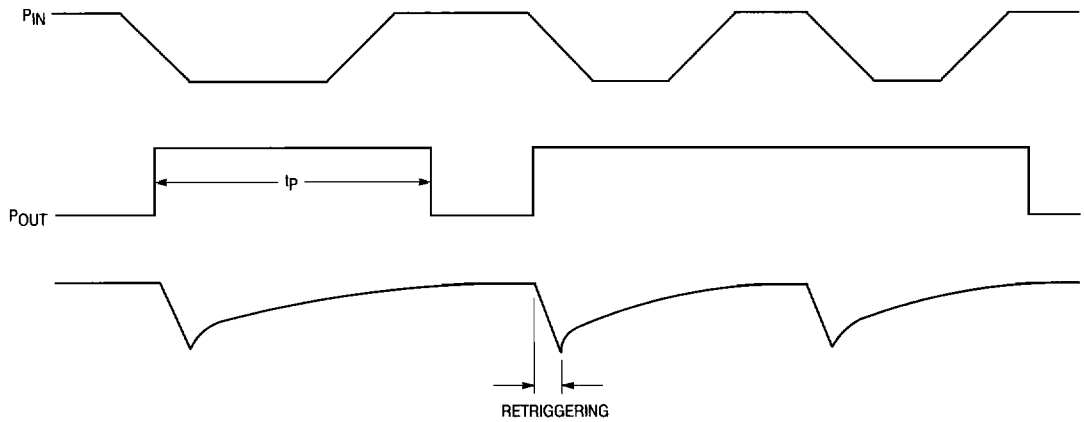


Figure 3

# 54LS122

EXTERNAL CAPACITANCE,  $C_{ext}$  ( $\mu F$ )

$5 k \leq R_{ext} \leq 260 k$



Figure 4

K versus  $V_{CC}$

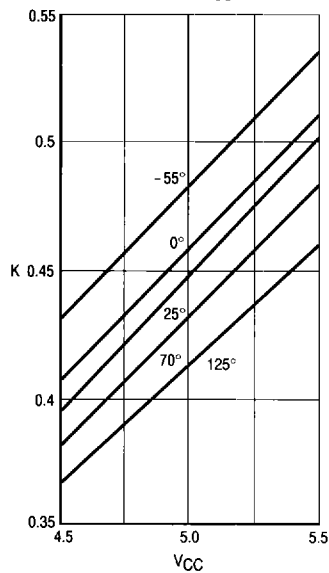


Figure 5

K versus  $V_{RC}$

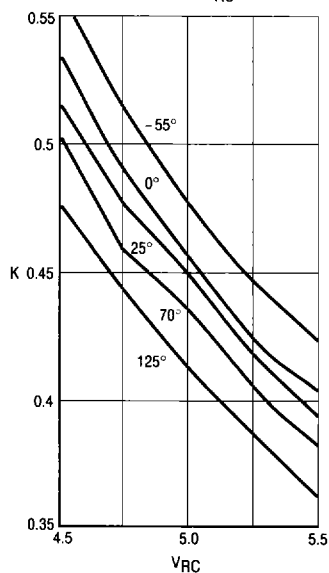


Figure 6

K versus  $V_{CC}$  and  $V_{RC}$

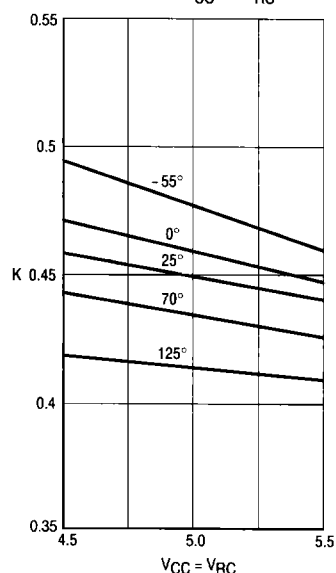


Figure 7

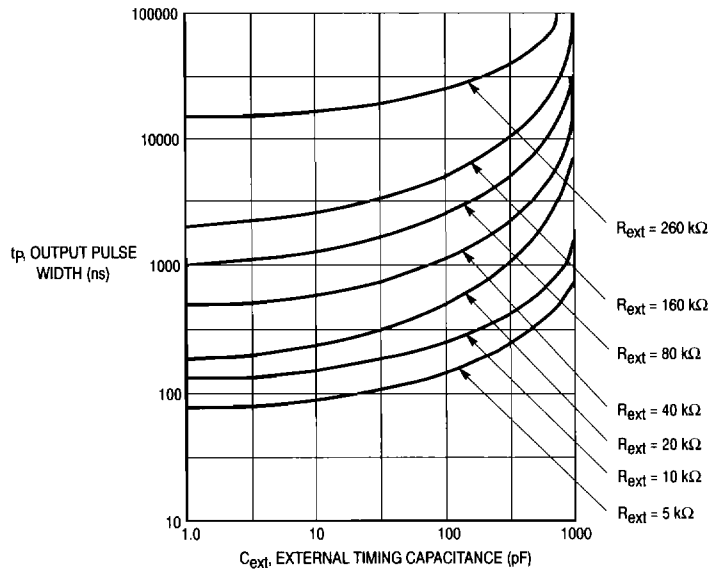


Figure 8

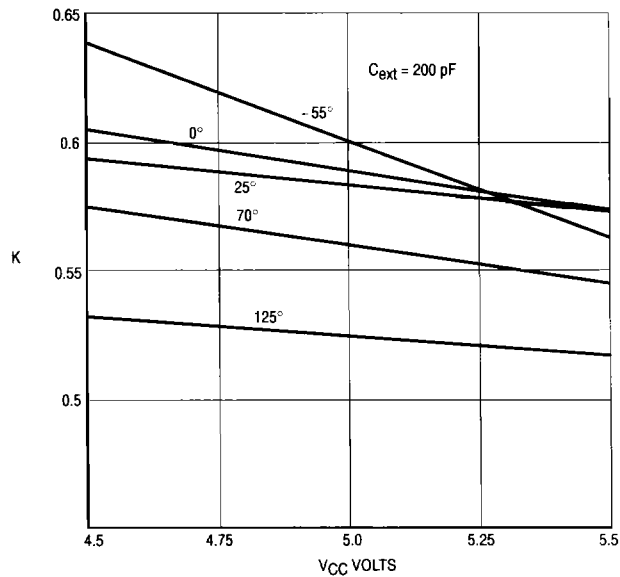


Figure 9

# 54LS122

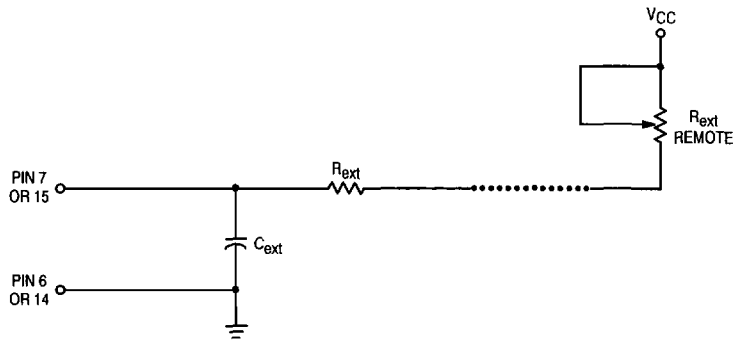


Figure 10. 'LS123 Remote Trimming Circuit

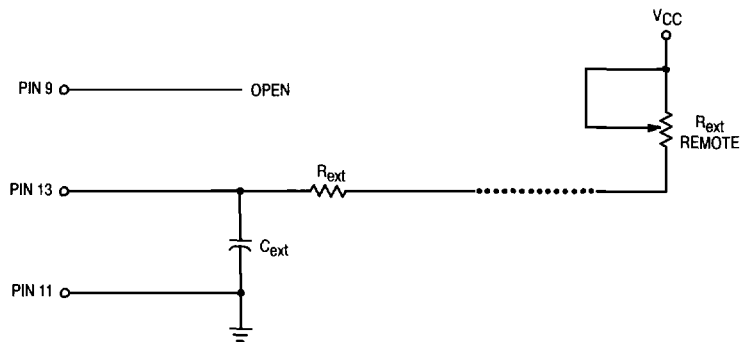


Figure 11. 'LS122 Remote Trimming Circuit Without  $R_{ext}$

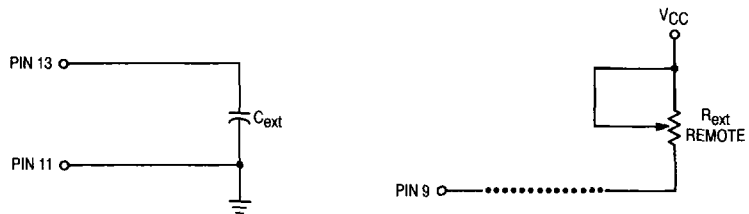
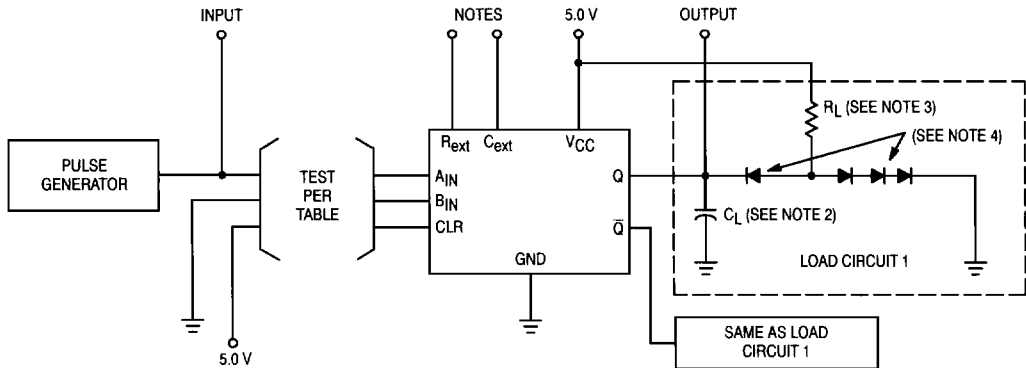


Figure 12. 'LS122 Remote Trimming Circuit With  $R_{INT}$

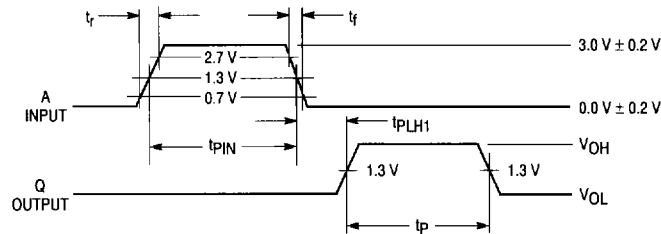
# 54LS122

## LOAD FOR OUTPUT UNDER TEST

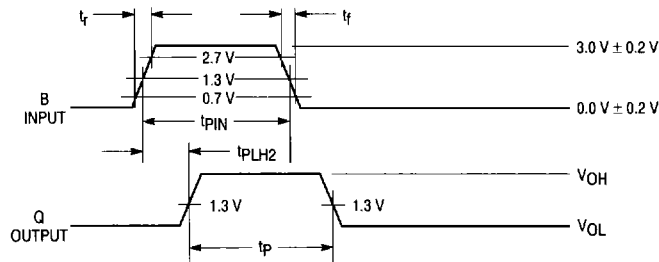


## SWITCHING WAVEFORMS

### $t_{PLH1}$ and $t_p$ Waveforms



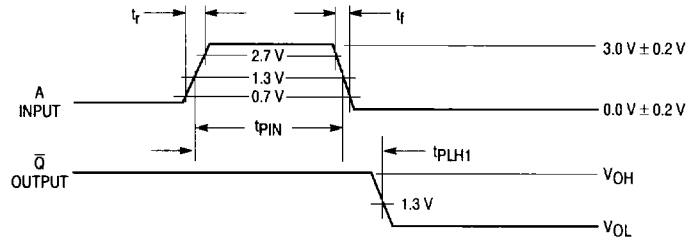
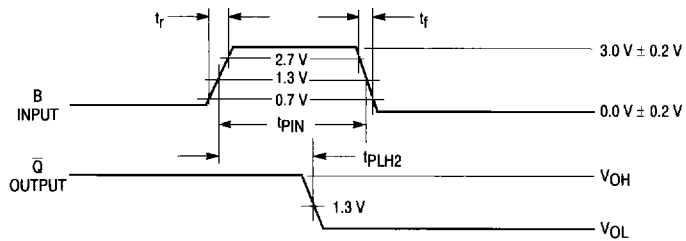
### $t_{PLH2}$ and $t_p$ Waveforms



## NOTES:

- Pulse generator has the following characteristics:  
 $PRR \leq 1.0 \text{ MHz}$ ,  $t_r \leq 15 \text{ ns}$ ,  $t_f \leq 6.0 \text{ ns}$ ,  $t_{PIN} \geq 40 \text{ ns}$  and  $Z_{OUT} = 50 \Omega$ .
- $C_L = 50 \text{ pF} \pm 10\%$ , including scope probe, wiring and stray capacitance without package in test fixture.
- $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$ .
- All diodes are 1N3064 or 1N916 or equivalent.
- The limits specified for  $C_L = 15 \text{ pF}$  are guaranteed but not tested.
- $t_{setup}(\text{max})$  shall be  $\leq 50\%$  of the typical output pulse width for the actual  $C_{ext}$  used.
- $C_{ext}$  connected to  $R_{ext}/C_{ext}$  through a  $1,000 \text{ pF} \pm 10\%$  capacitor.
- $R_{ext}/C_{ext}$  connected to  $V_{CC}$  through a  $5.0 \text{ k}\Omega \pm 10\%$  resistor.
- $R_{ext}/C_{ext}$  connected to  $V_{CC}$  through a  $5.0 \text{ k}\Omega$  to  $180 \text{ k}\Omega$  resistor, and  $C_{ext}$  connected to  $R_{ext}/C_{ext}$  through a  $\leq 1,000 \text{ pF}$  capacitor.
- $R_{ext}/C_{ext}$  connected to  $V_{CC}$  through a  $10 \text{ k}\Omega \pm 10\%$  resistor.
- $C_{ext}$  connected to  $R_{ext}/C_{ext}$  through a  $\geq 45 \text{ pF}$  capacitor,  $R_{ext}/C_{ext}$  connected to  $V_{CC}$  through a  $10 \text{ k}\Omega \pm 10\%$  resistor.

## SWITCHING WAVEFORMS

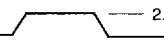
 $t_{PLH1}$  Waveforms $t_{PLH2}$  Waveforms



## 54LS122

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –0.4 mA, V <sub>IH</sub> = 2.0 V, other input = 0.7 V, B <sub>2</sub> = (See Note 1) or 0.7 V, R <sub>int</sub> = GND or 4.5 V, R <sub>ext</sub> = GND, CLR = 4.5 V.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = 4.0 mA, V <sub>IH</sub> = 2.0 V, other input = 0.7 V, B <sub>2</sub> = (See Note 1) or 0.7 V, R <sub>int</sub> = GND or 4.5 V, R <sub>ext</sub> = GND, CLR = 4.5 V.
V <sub>IC</sub>	Input Clamping Voltage		–1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IH</sub> = –18 mA, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other input is GND, CLR = 2.7 V.
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other input is GND, CLR = 5.5 V.
I <sub>IL</sub>	Logical "0" Input Current	–120	–360	–120	–360	–120	–360	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, other inputs = 0.4 V.
I <sub>OS</sub>	Output Short Circuit Current	–15	–100	–15	–100	–15	–100	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, B <sub>2</sub> = (See Note 1) or GND, CLR = 4.5 V, R <sub>int</sub> = GND or 4.5 V, other inputs = GND, V <sub>OUT</sub> = GND.
I <sub>CCH</sub>	Power Supply Current		11		11		11	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V, A = (See Note 1), R <sub>int</sub> = 5.5 V, R <sub>ext</sub> = 0.9 V.
I <sub>CCL</sub>	Power Supply Current		11		11		11	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V, B = GND, R <sub>int</sub> = 5.5 V.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.5 V.

## NOTE:

1. Apply input pulse:  2.5 V minimum to 5.5 V maximum  
0.0 V

# 54LS122

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub> t <sub>PHL1</sub>	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0 —	50 45	5.0 —	75 70	5.0 —	75 70	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 5.0 kΩ.
t <sub>PLH1</sub> t <sub>PLH1</sub>	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0 —	38 33	5.0 —	57 52	5.0 —	57 52	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 5.0 kΩ.
t <sub>PHL2</sub> t <sub>PHL2</sub>	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0 —	61 56	5.0 —	92 87	5.0 —	92 87	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 5.0 kΩ.
t <sub>PLH2</sub> t <sub>PLH2</sub>	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0 —	49 44	5.0 —	74 69	5.0 —	74 69	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 5.0 kΩ.
t <sub>PHL3</sub> t <sub>PHL3</sub>	Propagation Delay /Data-Output Output <u>High-Low</u>	5.0 —	32 27	5.0 —	48 43	5.0 —	48 43	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 5.0 kΩ.
t <sub>PLH3</sub> t <sub>PLH3</sub>	Propagation Delay /Data-Output Output <u>Low-High</u>	5.0 —	50 45	5.0 —	75 70	5.0 —	75 70	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 5.0 kΩ.
t <sub>P(min)</sub>	A or B to Q		205 200	5.0 —		5.0 —		ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 5.0 kΩ.
t <sub>PQ</sub>	A to B to Q	5.0 4.0	6.0 6.0	3.0 —	6.25 —	3.0 —	6.25 —	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ. R <sub>ext</sub> = 10 kΩ, C <sub>ext</sub> = 1000 pF.