TBB1016

Twin Built in Biasing Circuit MOS FET IC VHF/VHF RF Amplifier

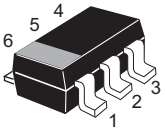
R07DS0318EJ0400
Rev.4.00
Jan 10, 2014

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Very useful for total tuner cost reduction.
- Suitable for World Standard Tuner RF amplifier.
- High gain; PG = 32 dB at 200 MHz
- Low noise; NF = 1.0 dB at 200 MHz
- Power supply voltage: 5 V

Outline

RENESAS Package code: PTSP0006JA-A
(Package name: CMPAK-6)



1. Drain(1)
2. Source
3. Drain(2)
4. Gate-1(2)
5. Gate-2
6. Gate-1(1)

Notes: 1. Marking is “RM”.
2. TBB1016 is indivisual type number of RENESAS TBBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 –0	V
Gate2 to source voltage	V_{G2S}	+6 –0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch[Note3]	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 3. Value on the glass epoxy board (50 mm × 40 mm × 1 mm)

Electrical Characteristics

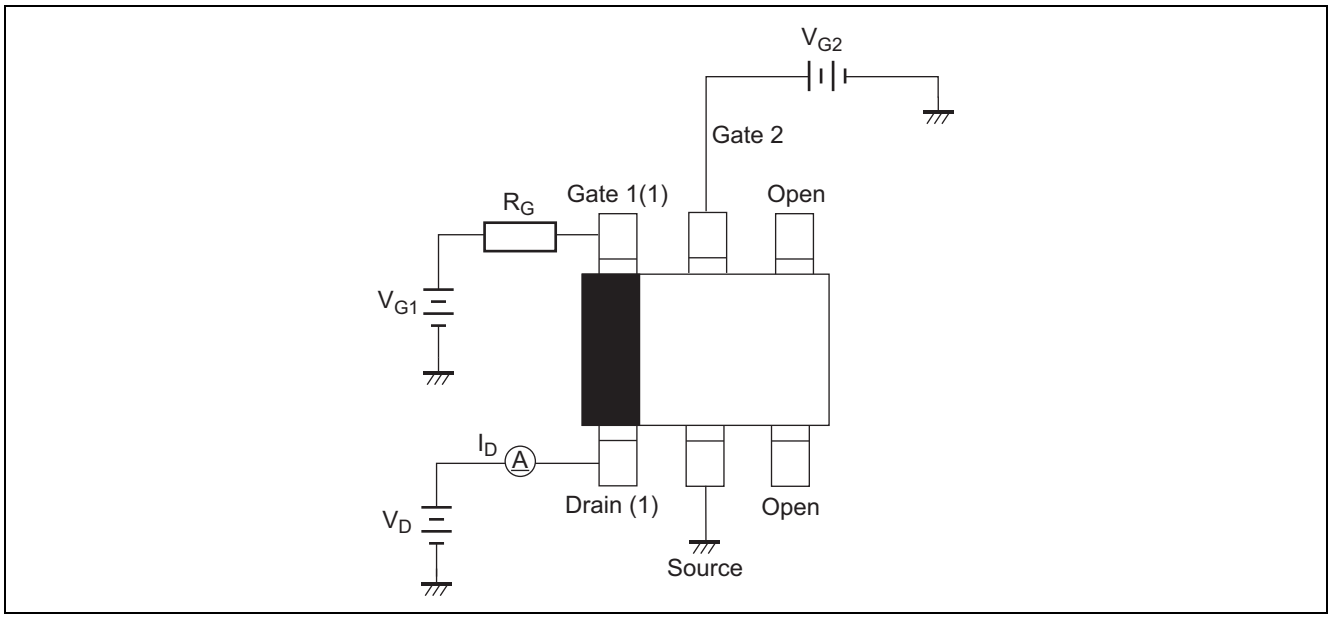
• The below specification are applicable for FET1 and FET2 unit

(Ta = 25°C)

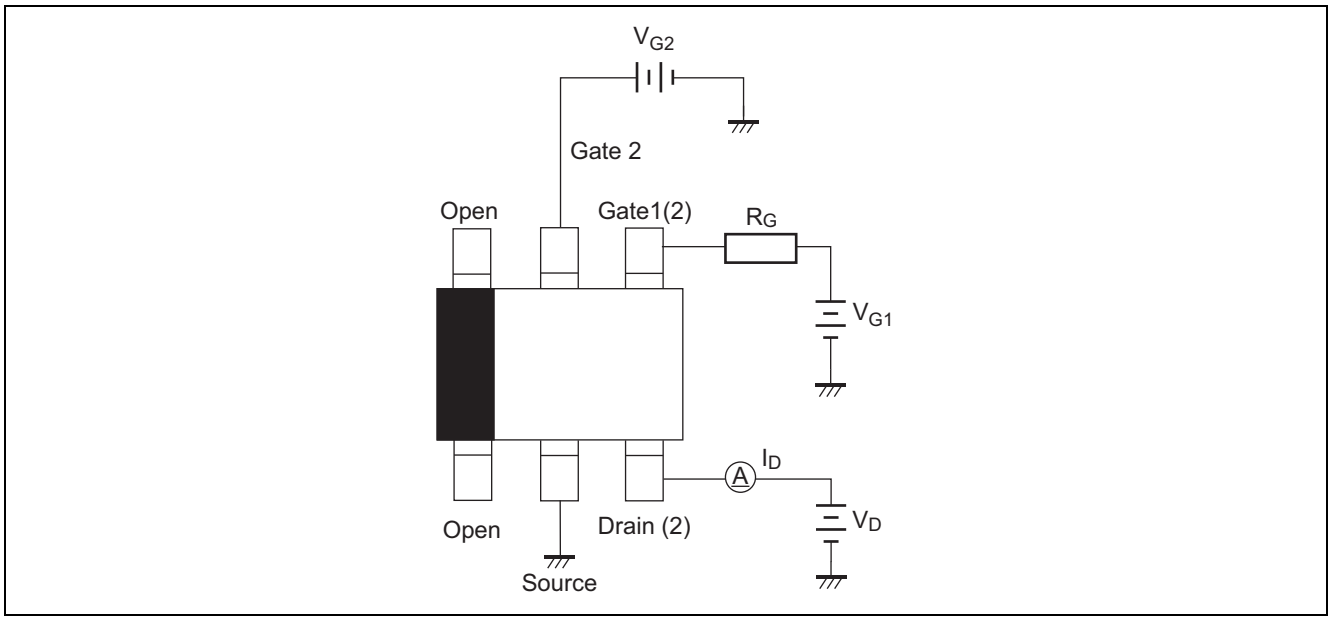
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.8	1.1	V	V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 100 µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	0.7	1.0	V	V_{DS} = 5 V, V_{G1S} = 5 V, I_D = 100 µA
Drain current	$I_{D(op)}$	11	15	19	mA	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 120 kΩ
Forward transfer admittance	$\|y_{fs}\|$	30	35	42	mS	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V, f = 1 kHz, R_G = 120 kΩ
Input capacitance	Ciss	1.8	2.2	2.6	pF	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V, f = 1 MHz, R_G = 120 kΩ
Output capacitance	Coss	0.9	1.3	1.7	pF	
Power gain	PG	27	32	37	dB	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V, R_G = 120 kΩ, f = 200 MHz
Noise figure	NF	—	1.0	1.7	dB	

DC Biasing Circuit for Operating Characteristic Items ($I_{D(op)}$, $|y_{fs}|$, Ciss, Coss, NF, PG)

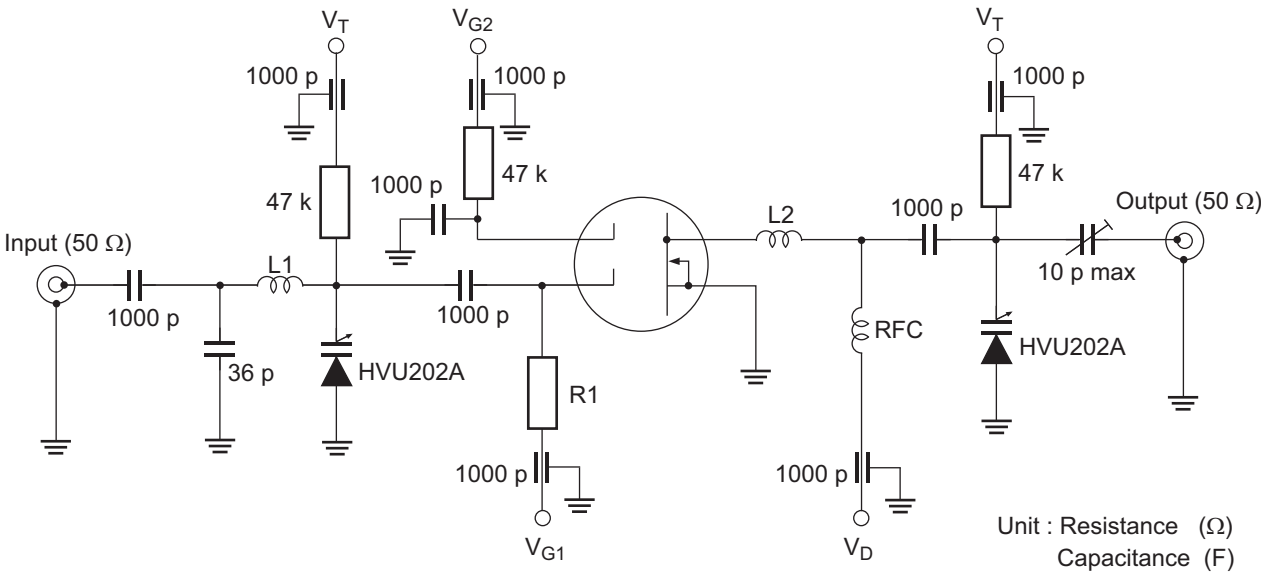
- **Measurement of FET1**



- **Measurement of FET2**



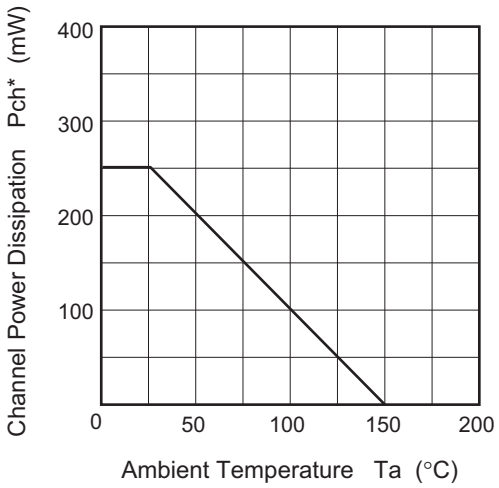
200 MHz Power Gain, Noise Figure Test Circuit



R1 : 120 kΩ
L1 : ϕ1 mm Enameled Copper Wire, Inside dia 10 mm, 2 Turns
L2 : ϕ1 mm Enameled Copper Wire, Inside dia 10 mm, 2 Turns
RFC : ϕ1 mm Enameled Copper Wire, Inside dia 5 mm, 2 Turns

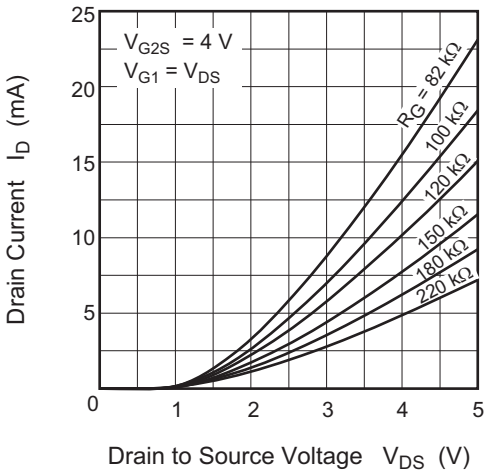
Main Characteristics

Maximum Channel Power Dissipation Curve

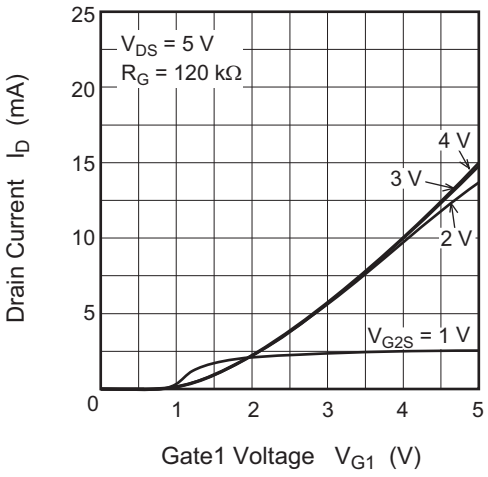


* Value on the glass epoxy board (50 mm × 40 mm × 1 mm)

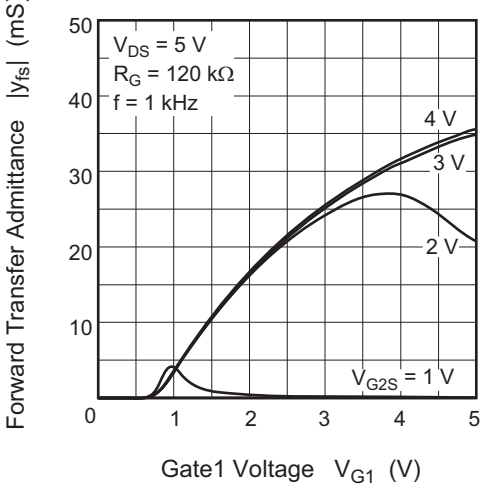
Typical Output Characteristics



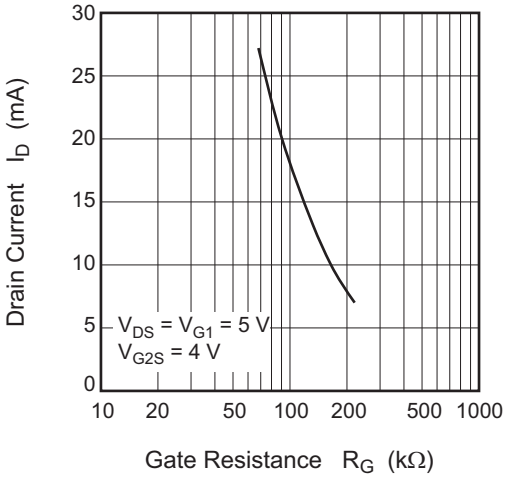
Drain Current vs. Gate1 Voltage



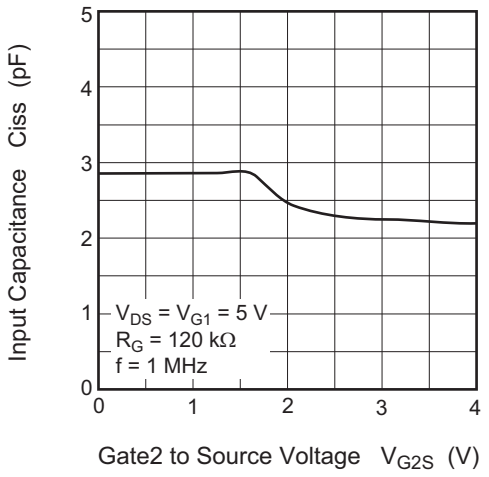
Forward Transfer Admittance vs. Gate1 Voltage



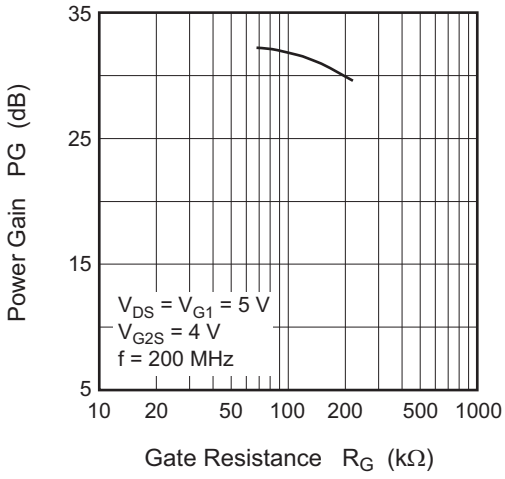
Drain Current vs. Gate Resistance



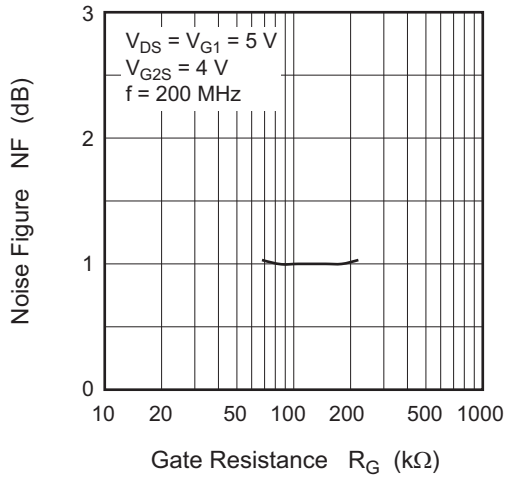
Input Capacitance vs. Gate2 to Source Voltage



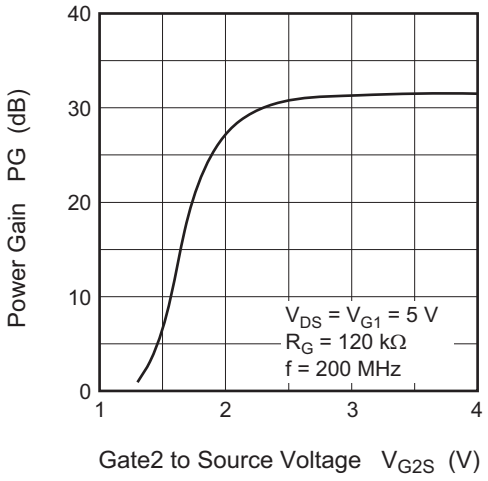
Power Gain vs. Gate Resistance



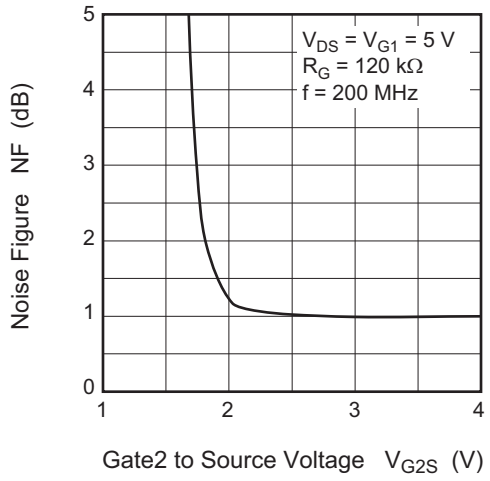
Noise Figure vs. Gate Resistance



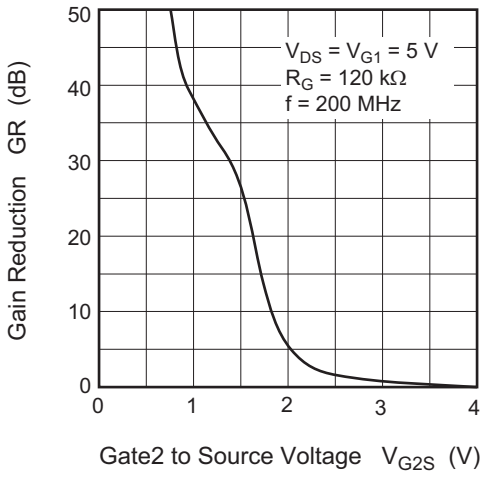
Power Gain vs.
Gate2 to Source Voltage



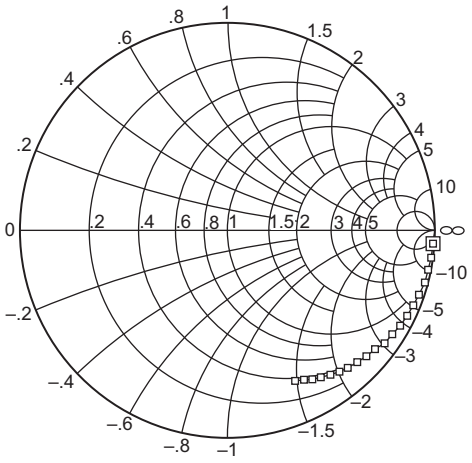
Noise Figure vs.
Gate2 to Source Voltage



Gain Reduction vs.
Gate2 to Source Voltage



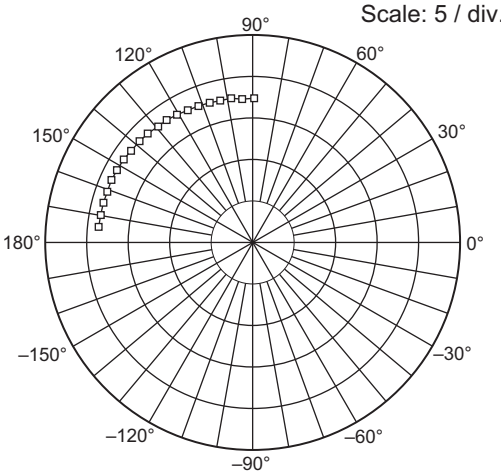
S_{11} Parameter vs. Frequency



Test condition: V_{DS} = 5 V, V_{G1} = 5 V,
V_{G2S} = 4 V, R_G = 120 kΩ
0.05 to 1.0 GHz (0.05 GHz step)

S_{21} Parameter vs. Frequency

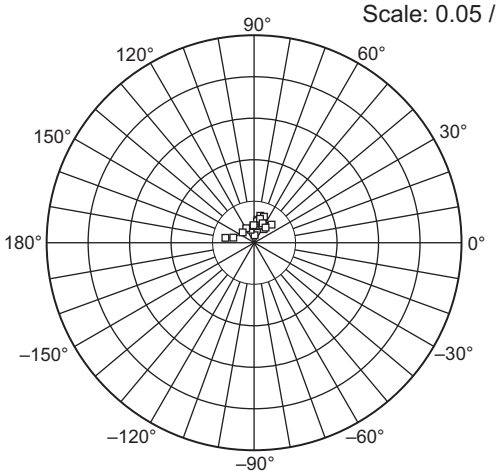
Scale: 5 / div.



Test condition: V_{DS} = 5 V, V_{G1} = 5 V,
V_{G2S} = 4 V, R_G = 120 kΩ
0.05 to 1.0 GHz (0.05 GHz step)

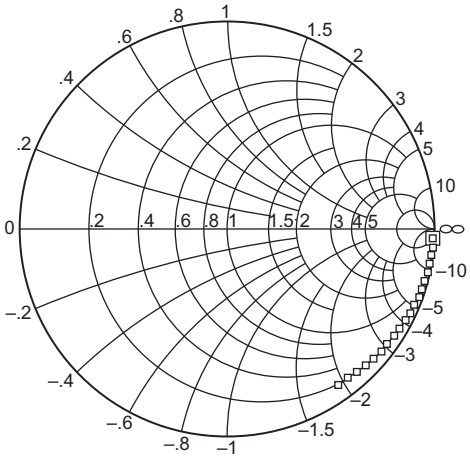
S_{12} Parameter vs. Frequency

Scale: 0.05 / div.



Test condition: V_{DS} = 5 V, V_{G1} = 5 V,
V_{G2S} = 4 V, R_G = 120 kΩ
0.05 to 1.0 GHz (0.05 GHz step)

S_{22} Parameter vs. Frequency



Test condition: V_{DS} = 5 V, V_{G1} = 5 V,
V_{G2S} = 4 V, R_G = 120 kΩ
0.05 to 1.0 GHz (0.05 GHz step)

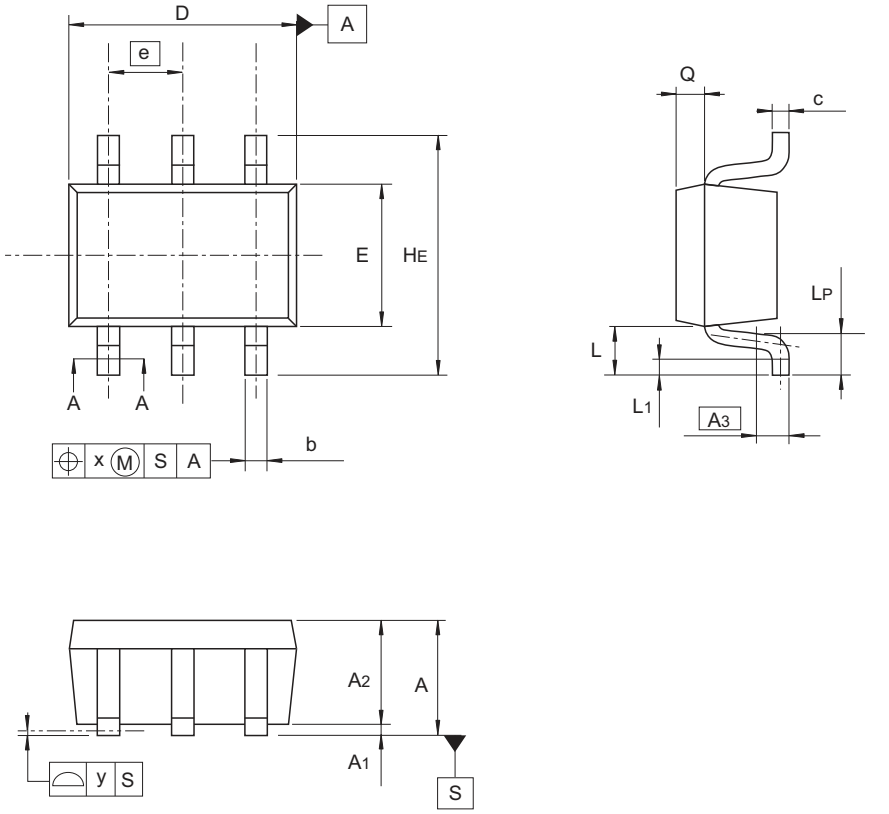
S parameter

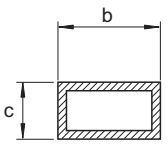
(V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V, R_G = 120 kΩ, Zo = 50 Ω)

Freq. (MHz)	S11		S21		S12		S22	
	Mag	Deg	Mag	Deg	Mag	Deg	Mag	Deg
50	0.994	–3.7	3.73	175.3	0.002	88.4	0.992	–2.4
100	0.992	–7.6	3.72	170.7	0.003	107.7	0.996	–5.1
150	0.987	–11.1	3.72	166.1	0.004	54.7	0.992	–7.2
200	0.985	–14.8	3.70	161.7	0.004	62.4	0.990	–9.6
250	0.975	–18.6	3.71	157.0	0.005	81.1	0.990	–12.0
300	0.967	–21.9	3.69	152.9	0.005	83.3	0.984	–14.6
350	0.960	–25.4	3.68	148.1	0.004	65.3	0.982	–17.1
400	0.952	–28.9	3.65	143.8	0.006	68.8	0.982	–19.4
450	0.940	–32.2	3.64	138.9	0.006	77.6	0.972	–21.9
500	0.934	–35.7	3.62	134.7	0.006	69.3	0.971	–24.6
550	0.914	–38.8	3.58	130.0	0.006	77.0	0.965	–26.9
600	0.904	–42.1	3.58	125.9	0.006	45.7	0.959	–29.9
650	0.892	–45.4	3.55	121.4	0.005	66.8	0.955	–32.5
700	0.881	–48.8	3.52	116.9	0.004	52.5	0.948	–35.6
750	0.870	–51.5	3.51	112.5	0.004	93.5	0.949	–38.3
800	0.855	–54.4	3.49	107.9	0.004	92.7	0.941	–41.4
850	0.839	–57.5	3.47	103.7	0.004	121.0	0.936	–44.4
900	0.827	–60.3	3.48	99.3	0.004	140.2	0.929	–47.7
950	0.809	–62.8	3.43	95.0	0.005	167.7	0.921	–50.9
1000	0.796	–65.7	3.43	90.3	0.007	171.4	0.921	–54.5

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-88	PTSP0006JA-A	CMPAK-6 / CMPAK-6V	0.006





A-A Section

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	0.8	—	1.1
A_1	0	—	0.1
A_2	0.8	0.9	1.0
$\boxed{A_3}$	—	0.25	—
b	0.15	0.2	0.25
c	0.1	0.15	0.25
D	1.8	2.0	2.2
E	1.15	1.25	1.35
$\boxed{e}$	—	0.65	—
H_E	2.0	2.1	2.2
L	0.3	—	0.7
L_1	0.1	—	0.5
L_P	0.2	—	0.6
x	—	—	0.05
y	—	—	0.05
Q	—	0.25	—

Ordering Information

Part Name	Quantity	Shipping Container
TBB1016RMTL-E TBB1016RMTL-H	3000 pcs	ϕ178mm reel, 8mm emboss taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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Colophon 3.0