
PART NUMBER

54LS395ABEA-ROCV

Rochester Electronics

Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

INCH-POUND

MIL-M-38510/306E
17 June 2003
SUPERSEDING
MIL-M-38510/306D
16 NOVEMBER 1987

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, LOW-POWER SCHOTTKY TTL,
SHIFT REGISTERS, CASCADABLE, MONOLITHIC SILICON

Inactive for new design after 18 April 1997.

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, low power, shift register microcircuits. Two product assurance classes and a choice of case outlines and lead finishes and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3).

1.2 Part number. The part number should be in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types should be as follows:

<u>Device type</u>	<u>Circuit</u>
01	4 bit bi-directional shift register
02	4 bit parallel-access shift register
03	4 bit parallel-access shift register
04	5 bit shift register
05	8 bit parallel-out shift register
06	4 bit right-shift, left-shift register, 3-state outputs
07	4 bit cascable shift register, 3-state outputs
08	8 bit parallel-in shift register with clock inhibit
09	8 bit parallel-in shift register with clear

1.2.2 Device class. The device class should be the product assurance level as defined in MIL-PRF-38535.

Beneficial comments (recommendations, additions deletions) and any pertinent data which may be used in improving this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P.O. Box 3990, Columbus OH 43216-5000, by using the self addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.2.3 Case outlines. The case outlines should be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
A	GDFP5-F14 or CDFP6-F14	14	Flat pack
B	GDFP4-14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
X	CQCC2-N20	20	Square leadless chip carrier
2	CQCC1-N20	20	Square leadless chip carrier

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to 7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to 5.5 V dc
Storage temperature range	-65° to +150°C
Maximum power dissipation per register, (P_D) <u>1</u> :	
Device type 01	127 mW dc
Device type 02, 03	116 mW dc
Device type 04	110 mW dc
Device type 05	149 mW dc
Device type 06, 07	160 mW dc
Device type 08	198 mW dc
Device type 09	209 mW dc
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction to case (θ_{JC}):	
Cases A, B, C, D, E, F, 2, and X	(See MIL-STD-1835)
Junction temperature (T_J) <u>2</u>	175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55° to +125°C
Minimum clock pulse width:	
Device type 01, 03, 05, 07, 09.....	20 ns
Device type 02	18 ns
Device type 04, 06, 08.....	25 ns
Minimum clear pulse width:	
Device type 01, 09	20 ns
Device type 02	15 ns
Device type 04	30 ns
Device type 05, 07	25 ns
Minimum load pulse width:	
Device type 08	30 ns
Minimum setup time at mode control:	
Device type 01	30 ns
Device type 03, 06	20 ns

1/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with MIL-PRF-38535.

Minimum setup time at shift/load:

Device type 02	25 ns
Device type 07	20 ns
Device type 08	42 ns
Device type 09	30 ns
Minimum setup time at serial data:	
Device type 08	10 ns
Minimum setup time at serial or parallel data:	
Device type 01, 02, 03, 05, 06, 07.....	20 ns
Device type 04	30 ns
Device type 09	18 ns
Minimum setup time at preset:	
Device type 04	30 ns
Minimum setup time at inhibit:	
Device type 08	30 ns
Minimum hold time:	
Device type 01, 02, 03, 04, 05, 07.....	10 ns
Device type 06	20 ns
Device type 08	3 ns
Device type 09	2 ns
Minimum enable or inhibit time of clock:	
Device type 03	20 ns
Maximum release time shift/load:	
Device type 02	10 ns

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Departments of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Unless otherwise indicated, copies of the above specifications and standards are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections and logic diagrams. The terminal connections and logic diagrams shall be as specified on figure 1.

3.3.2 Truth tables. The truth tables and timing diagrams shall be as specified on figure 2.

3.3.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3.4 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VAS) upon request.

3.3.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 12 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified		Device types	Limits		Unit
					Min	Max	
High-level output voltage	V _{OH}	V _{CC} = 4.5 V V _{IN} = 2.0 V	I _{OH} = -1.0 mA	06,07	2.4		V
			I _{OH} = -400 μA	01,02,03 04,05, 07 (QD'), 08,09	2.5		V
Low-level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IN} = 0.7 V	I _{OL} = 4 mA	01,02,03 04,05, 07 (QD'), 08,09		0.4	V
			I _{OL} = 12 mA	06,07			
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA, T _C = 25°C		All		-1.5	V
High-level input current for all inputs except S/L for type 08	I _{IH1}	V _{CC} = 5.5 V, I _{IN} = 2.7 V		01,02,05, 06,07,08, 09		20	μA
	I _{IH2}	V _{CC} = 5.5 V, I _{IN} = 5.5 V				100	
High-level input current at any input except mode	I _{IH3}	V _{CC} = 5.5 V, I _{IN} = 2.7 V		03		20	μA
	I _{IH4}	V _{CC} = 5.5 V, I _{IN} = 5.5 V				100	
High-level input current at any input except preset enable	I _{IH5}	V _{CC} = 5.5 V, I _{IN} = 2.7 V		04		20	μA
	I _{IH6}	V _{CC} = 5.5 V, I _{IN} = 5.5 V				100	
High-level input current at mode	I _{IH7}	V _{CC} = 5.5 V, I _{IN} = 2.7 V		03		40	μA
	I _{IH8}	V _{CC} = 5.5 V, I _{IN} = 5.5 V				200	
High-level input current at preset enable	I _{IH9}	V _{CC} = 5.5 V, I _{IN} = 2.7 V		04		100	μA
	I _{IH10}	V _{CC} = 5.5 V, I _{IN} = 5.5 V				500	
High-level input current at S/L	I _{IH11}	V _{CC} = 5.5 V, I _{IN} = 2.7 V		08		60	μA
	I _{IH12}	V _{CC} = 5.5 V, I _{IN} = 5.5 V				300	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Off-state output current, high level voltage applied	I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	06,07		20	μA
Off-state output current, low level voltage applied	I _{OZL}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	06,07		-20	μA
Low-level input current (for all inputs except S/L, serial in & data for types 08 and 09)	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	01,02,06	-.03	-.44	mA
			05	-.10	-.44	
			07	-.03	-.40	
			08,09	-.001	-.72	
Low-level input current at any input except clock	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	03	-.06	-.76	mA
Low-level input current at any input except preset enable	I _{IL3}		04	-.16	-.4	mA
Low-level input current at clock	I _{IL4}		03	-.03	-.44	mA
Low-level input current at preset enable	I _{IL5}		04	-.6	-2.0	mA
Low-level input current at data and serial in	I _{IL6}		08	-.100	-.380	mA
			09	-.100	-.340	mA
Low-level input current at S/L	I _{IL7}		08	-.001	-1.14	mA
			09	-.001	-.380	mA
Short-circuit output current	I _{OS}		V _{CC} = 5.5 V <u>2/</u>	01,02,03, 04,05,08, 09	-15	-100
		06,07		-15	-130	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Supply current	I _{CC}	V _{CC} = 5.5 V	04		20	mA
			02,03		21	
			01		23	
			05		27	
			06		29	
			07		34	
			08		36	
			09		38	
Maximum shift frequency	f _{MAX}	V _{CC} = 5.0 V	04	17		MHz
			06	18		
			01,03, 05,07	20		
			02	25		
			08	20		
			09	20		
Propagation delay time, low-to-high level from clock	t _{PLH1}	V _{CC} = 5.0 V, C _L = 50 pF ±10% R _L = 2 kΩ for types 01 thru 05, 08 and 09. See figures 9 and 10 for R _L for types 06 and 07	01,02	5	41	ns
			03,05		48	
			07		56	
			04		68	
			06		46	
			08		58	
			09		40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1</u> / -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Propagation delay time, low-to-high level form preset or preset enable	t _{PLH2}	V _{CC} = 5.0, C _L = 50 pF ±10% R _L = 2 kΩ for types 01 thru 05, 08 and 09. See figures 9 and 10 for R _L types 06 and 07	02	5	53	ns
			04		60	
Propagation delay time, high-to-low level from clock	t _{PLH1}		01,02	5	47	ns
			03,05,07		56	
			04		68	
			06		52	
			08		58	
			09		46	
			Propagation delay time, high-to-low level from clear		t _{PLH2}	
07	56					
05	62					
04	90					
Propagation delay time, low to high level from S/L	t _{PLH5}		08,09	5	52	ns
Propagation delay time, high to low level from S/L or clear	t _{PHL5}		08,09	5	52	ns
Propagation delay time, high to low level from data	t _{PHL3}		08	5	46	ns
Propagation delay time, low to high level from data	t _{PLH3}		08	5	39	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Propagation delay time, low to high level from data	t _{PLH4}	V _{CC} = 5.0 V, C _L = 50 pF ±10% R _L = 2kΩ for types 01 thru 05, 08 and 09. See figures 9 and 10 for R _L types 06 and 07	08	5	46	ns
Propagation delay time, high to low level from data	t _{PHL4}		08	5	39	ns
Output enable time to low level	t _{ZL}	See figures 9 and 10 for conditions	06	5	45	ns
			07	5	53	ns
Output enable time to high level	t _{ZH}		06	5	39	ns
			07		53	
Output disable time from low level	t _{LZ}		07	5	53	ns
			06		71	
Output disable time from high level	t _{HZ}		07	5	53	ns
			06		84	

1/ Complete terminal condition shall be as specified in table III.2/ Not more than one output should be shorted at a time.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B test when using the method 5005 QCI option.	1, 2, 3, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 9, 10, 11	1, 2, 3
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535 .

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

Pin number	Device type 01		Device type 02		Device type 03		Device type 04	
	CASES							
	2, X	E,F	2, X	E,F	2, X	A,B,C, and D	2, X	E,F
1	NC	CLEAR	NC	CLR	NC	SER INP	NC	CLK
2	CLEAR	SHF RHT SER INP	CLR	J	SER INP	A	CLK	A
3	SHF RHT SER INP	A	J	$\overline{K}$	A	B	A	B
4	A	B	$\overline{K}$	A	B	C	B	C
5	B	C	A	B	NC	D	C	V _{CC}
6	NC	D	NC	C	C	MODE CONT	NC	D
7	C	SHF LEFT SER INP	B	D	NC	GND	V _{CC}	E
8	D	GND	C	GND	D	CLK 2 L SHF LOAD	D	PRESET ENABLE
9	SHF LEFT SER INP	SO	D	SHF/ LOAD	MODE CONT	CLK1 R SHF	E	SER INP
10	GND	S1	GND	CLK	GND	QD	PRESET ENABLE	QE
11	NC	CLOCK	NC	$\overline{Q}$ D	NC	QC	NC	QD
12	SO	QD	SHF/LOAD	Q D	CLK 2 L SHF/LOAD	QB	SER INP	GND
13	S1	QC	CLK	QC	CLK1 R SHF	QA	QE	QC
14	CLK	QB	$\overline{Q}$ D	QB	QD	V _{CC}	QD	QB
15	QD	QA	QD	QA	NC		GND	QA
16	NC	V _{CC}	NC	V _{CC}	QC		NC	CLR
17	QC		QC		NC		QC	
18	QB		QB		QB		QB	
19	QA		QA		QA		QA	
20	V _{CC}		V _{CC}		V _{CC}		CLR	

FIGURE 1. Terminal connections.

Pin number	Device type 05		Device type 06		Device type 07		Device type 08	
	2, X	A,B,C, and D	2, X	A,B,C and D	2, X	E,F	2, X	E, F
1	NC	A	NC	SER INP	NC	CLR	NC	SHF LOAD
2	A	B	SER INP	A	CLR	SER INP	SHF LOAD	CLOCK
3	B	QA	A	B	SER INP	A	CLOCK	E
4	QA	QB	B	C	A	B	E	F
5	NC	QC	NC	D	B	C	F	G
6	QB	QD	C	MODE CONT	NC	D	NC	H
7	NC	GND	NC	GND	C	LOAD SHF	G	$\bar{Q}$ H
8	QC	CLK	D	OUTPUT CONT	D	GND	H	GND
9	QD	CLR	MODE CONT	CLK	LOAD SHF	OUTPUT CONT	$\bar{Q}$ H	QH
10	GND	QE	GND	QD	GND	CLK	GND	SER INP
11	NC	QF	NC	QC	NC	QD'	NC	A
12	CLK	QG	OUTPUT CONT	QB	OUTPUT CONT	QD	QH	B
13	CLR	QH	CLK	QA	CLK	QC	SER INP	C
14	QE	V _{CC}	QD	V _{CC}	QD'	QB	A	D
15	NC		NC		QD	QA	B	CLOCK INHIBIT
16	QF		QC		NC	CC	NC	V _{CC}
17	NC		NC		QC		C	
18	QG		QB		QB		D	
19	QH		QA		QA		CLOCK INHIBIT	
20	V _{CC}		V _{CC}		V _{CC}		V _{CC}	

FIGURE 1. Terminal connections - Continued.

Pin number	Device type 09	
	2, X	E,F
1	NC	SERIAL INPUT
2	SERIAL INPUT	A
3	A	B
4	B	C
5	C	D
6	NC	CLOCK INHIBIT
7	D	CLOCK
8	CLOCK INHIBIT	GND
9	CLK	CLEAR
10	GND	E
11	NC	F
12	CLR	G
13	E	OUTPUT QH
14	F	INPUT H
15	G	SHIFT LOAD
16	NC	V _{CC}
17	QH	
18	INPUT H	
19	SHIFT LOAD	
20	V _{CC}	

FIGURE 1. Terminal connections - Continued.

Device type 01

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L'	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

H = high level (steady state)

L = low level (steady state)

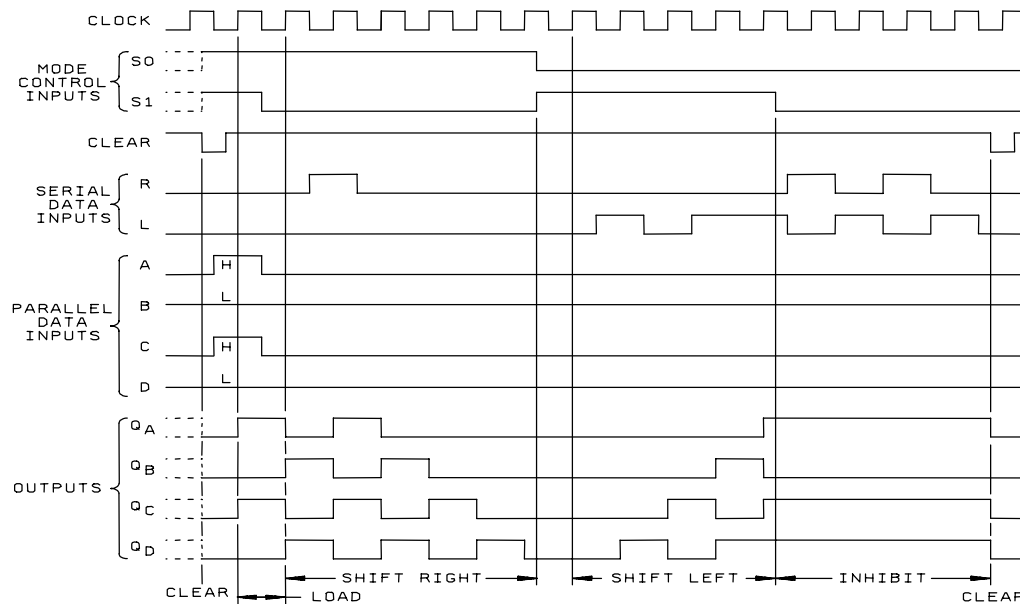
X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the most recent ↑ transition of the clock.

Typical clear, load, right-shift, left shift, inhibit, and clear sequences.

FIGURE 2. Truth tables and timing diagrams.

Device type 02

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q _{A0}	Q _{A0}	Q _{Bn}	Q _{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)

L = low level (steady state)

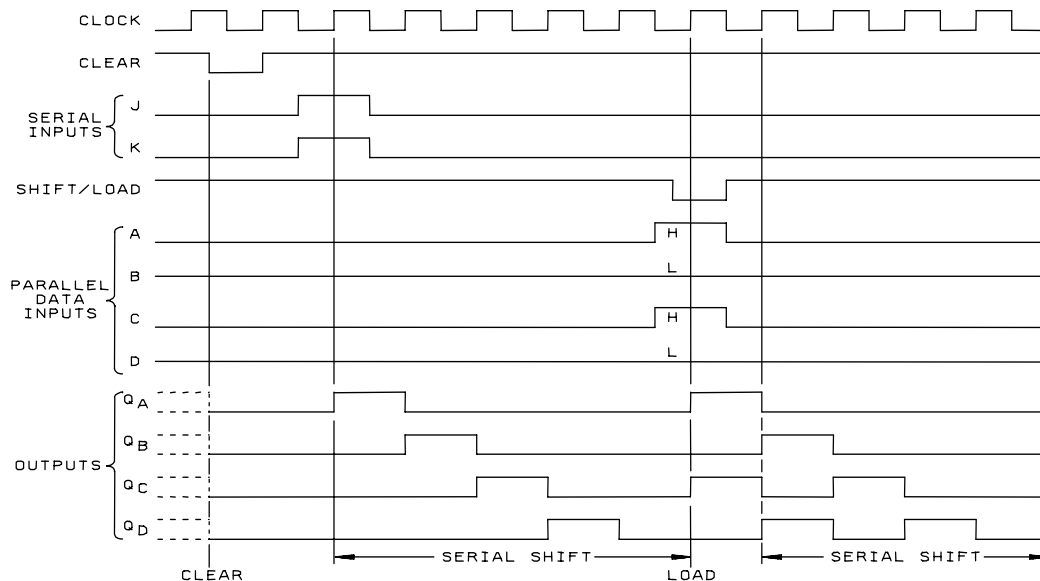
X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.Q_{An}, Q_{Bn}, Q_{Cn}, = the level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock.

Typical clear, shift, and load sequences.

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 03

MODE CONTROL	CLOCKS		SERIAL	PARALLEL				Q _A	Q _B	Q _C	Q _D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q _B ↑	Q _C ↑	Q _D ↑	d	Q _{Bn}	Q _{Cn}	Q _{Dn}	d
L	L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
L	X	↓	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
L	X	↓	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
↑	L	L	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↓	L	L	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↓	L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↑	H	L	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
↑	H	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

*Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C.
Serial data is entered to input D.

H = High level (steady state), L = Low level (steady state),

X = Irrelevant (any input, including transitions)

↓ = Transition from high to low level, ↑ = Transition from low to high level a, b, c,

d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = level of Q_A, Q_B, Q_C, or Q_D, respectively,
before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively,
most recent ↓ transition of the clock.

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 04

INPUTS													
CLEAR	PRESET ENABLE	PRESET					CLOCK	SERIAL	Q _A	Q _B	Q _C	Q _D	Q _E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	H	H	L	H	L	H	L	X	H	Q _{B0}	H	Q _{D0}	H
H	L	X	X	X	X	X	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	L	X	X	X	X	X	↑	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}
H	L	X	X	X	X	X	↑	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc., respectively before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively before the most recent ↑ transition of the clock.

Typical clear, shift, preset and shift sequences

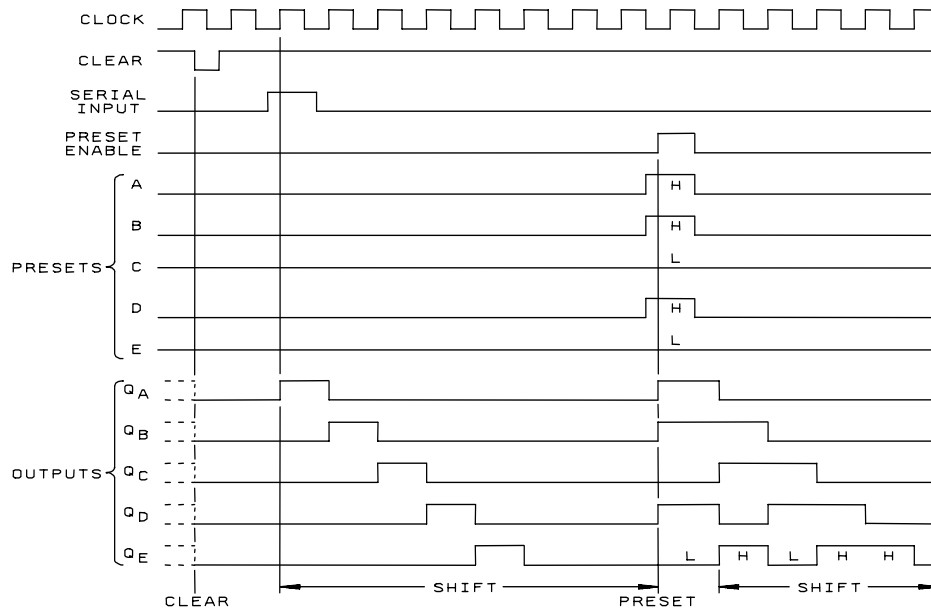


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 05

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B , or Q_H , respectively, before the indicated steady state input conditions were established.

Q_{An} , Q_{Gn} = the level of Q_A , or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

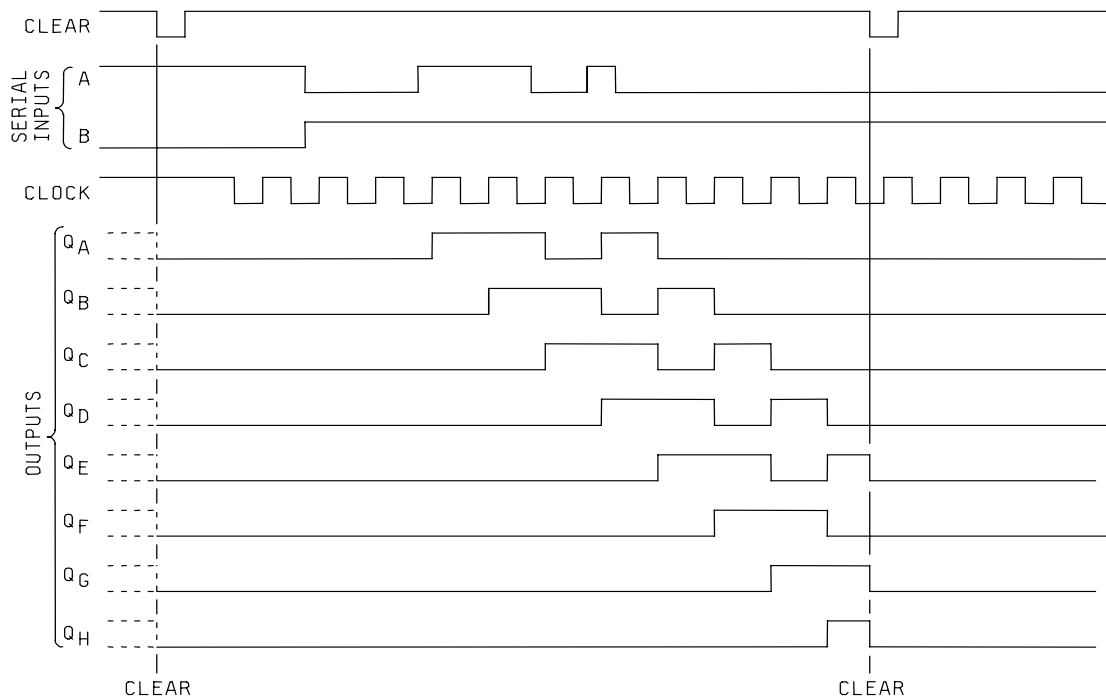


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 06

INPUTS							OUTPUTS			
MODE CONTROL	CLOCK	SERIAL	PARALLEL				Q _A	Q _B	Q _C	Q _D
			A	B	C	D	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q _B ↑	Q _C ↑	Q _D ↑	d	Q _{Bn}	Q _{Cn}	Q _{Dn}	d
L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
L	↓	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
L	↓	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}

When the output control is low, the outputs are disabled to high impedance state. however, sequential operation of the registers is not affected.

*Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered to input D.

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↓ = transition from high to low level.

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Device type 07

INPUTS								3 STATE OUTPUTS				CASCADE OUTPUT Q _{D'}
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL				Q _A	Q _B	Q _C	Q _D	
				A	B	C	D	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	L	↓	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	L	↓	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}

When the output control is low, the outputs are disabled to high impedance state. however, sequential operation of the registers is not affected.

H = high level (steady state), L = low level (steady state),

X = irrelevant (any input, including transitions)

↓ = transition from high to low level.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 08

Shift/ load	Inputs				Internal Outputs		Output Q_H
	Clock inhibit	Clock	Serial	Parallel A....H	Q_A	Q_B	
L	X	X	X	a.....h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High level (steady state), L = Low level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level

Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B , or Q_H , respectively, before the indicated steady state input conditions were established.

Q_{An} , Q_{Gn} = The level of Q_A or Q_G before the most recent transition of the clock; indicates a one-bit shift.

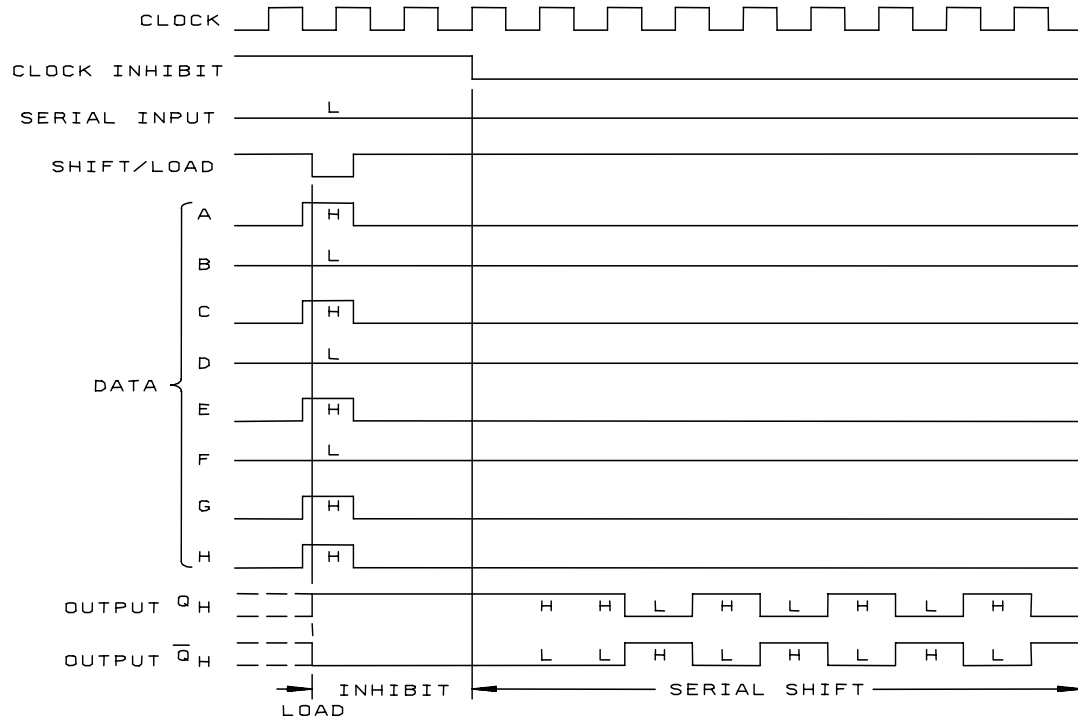


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 09

Clear	Shift/ load	Clock inhibit	Clock	Serial	Parallel	Internal Outputs		Output Q_H
					A....H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a....h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High level (steady state), L = Low level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level

Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B , or Q_H respectively, before the indicated steady state input conditions were established.

Q_{An} , Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

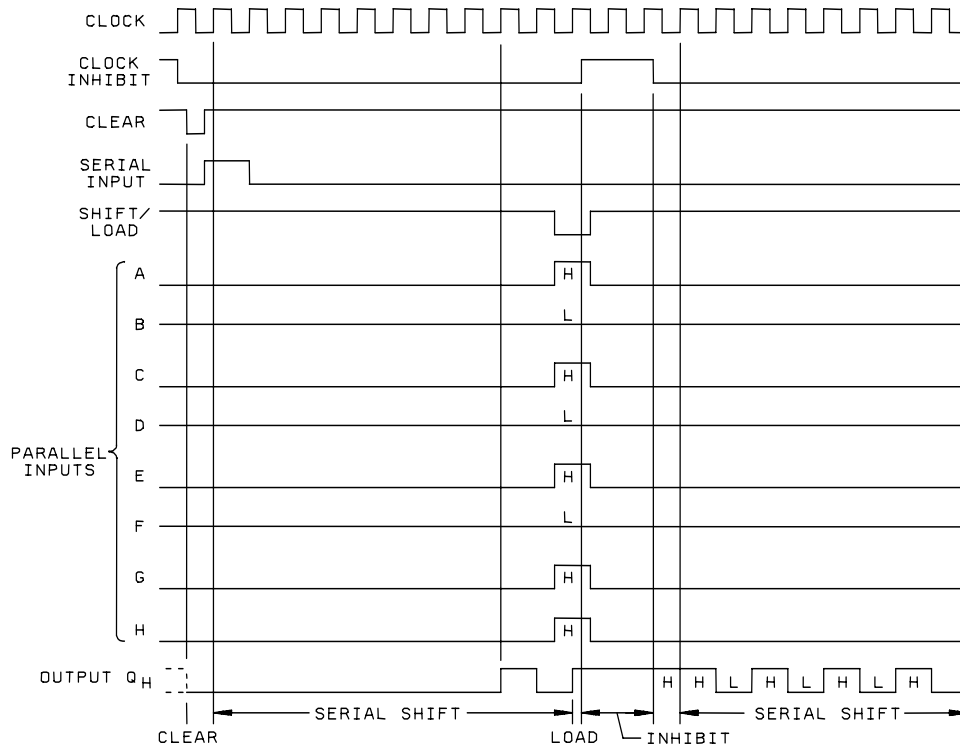
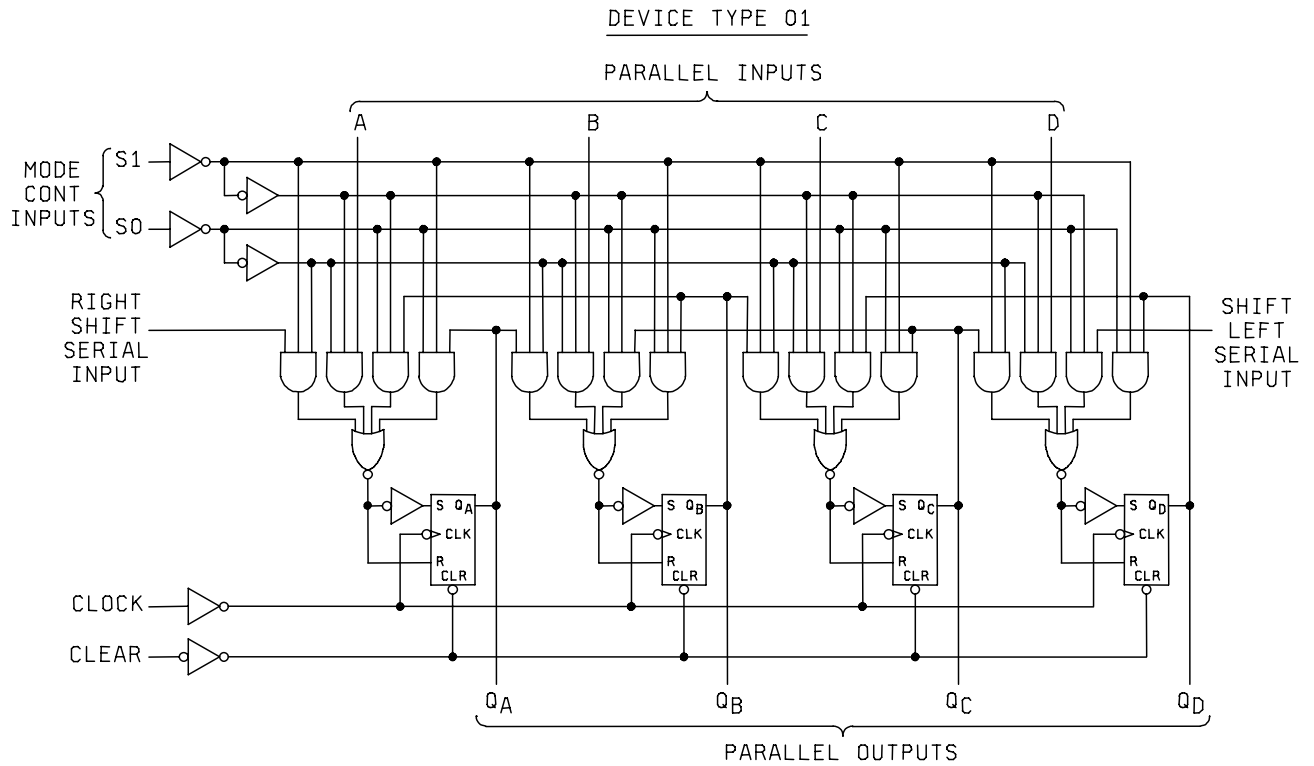
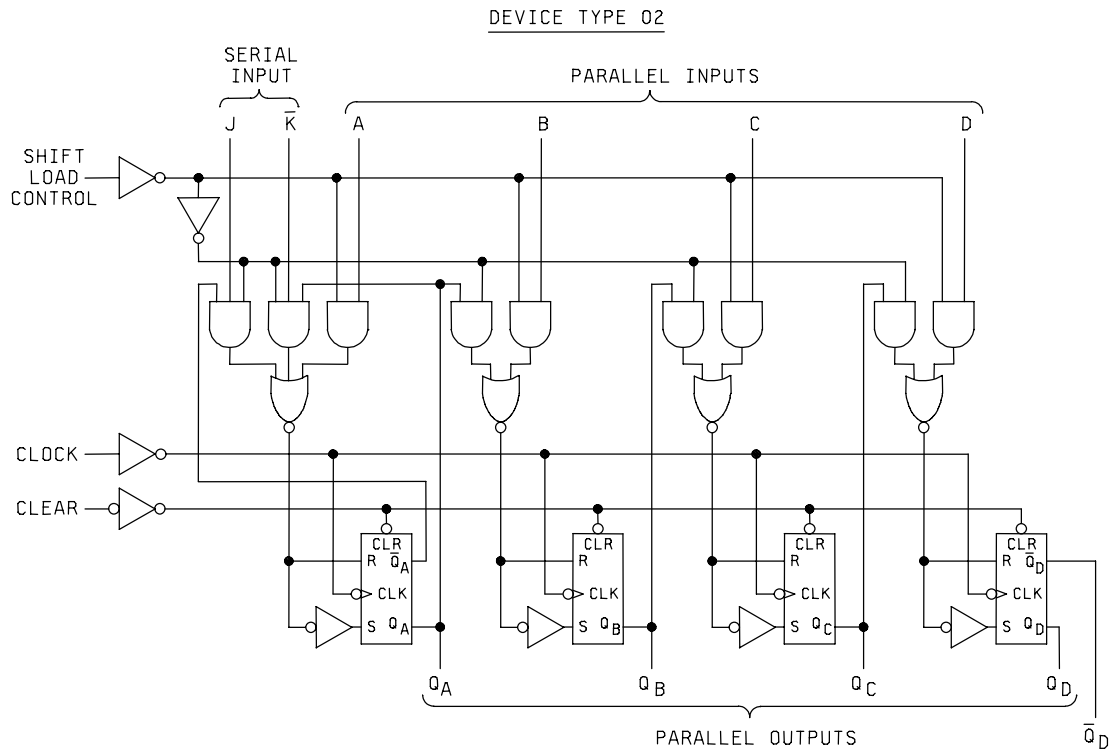


FIGURE 2. Truth tables and timing diagrams - Continued.

FIGURE 3. Logic diagrams.



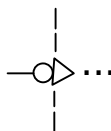
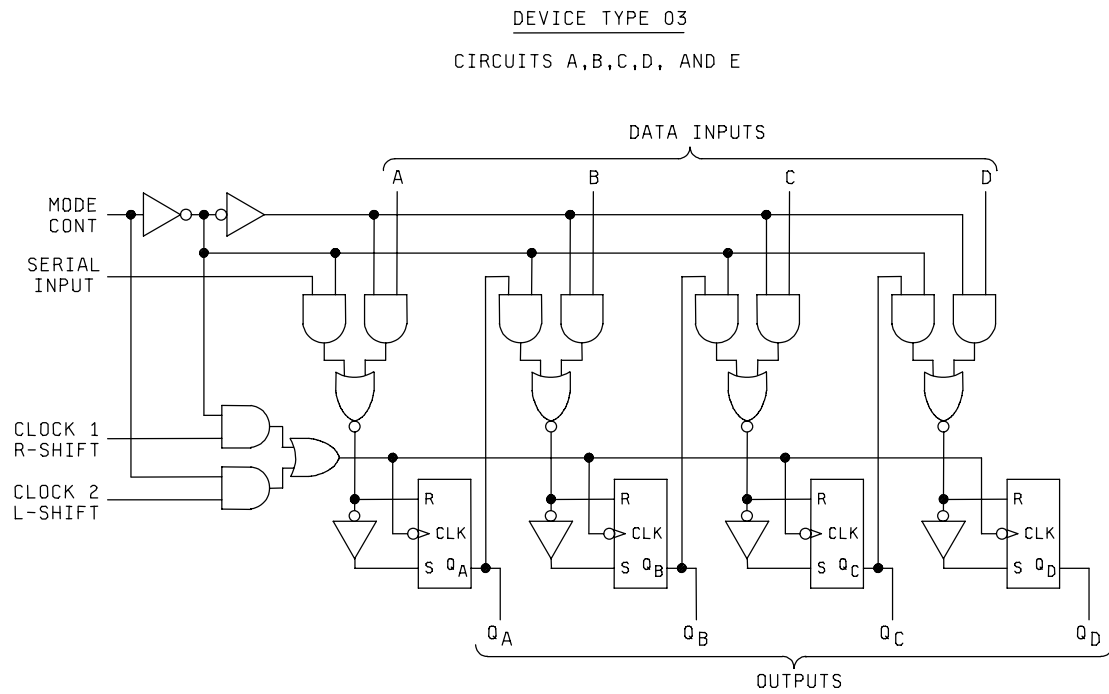
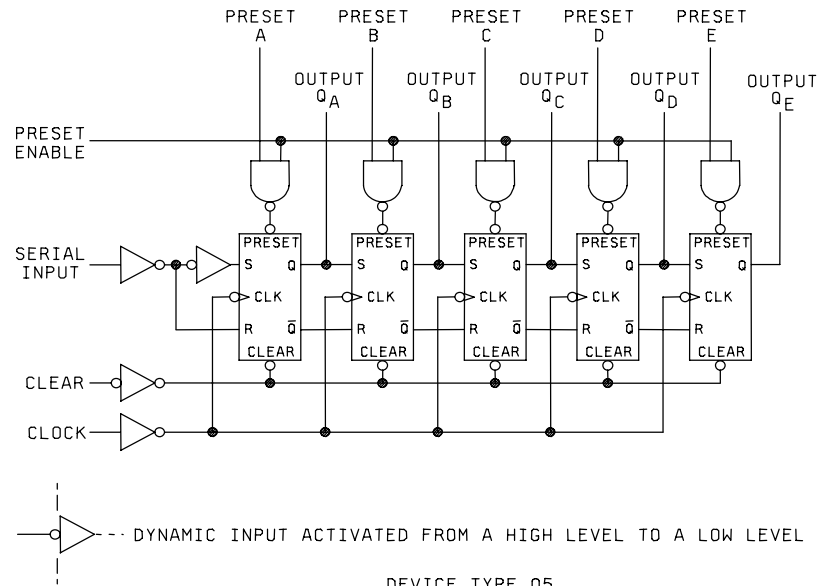
 ... dynamic input activated from a high level to a low level

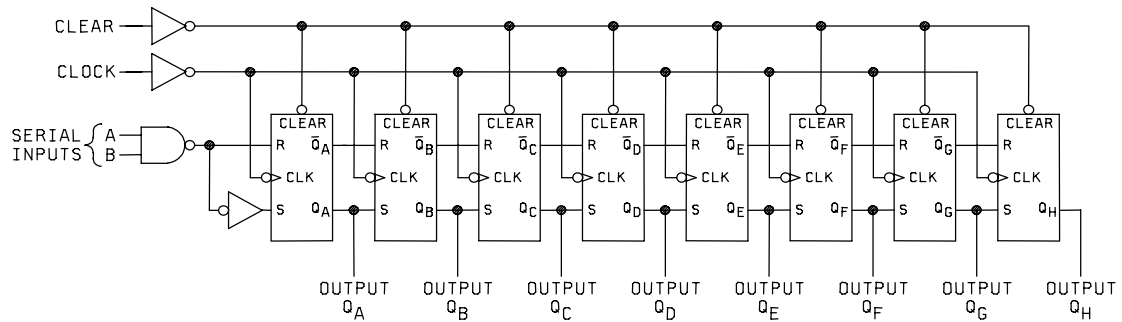
FIGURE 3. Logic diagrams - Continued.

FIGURE 3. Logic diagrams - Continued.

DEVICE TYPE 04



DEVICE TYPE 05

FIGURE 3. Logic diagram - Continued.

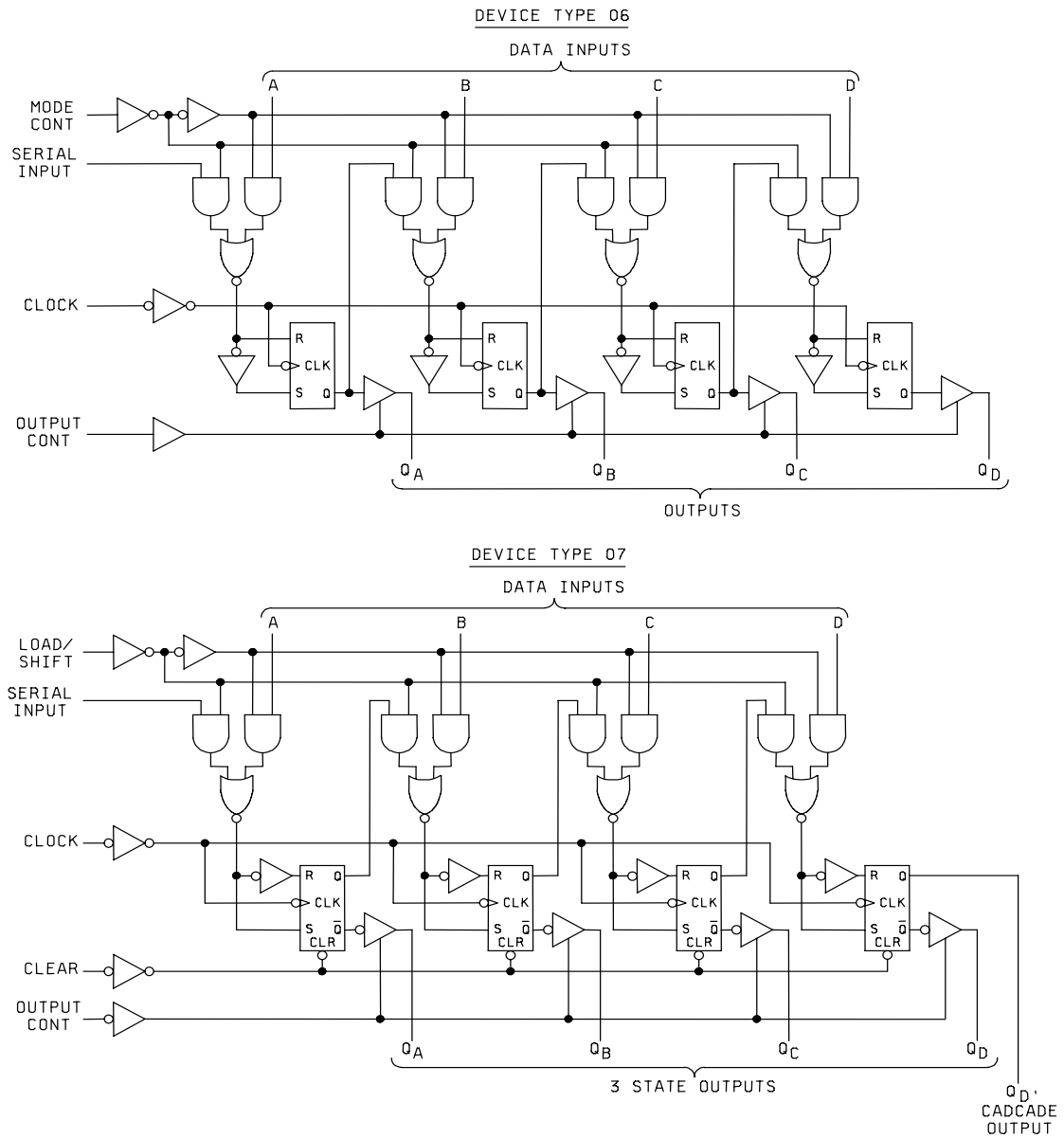
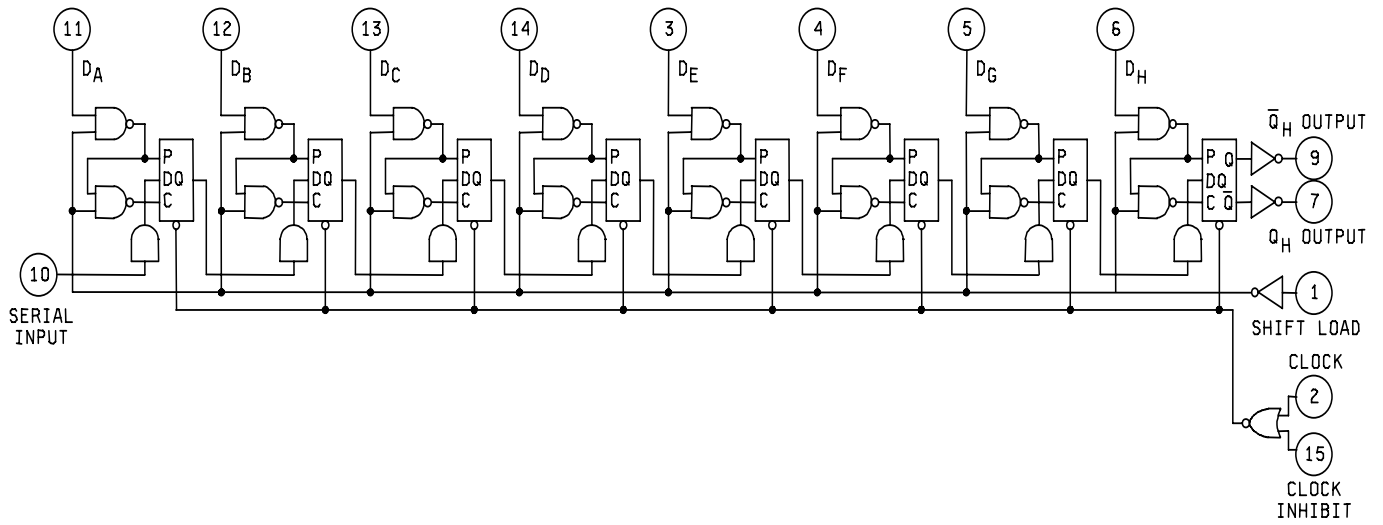


FIGURE 3. Logic diagrams - Continued.

DEVICE TYPE 08

CIRCUIT A

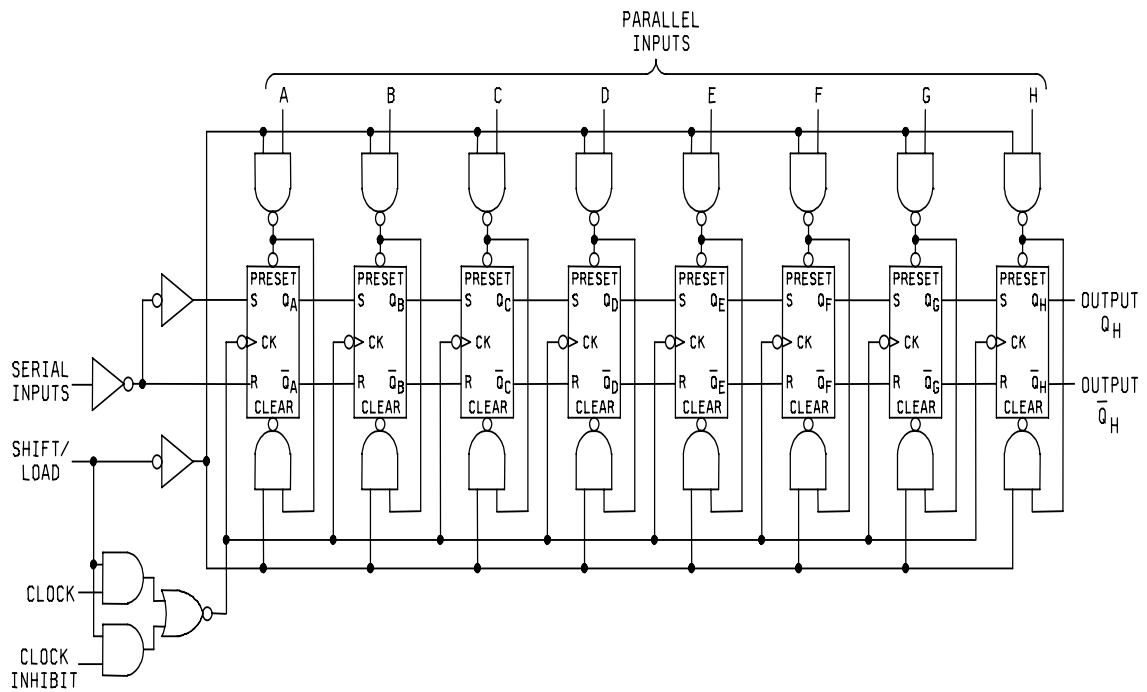


Pin numbers are for cases E and F only.

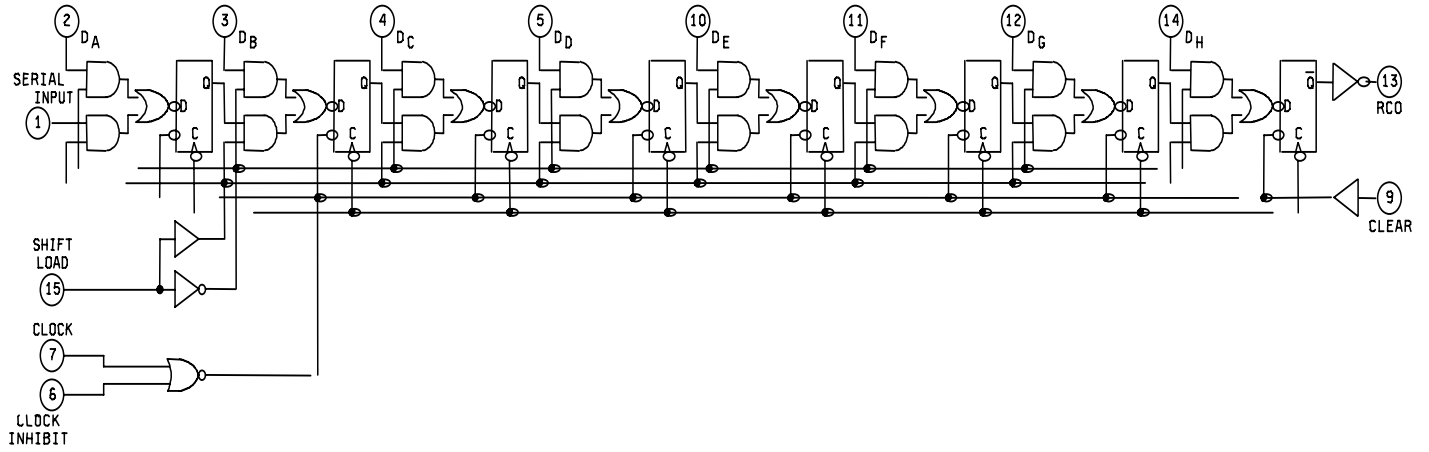
FIGURE 3. Logic diagrams - Continued.

DEVICE TYPE 08

CIRCUIT C AND F

FIGURE 3. Logic diagrams - Continued.

Device Type 09



Pin numbers are for cases E and F only.

FIGURE 3. Logic diagrams - Continued.

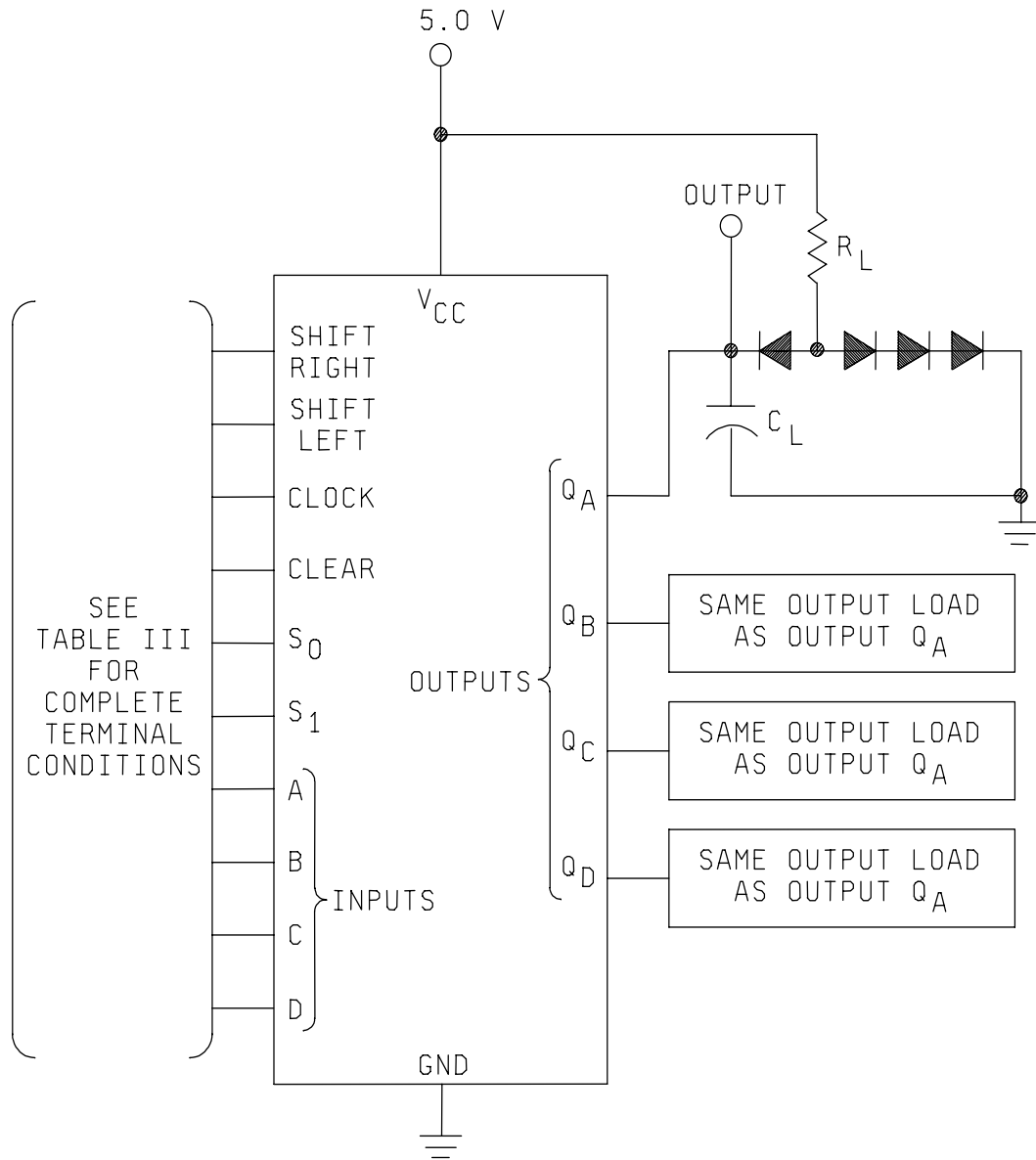
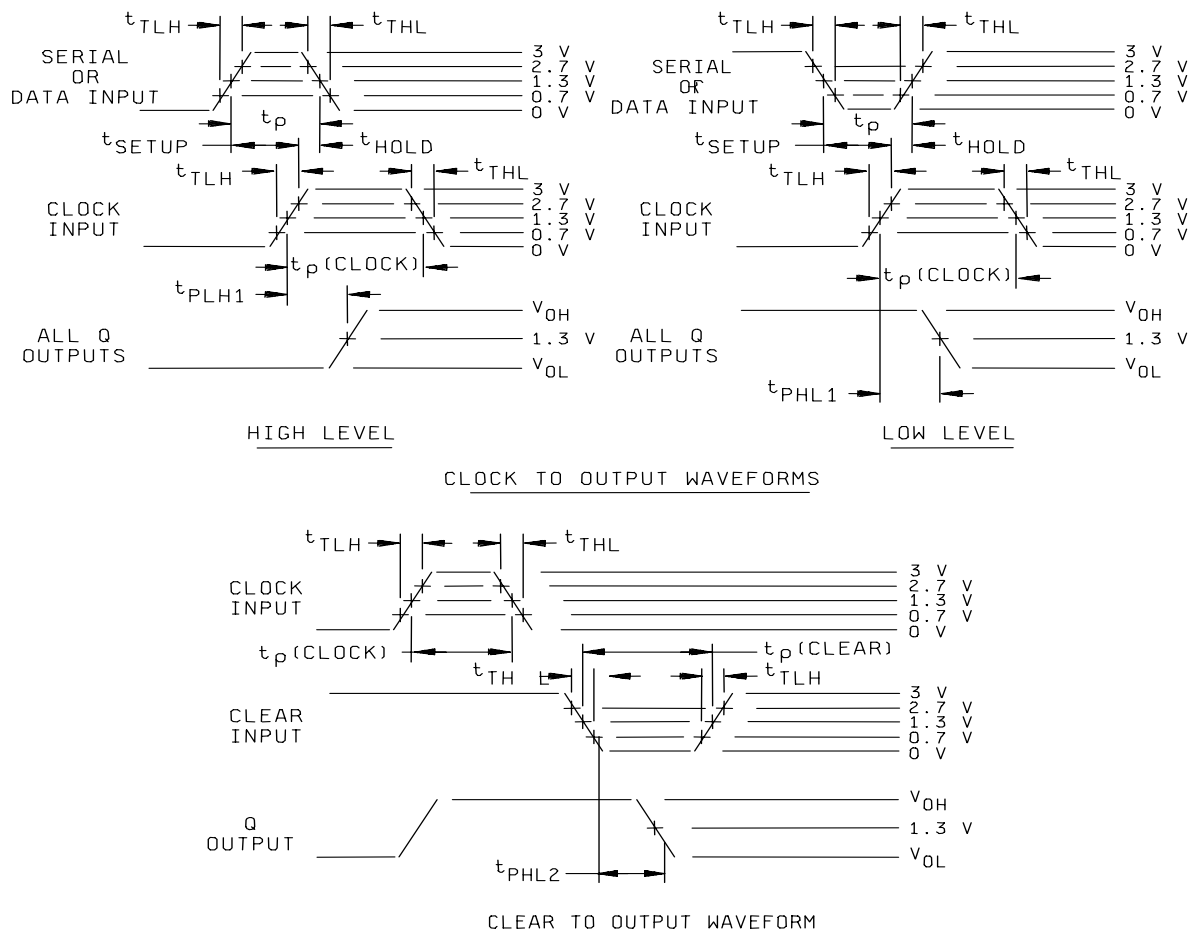


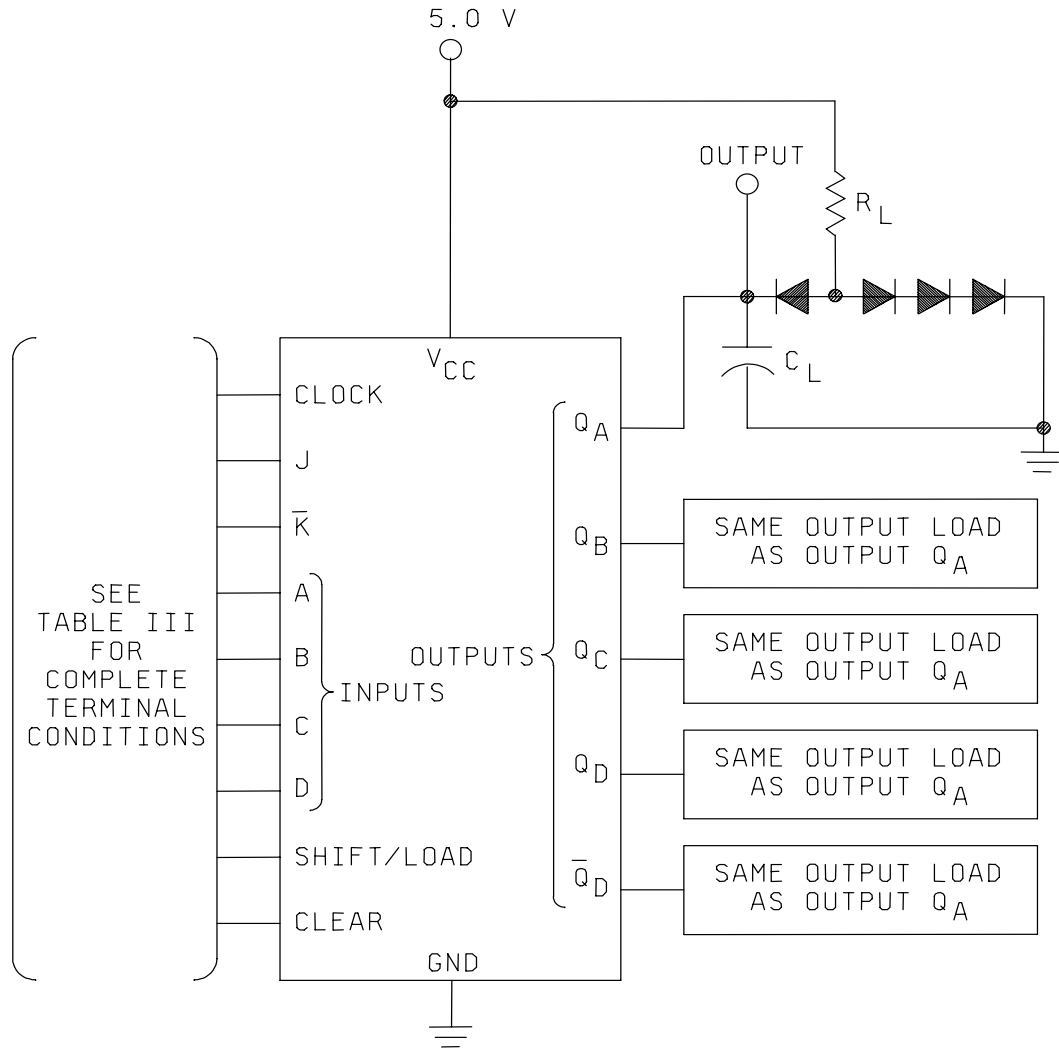
FIGURE 4. Switching test circuit and waveforms for device type 01.



NOTES:

1. Clock pulse characteristics: $PRR \leq 1.0$ Mhz, $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, $t_p(\text{clock}) \geq 20$ ns.
2. Serial or data pulse characteristics: $t_{THL} \leq 15$ ns, $t_{THL} \leq 6$ ns, $t_{SETUP} = 20$ ns, $t_{HOLD} = 10$ ns, $t_p(\text{serial})$ or $t_p(\text{data}) = 30$ ns.
3. Clear pulse characteristics: $t_{THL} \leq 15$ ns, $t_{THL} \leq 6$ ns; $t_p(\text{clear}) = 20$ ns.
4. $C_L = 50$ pF ± 10 percent including scope, probe, wiring and stray capacitance without package in test fixture.
5. All diodes are 1N3064, 1N916 or equivalent.
6. $R_L = 2.0$ k Ω ± 5 percent.
7. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 4. Switching test circuit and waveforms for device type 01 - Continued.

FIGURE 5. Switching test circuit and waveforms for device type 02.

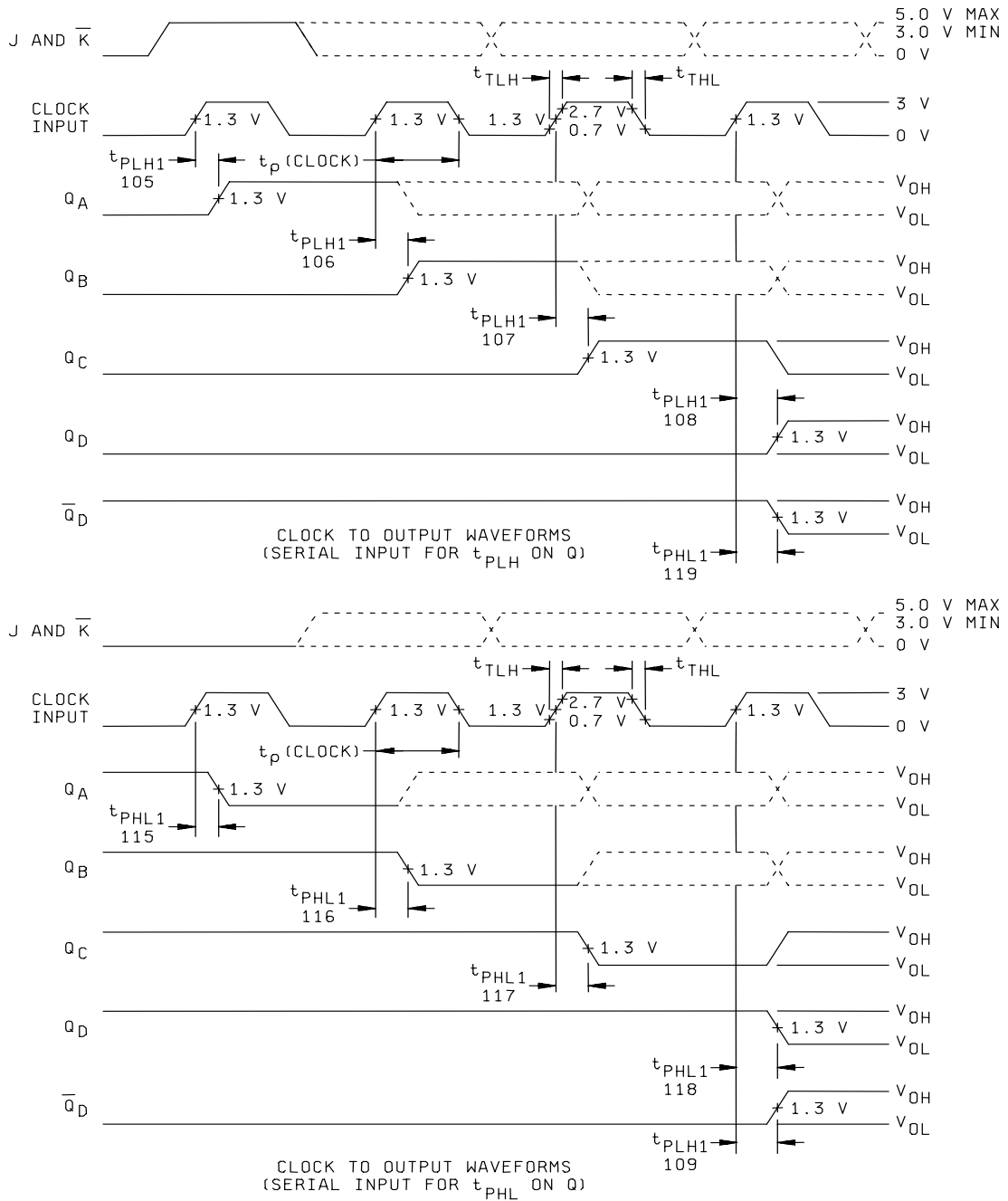
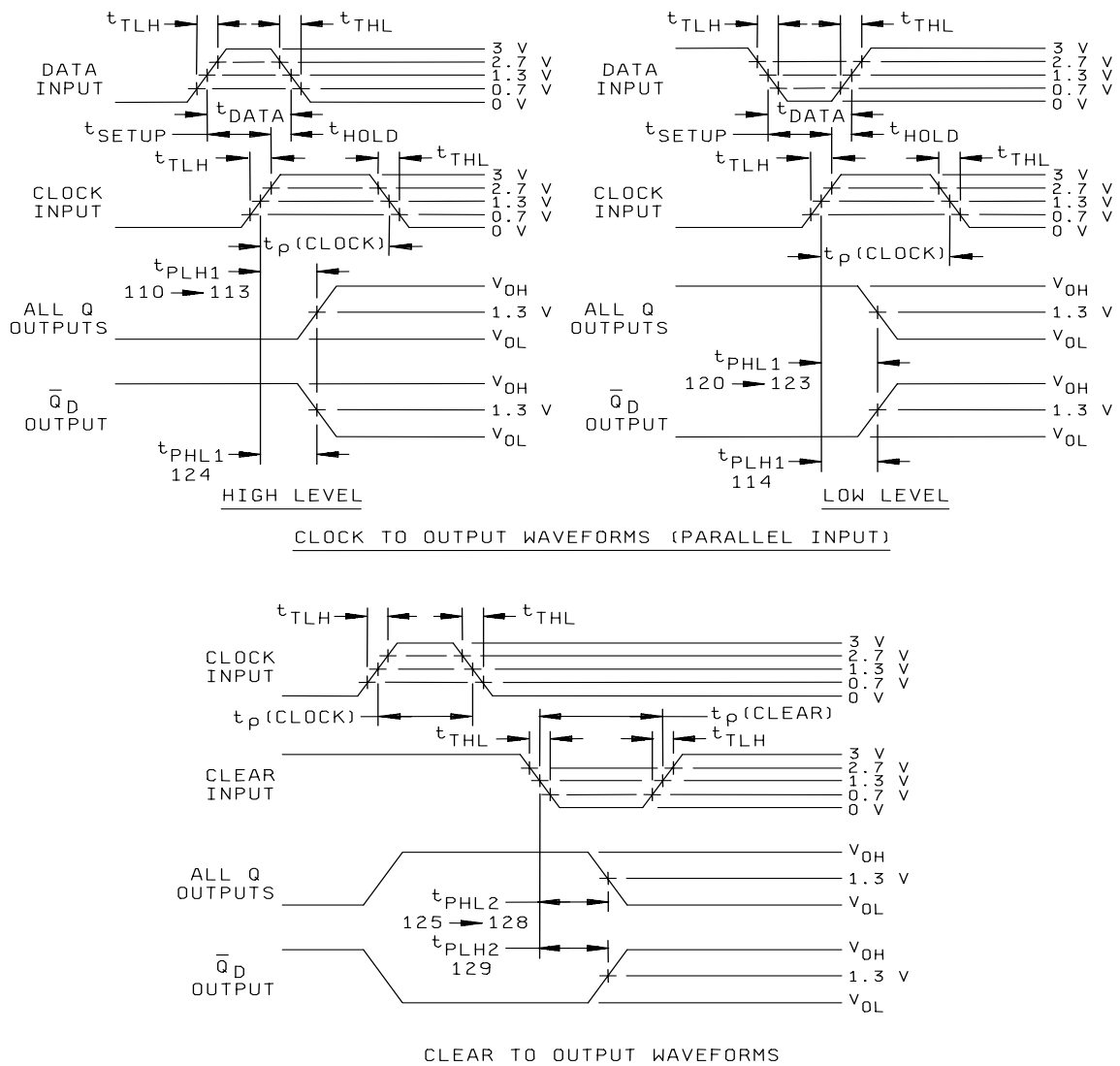


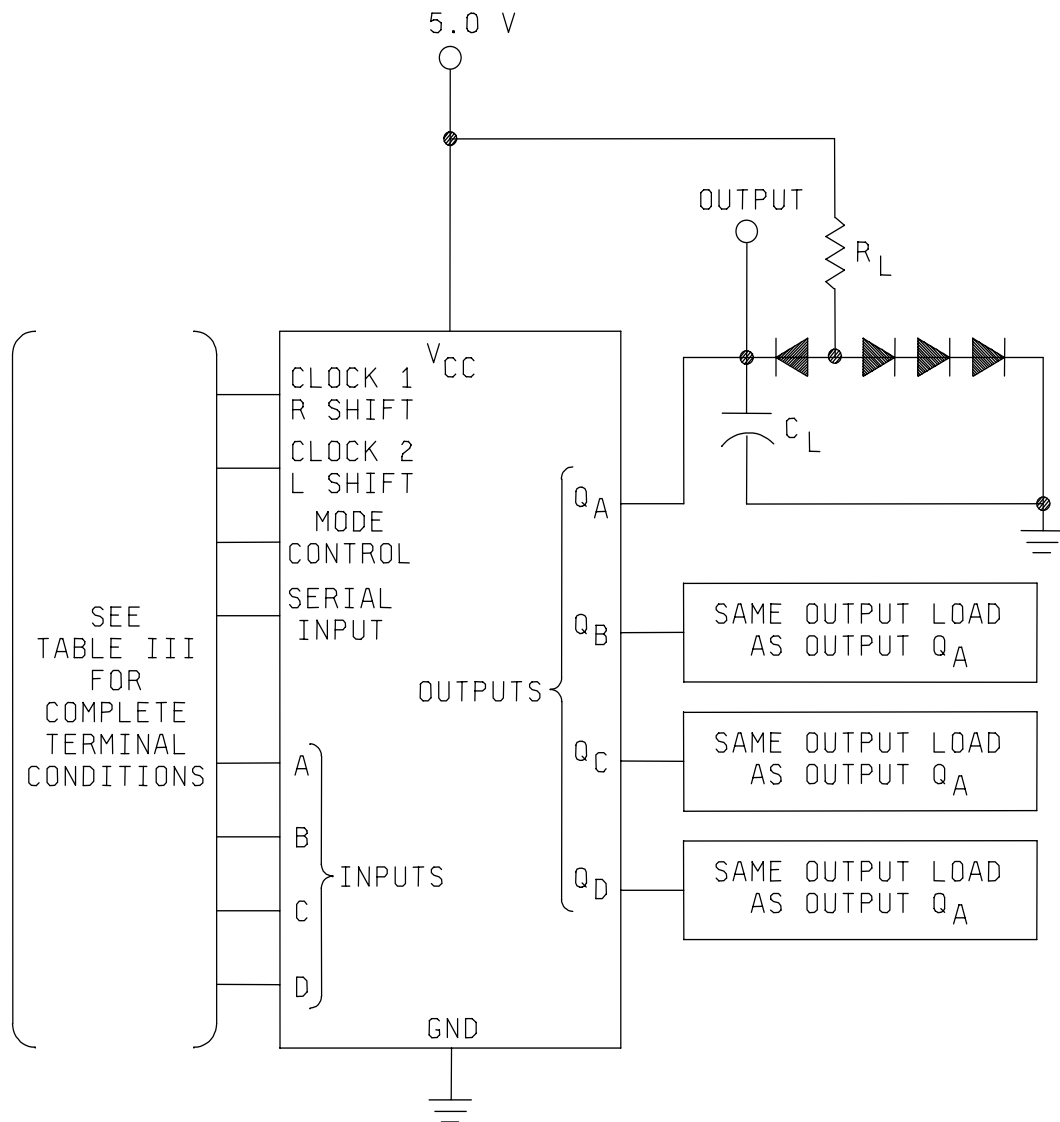
FIGURE 5. Switching test circuit and waveforms for device type 02 - Continued.



NOTES:

1. Clock pulse characteristics: $PRR \leq 1.0$ MHz, $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, $t_p(\text{clock}) \geq 18$ ns.
2. Data pulse characteristics: $t_{TLH} \leq 20$ ns, $t_{THL} \leq 6$ ns, $t_{SETUP} = 20$ ns, $t_{HOLD} = 10$ ns, $t_{DATA} = 30$ ns.
3. Clear pulse characteristics: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns; $t_p(\text{clear}) = 15$ ns.
4. $C_L = 50$ pF ± 10 percent including scope, probe, wiring and stray capacitance without package in test fixture.
5. All diodes are 1N3064, 1N916 or equivalent.
6. $R_L = 2.0$ k Ω ± 5 percent.
7. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 5. Switching test circuit and waveforms for device type 02 - Continued.

FIGURE 6. Switching test circuit and waveforms for device type 03.

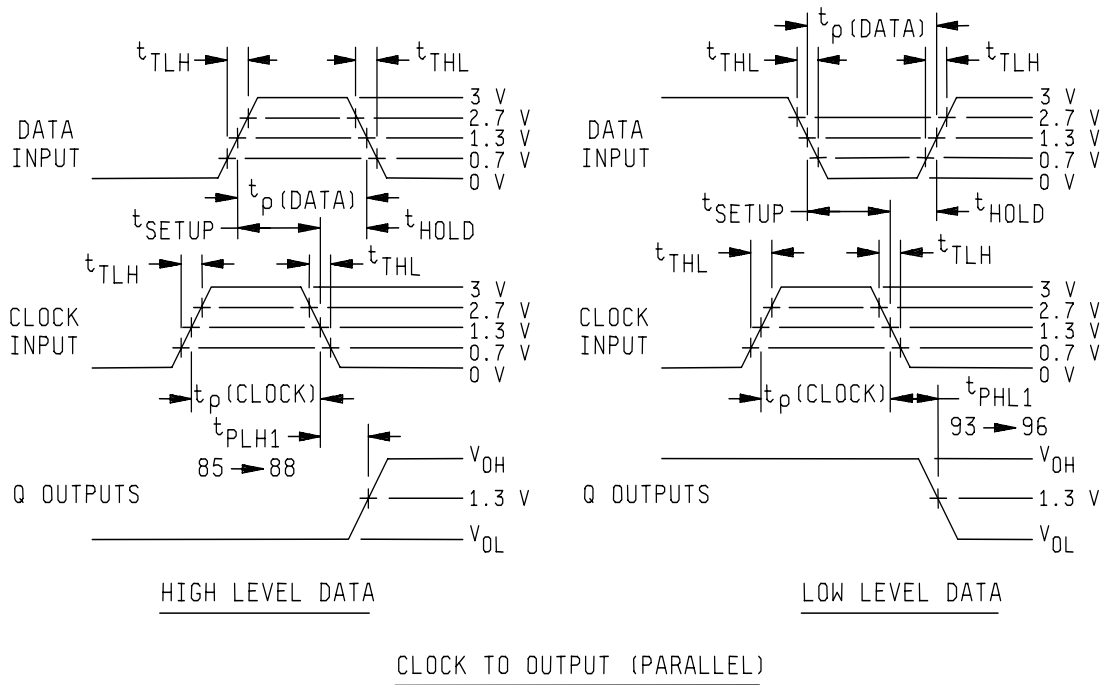
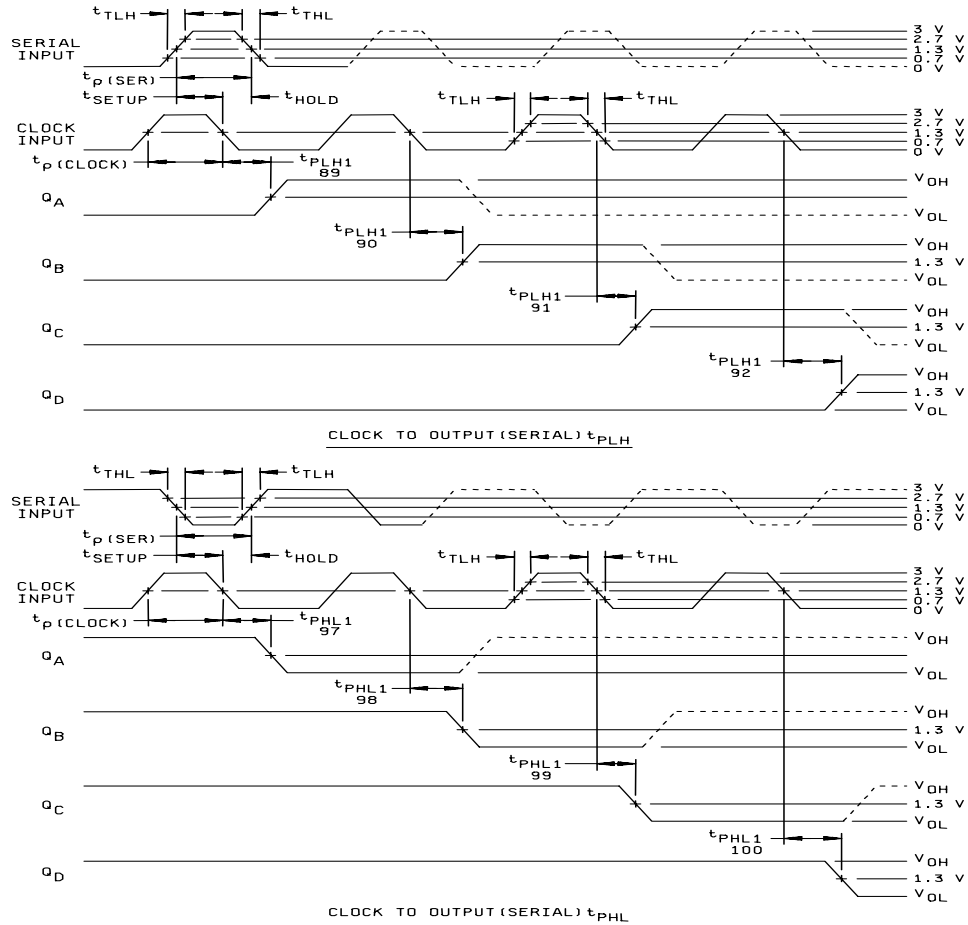


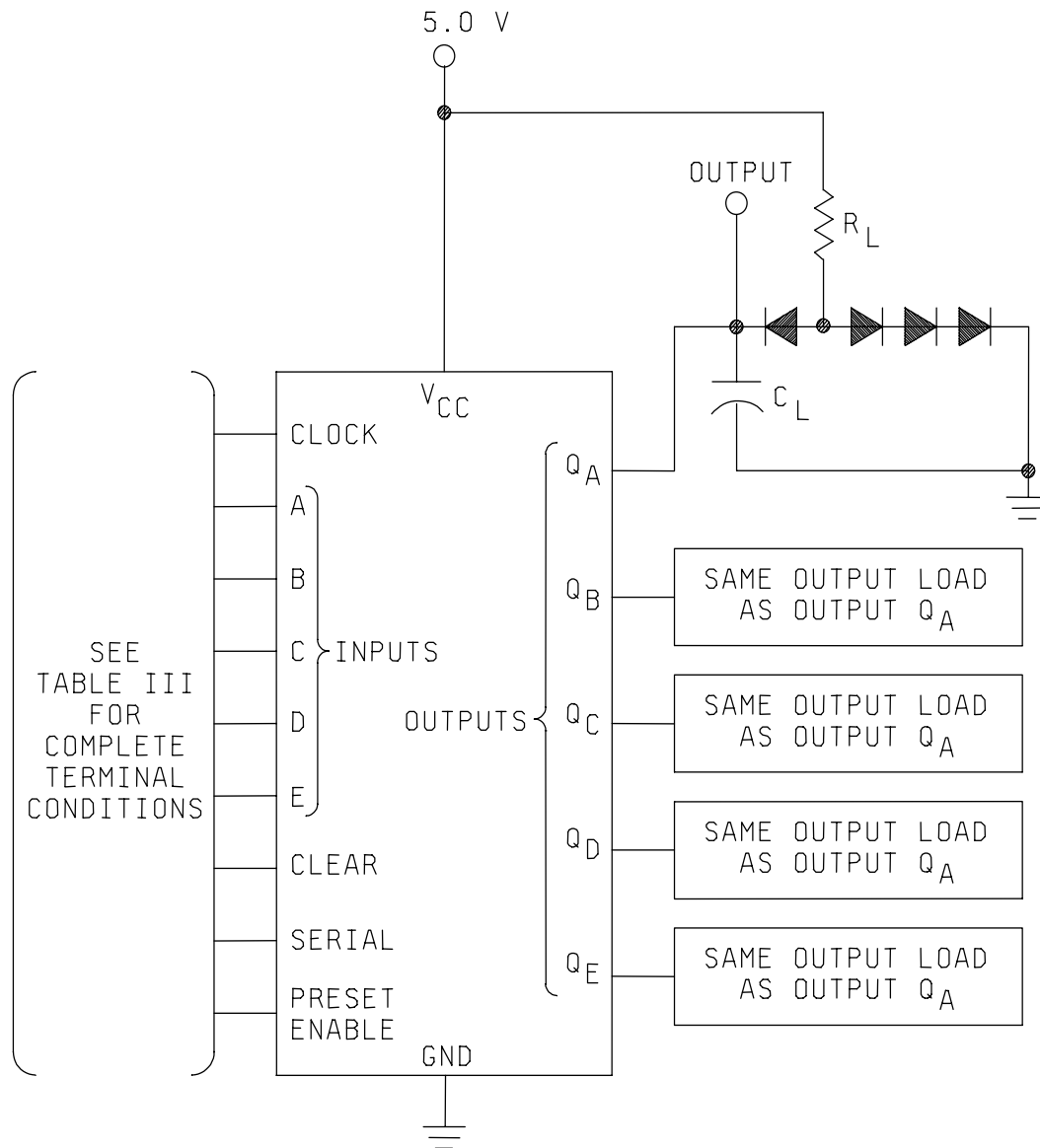
FIGURE 6. Switching test circuit and waveforms for device type 03 - Continued.



NOTES:

1. Clock pulse characteristics: $PRR \leq 1.0$ MHz, $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, $t_P(\text{clock}) \geq 20$ ns.
2. Serial data pulse characteristics: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, $t_P(\text{SER})$ or $t_P(\text{DATA}) = 30$ ns, $t_{SETUP} = 20$ ns, $t_{HOLD} = 10$ ns.
3. $C_L = 50$ pF ± 10 percent including scope, probe, wiring and stray capacitance without package in test fixture.
4. $R_L = 2.0$ k Ω $\pm 5\%$.
5. All diodes are 1N3064, 1N916 or equivalent.
6. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 6. Switching test circuit and waveforms for device type 03 - Continued.

FIGURE 7. Switching test circuit and waveforms for device type 04.

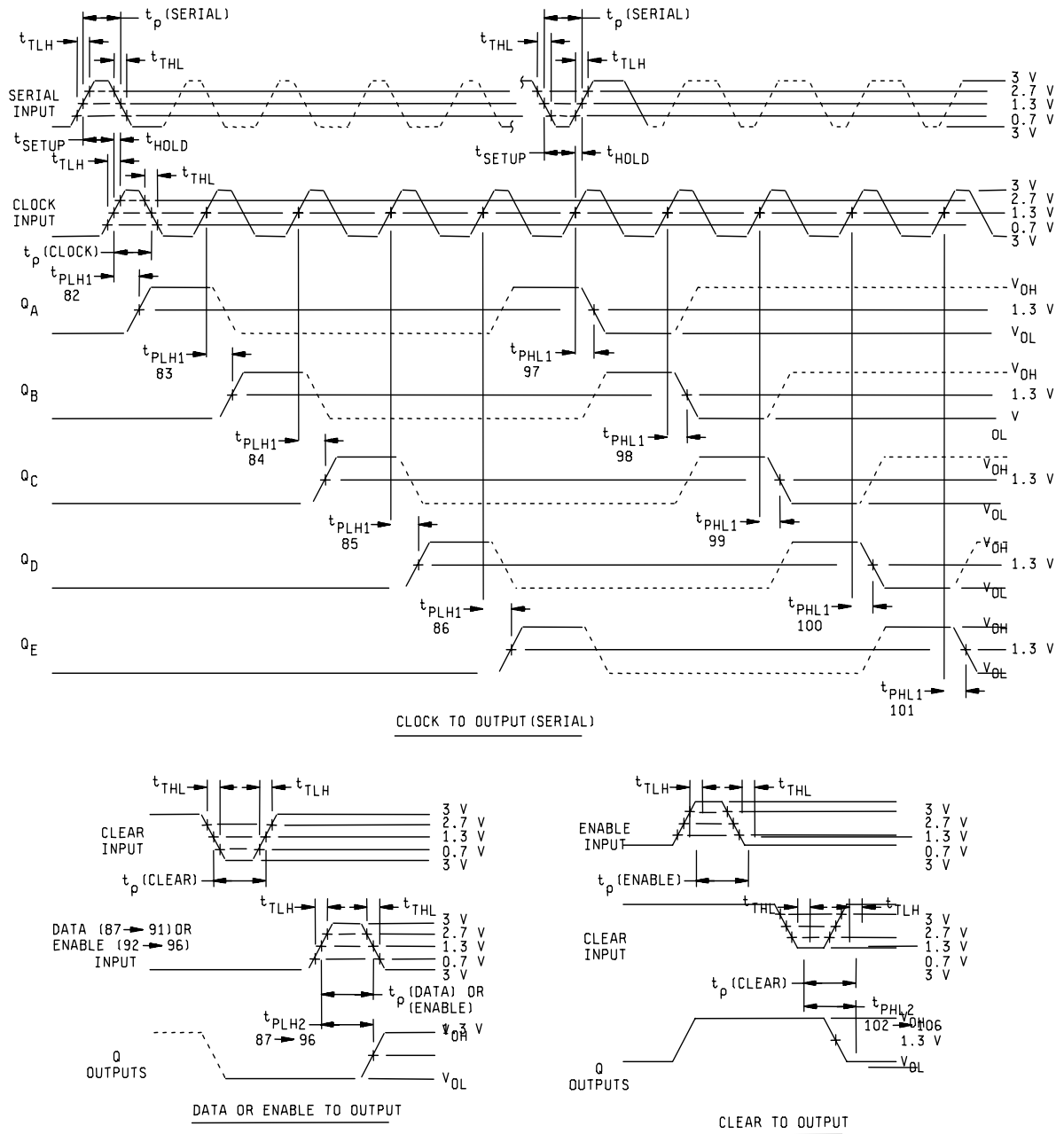
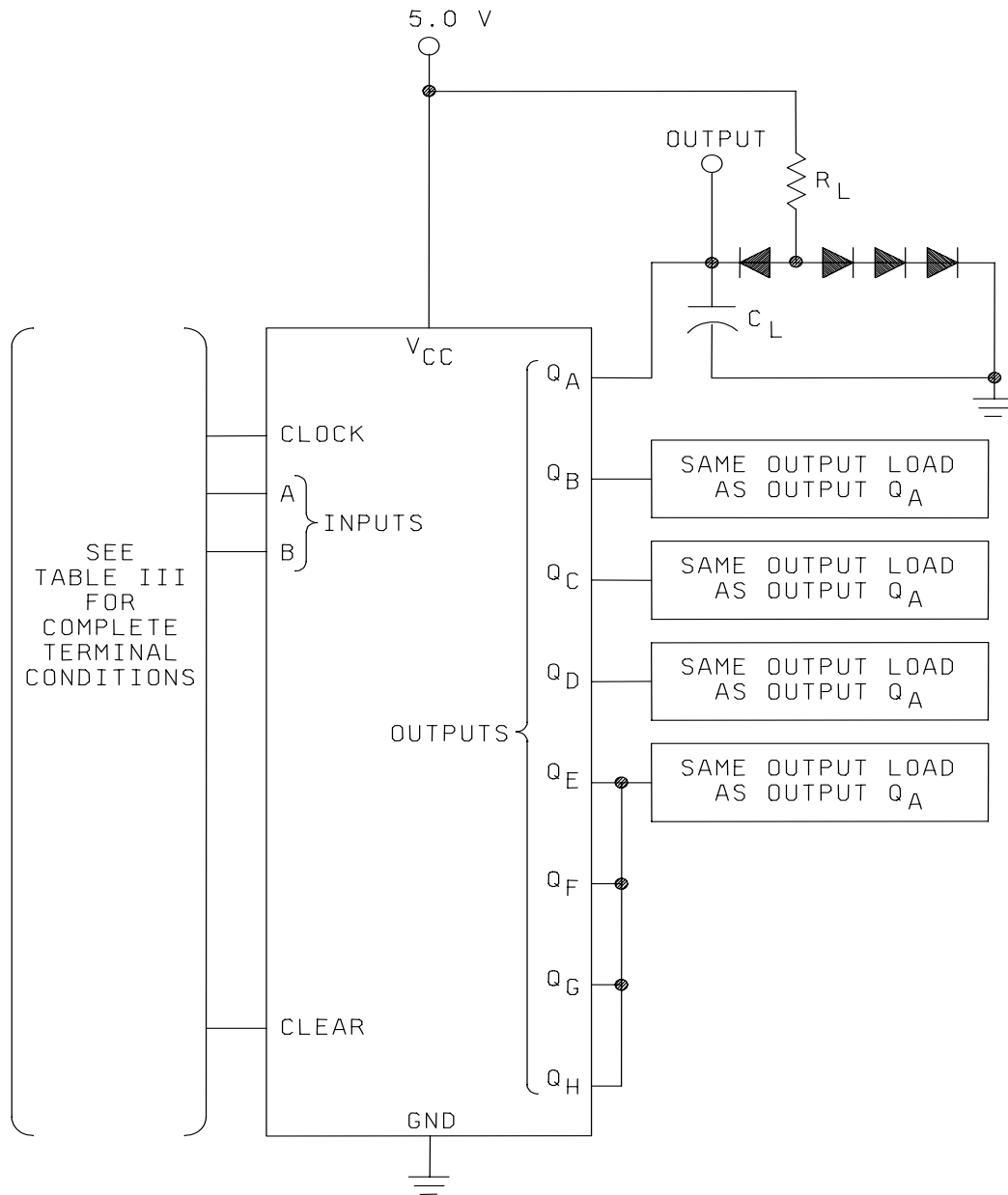


FIGURE 7. Switching test circuit and waveforms for device type 04 - Continued.

NOTES:

1. Clock pulse characteristics: $PRR \leq 1.0 \text{ MHz}$, $t_{TLH} \leq 15 \text{ ns}$,
 $t_{THL} \leq 6 \text{ ns}$, $t_p (\text{clock}) \geq 25 \text{ ns}$.
2. Serial data pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$,
 $t_p = 30 \text{ ns}$.
3. Clear, data, and enable pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$,
 $t_{THL} \leq 6 \text{ ns}$, $t_p = 30 \text{ ns}$.
4. $C_L = 50 \text{ pF} \pm 10 \text{ percent}$ including scope, probe, wiring and stray
capacitance without package in test fixture.
4. $R_L = 2.0 \text{ k}\Omega \pm 5\%$.
5. All diodes are 1N3064, 1N916 or equivalent.
6. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 7. Switching test circuit and waveforms for device type 04 - Continued.

FIGURE 8. Switching test circuit and waveforms for device type 05.

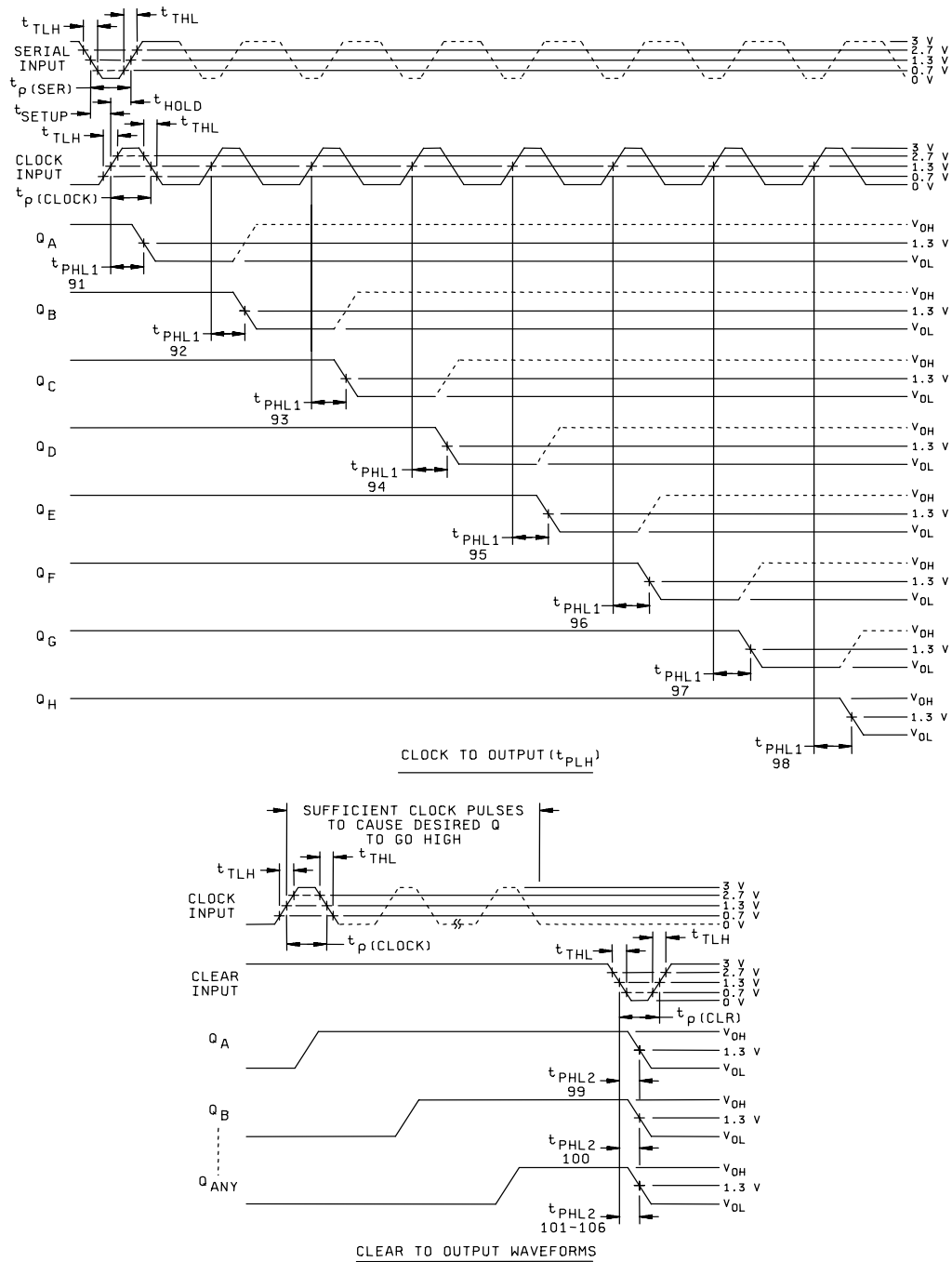
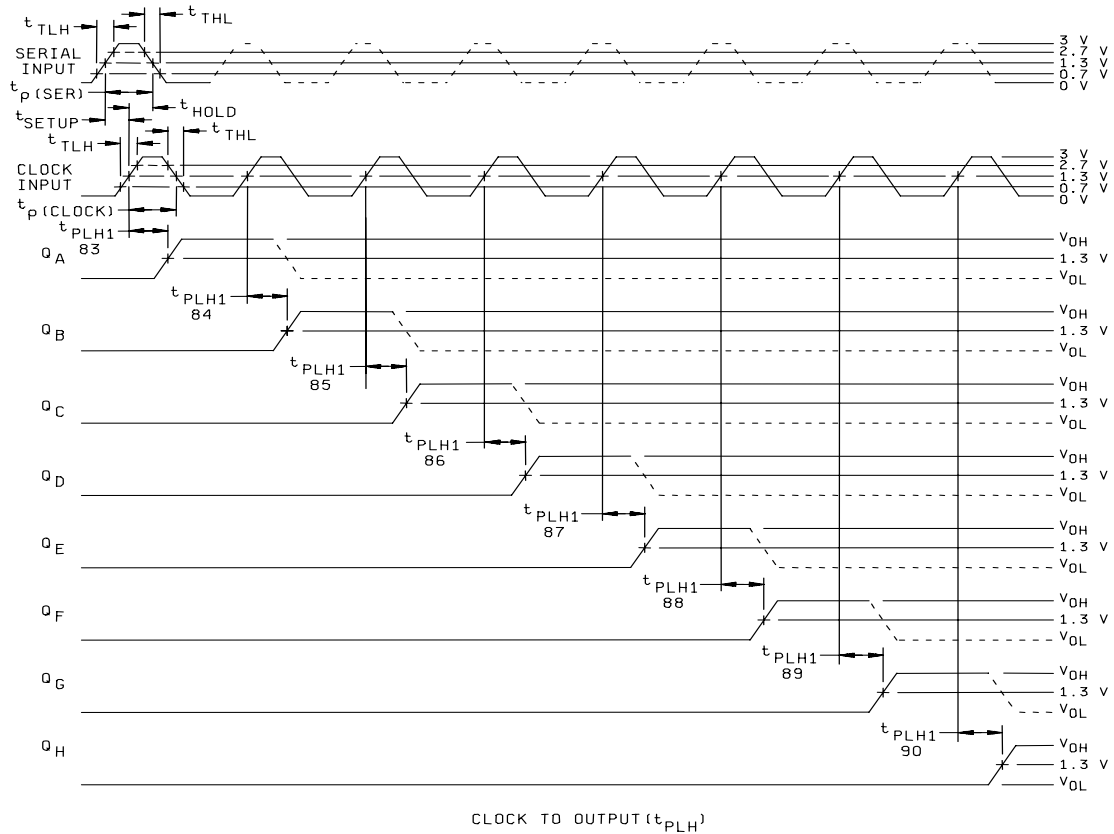


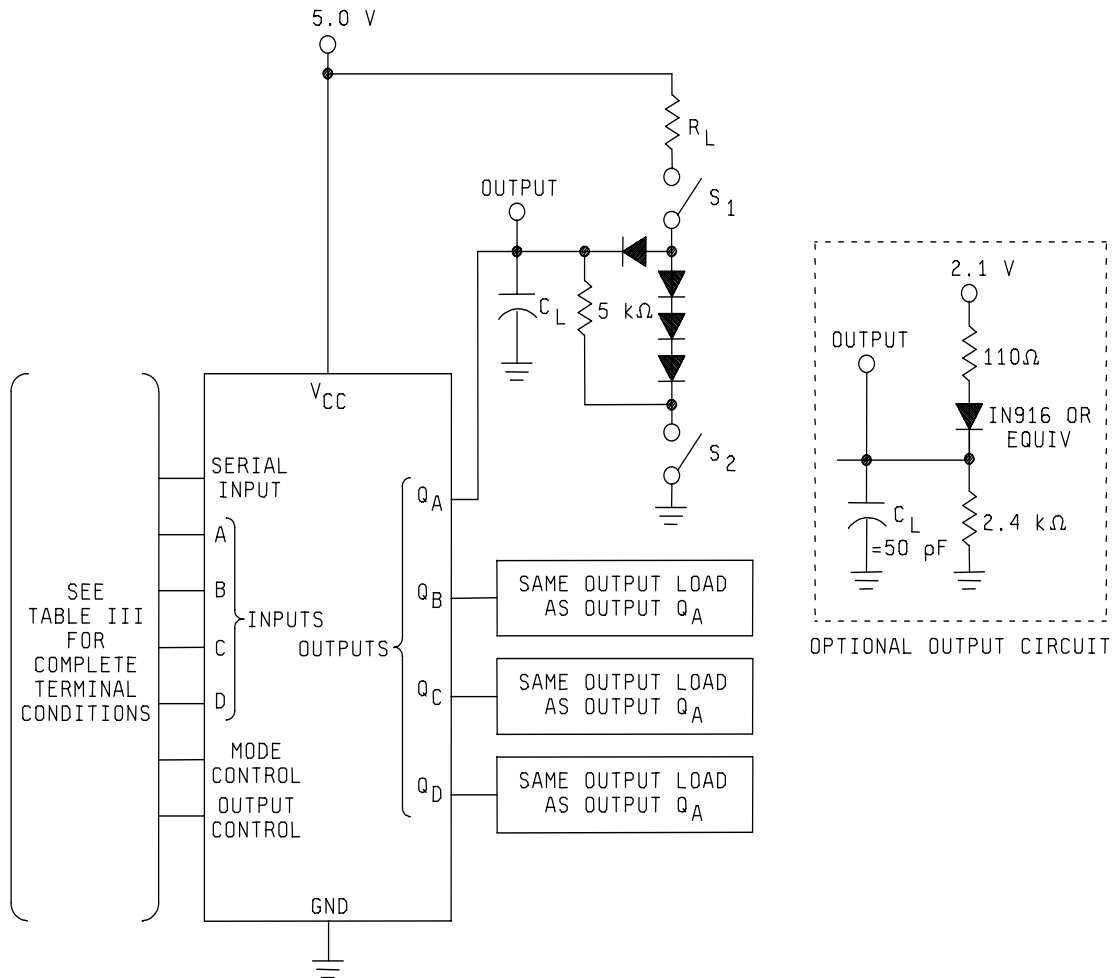
FIGURE 8. Switching test circuit and waveforms for device type 05 - Continued.



NOTES:

1. Clock pulse characteristics: $PRR \leq 1.0 \text{ MHz}$, $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{clock}) \geq 20 \text{ ns}$.
2. Clear pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{clear}) = 30 \text{ ns}$.
3. Serial pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{serial}) = 30 \text{ ns}$, $t_{SETUP} = 20 \text{ ns}$, $t_{HOLD} = 10 \text{ ns}$.
4. $C_L = 50 \text{ pF} \pm 10 \text{ percent}$ including scope, probe, wiring and stray capacitance without package in test fixture.
5. $R_L = 2.0 \text{ k}\Omega \pm 5\%$.
6. All diodes are 1N3064, 1N916 or equivalent.
7. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 8. Switching test circuit and waveforms for device type 05 - Continued.

FIGURE 9. Switching test circuit and waveforms for device type 06.

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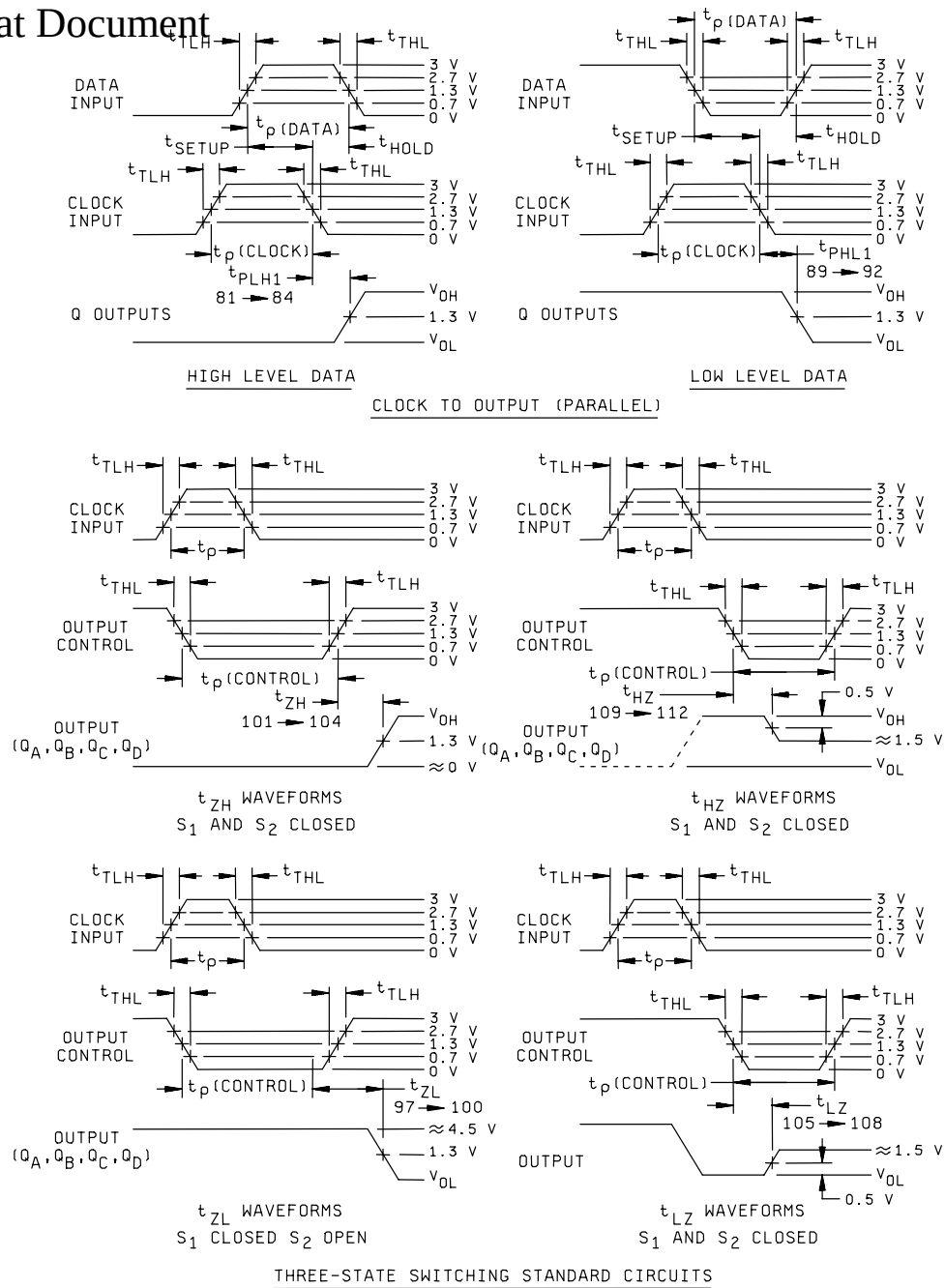
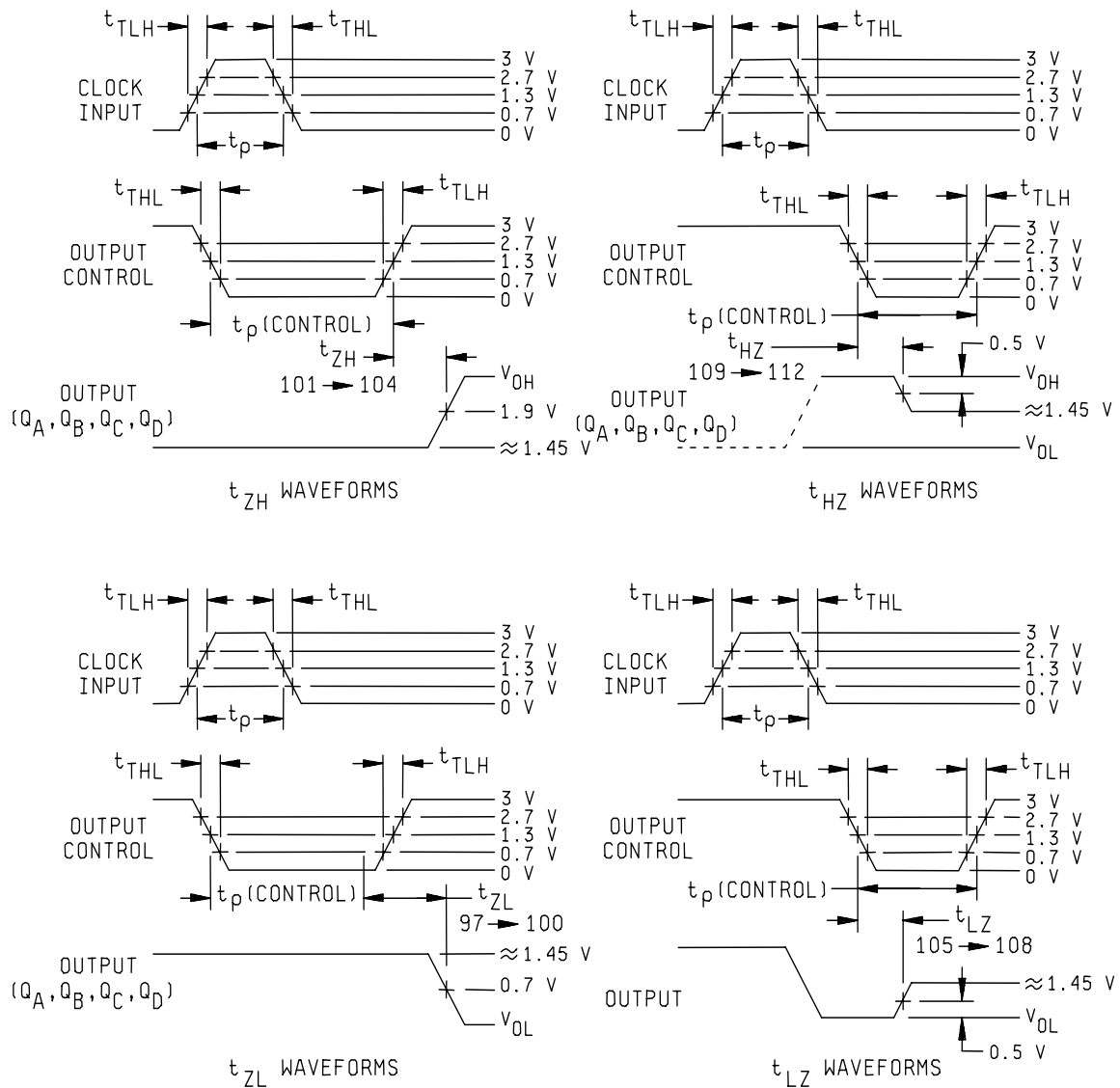
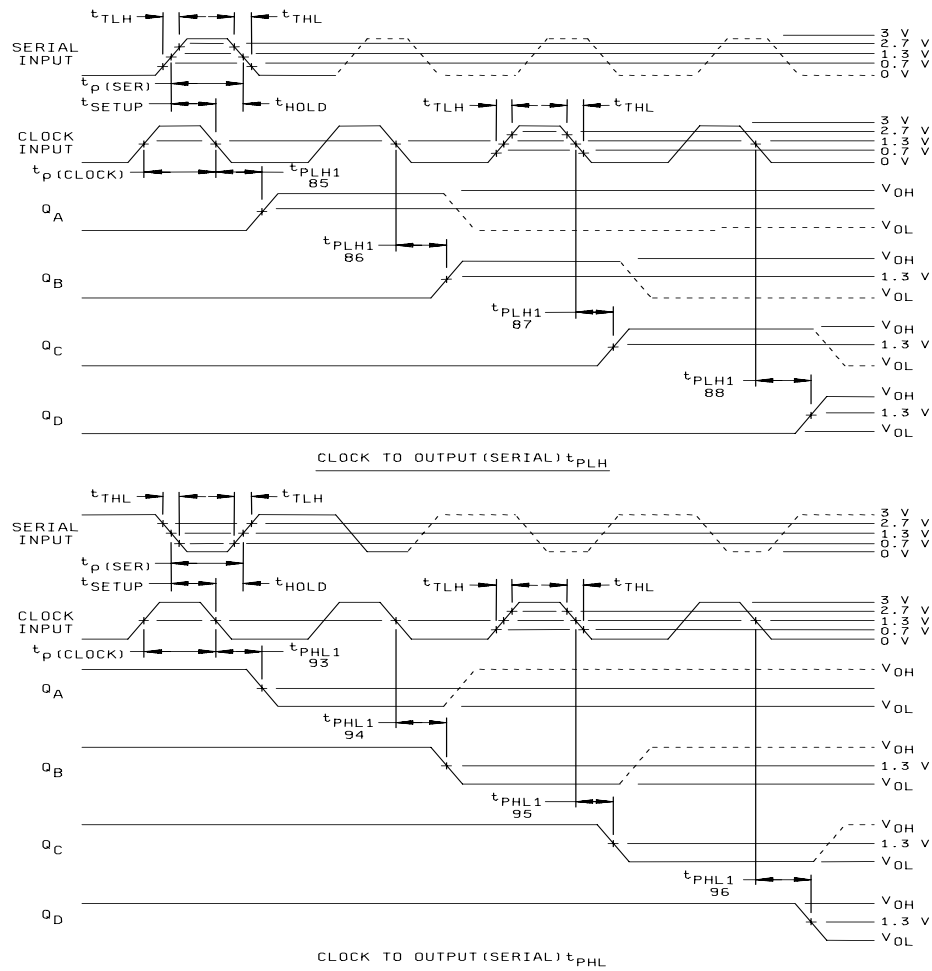


FIGURE 9. Switching test circuit and waveforms for device type 06 - Continued.



THREE-STATE SWITCHING OPTIONAL CIRCUITS

FIGURE 9. Switching test circuit and waveforms for device type 06 - Continued.



NOTES:

1. Clock pulse characteristics: $PRR \leq 1.0 \text{ MHz}$, $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{clock}) \geq 25 \text{ ns}$.
2. Data or serial pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{serial})$ or $t_p(\text{data}) = 40 \text{ ns}$, $t_{SETUP} = 20 \text{ ns}$, $t_{HOLD} = 20 \text{ ns}$.
3. Output control characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{control}) \geq 100 \text{ ns}$, except when optional load is used, $C_L = 50 \text{ pF} \pm 10\%$ for all tests.
4. $C_L = 50 \text{ pF} \pm 10\%$ for propagation delay, t_{ZL} , t_{ZH} , and $C_L = 15 \text{ pF}$ minimum for t_{HZ} , t_{LZ} except when optional load is used, $C_L = \text{pF} \pm 10\%$ for all tests.
 C_L includes scope probe, wiring, and stray capacitance without package in test fixture.
 All diodes are 1N3064, 1N916, or equivalent.
6. $R_L = 680 \Omega \pm 5\%$.
7. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 9. Switching test circuit and waveforms for device type 06 - Continued.

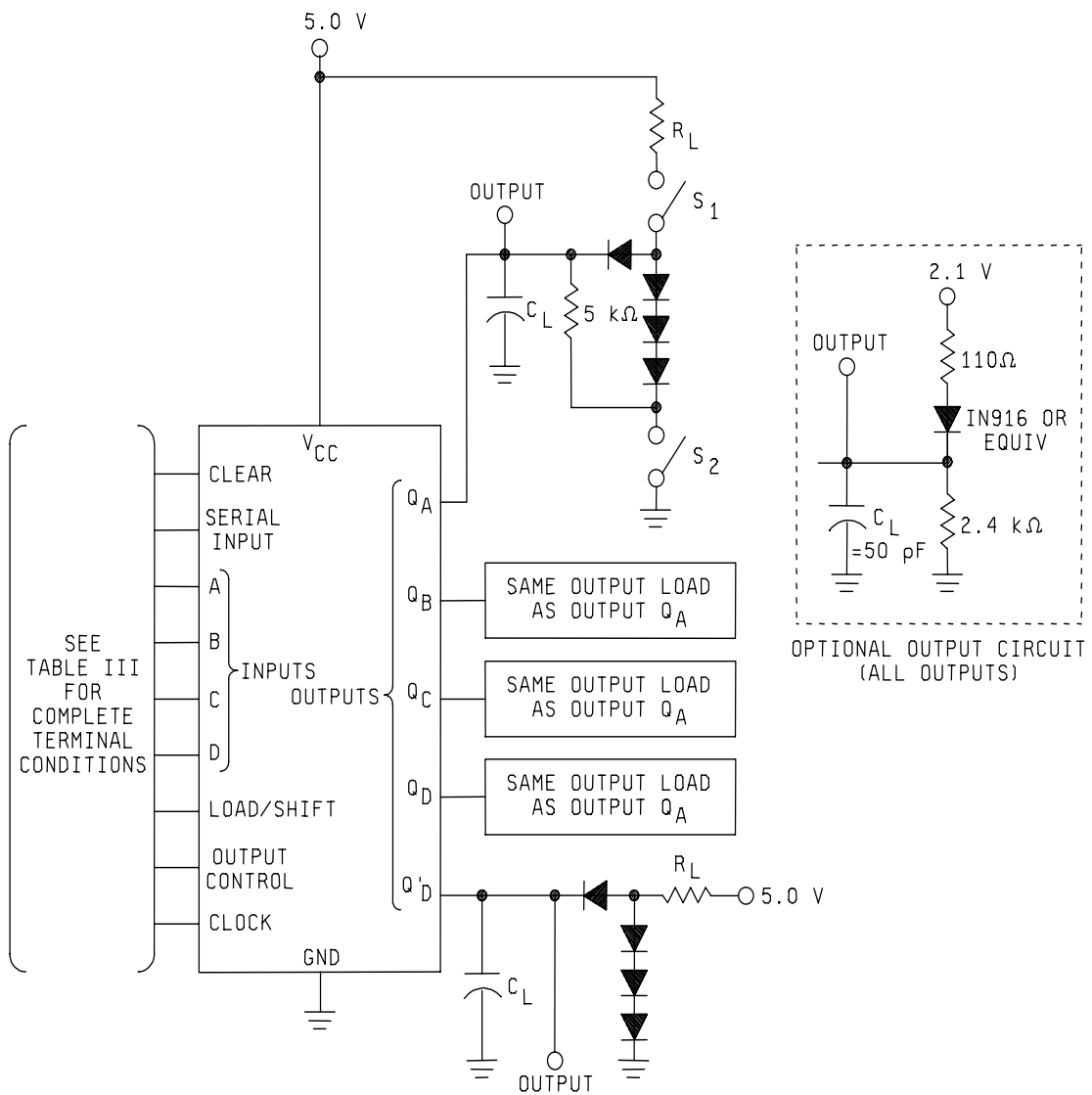
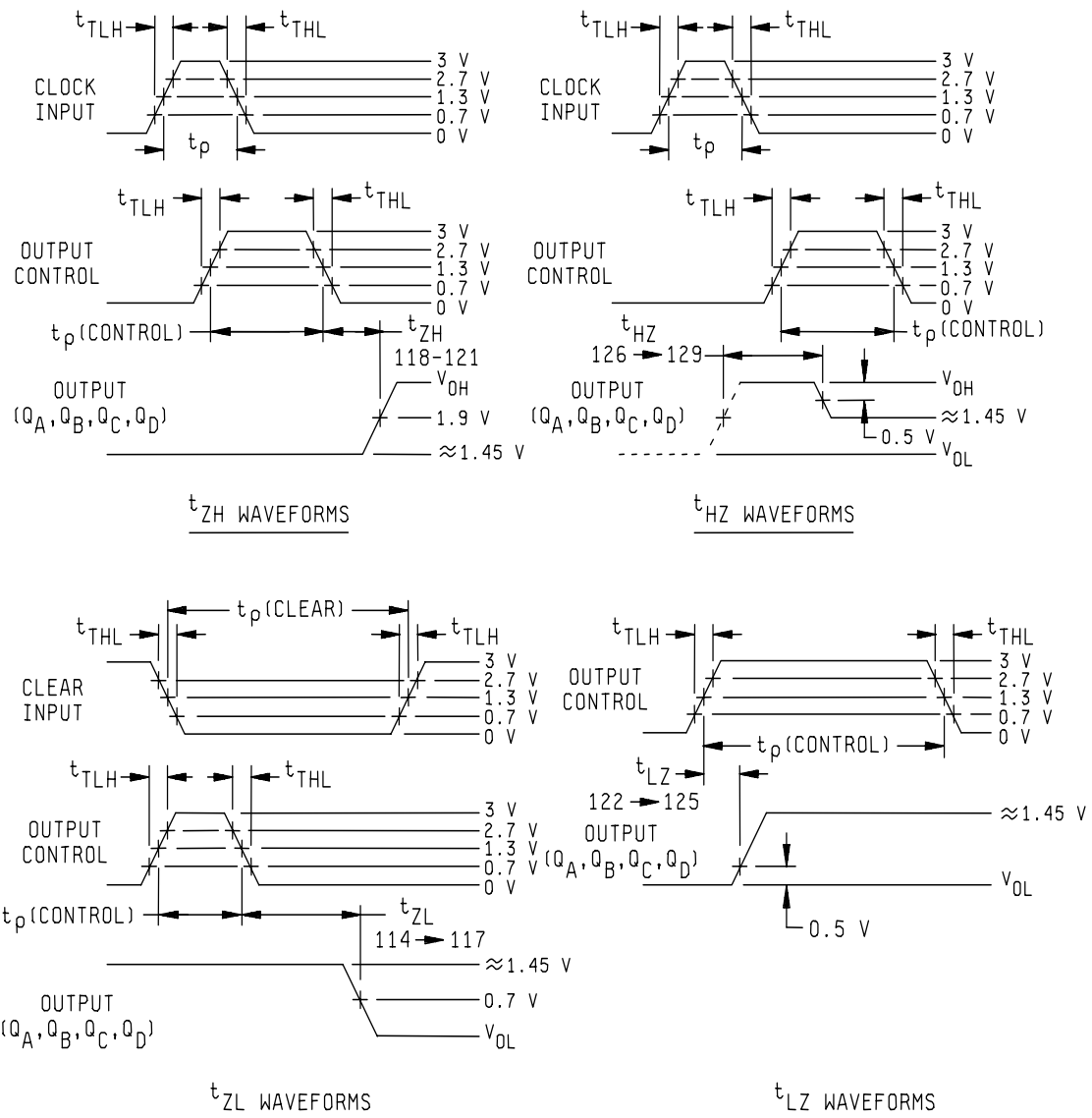
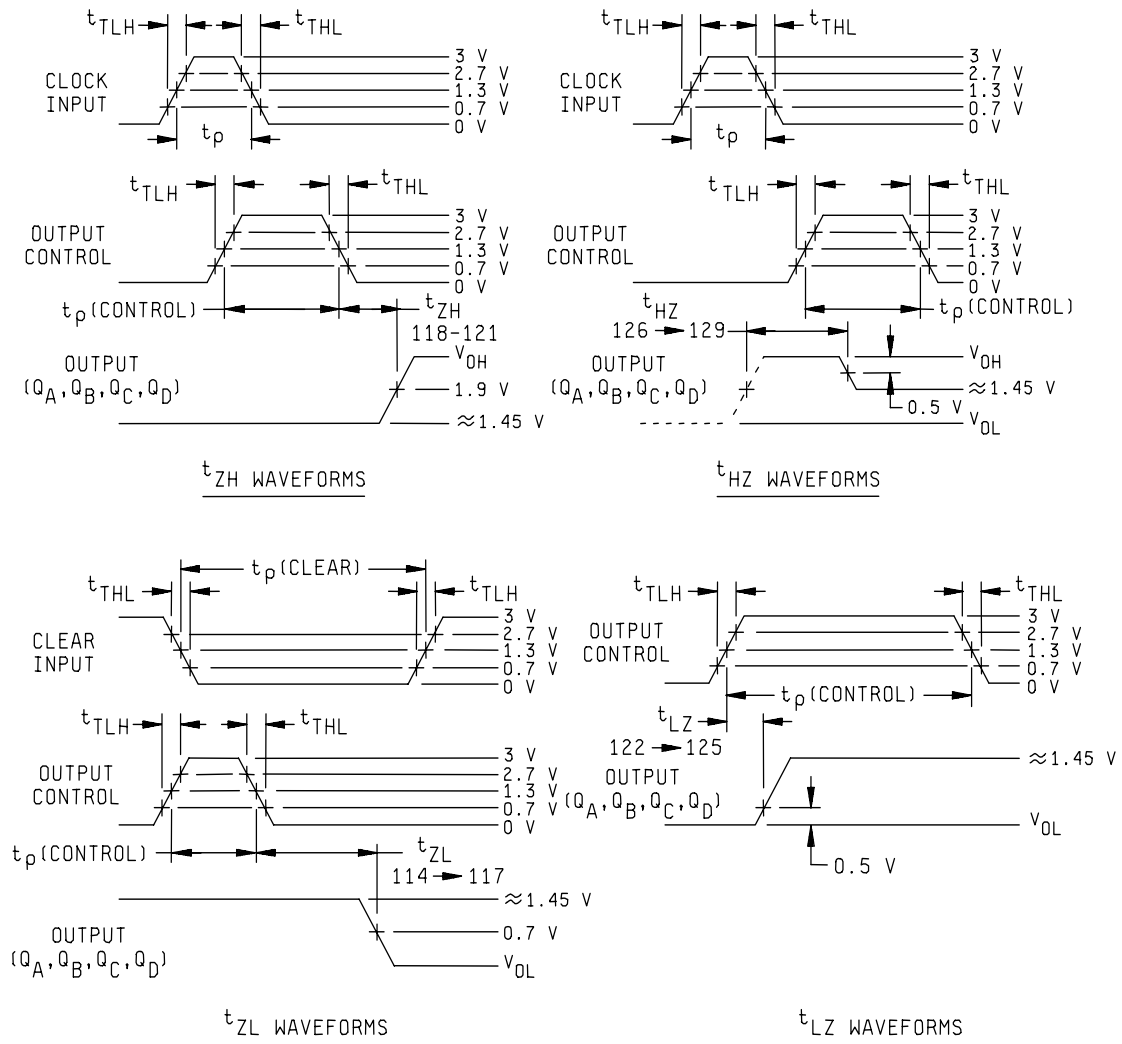


FIGURE 10. Switching test circuit and waveforms for device type 07.



THREE-STATE OPTIONAL CIRCUITS

FIGURE 10. Switching test circuit and waveforms for device type 07 - Continued.



THREE-STATE OPTIONAL CIRCUITS

FIGURE 10. Switching test circuit and waveforms for device type 07 - Continued.

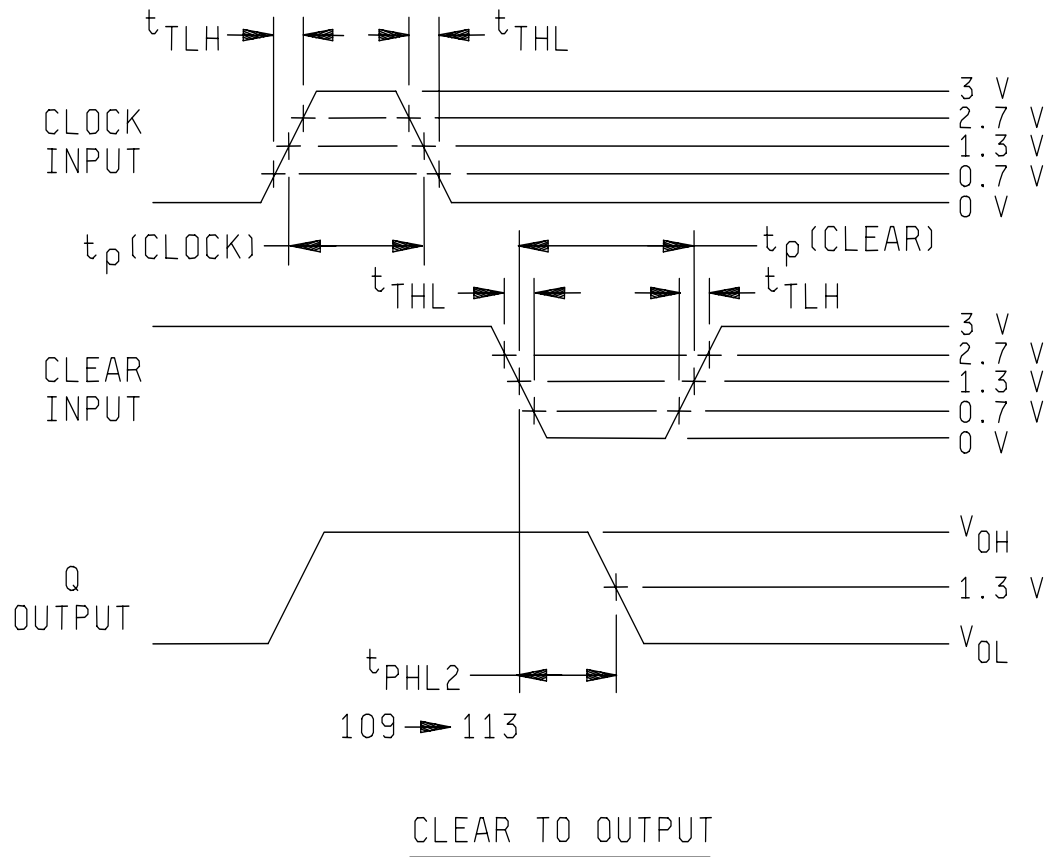
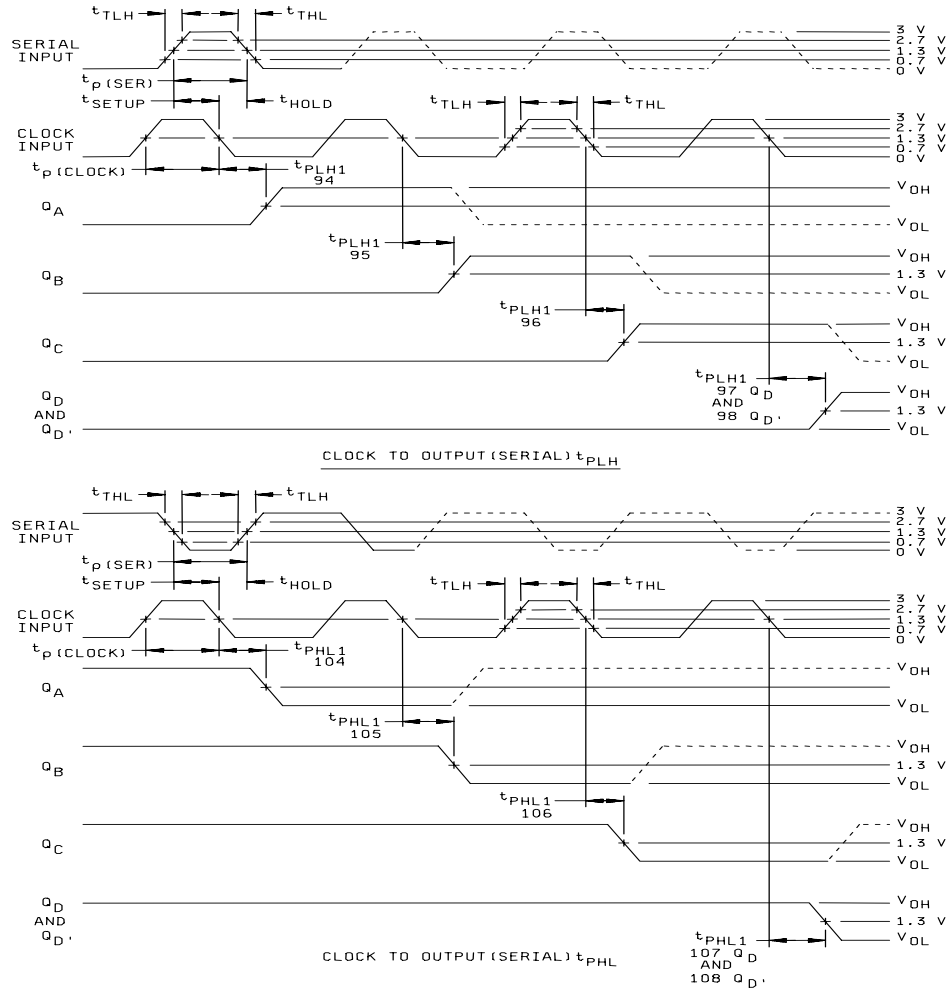


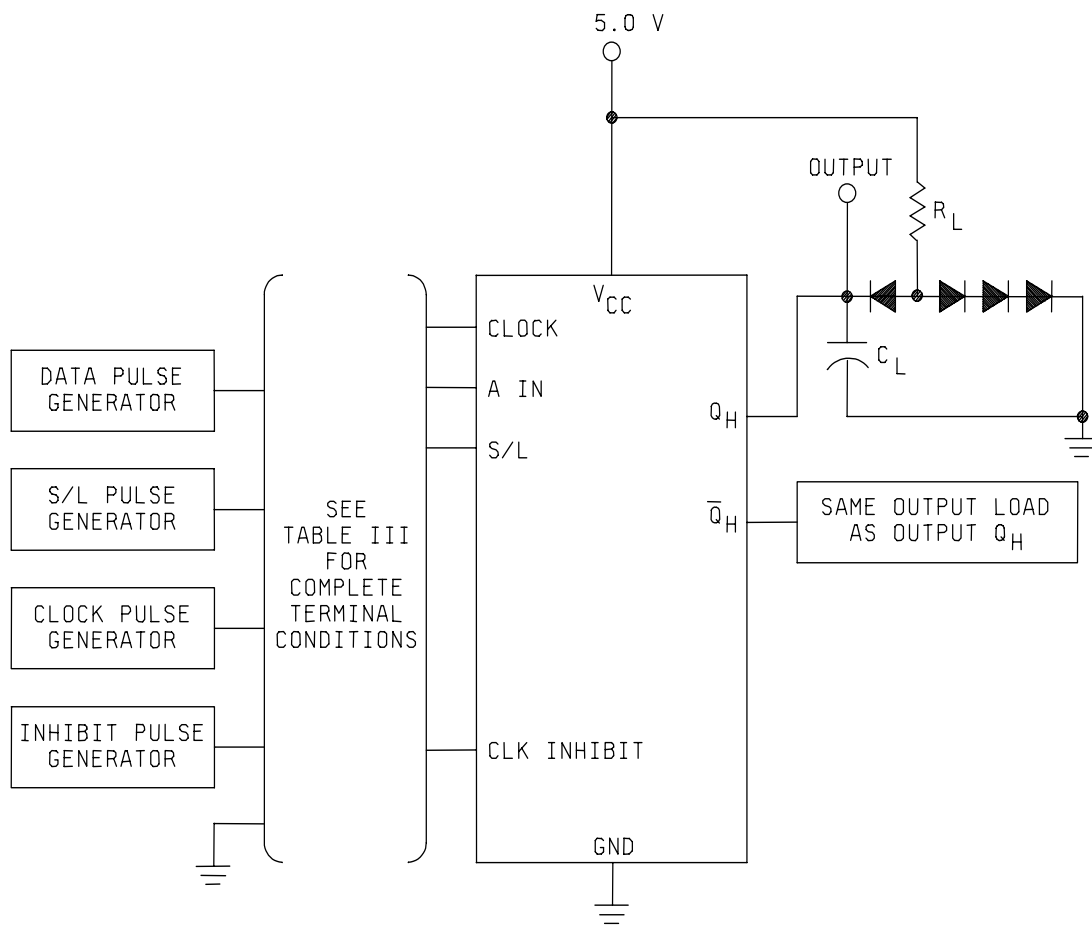
FIGURE 10. Switching test circuit and waveforms for device type 07 - Continued.

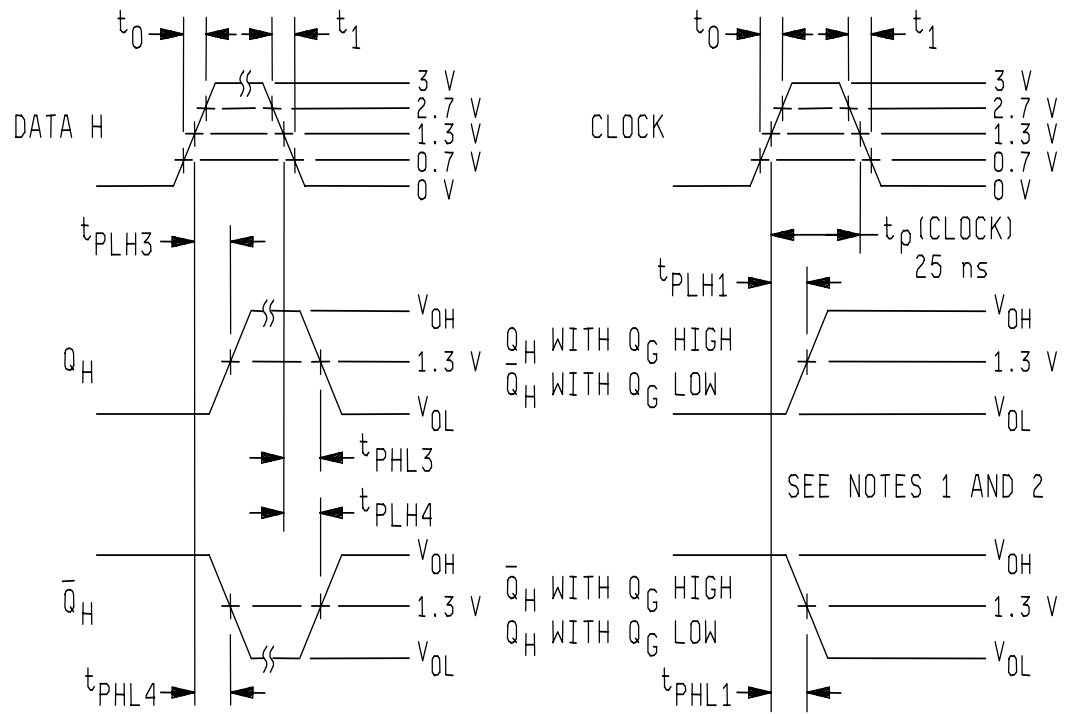


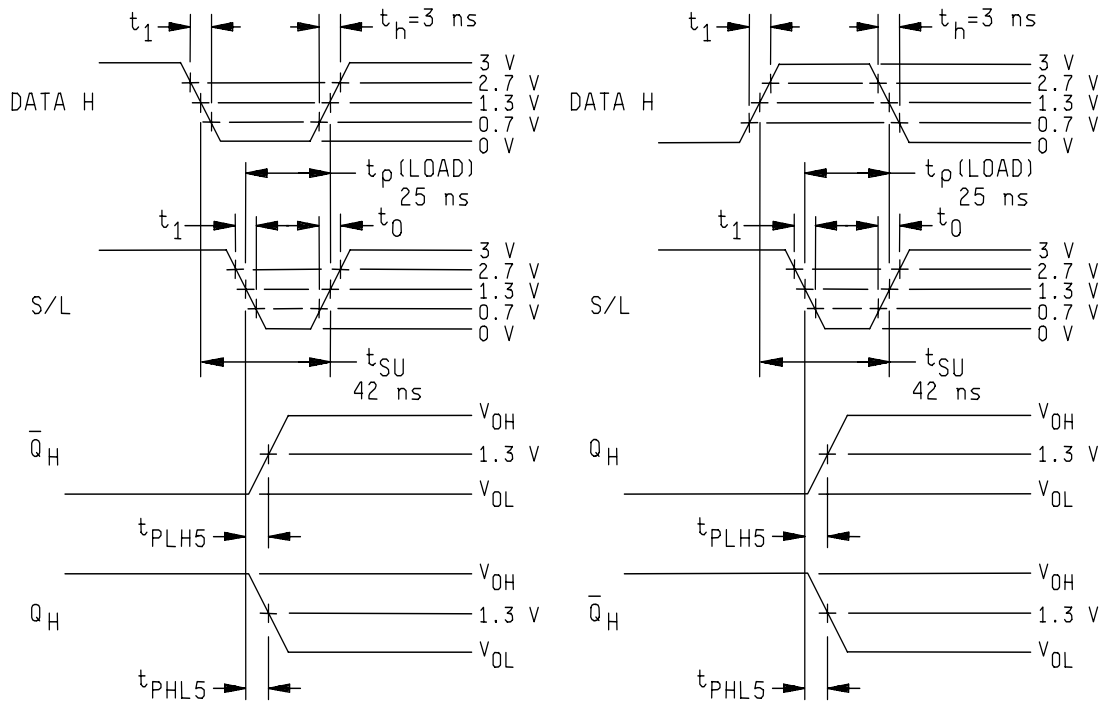
NOTES:

1. Clock pulse characteristics: $PRR \leq 1.0 \text{ MHz}$, $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{clock}) \geq 20 \text{ ns}$.
2. Data or serial pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{serial})$ or $t_p(\text{data}) = 30 \text{ ns}$, $t_{\text{SETUP}} = 20 \text{ ns}$, $t_{\text{HOLD}} = 10 \text{ ns}$.
3. Clear pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{clear}) = 25 \text{ ns}$, except $\geq 200 \text{ ns}$ for t_{ZL} test.
4. Output control pulse characteristics: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, $t_p(\text{control}) \geq 100 \text{ ns}$.
5. $C_L = 50 \text{ pF} \pm 10\%$ for propagation delay, t_{ZH} , t_{ZL} test, and $C_L = 15 \text{ pF}$ minimum (all except Q_D) for t_{HZ} , t_{LZ} tests except when optional load is used, $C_L = 50 \text{ pF} \pm 10\%$ for all tests. C_L includes scope probe, wiring, and stray capacitance without package in test fixture.
6. All diodes are 1N3064, 1N916, or equivalent.
7. $R_L = 680 \Omega \pm 5\%$ except for Q_D , $R_L = 2 \text{ k}\Omega \pm 5\%$.
8. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 10. Switching test circuit and waveforms for device type 07 - Continued.

FIGURE 11. Switching test circuit and waveforms for device type 08.

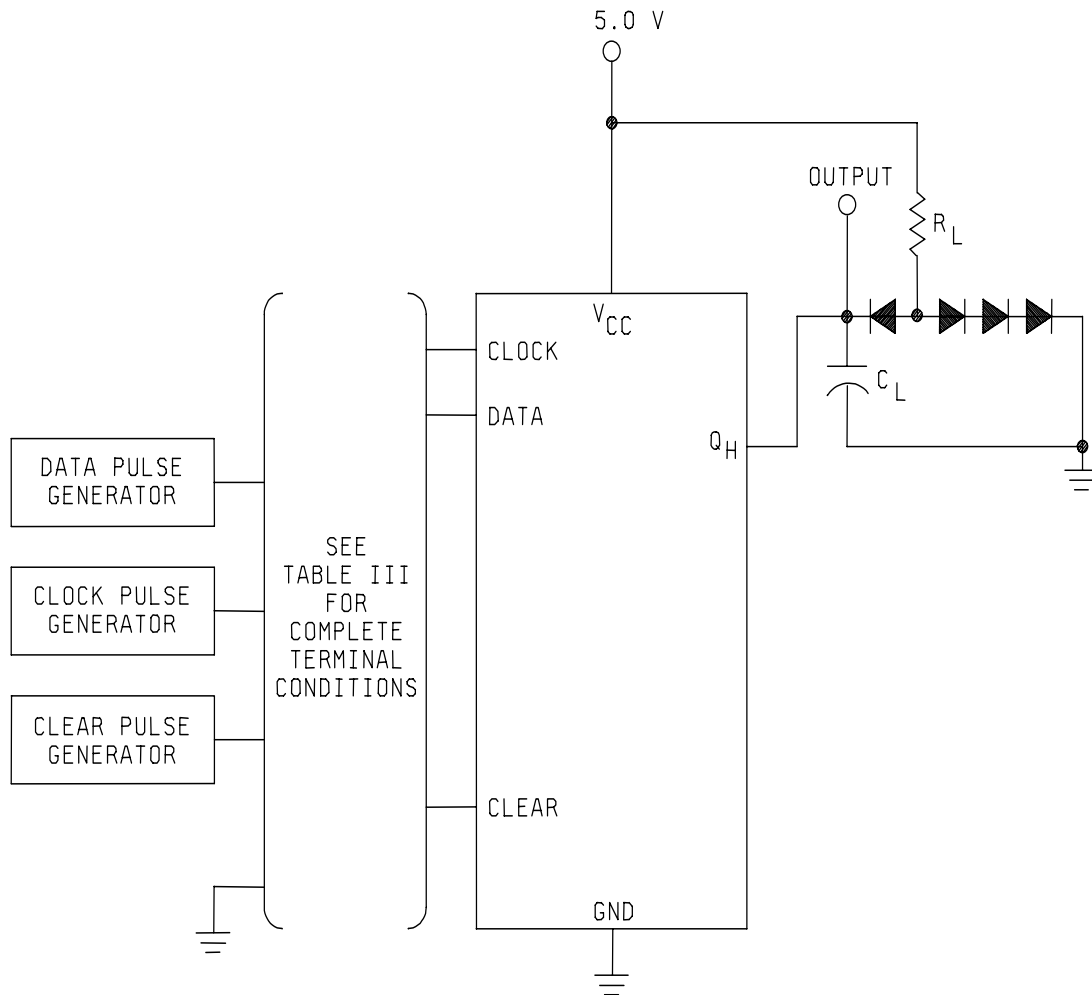
FIGURE 11. Switching test circuit and waveforms for device type 08 - Continued.

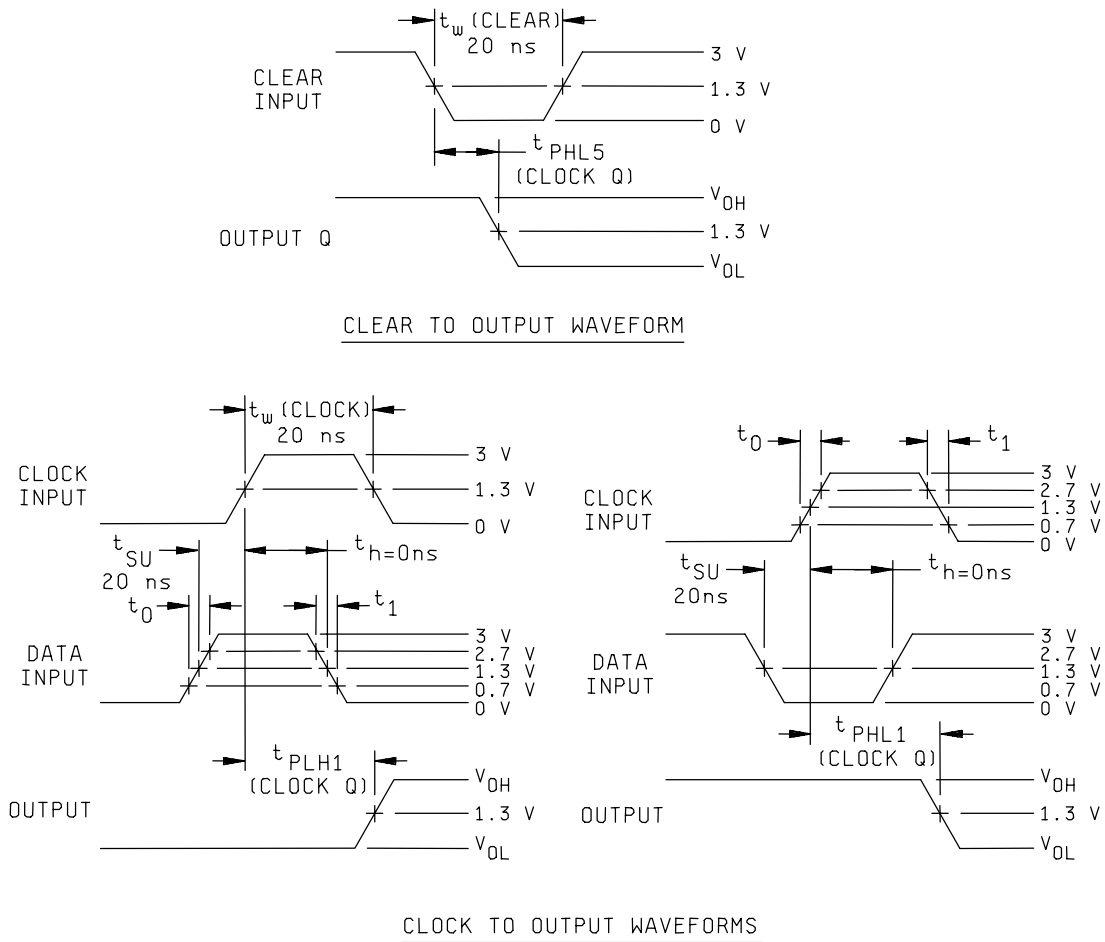


NOTES:

1. For t_{PHL2} measurements, internal output G must be set to a low and Q_H to a high prior to tests.
2. For t_{PHL2} measurements, internal output G must be set to a high and Q_H to a low prior to test.
3. $R_L = 2.0 \text{ k}\Omega \pm 5\%$.
4. $C_L = 50 \text{ pF} \pm 10\%$, which includes probe, and jig capacitance.
5. All pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_0 \leq 15 \text{ ns}$, $t_1 \leq 6 \text{ ns}$ and $PRR \leq 1 \text{ MHz}$.
6. All diodes 1N3064 or equivalent.

FIGURE 11. Switching test circuit and waveforms for device type 08 - Continued.

FIGURE 12. Switching test circuit and waveforms for device type 09.



NOTES:

1. $R_L = 2.0 \text{ k}\Omega \pm 5\%$.
2. $C_L = 50 \text{ pF} \pm 10\%$, which includes probe, and jig capacitance.
3. All pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_0 \leq 15 \text{ ns}$, $t_1 \leq 6 \text{ ns}$ and $\text{PRR} \leq 1 \text{ MHz}$.
4. All diodes 1N3064 or equivalent.

FIGURE 12. Switching test circuit and waveforms for device type 09 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLR	S/R Serial	A _{IN}	IN	IN	IN	S/L Serial	GND	S ₀	S ₁	CLK	QD	QC	QB	QA	V _{CC}				
1 T _c = 25°C	V _{OH}	3006	1	A	GND	2.0 V	GND	GND	GND	GND	GND	4.5 V	4.5 V	A 1/				-4 mA	4.5 V	QA	2.5		V
			2	"	"	GND	2.0 V	GND	GND	"	"	"	"	"			-4 mA	"	"	QB	"		"
			3	"	"	"	GND	2.0 V	GND	"	"	"	"	"		-4 mA			"	QC	"		"
			4	"	"	"	"	GND	2.0 V	"	"	"	"	"		-4 mA			"	QD	"		"
			5	"	2.0 V	"	"	GND	GND	"	"	"	0.7 V	"				-4 mA	"	QA	"		"
			6	"	GND	"	"	GND	GND	2.0 V	"	0.7 V	4.5 V	"		-4 mA			"	QD	"		"
			7	"	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	"	4.5 V	GND	"				-4 mA	"	QA	"		"
	V	3007	8	"	4.5 V	0.7 V	4.5 V	4.5 V	4.5 V	4.5 V	"	"	4.5 V	"				4 mA	"	QA		0.4	"
			9	"	"	4.5 V	0.7 V	4.5 V	4.5 V	"	"	"	"	"			4 mA	"	"	QB			"
			10	"	"	"	4.5 V	0.7 V	4.5 V	"	"	"	"	"		4mA			"	QC			"
			11	"	"	"	"	4.5 V	0.7 V	"	"	"	"	"		4 mA			"	QD			"
			12	"	0.7 V	"	"	4.5 V	4.5 V	"	"	"	0.7 V	"				4 mA	"	QA			"
			13	"	4.5 V	"	"	4.5 V	4.5 V	0.7 V	"	0.7 V	4.5 V	"		4 mA			"	QD			"
	V		14	-18 mA						"	"								"	CLR		-1.5	"
					-18 mA					"	"								"	S/R			"
						-18 mA				"	"								"	A _{IN}			"
			17				-18 mA			"	"								"	B _{IN}			"
								-18 mA		"	"								"	C _{IN}			"
									-18 mA	"	"								"	D _{IN}			"
										-18 mA	"								"	S/L			"
										"	-18 mA								"	S ₀			"
										"		-18 mA							"	S ₁			"
										"			-18 mA						"	CLK			"
	I	3010	24	2.7 V						"	"								5.5 V	CLR		20	μA
			21		2.7 V					"	GND	4.5 V							"	S/R			"
			22			2.7 V				"	"	GND							"	A _{IN}			"
			23				2.7 V			"	"	"							"	B _{IN}			"
			27					2.7 V		"	"	"							"	C _{IN}			"
			28						2.7 V	"	"	"							"	D _{IN}			"
			29							2.7 V	"	"	"						"	S/L			"
											2.7 V	"	4.5 V	"					"	S ₀			"
										"		2.7 V							"	S ₁			"
			33	GND						"			2.7 V						"	CLK			"
	I	31	34	5.5 V						"			5.5 V						"	CLR		100	"
					5.5 V					"	GND	4.5 V							"	S/R			"
						5.5 V				"	GND	GND							"	A _{IN}			"
			37				5.5 V			"	"	"	"						"	B _{IN}			"
			38					5.5 V		"	"	"	"						"	C _{IN}			"
			39						5.5 V	"	"	"	"						"	D _{IN}			"
										5.5 V	"	4.5 V	"						"	S/L			"
										"	"	5.5 V	"						"	S ₀			"
										"			5.5 V	"					"	S ₁			"
			43	GND						"				5.5 V					"	CLK			"

See footnotes at end of device types 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit	
			Cases 2, X	* 2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max		
			Test no.	CLR	S/R Serial	A _{IN}	IN	IN	IN	S/L Serial	GND	S ₀	1	CLK	QD	QC	QB	QA	V _{CC}					
1 T _C = 25°C	I _{IL1} I _{IL2}	3009	44	0.4 V		B	C	D			GND	S							5.5 V	CLR	2/	2/	mA	
			45		0.4 V						"	4.5 V	GND						"	S/R	"	"	"	
			46			0.4 V					"	"	4.5 V						"	A _{IN}		"	"	
			47				0.4 V				"	"	"						"	B _{IN}		"	"	
			48					0.4 V			"	"	"						"	C _{IN}		"	"	
			49						0.4 V		"	"	"						"	D _{IN}		"	"	
			50							0.4 V	"	GND	"						"	S/L	"	"	"	"
			51								"	0.4 V							"	S ₀		"	"	"
			52								"		0.4 V						"	S ₁		"	"	"
			53	4.5 V							"			0.4 V					"	CLK	"	"	"	"
	OS	3011	54	A		4.5 V	GND	GND	GND		"	4.5 V	4.5 V	A 1/				GND	"	QA	-15	-100	"	
			55	"		GND	4.5 V	GND	GND		"	"	"	"			GND		"	QB	"	"	"	"
			56	"		"	GND	4.5 V	GND		"	"	"	"		GND			"	QC	"	"	"	"
			57	"		"	GND	GND	4.5 V		"	"	"	"	GND				"	QD	"	"	"	"
	CC	3005	58	5.5 V	5.5 V	"	GND	GND	GND	5.5 V	"	5.5 V	5.5 V	"					"	V _{CC}		23	"	
2	Same tests, terminal conditions and limits as subgroup 1, except T _C = 125°C, and V _{IC} tests are omitted.																							
3	Same tests, terminal conditions and limits as subgroup 1, except T _C = -55°C, and V _{IC} tests are omitted.																							

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal All outputs	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLR	S/R Serial	A _N	B _N	C _N	D _N	S/L Serial	GND	S ₀	S ₁	CLK	QD	QC	QB	QA	V _{CC}				
7 T _C = 25°C	Truth table test	3014	59	C	B	B	B	B	B	B	B	GND	C	C	C	L	L	L	L	5.0V			
			60		B						B		C	C	B								
			61			B	B		C	D	B		C	C	C								
			62			C					C		B	B	C								
			63											B									
			64											C									
			65	B										C									
			66											B	H	H	H	H	H				
			67											C	H	H	H	H	H				
			68			B	C	C	C	C	C	B		C	H	H	H	H	H				
			69											B	L	L	L	L	L				
			70											C				L					
			71											C	C			L					
			72											B				H					
			73											C									
			74											B				H					
			75											C				H					
			76											B			H	H					
			77											C			H						
			78											B	H								
			79											C									
			80				C	B	B	B	B	B	C		C								
			81											B					L				
			82											C									
			83											B				L					
			84											C									
			85											B			L						
			86											C									
			87											B	L								
			88											C	L								
			89				B	C	C	C	C	C	B		C	B	C	L					
			90											B		H							
			91											C									
			92											B			H						
			93											C									
			94											B				H					
			95											C									
			96											B					H				
			97											C									
			97A											C	C								
			97B											C	B								
			97C											C	C								
			98				C	B	B	B	B	B	C		B		C						
			99												B	L							
			100												C								
			101												B		L						
			102												C								
			103												B			L					
			104												C								
			105												B				L				
			106												C								
			107												C	C							
			108												B								
			109												C								
			110						C	C	C	C			C								
			111						C	C	C	C			B								

See B, C, D, and E

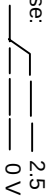
See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLR	S/R Serial	A _{IN}	IN	IN	IN	S/L Serial	GND	S ₀	1	CLK	QD	QC	QB	QA	V _{CC}				
8	Same tests, terminal conditions, and limits as subgroup 7, except ^B T _C = 125°C and ^D -55°C S																						
9 T _C = 25°C	f _{MAX} See F and J	(Fig. 4)	112	G		IN					GND	G	G	IN				OUT	5.0 V	CLK to QA	22		MHz
	PHL1	3003 (Fig. 4)	113	"		IN					"	"	"	"				OUT	"	CLK TO QA	5	27	ns
			114	"			IN				"	"	"	"			OUT	"	"	CLK TO QB	"	"	"
			115	"				IN			"	"	"	"		OUT		"	"	CLK TO QC	"	"	"
			116	"					IN		"	"	"	"		OUT		"	"	CLK TO QD	"	"	"
			117	"	IN						"	"	GND	"			OUT	"	"	CLK TO QA	"	"	"
	PHL1		118	"						IN	"	GND	G	"	OUT			"	"	CLK TO QD	"	"	"
			119	"		IN					"	G	"	"			OUT	"	"	CLK TO QA	"	31	"
			120	"			IN				"	"	"	"			OUT	"	"	CLK TO QB	"	"	"
			121	"				IN			"	"	"	"		OUT		"	"	CLK TO QC	"	"	"
			122	"					IN		"	"	"	"	OUT			"	"	CLK TO QD	"	"	"
	PHL2		123	"	IN						"	"	GND	"			OUT	"	"	CLK TO QA	"	"	"
			124	"						IN	"	GND	G	"	OUT			"	"	CLK TO QD	"	"	"
			125	IN		G					"	G	"	"			OUT	"	"	CLK TO QA	"	35	"
			126	"			G				"	"	"	"			OUT	"	"	CLK TO QB	"	"	"
			127	"				G			"	"	"	"		OUT		"	"	CLK TO QC	"	"	"
			128	"					G		"	"	"	"	OUT			"	"	CLK TO QD	"	"	"
10 T _C = 25°C	f _{MAX} See F and J	3003 (Fig. 4)	129	Same tests and terminal conditions as for subgroup 9																	20		MHz
	PHL1		130 to 135																		5	41	ns
	PHL1		136 to 141																		5	47	ns
	PHL2		142 to 145																		5	53	ns
11	Same tests, terminal conditions, and limits as subgroups 10, except T _C = -55°C.																						

See footnotes at end of device type 01.

FOOTNOTES:

A. Apply input pulse:  2.5 V minimum/5.5 V maximum
0 V

B. $V_{IN} = 2.5\text{ V}$.

C. $V_{IN} = 0.4\text{ V}$.

D. Test numbers 59 through 111 shall be run in sequence.

E. Output voltages shall be either: (1) $H \geq 2.5\text{ V}$ minimum and $L \leq 0.4\text{ V}$ maximum when using a high speed checker double comparator; (2) $H \geq 1.5\text{ V}$ and $L \leq 1.5\text{ V}$ when using a high speed checker single comparator.

F. f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the clock input frequency. The input frequency on the A_{IN} data shall be one-half of the clock input frequency and the A_{IN} shall be shifted such that the $A_{IN} \uparrow$ and $\downarrow$ are coincident with the clock $\downarrow$. Rise and fall times $\leq 6\text{ ns}$. Input peak voltage 3 to 5 volts.

G. 3.0 V minimum/5.0 V maximum.

J. At the manufacturer's option, the following alternate procedure may be used to guarantee f_{MAX} . Serial mode - f_{MAX} for the serial mode shall be guaranteed by clocking the device four times (after reset) at f_{MAX} and looking for the Q_D output to toggle within three periods ($3 \times 1/f_{MAX}$) plus allowed propagation delay. Two tests are performed, depending on the state of the data input, to guarantee both LH and HL transition of the output pulse.

1/ This pulse must occur after the clear pulse.

2/ I_L limits (mA) min/max values for circuits shown:

Parameter	Terminal	A	B	C	D	E	F	G
I_{L1}	CLR	-.16/-.4	-.11/-.35	-.16/-.4	-.12/-.35	-.12/-.36	-.12/-.36	-.16/-.4
I_{L2}	S/R, A_{IN} , B_{IN} C_{IN} , D_{IN} , S/L	"	-.11/-.35	"	-.16/-.4	-.105/-.345	"	"
I_{L3}	S_0 , S_1	"	-.03/-.3	"	-.12/-.36	-.12/-.36	"	"
I_{L4}	CLK	"	-.03/-.3	-.20/-.44	-.12/-.36	-.12/-.36	"	-.15/-.38

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
Test no.	CLR	J	$\bar{X}$	A _{IN}	B _{IN}	IN	GND	Shift Load	CLK	$\bar{Q}$ D	QD	QC	QB	QA	V _{CC}								
1 T _c = 25°C	V _{OH}	3005	1	B	2.0 V	2.0 V	2.0 V	2.0 V	0.7 V	GND	0.7 V	B $\bar{1}$	-4 mA						4.5 V	$\bar{Q}$ D	2.5		V
			2	"	"	"	"	"	2.0 V	"	"	"		-4 mA					"	QD	"		"
			3	"	"	"	"	"	"	"	"	"			-4 mA				"	QC	"		"
			4	"	"	"	"	"	"	"	"	"				-4 mA			"	QB	"		"
			5	"	"	"	"	"	"	"	"	"					-4 mA		"	QA	"		"
	OL	3007	6	"	"	"	0.7	0.7	0.7	"	"	"	"	4 mA					"	$\bar{Q}$ D		0.4	"
			7	"	"	"	"	"	"	0.7	"	"	"		4 mA				"	QD		"	"
			8	"	"	"	"	"	"	"	"	"	"			4 mA			"	QC		"	"
			9	"	"	"	"	"	"	"	"	"	"				4 mA		"	QB		"	"
			10	"	"	"	"	"	"	"	"	"	"					4 mA	"	QA		"	"
V	IC		11	-18 mA						"									"	CLR		-1.5	"
			12		-18 mA					"									"	J		"	"
			13			-18 mA				"									"	$\bar{K}$		"	"
			14				-18 mA			"									"	A _{IN}		"	"
			15					-18 mA		"									"	B _{IN}	"	"	"
			16						-18 mA	"									"	C _{IN}		"	"
			17							-18 mA	"								"	D _{IN}		"	"
			18							"	-18 mA								"	Shift load		"	"
			19							"		-18 mA							"	CLK		"	"
			20	2.7 V						"									5.5 V	CLR		20	μA
I	IH1	3010	21		2.7 V					"	GND	A							"	J		"	"
			22			2.7 V				"	GND								"	$\bar{K}$		"	"
			23				2.7 V			"	4.5 V								"	A _{IN}		"	"
			24					2.7 V		"	"								"	B _{IN}	"	"	"
			25						2.7 V	"	"								"	C _{IN}		"	"
			26							2.7 V	"	"							"	D _{IN}		"	"
			27							"	2.7 V								"	Shift load		"	"
			28							"		2.7 V							"	CLK		"	"
	IH2		29	5.5 V						"									"	CLR		100	"
			30		5.5 V					"	GND	A							"	J		"	"
			31			5.5 V				"	GND								"	$\bar{K}$		"	"
			32				5.5 V			"	4.5 V								"	A _{IN}		"	"
			33					5.5 V		"	"								"	B _{IN}	"	"	"
			34						5.5 V	"	"								"	C _{IN}		"	"
			35							5.5 V	"	"							"	D _{IN}		"	"
			36							"	5.5 V								"	Shift load		"	"
			37							"		5.5 V							"	CLK		"	"

See footnotes at end of device types 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLR	J	$\bar{K}$	A _{IN}	I _N	I _N	I _N	GND	Shift Load	CLK	$\bar{Q}$ D	QD	QC	QB	QA	V _{CC}				
1 T _C = 25°C	I _{IL1}	3009	38	0.4 V			B	C	D		GND								5.5 V	CLR	2/	2/	mA
			39	B	0.4 V						"	4.5 V							"	J	"	"	"
			40	B		0.4 V					"	4.5 V	1/ A or B						"	$\bar{K}$	"	"	"
			41				0.4 V				"	GND							"	A _{IN}	"	"	"
			42					0.4 V			"	"							"	B _{IN}	"	"	"
			43						0.4 V		"	"							"	C _{IN}	"	"	"
			44							0.4 V	"	"							"	D _{IN}	"	"	"
			45								"	0.4 V							"	Shift load	"	"	"
			46								"		0.4 V						"	CLK	"	"	"
	OS	3011	47	GND							"	4.5 V	4.5 V	GND					"	$\bar{Q}$ D	-15	-100	mA
			48	4.5 V			4.5 V	4.5 V	4.5 V	4.5 V	"	GND	B		GND				"	QD	"	"	"
			49	"			"	"	"	"	"	"	"			GND			"	QC	"	"	"
			50	"			"	"	"	"	"	"	"				GND		"	QB	"	"	"
			51	"			"	"	"	"	"	"	"					GND	"	QA	"	"	"
	CC	3005	52	B			"	"	"	"	"	"	4.5 V						"	V _{CC}		21	"
		3005	53	4.5 V			"	"	"	"	"	"	B						"	V _{CC}		21	"
2	Same tests, terminal conditions and limits as subgroup 1, except T _C = 125°C, and V _{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as subgroup 1, except T _C = -55°C, and V _{IC} tests are omitted.																						

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLR	J	$\overline{K}$	A _{IN}	IN	IN	IN	GND	Shift Load	CLK	$\overline{Q}_D$	QD	QC	QB	QA	V _{CC}				
7 T _C = 25°C	Truth table test	3014	54	D	C	C	C	C	C	C	GND	D	D	H	L	L	L	L	5.0V	All outputs	See C, D, E, and F		
			55	"	D	C	"	B	"	C	"	D	"	"	"	"	"	"	"				"
			56	"	D	D	"	"	"	D	"	D	"	"	"	"	"	"	"				"
			57	"	"	"	"	"	"	"	"	C	"	"	"	"	"	"	"				"
			58	C	"	"	"	"	"	"	"	C	"	"	"	"	"	"	"				"
			59	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"	"				"
			60	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"
			61	"	"	"	"	"	"	"	"	"	C	L	H	H	H	H	H				"
			62	"	C	C	D	D	D	D	"	D	L	H	H	H	H	H	H				"
			63	"	"	"	"	"	"	"	"	"	C	H	L	L	L	L	L				"
			64	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	L				"
			65	"	"	"	"	"	"	"	"	"	C	D	"	"	"	"	L				"
			66	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"	H				"
			67	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"				"
			68	"	"	"	"	"	"	"	"	"	C	"	"	"	"	H	"				"
			69	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"				"
			70	"	"	"	"	"	"	"	"	"	C	"	"	"	H	"	"				"
			71	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"				"
			72	"	"	"	"	"	"	"	"	"	C	L	H	"	"	"	"				"
			73	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"				"
			74	"	D	D	C	C	C	C	"	D	"	"	"	"	"	"	"				"
			75	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"	L				"
			76	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"				"
			77	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"	L				"
			78	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"				"
			79	"	"	"	"	"	"	"	"	"	C	"	"	"	"	L	"				"
			80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"
			81	"	"	"	"	"	"	"	"	"	C	H	L	"	"	"	"				"
			82	"	"	"	"	"	"	"	"	"	D	H	"	"	"	"	"				"
			83	"	C	"	D	D	D	D	"	D	"	"	"	"	"	"	"				"
			84	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"	"				H
			85	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	"				H
			86	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"	H				L
			87	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	H				L
			88	"	"	"	"	"	"	"	"	"	"	"	"	"	H	L	H				"
			89	"	"	"	"	"	"	"	"	"	D	"	"	"	H	L	H				"
			90	"	"	"	"	"	"	"	"	"	C	L	H	L	H	L	L				"
			91	"	"	"	"	"	"	"	"	"	D	L	H	L	H	L	L				"
			92	"	"	"	"	"	"	"	"	"	C	H	L	L	H	L	H				"
			93	"	"	"	"	"	"	"	"	"	D	H	L	L	H	L	H				"
			94	"	D	C	C	C	C	C	"	D	H	L	L	H	L	"	"				"
			95	"	"	"	"	"	"	"	"	"	C	L	H	L	L	H	"				"
			96	"	"	"	"	"	"	"	"	"	D	L	H	L	L	"	"				"
			97	"	"	"	"	"	"	"	"	"	C	H	L	L	H	"	"				"
			98	"	"	"	"	"	"	"	"	"	D	H	L	L	H	"	"				"
			99	"	"	"	"	"	"	"	"	"	C	L	H	L	H	"	"				"
8	Same tests, terminal conditions, and limits as subgroup 7 except T _C = 125°C and -55°C.																						
9 T _C = 25°C	f _{MAX} See G	(Fig. 5)	100	J			IN				GND	GND	IN					OUT	5.0 V	QA	27		MHz
			101	"				IN			"	"	"					"	"	QB	"		"
			102	"					IN		"	"	"			OUT		"	"	QC	"		"
			103	"						IN	"	"	"		OUT			"	"	QD	"		"
			104	"						IN	"	"	"	OUT				"	"	$\overline{Q}_D$	"		"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit			
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max				
			Test no.	CLR	J	$\bar{K}$	A_{IN}	IN	IN	IN	IN	GND	Shift load	CLK	$\bar{Q}$ D	QD	QC	QB	QA	V_{CC}						
9 $T_C = 25^{\circ}\text{C}$	t_{PHL1}	3003 (Fig. 5)	105	J	J	J	B	C	D			GND	J	IN					OUT	5.0 V	CLK to QA	5	27	ns		
			106	"	"	See Fig. 5	See Fig. 5						"	"	"				OUT		"	CLK TO QB	"	"	"	
			107	"	"	"	"						"	"	"			OUT			"	CLK TO QC	"	"	"	
			108	"	"	"	"						"	"	"			OUT			"	CLK TO QD	"	"	"	
			109	"	"	"	"						"	"	"	OUT					"	CLK TO $\bar{Q}$ D	"	"	"	
			110	"				IN					"	GND	"					OUT	"	CLK TO QA	"	"	"	
			111	"					IN				"	"	"				OUT		"	CLK TO QB	"	"	"	
			112	"						IN			"	"	"				OUT		"	CLK TO QC	"	"	"	
			113	"							IN		"	"	"			OUT			"	CLK TO QD	"	"	"	
			114	"							IN		"	"	"	OUT					"	CLK TO QD	"	"	"	
			PHL1		115	"	GND	GND					"	J	"					OUT	"	CLK TO QA	"	31	"	
				116	"	See Fig. 5	See Fig. 5						"	"	"					OUT		"	CLK TO QB	"	"	"
				117	"	"	"	"					"	"	"				OUT		"	CLK TO QC	"	"	"	
				118	"	"	"	"					"	"	"				OUT		"	CLK TO QD	"	"	"	
		119	"	"	"	"					"	"	"	OUT					"	CLK TO $\bar{Q}$ D	"	"	"			
	t		120	"				IN				"	GND	"					OUT	"	CLK TO QA	"	"	"		
			121	"					IN			"	"	"					OUT	"	CLK TO QB	"	"	"		
			122	"						IN		"	"	"					OUT	"	CLK TO QC	"	"	"		
			123	"							IN	"	"	"				OUT		"	CLK TO QD	"	"	"		
			124	"							IN	"	"	"	OUT					"	CLK TO $\bar{Q}$ D	"	"	"		
PHL2			125	IN			J				"	"	"					OUT	"	CLK TO QA	"	35	"			
		126	"					J			"	"	"					OUT	"	CLK TO QB	"	"	"			
		127	"						J		"	"	"					OUT	"	CLK TO QC	"	"	"			
		128	"							J	"	"	"					OUT	"	CLK TO QD	"	"	"			
PHL2			129	"							J	"	"	"	OUT				"	CLR TO $\bar{Q}$ D	"	"	"			
10 $T_C = 125^{\circ}\text{C}$	f_{MAX} See G		130 to 134	Same tests and terminal conditions as for subgroup 9																	25		MHz			
	t_{PLH1}		135 to 144																		5	41	ns			
	t_{PHL1}		145 to 154																		"	47	"			
	t_{PHL2}		155 to 158																		"	53	"			
	t_{PHL2}		159																		"	53	"			
	11	Same tests, terminal conditions, and limits as subgroups 10, except $T_C = -55^{\circ}\text{C}$.																								

See footnotes at end of device type 02.

FOOTNOTES:

A. Apply input pulse:  2.5 V minimum/5.5 V maximum
0 V

B. Apply input pulse:  2.5 V minimum/5.5 V maximum.
0 V

C. $V_N = 2.5$ V.

D. $V_N = 0.4$ V.

E. Test numbers 54 through 99 shall be run in sequence.

F. Output voltages shall be either: (1) $H \geq 2.5$ V minimum and $L \leq 0.4$ V maximum when using a high speed checker double comparator; (2) $H \geq 1.5$ V and $L \leq 1.5$ V when using a high speed checker single comparator.

f_{max} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the parallel input shall be one-half of the clock input frequency and the parallel input shall be shifted such that the parallel input $\uparrow$ and $\downarrow$ are coincident with the clock $\downarrow$. Rise and fall times ≤ 6 ns. Input peak voltage 3 to 5 volts.

J. 3.0 V minimum/5.0 V maximum.

J This pulse must occur after the clear pulse.

J I_L limits (mA) min/max values for circuits shown:

Parameter	Terminal	A	B	C	D	E	F	G
I_{L1}	CLR	-.16/- .4	-.11/- .35	-.16/- .4	-.12/- .35	-.12/- .36	-.12/- .36	-.16/- .4
	J, K, A_N , B_N , C_N , D_N	"	-.16/- .4	"	-.16/- .4	-.105/- .345	"	"
	Shift load	"	-.08/- .3	"	-.12/- .36	-.12/- .36	"	"
	CLK	"	-.03/- .3	-.20/- .44	-.12/- .36	-.12/- .36	"	-.15/- .38

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Cases 2,X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max	
			Test no.	Serial	A _{IN}	B _{IN}	_{IN}	_{IN}	Mode	GND	CLK ₂	CLK ₁	QD	QC	QB	QA	V _{CC}				
1 Tc = 25°C	V _{OH}	3006	1	2.0 V	GND	GND	GND	GND	0.7 V	GND	GND	A				-4 mA	4.5 V	QA	2.5		V
			2		2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	"	A	GND				-4 mA	"	QA	"		"
			3		"	"	"	"	"	"	"	"			-4 mA		"	QB	"		"
			4		"	"	"	"	"	"	"	"		-4 mA			"	QC	"		"
			5		"	"	"	"	"	"	"	"	-4 mA				"	QD	"		"
	V	3007	6	0.7 V	4.5 V	4.5 V	4.5 V	4.5 V	0.7 V	"	GND	A				4 mA	"	QA	"	0.4	"
			7		0.7 V	0.7 V	0.7 V	0.7	2.0 V	"	A	GND				4 mA	"	QA		"	"
			8		"	"	"	"	"	"	"	"			4 mA		"	QB		"	"
			9		"	"	"	"	"	"	"	"		4 mA			"	QC		"	"
			10		"	"	"	"	"	"	"	"	4 mA				"	QD		"	"
	V		11	-18 mA						"							"	Serial		-1.5	"
			12		-18 mA					"							"	A _{IN}		"	"
			13			-18 mA				"							"	B _{IN}		"	"
			14				-18 mA			"							"	C _{IN}		"	"
			15					-18 mA		"							"	D _{IN}		"	"
			16						-18 mA	"							"	Mode		"	"
			17							"	-18 mA						"	CLK ₂		"	"
			18							"		-18 mA					"	CLK ₁		"	"
	I	3010	19	2.7 V					4.5 V	"							5.5 V	Serial		20	μA
			20		2.7 V				GND	"							"	A _{IN}		"	"
			21			2.7 V			"	"							"	B _{IN}		"	"
			22				2.7 V		"	"							"	C _{IN}		"	"
			23					2.7 V	"	"							"	D _{IN}		"	"
			24						4.5 V	"	2.7 V						"	CLK ₂		"	"
			25						4.5 V	"		2.7 V					"	CLK ₁		"	"
			26	5.5 V					4.5 V	"							"	Serial		100	"
	I		27		5.5 V				GND	"							"	A _{IN}		"	"
			28			5.5 V			"	"							"	B _{IN}		"	"
			29				5.5 V		"	"							"	C _{IN}		"	"
			30					5.5 V	"	"							"	D _{IN}		"	"
			31						4.5 V	"	5.5 V						"	CLK ₂		"	"
			32						4.5 V	"		5.5 V					"	CLK ₁		"	"
			33						2.7 V	"	GND						"	Mode		40	"
	IH8		34						5.5 V	"	GND						"	Mode		200	"

See footnotes at end of device types 03.

TABLE III. Group A inspection for device type 03 - Continued
Terminal conditions (pins not designated may be high ≥ 2.0 V or low ≤ 0.7 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test Limits		Unit		
			Cases 2, X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max			
			Test no.	Serial	A _{IN}	IN	IN	IN	Mode	GND	CLK ₂	CLK ₁	QD	QC	QB	QA	V _{CC}						
1 T _C = 25°C	I _{IL2}	3009	35	0.4 V					GND	GND								5.5 V	Serial	1/	1/	mA	
			36		0.4 V _B		C	D	4.5 V	"								"	A	"	"	"	
			37			0.4 V			"	"								"	B	"	"	"	
			38				0.4 V			"	"							"	C	"	"	"	
			39					0.4 V	"	"								"	D	"	"	"	
			40						0.4 V	"	4.5 V							"	Mode	"	"	"	
	IL4		41						4.5 V	"	0.4 V						"	CLK ₂		"	"	"	
			42						GND	"		0.4 V					"	CLK ₁		"	"	"	
	OS	3011	43		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	"	A	GND					GND	"	QA	"	-15	-100	"
			44		"	"	"	"	"	"	"	"			GND		"	QB	"	"	"	"	
45				"	"	"	"	"	"	"	"		GND		"	QC	"	"	"	"	"		
46				"	"	"	"	"	"	"	"	GND			"	QD	"	"	"	"	"		
CC	3005	47		GND	GND	GND	GND	5.5 V	"	"	A					"	V _{CC}		21	"			
2	Same tests, terminal conditions and limits as subgroup 1, except T _C = 125°C and V _{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																						
7 T _C = 25°C	Truth table test	3014	48	B	B	B	B	B	B	GND	B	C	X	X	X	X	5.0 V	All outputs	See B,C,D, and E				
			49	B	B	B	B	B	"	"	C	"	H	H	H	H	"						
			50	"	B	B	B	B	"	"	B	"	H	H	H	H	"						
			51	"	C	C	C	C	"	"	B	"	H	H	H	H	"						
			52	"	C	C	C	C	"	"	C	"	L	L	L	L	"						
			53	"	B	B	B	B	C	"	"	B	"	"	"	L	"						
			54	"	C	C	C	C	"	"	"	B	"	"	"	L	"						
			55	"	"	"	"	"	"	"	"	C	"	"	"	H	"						
			56	"	"	"	"	"	"	"	"	B	"	"	"	"	"						
			57	"	"	"	"	"	"	"	"	C	"	"	H	"	"						
			58	"	"	"	"	"	"	"	"	B	"	"	"	"	"						
			59	"	"	"	"	"	"	"	"	C	"	H	"	"	"						
			60	"	"	"	"	"	"	"	"	B	"	H	"	"	"						
			61	"	"	"	"	"	"	"	"	C	H	H	"	"	"						

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

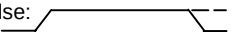
Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Cases 2, X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max	
			Test no.	Serial	A _{IN}	_{IN}	_{IN}	_{IN}	Mode	GND	CLK ₂	CLK ₁	QD	QC	QB	QA	V _{CC}				
7 T _C = 25°C tests	Truth table	3014	62	B	C	C	C	C	C	GND	C	B	H	H	H	H	5.0 V	All outputs	See B,C,D, and E		
			63	C	B _B	B _C	B _D	B	"	"	B	B	"	"	"	H	"				
			64	"	"	"	"	"	"	"	"	C	"	"	"	L	"				
			65	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			66	"	"	"	"	"	"	"	"	C	"	"	L	"	"				
			67	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			68	"	"	"	"	"	"	"	"	C	"	L	"	"	"				
			69	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			70	"	"	"	"	"	"	"	"	C	L	"	"	"	"				
			71	"	"	"	"	"	"	"	"	C	"	"	"	"	"				
			72	"	"	"	"	"	"	B	"	C	"	"	"	"	"				
			73	"	"	"	"	"	"	C	"	C	"	"	"	"	"				
			74	"	"	"	"	"	"	C	"	B	"	"	"	"	"				
			75	"	"	"	"	"	"	B	"	B	"	"	"	"	"				
			76	"	"	"	"	"	"	B	"	C	B	H	H	H	H				
			77	"	"	"	"	"	"	C	"	C	"	"	"	"	"				
			78	"	"	"	"	"	"	C	"	B	"	"	"	"	"				
			79	"	"	"	"	"	"	B	"	B	"	"	"	"	"				
8	Same tests, terminal conditions, and limits as subgroup 7 except T _C = 125°C and -55°C.																				
9 T _C = 25°C t	f _{MAX} See F,J	(Fig. 6)	80		IN				G	GND	IN					OUT	5.0 V	QA	22		MHz
			81			IN			"	"	"				OUT		"	QB	"		"
			82				IN		"	"	"						"	QC	"		"
			83					IN	"	"	"		OUT				"	QD	"		"
	PLH1	3003 (Fig. 6)	84	IN					GND	"		IN				OUT	"	QA	"		"
			85		IN				G	"	IN		OUT			OUT	"	CLK to QA	5	32	ns
			86			IN			"	"	"				OUT		"	CLK to QB	"	"	"
			87				IN		"	"	"			OUT			"	CLK to QC	"	"	"
			88					IN	"	"	"		OUT			"	"	CLK to QD	"	"	"
			89	IN					GND	"		IN				OUT	"	CLK to QA	"	"	"
			90	"					"	"		"				OUT	"	CLK to QB	"	"	"
			91	"					"	"		"			OUT		"	CLK to QC	"	"	"
	PLH1		92	"					"	"		"		OUT			"	CLK to QD	"	"	"
			93		IN				G	"	IN					OUT	"	CLK to QA	"	37	"
94					IN			"	"	"					OUT	"	CLK to QB	"	"	"	
95						IN		"	"	"			OUT		"	"	CLK to QC	"	"	"	
96							IN	"	"	"		OUT			"	"	CLK to QD	"	"	"	
97			IN					GND	"		IN					OUT	"	CLK to QA	"	"	"
98			"					"	"		"				OUT	"	CLK to QB	"	"	"	
t			99	"					"	"			OUT		"	CLK to QC	"	"	"		
			100	"					"	"		"	OUT		"	"	CLK to QD	"	"	"	

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V or low ≤ 0.7 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Cases 2, X	2	3	4	6	8	9	10	12	13	14	16	18	19	20				
			Test no.	Serial	A _{IN}	IN	IN	IN	Mode	GND	CLK ₂	CLK ₁	QD	QC	QB	QA	V _{CC}		Min	Max	
10 T _C = 25°C	f _{MAX} See F,J	3003 (Fig. 6)	101 to 105	B C D Same tests and terminal conditions as for subgroup 9.															20	---	MHz
	t _{PLH1}	3003 (Fig. 6)	106 to 113																5	48	ns
	t _{PHL1}	3003 (Fig. 6)	114 to 121																5	56	ns
11	Same tests, terminal conditions as subgroup 10 except T _C = -55°C.																				

Notes:

A. Apply input pulse:  2.5 V minimum/5.5 V maximum
0 V

V_{IN} = 2.5 V.

B.

C. V_{IN} = 0.4 V.

D. Tests numbers 48 through 79 shall be run in sequence.

E. Output voltages shall be either: (1) H ≥ 2.5 minimum and L ≤ 0.4 V maximum when using a high speed checker double comparator; (2) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

F. f_{MAX} minimum limit specified is the frequency of the clock input pulse.
The output frequency shall be one-half of the input clock frequency. The input frequency on the serial input shall be one-half of the clock input frequency and the input shall be shifted such that the input $\uparrow$ and $\downarrow$ are coincident with the clock $\uparrow$. Rise and fall times ≤ 6 ns. Input peak voltage 3 to 5 volts.

G. 3.0 V minimum/5.0 V maximum.

J. At the manufacturer's option, the following alternate procedures may be used to guarantee f_{MAX}:

- a. Parallel mode. f_{MAX} for the parallel mode shall be guaranteed by performing propagation delay measurements with the clock pulse width at $1/2 \times 1/f_{MAX}$. In addition to the constraints on the clock pulse, the inputs are set to the worst-case condition for the t_{set-up} and t_{hold} requirements. Both positive and negative clock pulse widths shall be tested. The five tests to justify each JAN f_{MAX} requirement shall be used to test all possible input/output combinations. A failing limit or nontoggle will indicate that the device fails to function at f_{MAX} and/or the propagation delay from input to output has exceeded the allowed limit.
- b. Serial mode. f_{MAX} for the serial mode shall be guaranteed by clocking the device four times (after reset) at f_{MAX} and looking for the Q_D output to toggle within three periods ($3 \times 1/f_{MAX}$) plus allowed propagation delay. Two tests are performed, depending on the state of data input, to guarantee both LH and HL transition of the output pulse.

1/ I_L limits (mA) min/max values for circuits shown:

Parameter	Terminal	A	B	C	D	E
I _{IL2}	Serial A, B, C, D	-.16/-.4	-.11/-.35	-.16/-.4	-.105/-.345	-.12/-.35
I _{IL4}	Mode	"	-.06/-.6	-.30/-.75	-.24/-.72	"
	CLK ₂ , 1	"	-.03/-.3	-.20/-.44	-.12/-.36	"

CLK

TABLE III. Group A inspection for device type 04.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLK	A _{IN}	B _{IN}	_{IN}	CC	_{IN}	E _{IN}	Enable	Serial	QE	QD	GND	QC	QB	QA	CLR				
1 T _C = 25°C	V _{OH}	3006	1	2.0 V	2.0 V	2.0 V	2.0 V	4.5 V	2.0 V	2.0 V	2.0 V	2.0 V			GND			-4 mA	2.0 V	QA	2.5		V
			2	"	"	"	C	"	V	"	D	"			"		-4 mA		"	QB	"		"
			3	"	"	"	"	"	"	"	"	"			"	-4 mA			"	QC	"		"
			4	"	"	"	"	"	"	"	"	"		-4 mA	"				"	QD	"		"
			5	"	"	"	"	"	"	"	"	"	-4 mA		"				"	QE	"		"
	V	3007	6	"	"	"	"	"	"	"	0.7 V				"			4 mA	0.7 V	QA		0.4	"
			7	"	"	"	"	"	"	"	"				"		4 mA		"	QB	"		"
			8	"	"	"	"	"	"	"	"				"	4 mA			"	QC	"		"
			9	"	"	"	"	"	"	"	"			4 mA	"				"	QD	"		"
			10	"	"	"	"	"	"	"	"		4 mA		"				"	QE	"		"
	V	IC	11	-18 mA				"							"					CLK		-1.5	"
			12		-18 mA			"							"					A _{IN}		"	"
			13			-18 mA		"							"					B _{IN}		"	"
			14				-18 mA	"							"					C _{IN}		"	"
			15					"	-18 mA						"					D _{IN}		"	"
			16					"		-18 mA					"					E _{IN}		"	"
			17					"			-18 mA				"					Enable		"	"
			18					"				-18 mA			"					Serial		"	"
			19					"							"			-18 mA		CLR		"	"
	I	IH5	20	2.7 V	GND	GND	GND	5.5 V	GND	GND	GND	GND			"				GND	CLK		20	μA
			21	GND	2.7 V	GND	GND	"	"	"	"	"			"				"	A _{IN}		"	"
			22	"	GND	2.7 V	GND	"	"	"	"	"			"				"	B _{IN}		"	"
			23	"		GND	2.7 V	"	"	"	"	"			"				"	C _{IN}		"	"
			24	"	"	"	GND	2.7 V	"	"	"	"			"				"	D _{IN}		"	"
			25	"	"	"	"	"	GND	2.7 V	"	"			"				"	E _{IN}		"	"
			26	"	"	"	"	"	"	GND	"	2.7 V			"				"	Serial		"	"
			27	"	"	"	"	"	"	"	"	GND			"				2.7 V	CLR		"	"
	I	IH6	28	5.5 V	"	"	"	"	"	"	"	"			"				GND	CLK		100	"
			29	GND	5.5 V	"	"	"	"	"	"	"			"				"	A _{IN}		"	"
			30	"	GND	5.5 V	"	"	"	"	"	"			"				"	B _{IN}		"	"
			31	"	"	GND	5.5 V	"	"	"	"	"			"				"	C _{IN}		"	"
			32	"	"	"	GND	"	5.5 V	"	"	"			"				"	D _{IN}		"	"
			33	"	"	"	"	"	GND	5.5 V	"	"			"				"	E _{IN}		"	"
			34	"	"	"	"	"	"	GND	"	5.5 V			"				"	Serial		"	"
			35	"	"	"	"	"	"	"	"	GND			"			5.5 V		CLR		"	"
	I	IH9	36	"	"	"	"	"	"	"	2.7 V	GND			"				GND	Enable		"	"
			37	"	"	"	"	"	"	"	5.5 V	GND			"				GND	Enable		"	"
	I	IL3	3009	38	0.4 V	4.5 V	4.5 V	4.5 V	"	4.5 V	4.5 V	4.5 V			"				4.5 V	CLK	1/500	1/	mA
				39	4.5 V	0.4 V	4.5 V	"	"	"	"	"			"				"	A _{IN}	"	"	"
				40	"	4.5 V	0.4 V	"	"	"	"	"			"				"	B _{IN}	"	"	"
				41	"	"	4.5 V	0.4 V	"	"	"	"			"				"	C _{IN}	"	"	"
				42	"	"	4.5 V	4.5 V	"	0.4 V	"	"			"				"	D _{IN}	"	"	"

See footnotes at end of device types 04.

TABLE III. Group A inspection for device type 04 - Continued
Terminal conditions (pins not designated may be high ≥ 2.0 V or low ≤ 0.7 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
1 $T_C = 25^\circ\text{C}$	I _{IL3}	3009	Test no.	CLK	A _{IN}	I _{IN}	I _{IN}	I _{CC}	I _{IN}	I _{IN}	Enable	Serial	QE	QD	GND	QC	QB	QA	CLR	E _{IN}	/	1/	mA
			43	4.5 V	4.5 V	4.5 V	4.5 V	5.5 V	4.5 V	0.4 V	4.5 V	4.5 V			GND				4.5 V	Serial	"	"	"
			44	"	" B	" C	" V	" D	" E	4.5 V	"	0.4 V			"				4.5 V	CLR ₁	"	"	"
			45	"	"	"	"	"	"	"	"	4.5 V			"				0.4 V		"	"	"
	I _{IL5}	3011	46	"	"	"	"	"	"	"	0.4 V	"			"				4.5 V	Enable	"	"	"
			47	"	"	"	"	"	"	"	4.5 V	"			"			GND	"	QA	-15	-100	"
			48	"	"	"	"	"	"	"	"	"			"		GND		"	QB	"	"	"
			49	"	"	"	"	"	"	"	"	"			"	GND			"	QC	"	"	"
			50	"	"	"	"	"	"	"	"	"		GND	"				"	QD	"	"	"
			51	"	"	"	"	"	"	"	"	"	GND		"				"	QE	"	"	"
	CC	3005	52					"							"				GND	V _{CC}		20	"
2 I	Same tests, terminal conditions, and limits as subgroup 1, except $T_C = 125^\circ\text{C}$ and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as subgroup 1, except $T_C = -55^\circ\text{C}$ and V_{IC} tests are omitted.																						
7 $T_C = 25^\circ\text{C}$	Truth table test	3014	53	B	A	A	A	5.0 V	A	A	B	B	L	L	GND	L	L	L	B	All outputs	See A,B,C, and D		
			54	A	"	"	"	"	"	"	B	A	L	L	"	L	L	L	B				
			55	B	"	"	"	"	"	"	B	B	L	L	"	L	L	L	B				
			56	"	"	"	"	"	"	"	A	"	H	H	"	H	H	H	A				
			57	"	B	B	B	"	B	B	"	"	H	H	"	H	H	H	A				
			58	"	"	"	"	"	"	"	"	"	L	L	"	L	L	L	B				
			59	"	"	"	"	"	"	"	B	"	"	"	"	"	"	L	A				
			60	"	"	"	"	"	"	"	"	A	"	"	"	"	"	L	"				
			61	A	"	"	"	"	"	"	"	"	"	"	"	"	"	H	"				
			62	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			63	A	"	"	"	"	"	"	"	"	"	"	"	"	H	"	"				
			64	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			65	A	"	"	"	"	"	"	"	"	"	"	"	H	"	"	"				
			66	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			67	A	"	"	"	"	"	"	"	"	"	H	"	"	"	"	"				
			68	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			69	A	"	"	"	"	"	"	"	"	H	"	"	"	"	"	"				
			70	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			71	B	A	A	A	"	A	A	"	B	"	"	"	"	"	"	"				
			72	A	"	"	"	"	"	"	"	"	"	"	"	"	"	L	"				
			73	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			74	A	"	"	"	"	"	"	"	"	"	"	"	"	L	"	"				
			75	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			76	A	"	"	"	"	"	"	"	"	"	"	"	L	"	"	"				
			77	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			78	A	"	"	"	"	"	"	"	"	"	L	"	"	"	"	"				
			79	B	"	"	"	"	"	"	"	"	"	L	"	"	"	"	"				
			80	A	"	"	"	"	"	"	"	"	L	L	"	"	"	"	"				

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit	
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max		
			Test no.	CLK	A _{IN}	IN	IN	CC	D _{IN}	IN	Enable	Serial	QE	QD	GND	QC	QB	QA	CLR					
8	Same tests, terminal conditions, and limits as subgroup 7, except T _C $\bar{V}$ 125°C and -55°C _E																							
9 T _C = 25°C	t	f _{MAX} see note E	(Fig. 7)	81	IN				5.0 V			GND	IN			GND			OUT	F	QA	20		MHz
		PLH1	3003 (Fig. 7)	82	"				"			"	IN			"			OUT	"	CLK TO QA	5	45	ns
				83	"						"	See figure 7			"			OUT		"	CLK TO QB	"	"	"
				84	"						"				"	OUT		"	CLK TO QC	"	"	"		
				85	"				"		"			OUT	"			"	CLK TO QD	"	"	"		
				86	"						"		OUT		OUT			"	CLK TO QE	"	"	"		
	t	PLH2		87	GND	IN		"	"		F			"				OUT	IN	A _{IN} TO QA	"	40	"	
				88	"		IN	"	"		"			"			OUT		"	B _{IN} TO QB	"	"	"	
				89	"			IN	"		"			"		OUT		"	C _{IN} TO QC	"	"	"		
				90	"				"	IN	"			OUT	"			"	D _{IN} TO QD	"	"	"		
				91	"				"		IN	"		OUT	"			"	E _{IN} TO QE	"	"	"		
				92	"	F					IN				"			OUT	"	Enable to QA	"	"	"	
				93	"		F		"			"			"			OUT	"	Enable to QB	"	"	"	
				94	"			F	"		"				"		OUT		"	Enable to QC	"	"	"	
				95	"				"	"	F	"			OUT	"			"	Enable to QD	"	"	"	
				96	"				"	"	F	"		OUT		"			"	Enable to QE	"	"	"	
	t	PHL1		97	IN			"			GND	IN			"			OUT	F	CLK TO QA	"	45		
				98	"			"			"			"			OUT		"	CLK TO QB	"	"		
				99	"						"			"		OUT		"	CLK TO QC	"	"			
				100	"				"		"			OUT	"			"	CLK TO QD	"	"			
				101	"				"		"		OUT		"			"	CLK to QE	"	"			
	t	PHL2		102	GND	F		"			IN			"				OUT	IN	CLR to QA	"	60		
				103	"		F				"				"			OUT	"	CLR to QB	"	"		
				104	"			F	"		"			"				"	CLR to QC	"	"			
				105	"			"	"	F	"			OUT	"			"	CLR to QD	"	"			
				106	"			"	"		F	"		OUT		"		"	CLR to QE	"	"			

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued
Terminal conditions (pins not designated may be high ≥ 2.0 V or low ≤ 0.7 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLK	A _{IN}	IN	IN	CC	IN	IN	Enable	Serial	QE	QD	GND	QC	QB	QA	CLR				
10 T _C = 25°C	f _{max} See E	(Fig. 7)	107	B C V D E																	17	---	MHz
	t _{PLH1}	3003 (Fig. 7)	108 to 112	Same tests and terminal conditions as for subgroup 9.																	5	68	ns
	t _{PLH2}		113 to 122																		"	60	"
	t _{PHL1}		123 to 127																		"	68	"
	t _{PHL2}		128 to 132																		"	90	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T _C = -55°C.																						

Notes:

A. V_{IN} = 2.5 V.

B. V_{IN} = 0.4 V.

C. Tests numbers 53 through 80 shall be run in sequence.

D. Output voltages shall be either: (1) H ≥ 2.5 V minimum and L ≤ 0.4 V maximum when using a high speed checker double double comparator; (2) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

E. f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the serial data shall be one-half of the clock input frequency and the serial shall be shifted such that the serial $\uparrow$ and $\downarrow$ are coincident with the clock $\downarrow$. Rise and fall times ≤ 6 ns. Input peak voltage 3 to 5 volts.

1/ I_{IL} limits (mA) min/max values for circuits shown:

Parameter	Terminal	A	B
I _{IL3}	CLK	-.16/- .40	-.16/- .40
	A _{IN} , B _{IN} , C _{IN}	-.16/- .40	-.12/- .36
	D _{IN} , E _{IN} , CLR		
	Serial	-.10/- .34	-.10/- .34
I _{IL5}	Enable	-.8/- 2.0	-.6/- 1.8

F. 3.0 V minimum/5.0 V maximum.

TABLE III. Group A inspection for device type 05.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max	
			Test no.	A _{IN}	B _{IN}	QA	QB	QC	QD	GND	CLK	CLR	QE	QF	QG	QH	V _{CC}				
1 T _c = 25°C	V _{OH}	3006	1	2.0 V	2.0 V	-4 mA				GND	J 1/ GND	2.0 V					4.5 V	QA	2.5		V
			2	"	"		-4 mA			"	" 2/ "	"					"	QB	"		"
			3	"	"			-4 mA		"	" 3/ "	"					"	QC	"		"
			4	"	"				-4 mA	"	" 4/ "	"					"	QD	"		"
			5	"	"					"	" 5/ "	"	-4 mA				"	QE	"		"
			6	"	"					"	" 6/ "	"		-4 mA			"	QF	"		"
			7	"	"					"	" 7/ "	"			-4 mA		"	QG	"		"
			8	"	"					"	" 8/ "	"				-4 mA	"	QH	"		"
	V	3007	9			4 mA				"		0.7 V					"	QA		0.4	"
			10				4 mA			"							"	QB		"	"
			11					4 mA		"							"	QC		"	"
			12						4 mA	"							"	QD		"	"
			13							"	"		4 mA				"	QE		"	"
			14							"	"			4 mA			"	QF		"	"
			15							"	"				4 mA		"	QG		"	"
	V	IC	16							"	"					4 mA	"	QH		"	"
			17	-18 mA						"	"						"	A _{IN}		-1.5	"
			18		-18 mA					"	"						"	B _{IN}		"	"
			19							"	-18 mA						"	CLK		"	"
	I	3010	20							"		-18 mA					"	CLR		"	"
			21	2.7 V	GND					"							5.5 V	A _{IN}		20	μA
			22	GND	2.7 V					"							"	B _{IN}		"	"
			23							"	2.7 V						"	CLK		"	"
	I	IH2	24							"		2.7 V					"	CLR		"	"
			25	5.5 V	GND					"							"	A _{IN}		100	"
			26	GND	5.5 V					"							"	B _{IN}		"	"
			27							"	5.5 V						"	CLK		"	"
	I	3009	28							"		5.5 V					"	CLR		"	"
			29	0.4 V	4.5 V					"							"	A _{IN}	10/	10/	mA
			30	4.5 V	0.4 V					"							"	B _{IN}	"	"	"
			31							"	0.4 V						"	CLK	"	"	"
			32							"		0.4 V					"	CLR	"	"	"

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued
Terminal conditions (pins not designated may be high ≥ 2.0 V or low ≤ 0.7 V or open).

Terminal conditions (pins not designated may be high ≥ 2.0 V or low ≤ 0.7 V or open).																						
Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test Limits		Unit	
			Cases 2, X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max		
			Test no.	A _{IN}	B _{IN}	QA	QB	QC	QD	GND	CLK	CLR	QE	QF	QG	QH	V _{CC}					
1 T _C = 25°C	I _{OS}	3011	33 9/	4.5 V	4.5 V	GND					"	A 1/	4.5 V					5.5 V	QA	-15	-100	mA
			34 "	"	"		GND			"	2/	"					"	QB	"	"	"	
			35 "	"	"			GND		"	3/	"					"	QC	"	"	"	
			36 "	"	"				GND	"	4/	"					"	QD	"	"	"	
			37 "	"	"					"	5/	"	GND				"	QE	"	"	"	
			38 "	"	"					"	6/	"		GND			"	QF	"	"	"	
			39 "	"	"					"	7/	"			GND		"	QG	"	"	"	
			40 "	"	"					"	8/	"				GND	"	QH	"	"	"	
CC	3005	41	GND	GND					"	5.5 V	J					"	V _{CC}			"		
2	Same tests, terminal conditions and limits as subgroup 1, except T _C = 125°C and V _{IC} tests are omitted.																				27	
3	Same tests, terminal conditions and limits as subgroup 1, except T _C = 125°C and V _{IC} tests are omitted																					
7 T _C = 25°C	Truth table	3014	42	B	B	L	L	L	L	GND	C	C	L	L	L	L	5.0 V	All outputs	See B,C,D and E			
			43	"	"	"	"	"	"	"	"	B	C	"	"	"	"					"
			44	"	"	"	"	"	"	"	"	C	C	"	"	"	"					"
			45	"	"	"	"	"	"	"	"	"	B	"	"	"	"					"
			46	C	C	"	"	"	"	"	"	"	"	"	"	"	"					"
			47	B	B	"	"	"	"	"	"	"	"	"	"	"	"					"
			48	"	"	H	"	"	"	"	"	B	"	"	"	"	"					"
			49	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			50	"	"	"	H	"	"	"	"	B	"	"	"	"	"					"
			51	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			52	"	"	"	"	H	"	"	"	B	"	"	"	"	"					"
			53	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			54	"	"	"	"	"	"	H	"	B	"	"	"	"	"					"
			55	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			56	"	"	"	"	"	"	"	"	B	"	H	"	"	"					"
			57	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			58	"	"	"	"	"	"	"	"	B	"	"	H	"	"					"
			59	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			60	"	"	"	"	"	"	"	"	B	"	"	"	H	"					"
			61	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			62	"	"	"	"	"	"	"	"	B	"	"	"	"	H					"
			63	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			64	C	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			65	"	"	L	"	"	"	"	"	B	"	"	"	"	"					"
			66	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			67	"	"	"	L	"	"	"	"	B	"	"	"	"	"					"
			68	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			69	"	C	"	"	"	"	"	"	C	"	"	"	"	"					"
			70	"	"	"	"	"	L	"	"	B	"	"	"	"	"					"
			71	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			72	"	"	"	"	"	"	"	L	"	B	"	"	"	"					"
			73	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			74	B	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			75	"	"	"	"	"	"	"	"	B	"	L	"	"	"					"
			76	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			77	"	"	"	"	"	"	"	"	B	"	"	L	"	"					"
			78	"	"	"	"	"	"	"	"	C	"	"	"	"	"					"
			79	"	"	"	"	"	"	"	"	B	"	"	"	L	"					"
			80	"	"	"	"	"	"	"	"	C	"	"	"	L	"					"
			81	"	"	"	"	"	"	"	"	B	"	"	"	L	L					"

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

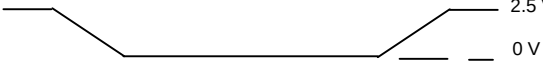
Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Cases 2, X	2	3	4	6	8	9	10	12	13	14	16	18	19	20		Min	Max	
			Test no.	A _{IN}	_{IN}	QA	QB	QC	QD	GND	CLK	CLR	QE	QF	QG	QH	V _{CC}				
8	Same tests, terminal conditions, and limits as subgroup 7 except T _C = 125°C and -55°C.																				
9 T _C = 25°C	f _{MAX} See note F	(Fig. 8)	82	IN	G	OUT				GND	IN	G					5.0 V	QA	22		MHz
	PLH1	3003 (Fig. 8)	83	IN	G	OUT				"	"	"					"	CLK TO QA	5	32	ns
			84	See fig. 8	See fig. 8					"	"	"				"	CLK TO QB	"	"	"	
			85	"	"			OUT		"	"	"				"	CLK TO QC	"	"	"	
			86	"	"	OUT			OUT	"	"	"				"	CLK TO QD	"	"	"	
			87	"	"					"	"	"	OUT			"	CLK TO QE	"	"	"	
			88	"	"					"	"	"		OUT		"	CLK TO QF	"	"	"	
			89	"	"					"	"	"			OUT	"	CLK TO QG	"	"	"	
			90	"	"					"	"	"				OUT	"	CLK TO QH	"	"	"
	PHL1		91	"	"	OUT			"	"	"					"	CLK TO QA	"	37	ns	
			92	"	"		OUT		"	"	"					"	CLK TO QB	"	"	"	
			93	"	"			OUT		"	"	"				"	CLK TO QC	"	"	"	
			94	"	"				OUT	"	"	"				"	CLK TO QD	"	"	"	
			95	"	"					"	"	"	OUT			"	CLK TO QE	"	"	"	
			96	"	"					"	"	"		OUT		"	CLK TO QF	"	"	"	
			97	"	"					"	"	"			OUT	"	CLK TO QG	"	"	"	
			98	"	"					"	"	"				"	CLK TO QH	"	"	"	
	PHL2		99	G	G	OUT			"	"	IN					"	CLK TO QA	"	41	"	
			100	"	"		OUT		"	"	"					"	CLK TO QB	"	"	"	
			101	"	"			OUT		"	"	"			OUT	"	CLK TO QC	"	"	"	
			102	"	"				OUT	"	"	"				"	CLK TO QD	"	"	"	
			103	"	"					"	"	"	OUT			"	CLK TO QE	"	"	"	
			104	"	"					"	"	"		OUT		"	CLK TO QF	"	"	"	
			105	"	"					"	"	"			OUT	"	CLK TO QG	"	"	"	
			106	"	"					"	"	"				"	CLK TO QH	"	"	"	
10 T _C = 125°C	f _{MAX} See F	(Fig. 8)	107	OUT															20		MHz
	t _{PLH1}	3003 (Fig. 8)	108 to 115																5	48	ns
	t _{PHL1}	3003 (Fig. 8)	116 to 123																5	66	ns
	t _{PHL2}	3003 (Fig. 8)	124 to 131																5	62	ns
11	Same tests, terminal conditions, and limits as subgroup 10, except T _C = -55°C.																				

See footnotes at end of device type 05.

FOOTNOTES:

- A.

Apply input pulse:


- B.

$V_{IN} = 2.5\text{ V}.$
- C.

$V_{IN} = 0.4\text{ V}.$
- D.

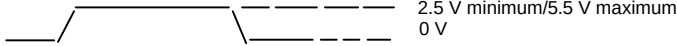
Test numbers 42 through 81 shall be run in sequence.
- E.

Output voltages shall be either: (1) $H \geq 2.5\text{ V}$ minimum and $L \leq 0.4\text{ V}$ maximum when using a high speed checker double comparator; (2) $H \geq 1.5\text{ V}$ and $L \leq 1.5\text{ V}$ when using a high speed checker single comparator.

 f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the A_{IN} data shall be one-half of the clock input frequency and the A_{IN} shall be shifted such that the A_{IN} and are coincident with the clock. Rise and fall times $\leq 6\text{ ns}$. Input peak voltage 3 to 5 volts.
- F.
- G.

3.0 V minimum/5.0 V maximum.
- J.

Apply input pulse:


- ☐

One pulse minimum.
- 1

☐

Two pulses minimum.
- 2

☐

Three pulses minimum.
- 3

☐

Four pulses minimum.
- 4

☐

Five pulses minimum.
- 5

☐

Six pulses minimum.
- 6

☐

Seven pulses minimum.
- 7

☐

Eight pulses minimum.
- 8

☐

At the manufacturer's option, I_{OS} tests 33 through 40, the following alternate procedure may be used; apply 2.75 volts @; test 33, QA , test 34, QB, test 35, QC, test 36, QD, test 37, QE, test 38, QF, test 39, QG, test 40, QH, and min/max limits of -7.5/-50 mA.
- 9

☐

I_{IL} limits (mA) min/max values for circuits shown:

10

Parameter	Terminal	A	B	C	D	E	F	G
I_{IL1}	IN, B_{IN}	0/- .34	-.10/- .34	-.16/- .40	-.16/- .40	-.135/- .370	-.12/- .36	-.16/- .40
	CLK	0/- .4	-.16/- .4	-.12/- .36	-.20/- .44	"	"	"
A	CLR	0/- .4	-.16/- .4	-.12/- .36	-.16/- .40	"	"	"

TABLE III. Group A inspection for device type 06.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Cases 2,X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max	
			Test no.	Serial	A _{IN}	B _{IN}	_{IN}	_{IN}	Mode	GND	CONT	CLK	QD	QC	QB	QA	V _{CC}				
1 T _c = 25°C	V _{OH}	3006	1	2.0 V					0.7 V	GND	4.5 V	A				-1.0 mA	4.5 V	QA	2.4		V
			2		2.0 V		D		2.0 V	"	"	"				-1.0 mA	"	QA	"		"
			3			2.0 V			"	"	"	"			-1.0 mA		"	QB	"		"
			4				2.0 V		"	"	"	"		-1.0 mA			"	QC	"		"
			5					2.0 V	"	"	"	"	-1.0 mA				"	QD	"		"
	OL	3007	6	0.7 V					0.7 V	"	"	"				12 mA	"	QA		0.4	"
			7		0.7 V				2.0 V	"	"	"				12 mA	"	QA		"	"
			8			0.7 V			"	"	"	"			12 mA		"	QB		"	"
			9				0.7 V		"	"	"	"		12 mA			"	QC		"	"
			10					0.7 V	"	"	"	"	12 mA				"	QD		"	"
	V	IC	11	-18 mA						"							"	Serial		-1.5	"
			12		-18 mA					"							"	A _{IN}		"	"
			13			-18 mA				"							"	B _{IN}		"	"
			14				-18 mA			"							"	C _{IN}		"	"
			15					-18 mA									"	D _{IN}		"	"
			16						-18 mA	"							"	Mode		"	"
			17							"	-18 mA						"	CONT		"	"
			18						"	"		-18 mA					"	CLK		"	"
	I	IH1	19	2.7 V					4.5 V	"							5.5 V	Serial		20	μA
			20		2.7 V				GND	"							"	A _{IN}		"	"
			21			2.7 V			"	"							"	B _{IN}		"	"
			22				2.7 V		"	"							"	C _{IN}		"	"
			23					2.7 V	"	"							"	D _{IN}		"	"
			24						2.7 V	"							"	Mode		"	"
			25							"	2.7 V						"	CONT		"	"
			26							"		2.7 V					"	CLK		"	"
	I	IH2	27	5.5 V					4.5 V	"							"	Serial		100	"
			28		5.5 V				GND	"							"	A _{IN}		"	"
			29			5.5 V			"	"							"	B _{IN}		"	"
			30				5.5 V		"	"							"	C _{IN}		"	"
			31					5.5 V	"	"							"	D _{IN}		"	"
			32						5.5 V	"							"	Mode		"	"
			33							"	5.5 V						"	CONT		"	"
			34							"		5.5 V					"	CLK		"	"
	I	OZH	35		0.7 V				4.5 V	"	0.7 V	A				2.7 V	"	QA		20	"
			36			0.7 V			"	"	"	"			2.7 V		"	QB		"	"
			37				0.7 V		"	"	"	"		2.7 V			"	QC		"	"
			38					0.7 V	"	"	"	"	2.7 V				"	QD		"	"
	I	OZL	39		2.0 V				"	"	"	"				0.4 V	"	QA		-20	"
			40			2.0 V			"	"	"	"			0.4 V		"	QB		"	"
			41				2.0 V		"	"	"	"		0.4 V			"	QC		"	"
			42					2.0 V	"	"	"	"	0.4 V				"	QD		"	"

See footnotes at end of device types 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test Limits		Unit
			Cases 2, X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max	
			Test no.	Serial	A _{IN}	B _{IN}	_{IN}	_{IN}	Mode	GND	CONT	CLK	QD	QC	QB	QA	V _{CC}				
1 T _C = 25°C	I _{IL1}	3009	43	0.4 V					GND	"							5.5 V	Serial	1/	1/	mA
			44		0.4 V				4.5 V	"							"	A _{IN}	"	"	"
			45			0.4 V			"	"							"	B _{IN}		"	"
			46				0.4 V		"	"							"	C _{IN}		"	"
			47					0.4 V	"	"							"	D _{IN}		"	"
			48						0.4 V	"							"	Mode	"	"	"
			49						"	"	0.4 V						"	CONT	"	"	"
			50						"	"		0.4 V					"	CLK	"	"	"
			51		4.5 V				4.5 V	"	4.5 V	A				GND	"	QA	2/	2/	"
			52			4.5 V			"	"	"	"			GND		"	QB	"	"	"
	OS	3011	53				4.5 V		"	"	"	"		GND			"	QC	"	"	"
			54					4.5 V	"	"	"	"	GND				"	QD	"	"	"
			55	5.5 V	GND	GND	GND	GND	5.5 V	"	5.5 V	"					"	V _{CC}			"
			56	5.5 V	GND	GND	GND	GND	5.5 V	"	GND	GND					"	V _{CC}			"
	CC	3005																			
	CC	3005																			
	Same tests, terminal conditions and limits as subgroup 1 except T _C = 125°C and V _{IC} tests are omitted.																		27		
																			29		
3	Same tests, terminal conditions and limits as subgroup 1 except T _C = -55°C and V _{IC} tests are omitted.																				

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit
			Cases 2, X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max	
			Test no.	Serial	A _{IN}	_{IN}	_{IN}	_{IN}	Mode	GND	CONT	CLK	QD	QC	QB	QA	V _{CC}				
7 T _C = 25°C	Truth table	3014	57	B	B	B	B	B	B	GND	B	B	X	X	X	X	5.0 V	All outputs	See B,C,D, and E		
			58	"	B _B	B _C	B _D	B	"	"	"	C	H	H	H	H	"				
			59	"	B	B	B	B	"	"	"	B	H	H	H	H	"				
			60	"	C	C	C	C	"	"	"	B	H	H	H	H	"				
			61	"	"	"	"	"	"	"	"	C	L	L	L	L	"				
			62	"	"	"	"	"	"	"	"	B	"	"	"	L	"				
			63	"	"	"	"	"	"	C	"	"	B	"	L	"	"				
			64	"	"	"	"	"	"	"	"	C	"	"	"	H	"				
			65	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			66	"	"	"	"	"	"	"	"	C	"	"	H	"	"				
			67	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			68	"	"	"	"	"	"	"	"	C	"	H	"	"	"				
			69	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			70	"	"	"	"	"	"	"	"	C	H	"	"	"	"				
			71	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			72	C	B	B	B	B	"	"	"	B	"	"	"	"	"				
			73	"	"	"	"	"	"	"	"	C	"	"	"	L	"				
			74	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			75	"	"	"	"	"	"	"	"	C	"	"	L	"	"				
			76	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
			77	"	"	"	"	"	"	"	"	C	"	L	"	"	"				
			78	"	"	"	"	"	"	"	"	B	"	L	"	"	"				
			79	"	"	"	"	"	"	"	"	C	L	L	"	"	"				
			8	Same tests, terminal conditions, and limits as subgroup 7 except T _C = 125°C and -55°C.																	
9 T _C = 25°C	f _{MAX} See note F	(Fig. 9)	80	IN					GND	GND	G	IN				OUT	5.0 V	QA	20		MHz
	PLH1	3003 (Fig. 9)	81		IN				G	"	"	"				OUT	"	CLK to QA	6	35	ns
			82			IN			"	"	"	"			OUT	"	CLK to QB	"	"	"	
			83				IN		"	"	"	"		OUT	"	CLK to QC	"	"	"		
			84					IN	"	"	"	"	OUT		"	CLK to QD	"	"	"		
			85	IN					GND	"	"	"	"			OUT	"	CLK to QA	"	"	"
			86	See fig. 9					"	"	"	"	"		OUT	"	CLK to QB	"	"	"	
			87	See fig. 9					"	"	"	"		OUT			CLK to QC	"	"	"	
			88	See fig. 9					"	"	"	"	OUT		"	"	CLK to QD	"	"	"	
	PHL1		89		IN				G	"	"	"				OUT	"	CLK to QA	"	40	"
			90			IN			"	"	"	"			OUT	"	CLK to QB	"	"	"	
			91						"	"	"	"		OUT			CLK to QC	"	"	"	
92								IN	"	"	"	"	OUT		"	CLK to QD	"	"	"		
93			IN					GND	"	"	"	"			OUT	"	CLK to QA	"	"	"	
94			See fig. 9		IN			"	"	"	"	"		OUT	"	CLK to QB	"	"	"		
95			See fig. 9					"	"	"	"	"		OUT	"	CLK to QC	"	"	"		
96			See fig. 9					"	"	"	"	"	OUT		"	CLK to QD	"	"	"		

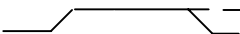
See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Limits		Unit	
			Cases 2, X	2	3	4	5	8	9	10	12	13	14	16	18	19	20		Min	Max		
			Test no.	Serial	A _{IN}	IN	N	IN	Mode	GND	CONT	CLK	QD	QC	QB	QA	V _{CC}					
9 T _C = 25°C	t _{ZL}	(Fig. 9)	97		GND				G	GND	IN	IN				OUT	5.0 V	CONT to QA	5	35	ns	
			98		B	GND	C	D		"	"	"	"			OUT		"	CONT TO QB	"	"	"
			99					GND		"	"	"	"		OUT			"	CONT TO QC	"	"	"
			100						GND	"	"	"	"	OUT			"	CONT TO QD	"	"	"	
t	z _H		101		G				"	"	"	"				OUT	"	CLK TO QA	"	30	"	
			102			G			"	"	"	"			OUT	OUT		"	CLK TO QB	"	"	"
			103				G		"	"	"	"		OUT			"	CLK TO QC	"	"	"	
			104					G	"	"	"	"	OUT				"	CLK TO QD	"	"	"	
t	L _Z				GND				"	"	"	"					"	CLK TO QA	"	55	"	
			106			GND			"	"	"	"			OUT		"	CLK TO QB	"	"	"	
			107				GND		"	"	"	"		OUT	OUT		"	CLK TO QC	"	"	"	
			108					GND	"	"	"	"	OUT				"	CLK TO QD	"	"	"	
t	H _Z	105	109		G				"	"	"	"				OUT	"	CLK TO QA	"	65	"	
			110			G			"	"	"	"			OUT		"	CLK TO QB	"	"	"	
			111				G		"	"	"	"		OUT			"	CLK TO QC	"	"	"	
			112					G	"	"	"	"	OUT				"	CLK TO QD	"	"	"	
10 T _C =125°C	f _{MAX} See F			Same test and terminal conditions as subgroup 9.															18		MHz	
	t _{PLH1}	3003 (Fig. 9)	114 to 121																5	46	ns	
	t _{PHL1}		122 to 129																"	52	"	
	t _{ZL}		130 to 133																"	45	"	
	t _{ZH}		134 to 137																"	39	"	
	t _{LZ}		138 to 141																"	71	"	
	t _{HZ}		142 to 145																"	84	"	
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C.																					

See footnotes at end of device type 06.

FOOTNOTES:

A. Apply input pulse:  2.5 V minimum/5.5 V maximum
0 V

$V_{IN} = 2.4 \text{ V}$.

B. C. $V_{IN} = 0.4 \text{ V}$.

D. Test numbers 57 through 79 shall be run in sequence.

E. Output voltages shall be either: (1) $H \geq 2.5 \text{ V}$ minimum and $L \leq 0.4 \text{ V}$ maximum when using a high speed checker double comparator; (2) $H \geq 1.5 \text{ V}$ and $L \leq 1.5 \text{ V}$ when using a high speed checker single comparator.

F. f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the serial shall be one-half of the clock input frequency and the serial shall be shifted such that the serial $\uparrow$ and $\downarrow$ are coincident with the clock $\uparrow$. Rise and fall times $\leq 6 \text{ ns}$. Input peak voltage 3 to 5 volts.

G. 3.0 V minimum/5.0 V maximum.

I_{IL} limits (mA) min/max values for circuits shown:

1

Parameter	Terminal	A	B	C	D	E
I_{IL1}	Serial	-.075/-.250	-.16/-.40	-.16/-.40	-.105/-.345	-.12/-.36
	$I_{IN}, B_{IN},$ C_{IN}, D_{IN}	-.12/-.36	-.16/-.40	-.16/-.40	-.105/-.345	-.12/-.36
	Mode	-.16/-.40	-.15/-.38	-.03/-.3	-.12/-.36	-.12/-.36
	CONT	-.16/-.40	-.16/-.40	-.03/-.3	-.12/-.36	-.12/-.36
A	CLK	-.16/-.40	-.20/-.44	-.03/-.3	-.12/-.36	-.12/-.36

I_{OS} limits (mA) min/max values for circuit A: -30/-130.
for circuits B, C, D, E: -15/-100.

2

TABLE III. Group A inspection for device type 07 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLR	Serial	A _{IN}	B _{IN}	_{IN}	_{IN}	Load	GND	CONT	CLK	QD'	QD	QC	QB	QA	V _{CC}				
1 T _c = 25°C	V _{OH}	3006	1	2.0 V		2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	GND	0.7 V	A					-1 mA	4.5 V	QA	2.4		V
			2	"		"	"	"	"	"	"	"	"	"			-1 mA		"	QB	"		"
			3	"		"	"	"	"	"	"	"	"	"		-1 mA			"	QC	"		"
			4	"		"	"	"	"	"	"	"	"	"	-1 mA				"	QD	"		"
			5	"		"	"	"	"	"	"	"	"	"	-4 mA				"	QD'	2.5		"
	V	3007	6	"		0.7 V	0.7 V	0.7 V	0.7 V	"	"	"	"	"				12 mA	"	QA		0.4	"
			7	"	"	"	"	"	"	"	"	"	"	"			12 mA		"	QB		"	"
			8	"	"	"	"	"	"	"	"	"	"	"		12 mA			"	QC		"	"
			9	"	"	"	"	"	"	"	"	"	"	"	12 mA			"	"	QD		"	"
			10	"	"	"	"	"	"	"	"	"	"	4 mA				"	"	QD'		"	"
	V	11		-18 mA							"								"	CLR		-1.5	"
			12		-18 mA						"								"	Serial		"	"
			13			-18 mA					"								"	A _{IN}		"	"
			14				-18 mA				"								"	B _{IN}		"	"
			15					-18 mA			"								"	C _{IN}		"	"
	I	11	16						-18 mA										"	D _{IN}		"	"
			17							-18 mA	"								"	Load		"	"
			18								"	-18 mA							"	CONT		"	"
			19							"			-18 mA						"	CLK		"	"
			20	2.7 V						"	"								5.5 V	CLR		20	μA
	I	3010	21		2.7 V					4.5 V	"								"	Serial		"	"
			22			2.7 V				GND	"								"	A _{IN}		"	"
			23				2.7 V			"	"								"	B _{IN}		"	"
			24					2.7 V		"	"								"	C _{IN}		"	"
			25						2.7 V	"	"								"	D _{IN}		"	"
	I	3010	26							2.7 V	"								"	Load		"	"
			27							GND	"	2.7 V							"	CONT		"	"
			28							GND	"		2.7 V						"	CLK		"	"
			29	5.5 V						"	"								"	CLR		100	"
			30		5.5 V					4.5 V	"								"	Serial		"	"
	I	3010	31			5.5 V				GND	"								"	A _{IN}		"	"
			32				5.5 V			"	"								"	B _{IN}		"	"
			33					5.5 V		"	"								"	C _{IN}		"	"
			34						5.5 V	"	"								"	D _{IN}		"	"
			35							5.5 V	"								"	Load		"	"
	I	3010	36							GND	"	5.5 V							"	CONT		"	"
			37							GND	"		5.5 V						"	CLK		"	"
			38	2.0 V		0.7 V	0.7 V	0.7 V	0.7 V	2.0 V	"	2.0 V	A					2.7 V	"	QA		20	"
			39	"		"	"	"	"	"	"	"	"				2.7 V		"	QB		"	"
			40	"		"	"	"	"	"	"	"	"			2.7 V			"	QC		"	"
	I	3010	41	"		"	"	"	"	"	"	"	"		2.7 V				"	QD		"	"
			42	"		2.0 V	2.0 V	2.0 V	2.0 V	"	"	"	"					0.4 V	"	QA		-20	"
			43	"	"	"	"	"	"	"	"	"	"						"	QB		"	"
			44	"	"	"	"	"	"	"	"	"	"			0.4 V			"	QC		"	"
			45	"	"	"	"	"	"	"	"	"	"		0.4 V				"	QD		"	"

See footnotes at end of device types 07.

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TABLE III. Group A inspection for device type 07 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 ; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	CLR	Serial	A _{IN}	IN	IN	IN	Load	GND	CONT	CLK	QD'	QD	QC	QB	QA	V _{CC}		CLR	1/	
1 T _C = 25°C	I _{IL1}	3009	46	0.4 V															5.5 V	CLR	1/	1/	mA
			47	B	0.4 V	B	C	D		GND	"		A						"	Serial	"	"	"
			48			0.4 V				4.5 V	"								"	A _{IN}		"	"
			49				0.4 V			"	"								"	B _{IN}		"	"
			50					0.4 V		"	"								"	C _{IN}		"	"
			51						0.4 V	"	"								"	D _{IN}		"	"
			52							0.4 V	"								"	Load _i	"	"	"
			53								4.5 V	"		0.4 V					"	CONT _i	"	"	"
	54								"	"			0.4 V				"	CLK	"	"	"		
	OS	3011	55	4.5 V	GND	4.5 V	4.5 V	4.5 V	4.5 V	"	"	GND	A					GND	"	Q _A	2/	2/	"
			56	"	"	"	"	"	"	"	"	"	"				GND	"	"	Q _B	"	"	"
			57	"	"	"	"	"	"	"	"	"	"			GND		"	"	Q _C	"	"	"
			58	"	"	"	"	"	"	"	"	"	"		GND			"	"	Q _D	"	"	"
	CC CC	3005 3005	59	"	"	"	"	"	"	"	"	"	"	GND				"	"	Q _{D'}	"	"	"
			60	5.5 V	5.5 V	GND	GND	GND	GND	5.5 V	"	5.5 V	"						"	V _{CC}			"
				61	GND	5.5 V	GND	GND	GND	GND	5.5 V	"	GND	GND					"	V _{CC}			"
2 ¹	Same tests, terminal conditions and limits as subgroup 1, except T _C = 125°C and V _{IC} tests are omitted.																				34		
3	Same tests, terminal conditions and limits as subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																				31		
7 T _C = 25° C	Truth table test	3014	62	D	C	C	C	C	C	C	GND	D	C	L	L	L	L	L	5.0v	All outputs	See C,D,E, and F		
			63	D	D	D	D	D	D	D	"	"	D	"	"	"	"	"	"				"
			64	D	C	C	C	C	C	C	"	"	C	"	"	"	"	"	"				"
			65	C	"	"	"	"	"	"	"	"	C	"	"	"	"	"	"				"
			66	C	"	"	"	"	"	"	"	"	D	H	H	H	H	H	"				"
			67	C	"	"	"	"	"	"	"	"	C	H	H	H	H	H	"				"

See footnotes at end of device types 07.

TABLE III. Group A inspection for device type 07 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits		Unit
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
7 T _C = 25°C	Truth table	3014	Test no.	CLK	Serial	A _{IN}	_{IN}	_{IN}	_{IN}	Load	GND	CONT	CLK	QD'	QD	QC	QB	QA	V _{CC}	All outputs	See C,D,E, and F		
			68	C	C	D	D	D	D	C	GND	D	C	H	H	H	H	H	5.0 V				
			69	"	"	"	B	C	D	"	C	"	"	C	L	L	L	L	L				"
			70	"	"	"	"	"	"	"	C	"	"	C	"	"	"	"	L				"
			71	"	"	"	"	"	"	"	D	"	"	C	"	"	"	"	L				"
			72	"	"	"	"	"	"	"	"	"	"	D	"	"	"	"	H				"
			73	"	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"				"
			74	"	"	"	"	"	"	C	"	"	"	D	"	"	"	H	"				
			75	"	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"				"
			76	"	"	"	"	"	"	"	"	"	"	D	"	"	"	H	"				
			77	"	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"				"
			78	"	"	"	"	"	"	"	"	"	"	D	H	H	"	"	"				
			79	"	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"				"
			80	"	D	C	C	C	C	"	"	"	C	"	"	"	"	"	"				"
			81	"	"	"	"	"	"	"	"	"	D	"	"	"	"	"	L				"
			82	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"	"				"
			83	"	"	"	"	"	"	"	"	"	D	"	"	"	"	L	"				"
			84	"	"	"	"	"	"	"	"	"	C	"	"	"	"	"	"				"
			85	"	"	"	"	"	"	"	"	"	D	"	"	"	L	"	"				"
			86	"	"	"	"	"	"	"	"	"	C	"	"	"	L	"	"				"
87	"	"	"	"	"	"	"	"	"	"	D	L	L	L	"	"	"						
8	Same tests, terminal conditions, as subgroup 7 except T _C = 125°C and -55°C.																						
9 T _C = 25°C	f _{MAX} See G	(Fig. 10)	88	J	IN					GND	GND	GND	IN					OUT	5.0 V	QA	22		MHz
		3003 (Fig. 10)	89	"		IN				J	"	"	"	"				OUT		CLK to QA	5	37	ns
			90	"			IN			"	"	"	"				OUT		CLK to QB	"	"	"	
			91	"				IN		"	"	"	"			OUT		"	CLK to QC	"	"	"	
			92	"					IN	"	"	"	"		OUT			"	CLK to QD	"	"	"	
				"					IN	"	"	"	"	OUT			"	"	CLK to QD'	"	"	"	
			94	"	IN					GND	"	"	"	"				OUT	"	CLK to QA	"	"	"
			95	"	See fig. 10					"	"	"	"				OUT		CLK to QB	"	"	"	
			96	"	"					"	"	"	"			OUT		"	CLK to QC	"	"	"	
	97	"	"					"	"	"	"		OUT			"	CLK to QD	"	"	"			
	PHL1	98	"	"					"	"	"	"	OUT				"	CLK to QD'	"	"	"		
		99	"		IN				J	"	"	"	"				OUT	CLK to QA	"	"	"		
		100	"			IN			"	"	"	"	"			OUT		CLK to QB	"	"	"		
		101	"				IN		"	"	"	"			OUT		"	CLK to QC	"	"	"		
		102	"					IN	"	"	"	"		OUT		"	"	CLK to QD	"	"	"		
		103	"					IN	"	"	"	"	OUT				"	CLK to QD'	"	"	"		
		104	"	IN					GND	"	"	"	"			OUT	"	CLK to QA	"	"	"		
		105	"	See (fig. 10)					"	"	"	"	"			OUT		CLK to QB	"	"	"		
106		"	"					"	"	"	"	"			OUT		CLK to QC	"	"	"			
107	"	"					"	"	"	"	"		OUT		"	CLK to QD	"	"	"				
108	"	"					"	"	"	"	"	OUT			"	CLK to QD'	"	"	"				

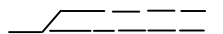
See footnotes at end of device type 07.

TABLE III. Group A inspection for device type 07 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	14	Measured terminal	Limits		Unit			
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max				
9 T _C = 25°C	t _{PHL2}	3003 (Fig. 10)	Test no.	CLK	Serial	A _{IN}	N	IN	IN	Load	GND	CONT	CLK	QD'	QD	QC	QB	QA	V _{CC}							
			109	IN		J				J	GND	GND	IN						OUT	OUT	5.0 V	CLR to QA	5	37	ns	
			110	"			B	J C		D		"	"	"	"				OUT		"	CLR to QB	"	"	"	
			111	"						J		"	"	"	"			OUT		"	"	CLR to QC	"	"	"	
			112	"							J	"	"	"	"		OUT			"	"	CLR to QD	"	"	"	
	t	ZL		113	"					J	"	"	"	"	OUT				"	"	CLR to QD'	"	"	"		
				114	"							"	IN						OUT	"	"	CONT to QA	"	35	"	
				115	"								"	"					OUT	"	"	CONT TO QB	"	"	"	
				116	"								"	"				OUT		"	"	CONT TO QC	"	"	"	
	t	ZH		117	"						"	"				OUT			"	"	CONT TO QD	"	"	"		
				118	J		J				J	"	"	IN					OUT	"	"	CONT TO QA	"	"	"	
				119	"			J			"	"	"	"					OUT	"	"	CONT TO QB	"	"	"	
				120	"				J		"	"	"	"	"			OUT		"	"	CONT TO QC	"	"	"	
	t	LZ		121	"				J	"	"	"	"	"		OUT			"	"	CONT TO QD	"	"	"		
					GND						"	"							OUT	"	"	CONT TO QA	"	"	"	
				123	"							"	"						OUT	"	"	CONT TO QB	"	"	"	
				124	"							"	"	"						"	"	CONT TO QC	"	"	"	
	t	HZ	122	125	"							"	"			OUT			"	"	CONT TO QD	"	"	"		
				126	J						J	"	"	IN					OUT	"	"	CONT TO QA	"	"	"	
				127	"			J			"	"	"	"	"			OUT		OUT	"	"	CONT TO QB	"	"	"
				128	"				J		"	"	"	"	"			OUT		"	"	CONT TO QC	"	"	"	
t			129	"	J				J	"	"	"	"		OUT			"	"	CONT TO QD	"	"	"			
			10 T _C = 125°C	f _{MAX} See G	(Fig. 10)	130	Same tests and terminal conditions as for subgroup 9.																	20		MHz
				t _{PLH1}	3003 (Fig. 10)	131 to 140																		5	56	ns
				t _{PHL1}		141 to 150																		"	56	"
t _{PHL2}		151 to 155		"	56	"																				
t _{ZL}		156 to 159		"	53	"																				
t _{ZH}		160 to 163		"	"	"																				
t _{LZ}		164 to 167		"	"	"																				
HZ		168 to 171		"	"	"																				
11 †	Same tests, terminal conditions, and limits as subgroup 10, except T _C = -55°C																									

See footnotes at end of device type 07.

FOOTNOTES:

- A. Apply input pulse:  2.5 V minimum/5.5 V maximum
0 V-
- B. Apply input pulse:  2.5 V minimum/5.5 V maximum.
0 V
- C. $V_{IN} = 2.4V$.
 $V_{IN} = 0.4 V$.
- D. E. Test numbers 62 through 87 shall be run in sequence.
- F. Output voltages shall be either: (1) $H \geq 2.5 V$ minimum and $L \leq 0.4 V$ maximum when using a high speed checker double comparator: (2) $H \geq 1.5 V$ and $L \leq 1.5 V$ when using a high speed checker single comparator.
- G. f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the parallel input shall be one-half of the clock input frequency and the parallel input shall be shifted such that the parallel input $\uparrow$ and $\downarrow$ are coincident with the clock $\uparrow$. Rise and fall times $\leq 6 ns$. Input peak voltage 3 to 5 volts.
- J. 3.0 V minimum/5.0 V maximum.
- / I_{IL} limits (mA) min/max values for circuits shown:

1

Parameter	Terminal	A	B	C	D
I_{IL1}	Serial	-.075/-.250	-.16/-.40	-.105/-.345	-.12/-.36
	I_{IN}, B_{IN}, C_{IN}	-.12/-.36	"	-.105/-.345	-.12/-.36
	I_{IN}	-.16/-.40	"	-.16/-.40	-.105/-.345
	CLR, Load, CONT, CLK	-.16/-.40	-.03/-.30	-.12/-.36	-.12/-.36

2/ I_{OS} limits for circuit A for QA through QD are -30 to -130 mA, for QD' is -20 to -100 mA, and for circuits B, C, and D are -15 to -100 mA.

D

TABLE III. Group A inspection for device type 08

See footnotes at end of device types 08.

TABLE III. Group A inspection for device type 08 - Continued
Terminal conditions (pins not designated may be high ≥ 2.0 V or low ≤ 0.7 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit			
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max				
			Test no.	Shift Load	CLK	E	F	G	H	$\overline{Q}_H$	GND	Q_H	Serial INP	A	B	C	D	CLK INHB	V_{CC}							
1 Tc = 25°C	I _{IL1}	3009	27										GND						0.4 V	5.5 V	CLK/INHB	<u>1</u>	<u>1</u>	mA		
	I _{IL7}		28	0.4 V									"						"			<u>1</u>	<u>1</u>	mA		
	I	IH1	3010	29		2.7 V							"							"	CLK		20	μA		
				30			2.7 V					"								"	E		"	"		
				31				2.7 V				"								"	F		"	"		
				32					2.7 V			"								"	G		"	"		
				33						2.7 V		"								"	H		"	"		
				34								"		2.7 V						"	S/INP		"	"		
				35								"			2.7 V					"	A		"	"		
				36								"				2.7 V				"	B		"	"		
37											"					2.7 V			"	C		"	"			
38											"						2.7 V		"	D		"	"			
39								"							2.7 V	"	CLK/INHB			"						
I	IH11		40	2.7 V								"							"	S/L	"	60	"			
			I	IH2		41		5.5 V					"								"	CLK		0.1	mA	
						42			5.5 V				"									"	E		"	"
						43				5.5 V			"									"	F		"	"
						44					5.5 V		"									"	G		"	"
						45						5.5 V		"								"	H		"	"
						46								"		5.5 V						"	S/INP		"	"
						47								"			5.5 V					"	A		"	"
						48								"				5.5 V				"	B		"	"
						49								"					5.5 V			"	C		"	"
50											"						5.5 V		"	D		"	"			
51								"							5.5 V	"	CLK/INHB		"	"						
I	IH12		52	5.5 V							"								"	S/L	"	0.3	"			
			OS	3011	53	GND					5.5 V		"	GND							"	Q_H	-15	-100	"	
				3011	54	"						GND	GND	"							"	$\overline{Q}_H$	-15	-100	"	
			CC	3005	55	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V		"		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	"	V_{CC}		36	"	
				3005	56	"	4.5 V	GND	GND	GND	GND		"		GND	GND	GND	GND	GND	4.5 V	"	V_{CC}		36	"	
			2	Same tests, terminal conditions, and limits as subgroup 1, except T _C = 125°C and V _{IC} tests are omitted.																						
			3	Same tests, terminal conditions, and limits as subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																						

See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits		Unit	
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max		
			Test no.	Shift Load	CLK	E	F	G	H	$\overline{Q}_H$	GND	Q_H	Serial INP	A	B	C	D	CLK INHB	V_{CC}					
7 2/ T _C = 25°C	Truth table	3014	57	B	B	B	A	B	A	L	GND	H	A	B	A	B	A	B	B	5.0 V		3/		
			58	A	B	"	"	"	"	"	L	"	H	A	"	"	"	"	"	"				"
			59	"	A	"	"	"	"	"	H	"	L	A	"	"	"	"	"	"				"
			60	"	B	"	"	"	"	"	H	"	L	B	"	"	"	"	"	"				"
			61	"	A	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			62	"	B	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			63	"	A	"	"	"	"	"	H	"	L	"	"	"	"	"	"	"				"
			64	"	B	"	"	"	"	"	H	"	L	"	"	"	"	"	"	"				"
			65	"	A	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			66	"	B	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			67	"	A	"	"	"	"	"	H	"	L	"	"	"	"	"	"	"				"
			68	"	B	"	"	"	"	"	H	"	L	"	"	"	"	"	"	"				"
			69	"	A	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			70	"	B	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			71	"	A	"	"	"	"	"	H	"	L	"	"	"	"	"	"	"				"
			72	"	B	"	"	"	"	"	H	"	L	"	"	"	"	"	"	"				"
			73	"	A	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			74	"	B	"	"	"	"	"	L	"	H	"	"	"	"	"	"	"				"
			75	"	A	"	"	"	"	"	H	"	L	"	"	"	"	"	"	"				"
76	"	B	"	"	"	"	"	H	"	L	A	"	"	"	"	"	A	"						
77	"	A	"	"	"	"	"	H	"	L	A	"	"	"	"	"	A	"						
8	Same tests, terminal conditions, as subgroup 7 except T _C = 125°C and -55°C.																							
9 T _C = 25°C	f _{MAX} 4/		78	5.0 v	IN						GND	OUT	IN					GND	5.0 V	CLK to Q _H	25		MHz	
	PLH5 PHL5 PLH5 PHL5	3003 See fig. 11	79	IN					IN		"	OUT							"	S/L to Q _H	5	40	ns	
			80	"					"	OUT	"							"	S/L to $\overline{Q}_H$	"	"	"		
			81	"					"	OUT	"							"	S/L to $\overline{Q}_H$	"	"	"		
			82	"					"		"	OUT						"	S/L to $\overline{Q}_H$	"	"	"		
	PLH1 PHL1 PLH1 PHL1		83	5.0 V	IN						"	OUT						GND	"	CLK to Q _H	"	45	"	
			84	"	"					OUT	"						"		CLK to $\overline{Q}_H$	"	"	"		
			85	"	"					OUT	"						"	"	CLK to $\overline{Q}_H$	"	"	"		
			86	"	"						"	OUT					"	"	CLK to $\overline{Q}_H$	"	"	"		
	PLH3 PHL3		87	GND					IN		"	OUT						"	H to Q _H	"	30	"		
			88	"					"		"	OUT						"	H to Q _H	"	35	"		
	PLH4 PHL4		89	"					"	OUT	"							"	H to $\overline{Q}_H$	"	35	"		
			90	"					"	OUT	"							"	H to $\overline{Q}_H$	"	30	"		

See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Terminal conditions (pins not designated may be high ≥ 2.0 V, or low ≤ 0.7 V, or open).																							
Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Limits		Unit
			Cases 2, X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	Shift Load	CLK	E	F	G	H	$\overline{Q}_H$	GND	Q_H	Serial INP	A	B	C	D	CLK INHB	V_{CC}				
10 $T_C = 125^\circ\text{C}$	f_{MAX}		91	Same tests and terminal conditions as subgroup 9, except $T_C = 125^\circ\text{C}$.																	20		MHz
t t t t t t t t t t t	PLH5 PHL5 PLH5 PHL5	3003 See fig. 11	92																		52		ns
			93																		"		"
			94																		"		"
			95																		"		"
	PLH1 PHL1 PLH1 PHL1																				5		"
			97																		58		"
			98																		"		"
			99																		"		"
	PLH3 PHL3 PLH4 PHL4	96	100																		39		"
			101																		46		"
			102																		46		"
			103																		39		"
11 $T_C = -55^\circ\text{C}$	Same tests, terminal conditions, and limits as subgroup 10, except $T_C = -55^\circ\text{C}$.																"						

NOTES:

2/ A = 2.5 V and B = 0.4 V.

3/ Output voltages shall be either:

- (a) H = 2.5 V minimum and L = 0.4 V maximum when using a high speed checker double comparator or,
- (b) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

4/ f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the serial shall be one-half of the clock input frequency and the serial shall be shifted such that the serial $\uparrow$ and $\downarrow$ are coincident with the clock $\downarrow$, but may be offset sufficiently to assure adequate t_{SETUP} and t_{HOLD} . Rise and fall times ≤ 6 ns. Input peak voltage 3 to 5 volts.

1/ I_{IL} limits (mA) min/max values for circuit shown:

Parameter	Terminal	A	C	F
I_{IL1}	CLK, CLK/INHIB	-.001/-.150	-.12/-.38	-.005/-.72
I_{IL6}	A,B,C,D, E,F,G,H	-.120/-.360	-.12/-.38	-.12/-.38
	S/IN	-.100/-.340	-.12/-.38	-.12/-.38
I_{IL7}	S/L	-.001/-.150	-.36/-1.08	-.005/-.72

TABLE III. Group A inspection for device type 09- Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	Ser. in	A	B	C	D	CLK INHB	CLK	GND	CLR	E	F	G	Q _H	H	Shift load	V _{CC}				
1 T _c = 25°C	V _{OH}	3006	1						0.7 V	<u>1</u> /	GND					-4 mA	2.0 V	0.7 V	4.5 V	Q _H	2.5		
	OL	3007	2						0.7 V	<u>1</u> /	"					4 mA	0.7 V	0.7 V	"	Q _H		0.4 V	"
	V V	IC	3	-18 mA							"								"	S/IN		-1.5	"
			4		-18 mA						"								"	A		"	"
			5			-18 mA					"								"	B		"	"
			6				-18 mA				"								"	C		"	"
			7					-18 mA			"								"	D		"	"
			8						-18 mA										"	CLK INHB		"	"
			9							-18 mA	"								"	CLK		"	"
			10								"	-18 mA							"	CLR		"	"
			11							"	"		-18 mA						"	E		"	"
			12								"			-18 mA					"	F		"	"
			13								"				-18 mA				"	G		"	"
			14								"						-18 mA		"	H		"	"
			15								"							-18 mA	"	Shift load		"	"
	I	IL6	16	0.4 V							"							"	5.5 V	S/IN	-100	-340	mA
			17		0.4 V						"							"	GND	A	"	"	"
			18			0.4 V					"							"	"	B	"	"	"
			19				0.4 V				"							"	"	C	"	"	"
	I I I I	IL1	20					0.4 V			"							"	"	D	"	"	"
			21						0.4 V		"							"	"	CLK INHB	-0.001	-150	"
			22							0.4 V	"							"	"	CLK	-0.001	-150	"
			23								"	0.4 V						"	"	CLR	-0.001	-150	"
	I	IL6	24								"		0.4 V					"	GND	E	-100	-340	"
			25								"			0.4 V				"	"	F	"	"	"
			26								"				0.4 V			"	"	G	"	"	"
			27								"						0.4 V	"	"	H	"	"	"
	I	IL7	28								"							0.4 V	"	Shift load	-0.001	-150	"
			29	2.7 V							"								"	S/IN		20	μA
			30		2.7 V						"								"	A		"	"
			31			2.7 V					"								"	B		"	"
			32				2.7 V				"								"	C		"	"
			33					2.7 V			"								"	D		"	"
			34						2.7 V		"								"	CLK INHB		"	"
			35							2.7 V	"								"	CLK		"	"
			36								"	2.7 V							"	CLR		"	"
			37								"		2.7 V						"	E		"	"
			38								"			2.7 V					"	F		"	"
			39								"				2.7 V				"	G		"	"
			40								"						2.7 V		"	H		"	"
			41								"							2.7 V	"	Shift load		"	"

See footnotes at end of device types 09

TABLE III. Group A inspection for device type 09- Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

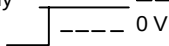
Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit		
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max			
			Test no.	Ser. in	A	B	C	D	CLK INHB	CLK	GND	CLR	E	F	G	Q _H	H	Shift load	V _{CC}						
1 T _C = 25°C	I _{IH2}	3010	42	5.5 V								GND							5.5 V	S/IN		0.1	mA		
			43		5.5 V															"	A		"		
			44			5.5 V															"	B		"	"
			45				5.5 V														"	C		"	"
			46					5.5 V													"	D		"	"
			47						5.5 V												"	CLK INHB		"	"
			48							5.5 V											"	CLK		"	"
			49									5.5 V									"	CLR		"	"
			50										5.5 V								"	E		"	"
			51											5.5 V							"	F		"	"
			52												5.5 V						"	G		"	"
			53														5.5 V				"	H		"	"
			54																5.5 V	"	Shift load		"	"	
I _{OS}	3011	55						GND	$\frac{1}{2}$						GND	5.5 V	GND	"	Q _H	-15	-100	"			
I _{CC}	3005	56	4.5	GND	GND	GND	GND	GND	$\frac{1}{2}$		GND	GND	GND	GND		GND	GND	"	V _{CC}		38	"			
2	Same tests, terminal conditions, and limits as subgroup 1, except T _C = 125° C and V _{IC} tests are omitted.																								
3	Same tests, terminal conditions, and limits as subgroup 1, except T _C = -55° C and V _{IC} tests are omitted.																								
7 $\frac{2}{1}$ T _C = 25°C	Truth table	3014	57	B	A	B	A	B	B	B	GND	B	A	B	A	L	A	B	5.0 V		$\frac{3}{1}$				
			58	"	"	"	"	"	"	"	B	"	A	"	"	"	L	"	B					"	
			59	"	"	"	"	"	"	"	A	"	"	"	"	"	H	"	B					"	
			60	"	"	"	"	"	"	"	B	"	"	"	"	"	"	"	A					"	
			61	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"	"					"	
			62	"	"	"	"	"	"	"	B	"	"	"	"	"	"	"	"					"	
			63	"	"	"	"	"	"	"	A	"	"	"	"	"	L	"	"					"	
			64	"	"	"	"	"	"	"	B	"	"	"	"	"	L	"	"					"	
			65	"	"	"	"	"	"	"	A	"	"	"	"	"	H	"	"					"	
			66	"	"	"	"	"	"	"	B	"	"	"	"	"	H	"	"					"	
			67	"	"	"	"	"	"	"	A	"	"	"	"	"	L	"	"					"	
			68	"	"	"	"	"	"	"	B	"	"	"	"	"	L	"	"					"	
			69	"	"	"	"	"	"	"	A	"	"	"	"	"	H	"	"					"	
			70	"	"	"	"	"	"	"	B	"	"	"	"	"	H	"	"					"	
			71	"	"	"	"	"	"	"	A	"	"	"	"	"	L	"	"					"	
			72	"	"	"	"	"	"	"	B	"	"	"	"	"	L	"	"					"	
			73	"	"	"	"	"	"	"	A	"	"	"	"	"	H	"	"					"	
74	"	"	"	"	"	"	A	B	"	"	"	"	"	H	"	"	"								
75	"	"	"	"	"	"	A	A	"	"	"	"	"	H	"	"	"								
8	Same tests, terminal conditions, and limits as subgroup 7, except T _C = 125° C and -55°C.																								

See footnotes at end of device types 09.

TABLE III. Group A inspection for device type 09- Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.7 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test Limits		Unit
			Cases 2,X	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20		Min	Max	
			Test no.	Ser. in	A	B	C	D	CLK INHB	CLK	GND	CLR	E	F	G	Q _H	H	Shift load	V _{CC}				
9 4/ T_C = 25°C t	f _{MAX}	3003	76						GND	IN	GND	5.0 V				OUT	IN	GND	5.0 V	CLK to Q _H	25		MHz
	PHL5	See fig. 12	77								"	IN				"			"	CLR to Q _H	5 "	40	ns
	PLH1		78						GND	IN	"	5.0 V				"	IN	GND	"	CLR to Q _H	"	31	ns
	t _{PHL1}		79						GND	IN	"	5.0 V				"	IN	GND	"	CLR to Q _H	"	35	ns
10 t	f _{MAX}		Same tests and terminal as subgroup 9, except T _C = 125°C.																		20		MHz
	PHL5																				5	52	ns
	t _{PLH1}																				5	40	ns
	t _{PHL1}																				5	46	ns
11	Same tests, terminal conditions, and limits as subgroup 10, except T _C = -55°C.																						

NOTES:

1/ Apply  2.5 V minimum, 5.5 V maximum to clock input prior to test.

2/ A = 2.5 V and B = 0.4 V.

3/ Output voltages shall be either:

- H = 2.5 V minimum and L = 0.4 V maximum when using a high speed checker double comparator or,
- H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

4/ f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the "H" shall be one-half of the clock input frequency and the "H" shall be shifted such that the "H" $\uparrow$ and $\downarrow$ are coincident with the clock $\downarrow$. Rise and fall times ≤ 6 ns. Input peak voltage 3 to 5 volts.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's system Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. Complete part number (see 1.2).
- c. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- j. Requirements for "JAN" marking.

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND	Ground zero voltage potential
I_{IN}	Current flowing into an input terminal
V_{IC}	Input clamp voltage
V_{IN}	Voltage level at an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Company							Generic Industry type
	Texas Instruments	Signetics Corp.	Raytheon Company	Advanced Micro Devices	Fairchild Semiconductor	Motorola, Inc.	National Semiconductor	
01, circuit--	A	B	C	D	E	F	G	54LS194A
02, circuit--	A	B	C	D	E	F	G	54LS195A
03, circuit--	A	B	C	---	D	E	---	54LS95B
04, circuit--	A	B	---	---	----	---	---	54LS96
05, circuit--	A	B	G	C	E	F	D	54LS164
06, circuit--	A	C	B	---	D	E	---	54LS295B
07, circuit--	A	B	---	---	C	D	---	54LS395A
08, circuit--	A	---	---	---	C	F	---	54LS165A
09, circuit--	A	---	---	---	---	F	---	54LS166

6.6 Change from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 DLA - CC

Preparing activity:
 DLA - CC

(Project 5962-1960)

Review activities:
 Army – SM
 Navy - AS, CG, MC, SH, TD
 Air Force - 03, 19, 99