

December 1996

Fast CMOS Octal Bidirectional Transceivers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2245T)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs

Description

These devices are 8-bit wide octal buffer bidirectional transceivers designed for asynchronous two-way communication between data buses. The transmit/receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

All CD74FCT2245T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT245ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245TQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

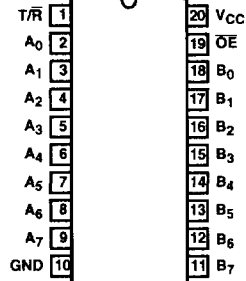
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 OCTAL 5V FCT
5V FCT 25Ω

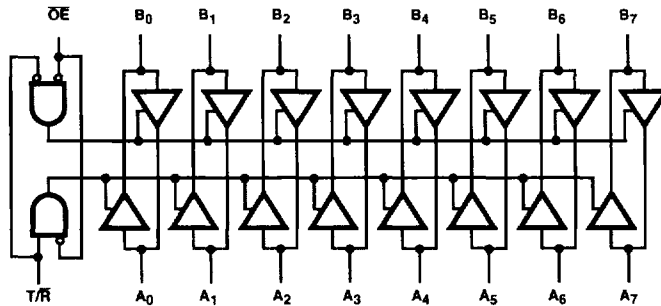
CD74FCT245T, CD74FCT640T, CD74FCT2245T

Pinout

CD74FCT245T, CD74FCT640T, CD74FCT2245T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



NOTE: CD74FCT245T, CD74FCT2245T are non-inverting options. CD74FCT640T is the inverting option.

TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
OE	T/R	
L	L	Bus B Data to Bus A (NOTE 2)
L	H	Bus A Data to Bus B (NOTE 2)
H	X	High Z State

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
2. CD74FCT640T is inverting from input to output.

Pin Descriptions

PIN NAME	DESCRIPTION
OE	Three-State Output Enable Inputs (Active LOW)
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or Three-State Outputs
B ₀ -B ₇	Side B Inputs or Three-State Outputs
GND	Ground
V _{CC}	Power

CD74FCT245T, CD74FCT640T, CD74FCT2245T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
SOIC Package 87
QSOP Package 110
Maximum Junction Temperature 150°C
Maximum Storage Temperature Range -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS	
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±5%							
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I _{IH}	(Except I/O Pins) V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input LOW Current	I _{IL}	(Except I/O Pins) V _{CC} = Max	V _{IN} = GND	-	-	-1	μA
Input HIGH Current	I _{IH}	(I/O Pins Only) V _{CC} = Max	V _{IN} = V _{CC}	-	-	1	μA
Input LOW Current	I _{IL}	(I/O Pins Only) V _{CC} = Max	V _{IN} = GND	-	-	-1	μA
HIGH Impedance Output Current	I _{OZH}	V _{CC} = Max	V _{OUT} = 2.7V	-	-	1	μA
	I _{OZL}		V _{OUT} = 0.5V	-	-	-1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I _{OS}	V _{CC} = Max (Note 6), V _{OUT} = GND		-60	-120	-	mA
Power Down Disable	I _{OFF}	V _{CC} = GND, V _{OUT} = 4.5V		-	-	100	μA
Input Hysteresis	V _H			-	200	-	mV
CAPACITANCE T _A = 25°C, f = 1MHz							
Input Capacitance (Note 7)	C _{IN}	V _{IN} = 0V		-	6	10	pF
Output Capacitance (Note 7)	C _{OUT}	V _{OUT} = 0V		-	8	12	pF

4

OCTAL 5V FCT
5V FCT 25Ω

CD74FCT245T, CD74FCT640T, CD74FCT2245T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS
POWER SUPPLY SPECIFICATIONS						
Quiescent Power Supply Current	I_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND or } V_{CC}$	-	0.1	500 μA
Supply Current per Input at TTL HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 8)	-	0.5	2.0 mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	$V_{CC} = \text{Max}$, Outputs Open $\overline{OE} = \text{GND}$ $T/\overline{R} = \text{GND or } V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25 mA/MHz
Total Power Supply Current (Note 11)	I_C	$V_{CC} = \text{Max}$, Outputs Open $f_T = 10\text{MHz}$, 50% Duty Cycle $T/\overline{R} = \overline{OE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	1.5	3.5 (Note 10) mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	1.8	4.5 (Note 10) mA
		$V_{CC} = \text{Max}$, Outputs Open $f_T = 2.5\text{MHz}$, 50% Duty Cycle $T/\overline{R} = \overline{OE} = \text{GND}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.0	6.0 (Note 10) mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	5.0	14.0 (Note 10) mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
CD74FCT245T, CD74FCT2245T											
Propagation Delay A to B, B to A	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	ns
Output Enable Time OE to A or B	t _{PZH} , t _{PZL}	C _L = 50pF R _L = 500Ω	1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time OE to A or B (Note 14)	t _{PHZ} , t _{PLZ}	C _L = 50pF R _L = 500Ω	1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns
Output Enable Time T/R to A or B	t _{PZH} , t _{PZL}	C _L = 50pF R _L = 500Ω	1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time T/R to A or B (Note 14)	t _{PHZ} , t _{PLZ}	C _L = 50pF R _L = 500Ω	1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns
CD74FCT640T											
Propagation Delay A to B, B to A	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	2	7.0	1.5	5.0	1.5	4.4	1.5	3.7	ns
Output Enable Time OE to A or B	t _{PZH} , t _{PZL}	C _L = 50pF R _L = 500Ω	2	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time OE to A or B (Note 14)	t _{PHZ} , t _{PLZ}	C _L = 50pF R _L = 500Ω	2	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

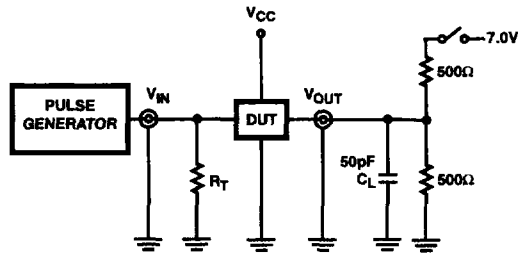
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
Output Enable Time T/R to A or B	t_{pZH} , t_{pZL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time T/R to A or B (Note 14)	t_{pHZ} , t_{pLZ}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ} , t_{PZL}	Closed
t_{PHZ} , t_{PZH} , t_{PLH} , t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 t_f , $t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

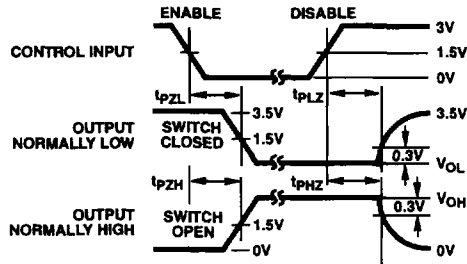


FIGURE 2. ENABLE AND DISABLE TIMING

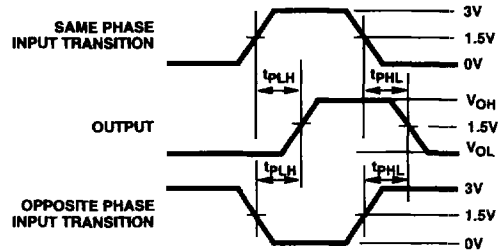


FIGURE 3. PROPAGATION DELAY