

Multichannel Network Interface Controller with 128 Channels Extended

The MUNICH128X is a 128-channel WAN protocol controller which provides four independent 24/32-channel HDLC Controllers, each with a dedicated 64-channel DMA controller and a serial PCM interface controller. The device is offered in a 160-pin MQFP package, making it ideal for high-port-density applications.

The MUNICH128X provides capability for up to 128 full duplex serial PCM channels. The chip performs layer-2 HDLC formatting/deformatting at data rates from 8 kbit/s up to 2.048 Mbit/s or V.110/X30 protocols up to data rates of 38.4 kbit/s.

The MUNICH128X also performs transparent transmission for DMI mode 0, 1 and 2. Processed data is transferred to host memory via the PCI interface or demultiplexed bus interface.



MUNICH128X

Potential Application

- Central office switches/routers
- As a central D-channel controller to 128 ISDN basic access D-channels
- As a multiplexer for terminals and other peripherals
- Frame relay switches
- Remote access server
- Internet service provider node
- E1/T1-line-card, e.g. for PC

Features

Four independent 24/32-channel HDLC Controllers
Each of them provides:

- Serial PCM traffic at 2.048, 4.096, 1.544, 1.536, 3.088, 6.176 or 8.192 Mbit/s
- Compatible with T1/DS1 24-channel and CEPT 32-channel PCM byte format
- Concatenation of any, not necessarily consecutive, time-slot to superchannels independently for receive and transmit direction
- Support of H0, H11, H12 ISDN channels
- Subchannelling on each time-slot possible
- Transparent mode or HDLC protocol selectable
- Shared opening and closing flags
- Flag stuffing and flag adjustment for rate adaption
- Detection of interframe-time-fill change
- CRC generation and checking (16 or 32 Bits)
- Transparent CRC option
- Error detection as well as ABORT/IDLE generation and transmission
- V.110, X.30 80-Bit framing, network data rate up to 38.4 kbit/s
- Dedicated 1024 byte Tx buffer
- Dedicated 1024 byte Rx buffer
- Dedicated 64-channel DMA controller
- Interrupt circular-buffers with variable size for Tx and Rx

- 20-Bit timer clocked with serial sync pulse, single shot or continuous mode
- Reception/transmission of ISLP frames of any length
- Optimized bus load performance: 128 channels, full duplex, frames > 128 bytes ≥ bus load < 3%
- 32-Bit/33 MHz PCI 2.1 interface
- 32-Bit/33 MHz demultiplexed bus interface option
- 0.35 μ, 3.3 V - optimized technology
- 3.3 V I/O capability with 5.0 V input tolerance
- 160-pin MQFP package

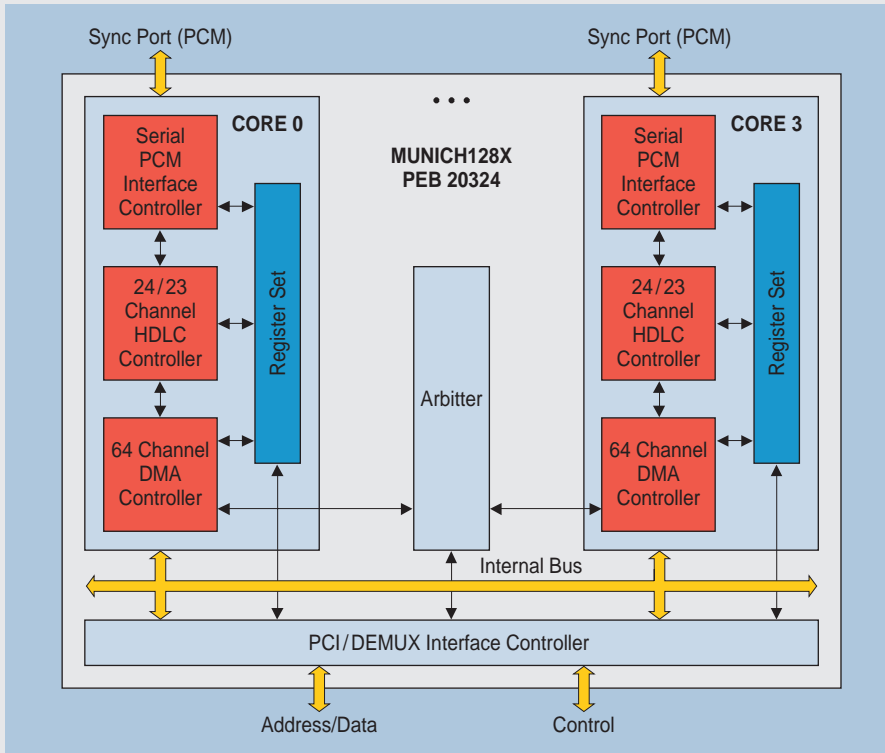
Documentation and Support Package

- Product Overview
- Programmer's Reference Manual
- Delta Sheet
- System Test Description
- Evaluation System 324

M U N I C H 1 2 8 X
P E B 2 0 3 2 4



MUNICH128X Block Diagram



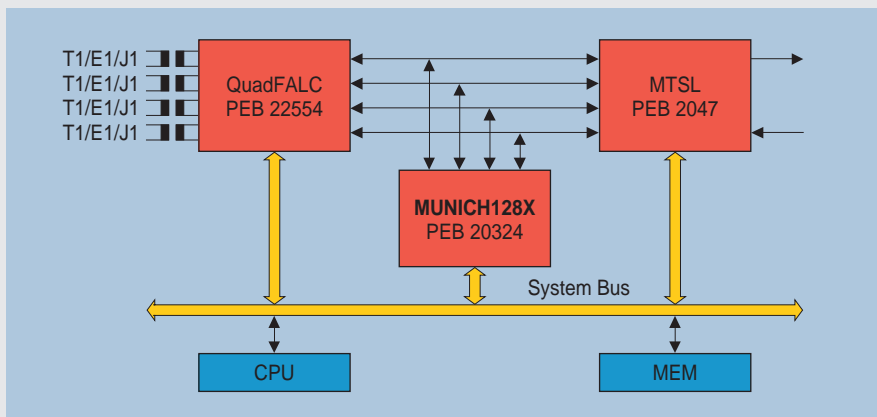
MUNICH128X Evaluation Board available



The MUNICH128X is compatible with the LAPD ISDN (Integrated Services Digital Network) protocol specified by CCITT, as well as with HDLC, SDLC, LAPB and DMI protocols. It provides rate adaption for time-slot transmission from 64 kbit/s down to 8 kbit/s and the concatenation of time-slots, supporting the ISDN H0, H11, H12 superchannels.

Availability

The MUNICH128X device is available with complete documentation and support package. A dedicated engineering support team is there to assist you. Please contact your local Infineon Technologies office for further details.



MUNICH128X PEB 20324 Application Example

Frame Relay over E1/T1/J1 using QuadFALC™, MUNICH128X and MTSL

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