M62009L/P/FP

Low Power 2 Output System Reset IC with External Input

REJ03D0782-0100
Rev.1.00
Sep 14, 2005

Description

As applications for microcomputers are increasing, a desire has arisen for a RAM backup function. Let us introduce Renesas new low power dissipation, high-performance system reset IC, which is suitable for such RAM backup.

The M62009, which is a low power dissipation 2-output microcomputer system reset IC, is a 2-output system reset IC which provides for RAM backup in microcomputers, and reduces power dissipation by using the Bi-CMOS process. The M62009 considerably reduces the number of components in the reset circuit.

The M62009 performs two-step detection of normal supply voltage and backup supply voltage required for backup mode. When the supply voltage is switched from normal supply voltage to backup supply voltage the interruption output, which is one of the two outputs, gives the interruption signal to a microcomputer, in this way, the microcomputer reduces power dissipation and enters in the backup mode. If the backup supply voltage goes lower than the voltage required for backup, the reset output ($\overline{\text{RESET}}$ output) which is different from the $\overline{\text{INT}}$ output gives the reset signal (forced reset) to the microcomputer. The interruption signal from the $\overline{\text{INT}}$ output recovers the microcomputer from the backup mode. To recover from reset, $\overline{\text{RESET}}$ output is canceled when the specified interval of time (delay time) elapses after the signal is given from the $\overline{\text{INT}}$ output.

Features

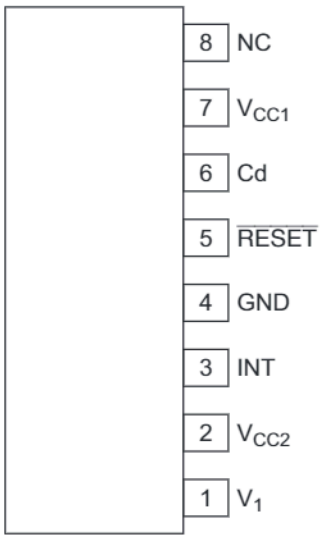
- Bi-CMOS process realizes a configuration of low current dissipating circuits.
  I_{CC} = 7 µA (Typ, normal mode, V_{CC1} = V_{CC2} = 5.0 V)
  I_{CC} = 5 µA (Typ, backup mode, V_{CC1} = 5.0 V)
  I_{CC} = 1 µA (Typ, backup mode, V_{CC1} = 2.5 V)
- Two-step detection of supply voltage
  V_{CC1} ($\overline{\text{RESET}}$):
  V_{S1-1} = 4.0 V (Typ, increase of V_{CC1})
  V_{S1-2} = 2.0 V (Typ, decrease of V_{CC1})
  V_{CC2} ($\overline{\text{INT}}$):
  Free setup
- Two outputs (open drain type)
  Reset output ($\overline{\text{RESET}}$): Forced reset signal output
  Interruption output ($\overline{\text{INT}}$): Output of the signal for interruption processing (output of the switching signal for backup mode)
- Three types of outline packages
  8-pin plastic SIP (single in-line package)
  8-pin plastic DIP (dual in-line package)
  8-pin plastic SOP (mini flat package)
- Output based on RAM backup mode (see the timing chart)

Application

- Prevention of errors in microcomputer system in electronic equipment that requires RAM backup, such as office, industrial, and home-use equipment.

Pin Arrangement

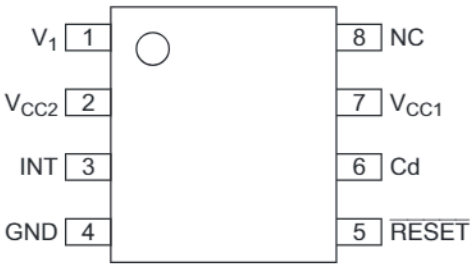
M62009L



(Top view)

Package: (8P5): L

M62009P
M62009FP

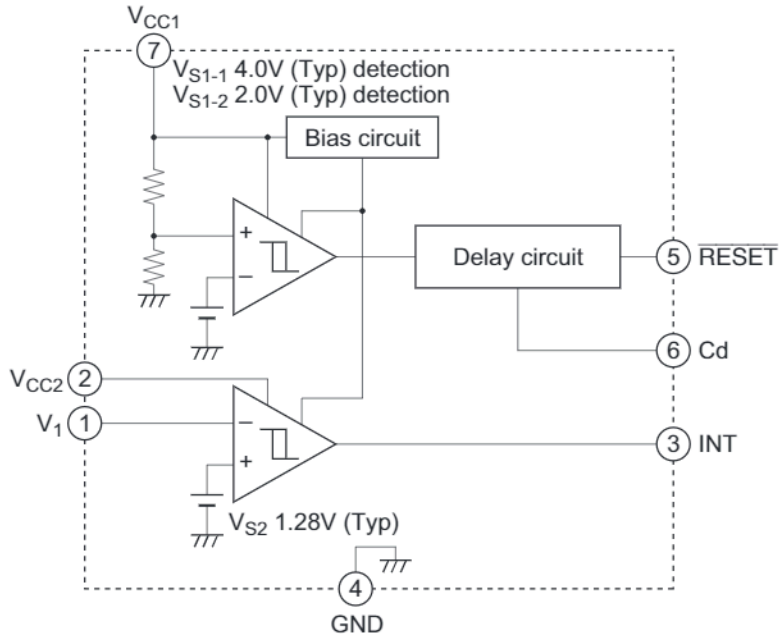


(Top view)

NC: No Connection

Package: PRDP0008AA-A (8P4): P
PRSP0008DA-A (8P2S-A): FP

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

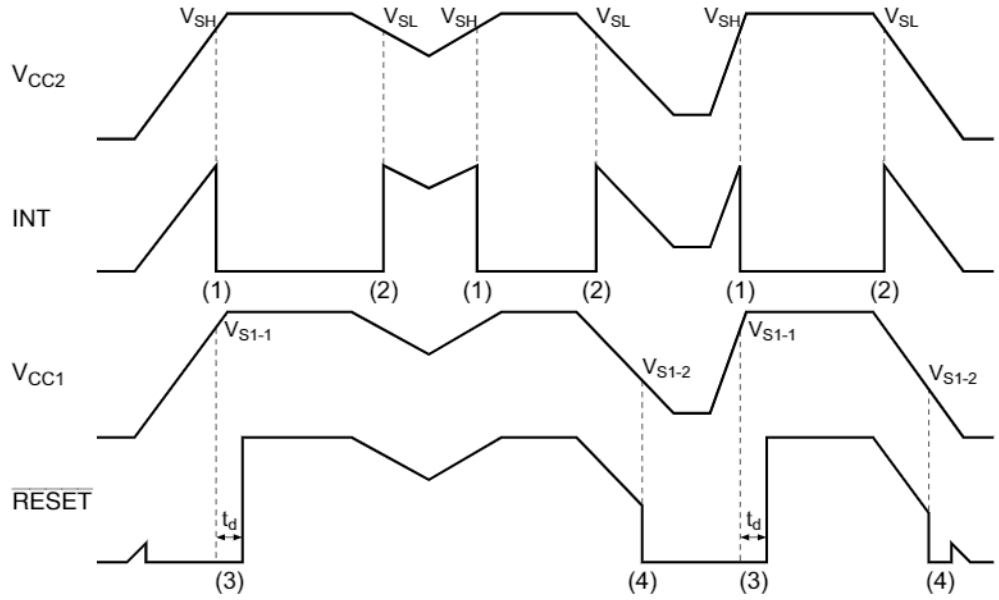
Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	8	V	
Output sink current	Isink	5	mA	
Power dissipation	Pd	800	mW	8-pin SIP
		625		8-pin DIP
		440		8-pin SOP
Thermal derating	Kθ	4.4	mW/°C	Ta ≥ 25°C
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	V_{S1-1}	3.8	4.0	4.2	V	Increase of V_{CC1}
	V_{S1-2}	1.85	2.00	2.15		Decrease of V_{CC1}
Reference voltage	V_{S2}	1.23	1.28	1.33	V	Decrease of V_1
Hysteresis voltage	ΔV_S	—	87	—	mV	V_{CC2} = Detection voltage of hysteresis voltage (Detection voltage = 4V setup)
Circuit current	I_{CC1}	—	7	15	µA	V_{CC1} = V_{CC2} = 5V
	I_{CC2-1}	—	5	10		V_{CC1} = 5V, V_{CC2} = 0V
	I_{CC2-2}	—	1	3		V_{CC1} = 2.5V, V_{CC2} = 0V
Delay time	t_d	—	50	—	ms	Cd = 0.33µF
Output saturation voltage	Vsat	—	0.2	0.4	V	V_{IN} = 5V, I_O = 4mA (NMOS)
Reset output response time	$t_{\overline{RESET}}$	—	30	—	µs	Time between V_{CC1} (when falling) = V_{S1-2} and output of $\overline{RESET}$ signal
Interruption output reset time	t_{INT}	—	100	—	µs	Time between V_{CC2} (when falling) = V_{S2} and output of $\overline{INT}$ signal

Operating Description



(1): $V_{CC2} = V_{SH}$ (increase of V_{CC2}) $\overline{INT}$ output → Low ($V_{SH} = V_{SL} + \Delta V_S$)

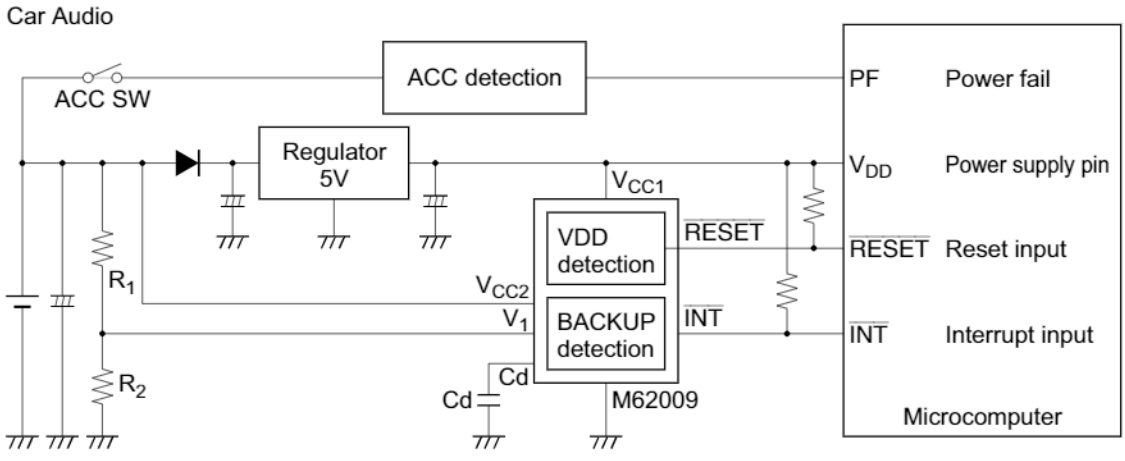
(2): $V_{CC2} = V_{SL}$ (decrease of V_{CC2}) $\overline{INT}$ output → High ($V_{SL} = \frac{R_1 + R_2}{R_2} V_{S2}$)

(3): Delay time obtained from V_{S1-1}. td = 50ms (Cd = 0.33µF): $t_d \approx 1.52 \times 10^5 \times C$ (s)
$\overline{RESET}$ output: reset cancel (cancel)

(4): $V_{CC1} = V_{S1-2}$ (V_{CC1} decrease)
$\overline{RESET}$ output: forced reset output (L reset)

Figure 1 Operating Waveform

Application Example



Note: Interrupt detection V_{SL} is set by resistance R_1 between V_{CC2} and V_1 and resistance R_2 between R_1 and V_1.

$$V_{SL} = \frac{R_1 + R_2}{R_2} V_{S2}$$

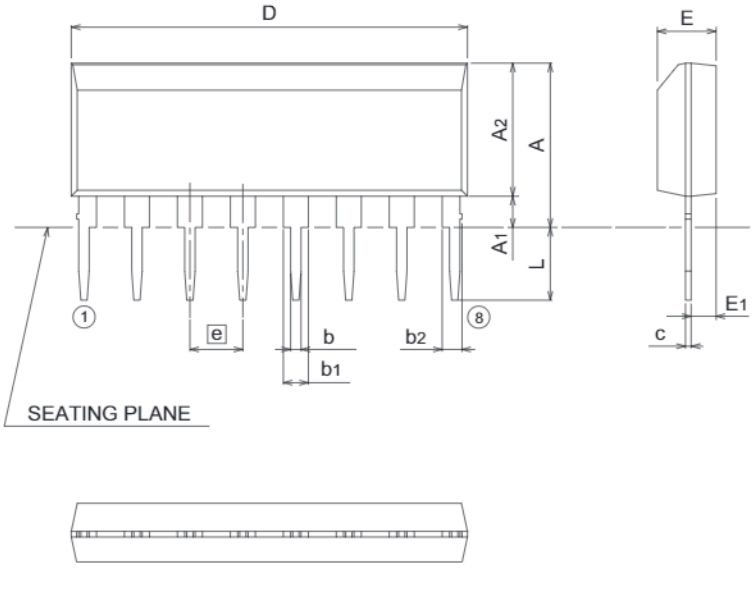
Figure 2 Application Example

Package Dimensions

8P5

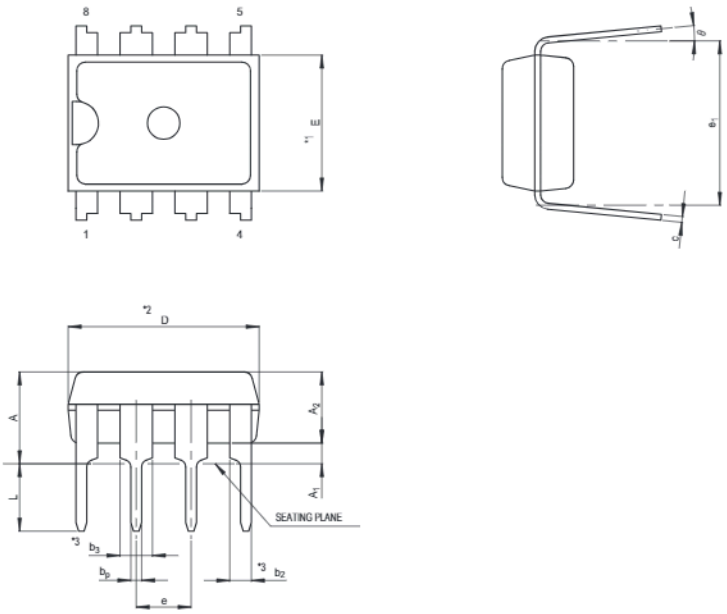
Plastic 8pin 340mil SIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SIP8-P-340-2.54	—	0.73	Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	8.3
A1	1.2	—	—
A2	—	6.4	—
b	0.4	0.5	0.6
b1	1.1	1.2	1.5
b2	0.75	0.85	1.15
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	2.6	2.8	3.0
E1	1.1	1.2	1.3
e	—	2.54	—
L	3.0	—	—

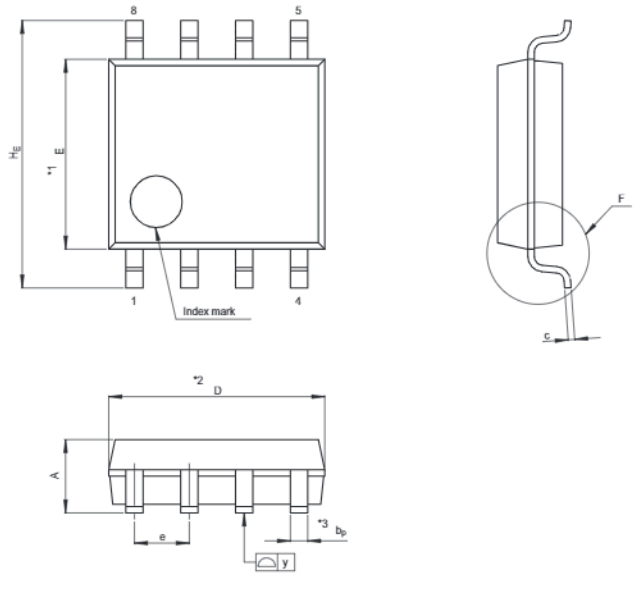
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x8.84-2.54	PRDP0008AA-A	8P4	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	8.7	8.84	9.1
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	—	1.5	—
A_1	0.05	—	—
A	—	—	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

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