Ordering number : EN*A0160

Preliminary

SANYO Semiconductors
DATA SHEET

LC75876E
LC75876W

CMOS IC

1/4-Duty General-Purpose LCD Display Driver

Overview

The LC75876E and LC75876W are 1/4-duty general-purpose microprocessor-controlled LCD driver that can be used in applications such as frequency display in products with electronic tuning. In addition to being able to drive up to 272 segments directly, the LC75876E and LC75876W can also control up to 8 general-purpose output ports. Incorporation of an oscillation circuit helps reduce the number of external resistors and capacitors required.

Features

- Support for 1/4-duty 1/2-bias or 1/4-duty 1/3-bias drive techniques under serial data control (up to 272 segments)
- Serial data input supports CCB* format communication with the system controller (support 3V operation).
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port functions.
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- Display contrast adjuster circuit
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 to +7.0	V
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	-0.3 to +7.0	V
	$V_{IN}2$	OSCI, $V_{DD}1$, $V_{DD}2$	-0.3 to V_{DD}+0.3	
Output voltage	V_{OUT}	S1 to S68, COM1 to COM4, P1 to P8	-0.3 to V_{DD}+0.3	V
Output current	$I_{OUT}1$	S1 to S67	300	μA
	$I_{OUT}2$	COM1 to COM4, S68	3	mA
	$I_{OUT}3$	P1 to P8	5	
Allowable power dissipation	Pdmax	Ta=85°C	200	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
Input voltage*1	$V_{DD}1$	$V_{DD}1$		2/3$V_{DD}0$	$V_{DD}0$	V
	$V_{DD}2$	$V_{DD}2$		1/3$V_{DD}0$	$V_{DD}0$	
Input high-level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.4V_{DD}		6.0	V
	$V_{IH}2$	OSCI external clock operating mode	0.4V_{DD}		V_{DD}	
Input low-level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSCI external clock operating mode	0		0.2V_{DD}	
External clock operating frequency	f_{CK}	OSCI external clock operating mode [Figure 4]	150	300	600	kHz
External clock duty cycle	D_{CK}	OSCI external clock operating mode [Figure 4]	30	50	70	%
Data setup time	tds	CL, DI [Figure 2][Figure 3]	160			ns
Data hold time	tdh	CL, DI [Figure 2][Figure 3]	160			ns
CE wait time	tcp	CE, CL [Figure 2][Figure 3]	160			ns
CE setup time	tcs	CE, CL [Figure 2][Figure 3]	160			ns
CE hold time	tch	CE, CL [Figure 2][Figure 3]	160			ns
High-level clock pulse width	tϕH	CL [Figure 2][Figure 3]	160			ns
Low-level clock pulse width	tϕL	CL [Figure 2][Figure 3]	160			ns
Rise time	tr	CE, CL, DI [Figure 2][Figure 3]		160		ns
Fall time	tf	CE, CL, DI [Figure 2][Figure 3]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure 5]	10			μs

Note: *1 $V_{DD}0$=0.70V_{DD} to V_{DD}

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.03V_{DD}$		V
Input high-level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 6.0V			5.0	μA
	$I_{IH}2$	OSCI	$V_I = V_{DD}$ external clock operating mode			5.0	
Input low-level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0V	-5.0			μA
	$I_{IL}2$	OSCI	V_I = 0V external clock operating mode	-5.0			
Output high-level voltage *1	$V_{OH}1$	S1 to S68	I_O = -20μA	$V_{DD}0$-0.9			V
	$V_{OH}2$	COM1 to COM4	I_O = -100μA	$V_{DD}0$-0.9			
	$V_{OH}3$	P1 to P8	I_O = -1mA	V_{DD}-0.9			
Output low-level voltage	$V_{OL}1$	S1 to S68	I_O =20μA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O =100μA			0.9	
	$V_{OL}3$	P1 to P8	I_O =1mA			0.9	
Output middle-level voltage *1 *2	$V_{MID}1$	COM1 to COM4	1/2 bias I_O = ±100μA	$1/2V_{DD}0$ -0.9		$1/2V_{DD}0$ +0.9	V
	$V_{MID}2$	S1 to S68	1/3 bias I_O = ±20μA	$2/3V_{DD}0$ -0.9		$2/3V_{DD}0$ +0.9	
	$V_{MID}3$	S1 to S68	1/3 bias I_O = ±20μA	$1/3V_{DD}0$ -0.9		$1/3V_{DD}0$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias I_O = ±100μA	$2/3V_{DD}0$ -0.9		$2/3V_{DD}0$ +0.9	
	$V_{MID}5$	COM1 to COM4	1/3 bias I_O = ±100μA	$1/3V_{DD}0$ -0.9		$1/3V_{DD}0$ +0.9	
Oscillator frequency	fosc	Internal oscillator circuit	Internal oscillator operating mode	240	300	360	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			5	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 6.0V output open Internal oscillator operating mode		1300	2600	
	$I_{DD}3$	V_{DD}	V_{DD} = 6.0V output open External clock operating mode f_{CK} = 300kHz $V_{IH}2 = 0.5V_{DD}$ $V_{IL}2 = 0.1V_{DD}$		1400	2800	

Note: *1 $V_{DD}0=0.70V_{DD}$ to V_{DD}

*2 Excluding the bias voltage generation divider resistors built in the $V_{DD}1$ and $V_{DD}2$. (See Figure 1.)

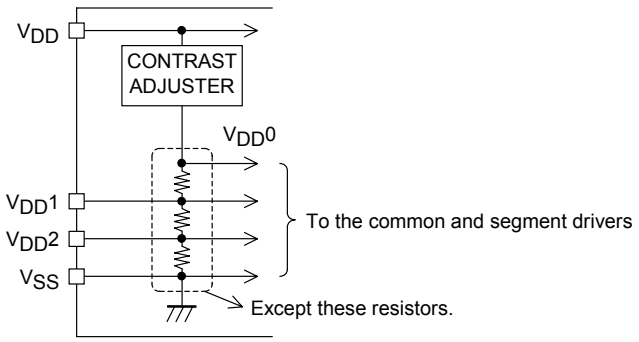


Figure 1

1. When CL is stopped at the low level

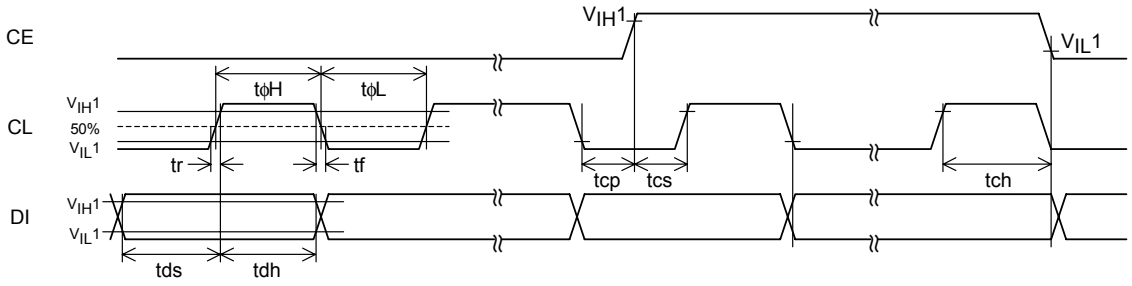


Figure 2

2. When CL is stopped at the high level

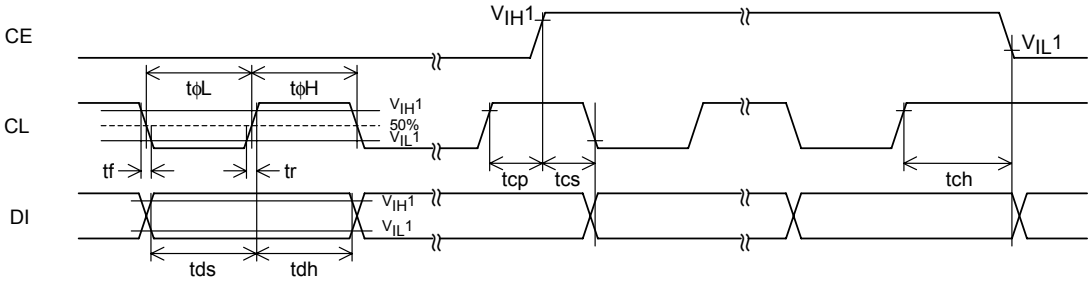
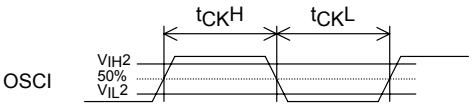


Figure 3

3. OSCI pin clock timing in external clock mode



$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \quad [kHz]$$

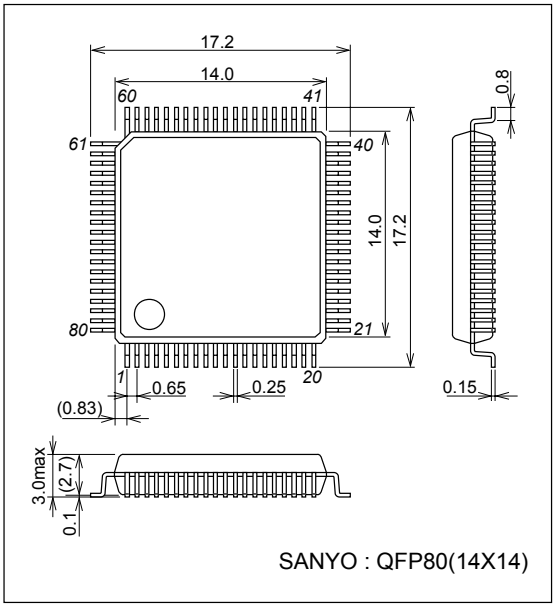
$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

Figure 4

Package Dimensions

unit : mm

3255 [LC75876E]

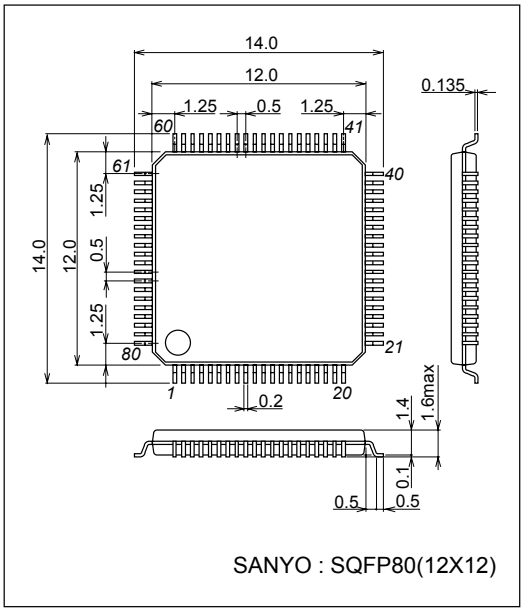


SANYO : QFP80(14X14)

Package Dimensions

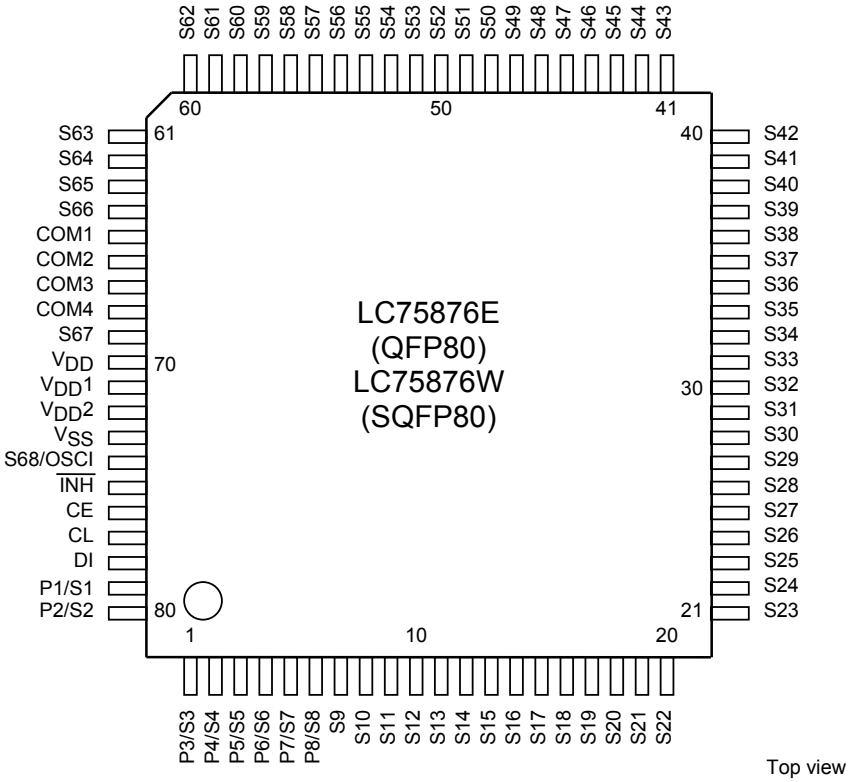
unit : mm

3220 [LC75876W]



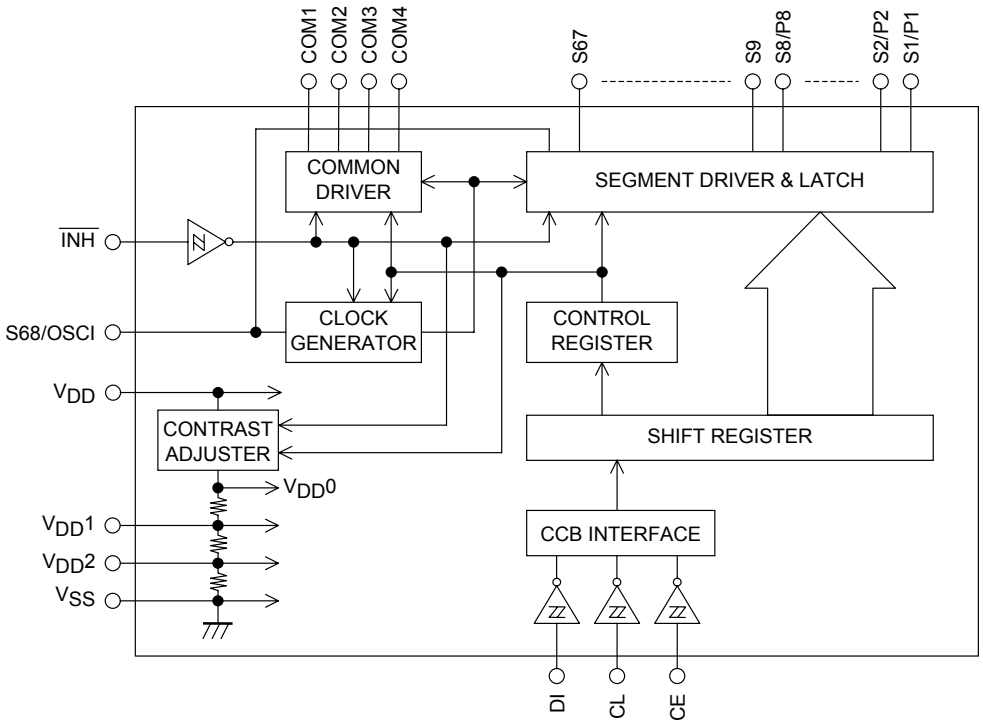
SANYO : SQFP80(12X12)

Pin Assignments



Top view

Block Diagram



Pin Functions

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S8/P8 S9 to S66 S67	79,80, 1 to 6 7 to 64 69	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S8/P8 pins can be used as general-purpose output ports when so set up by the control data.	-	O	OPEN
COM1 to COM4	65 to 68	Common driver outputs. The frame frequency is fo [Hz].	-	O	OPEN
S68/OSCI	74	Segment output. This pin can also be used as the external clock input pin when the external clock operating mode is selected by control data.	-	I/O	OPEN
CE CL DI	76 77 78	Serial data transfer inputs. Must be connected to the controller. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ -	I I I	GND

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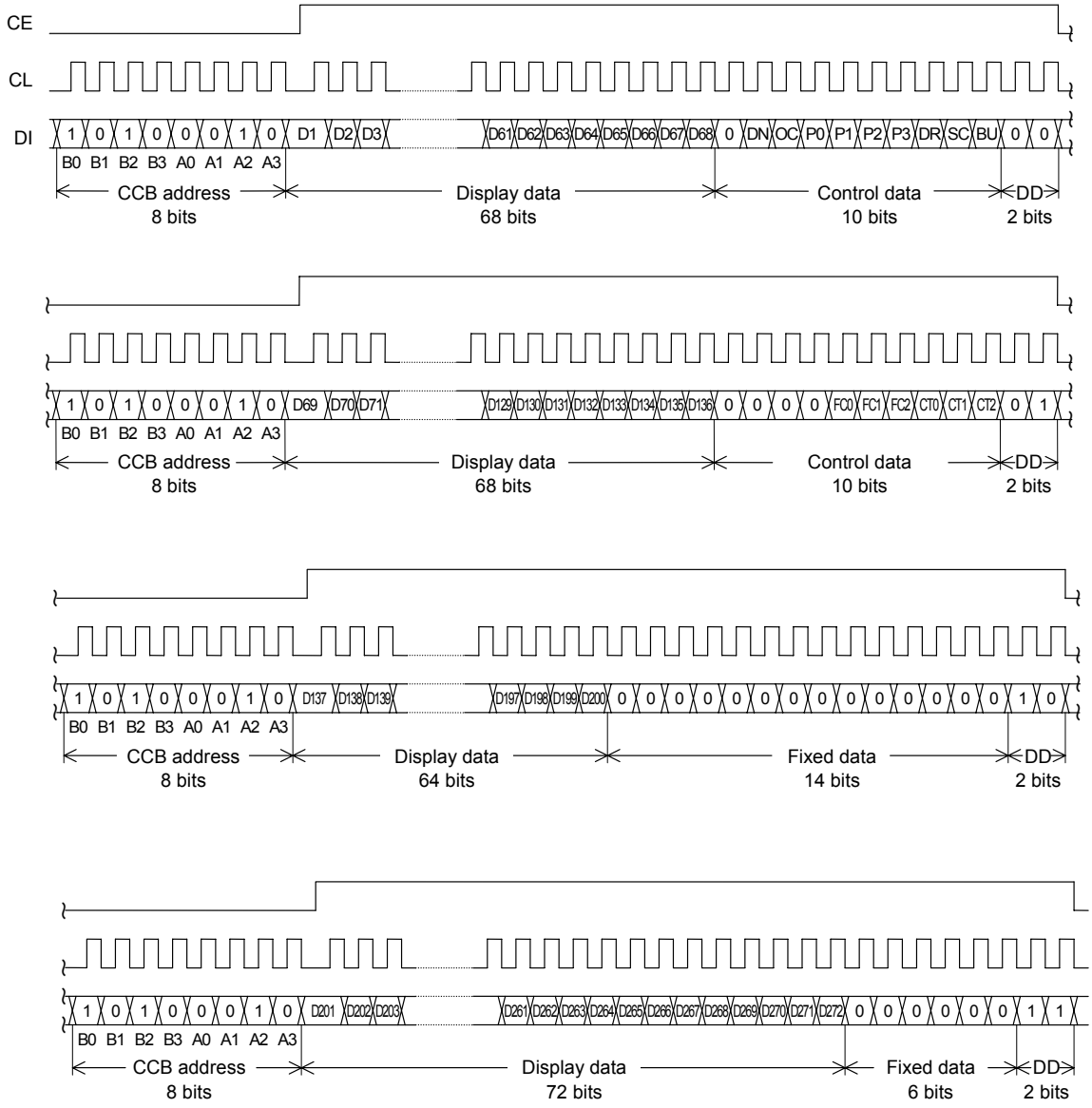
Symbol	Pin No.	Function	Active	I/O	Handling when unused
$\overline{INH}$	75	Display off control input • $\overline{INH}$ = low (V_{SS}) ...Display forced off S1/P1 to S8/P8 = low (V_{SS}) (These pins are forcibly set to the segment output port function and held at the V_{SS} level.) S9 to S67 = low (V_{SS}) COM1 to COM4 = low (V_{SS}) S68/OSCI = low (V_{SS}) (This pin is forcibly set to the segment output port function and held at the V_{SS} level.) Stops the internal oscillator. Inhibits external clock input. Stops the display contrast adjuster circuit. • $\overline{INH}$ = high (V_{DD})...Display on Enables the internal oscillator circuit (internal oscillator operating mode). Enables external clock input (external clock operating mode). Enables the display contrast adjuster circuit. However, serial data transfer is possible when the display is forced off.	L	I	GND
$V_{DD}1$	71	Used to apply the LCD drive 2/3 bias voltage externally. Connect this pin to $V_{DD}2$ when using a 1/2-bias drive scheme.	-	I	OPEN
$V_{DD}2$	72	Used to apply the LCD drive 1/3 bias voltage externally. Connect this pin to $V_{DD}1$ when using a 1/2-bias drive scheme.	-	I	OPEN
V_{DD}	70	Power supply pin. A power voltage of 4.5 to 6.0V must be applied to this pin.	-	-	-
V_{SS}	73	Ground pin. Must be connected to ground.	-	-	-

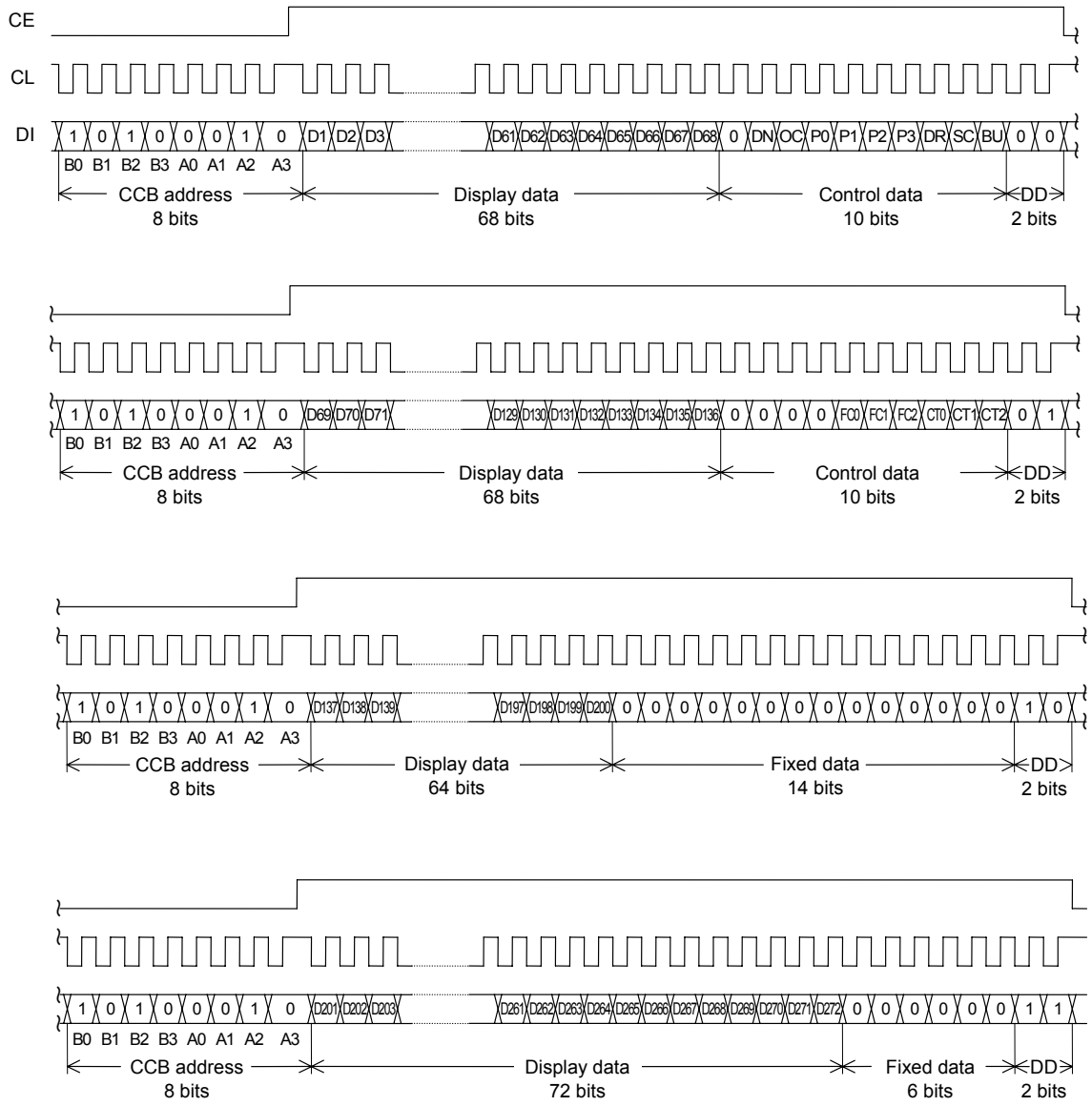
Serial Data Transfer Formats

1. When CL is stopped at the low level



Note: DD is the direction data.

2. When CL is stopped at the high level

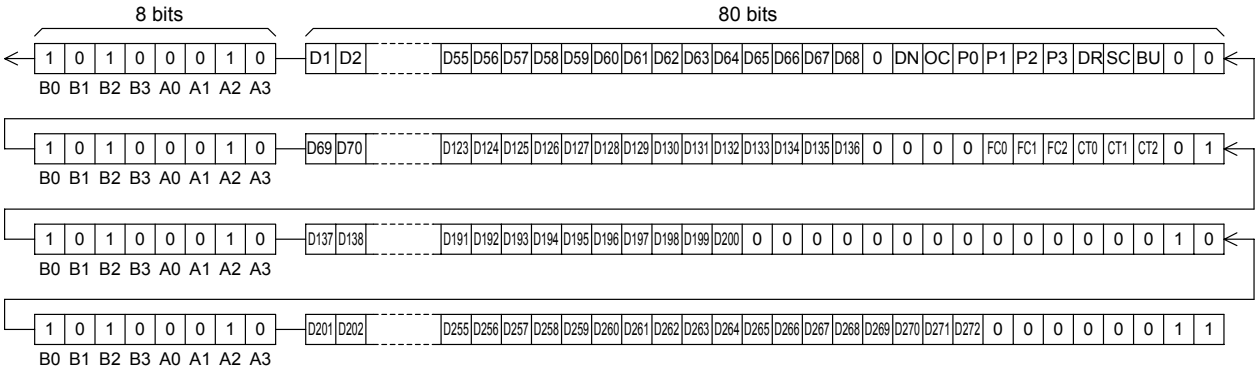


Note: DD is the direction data.

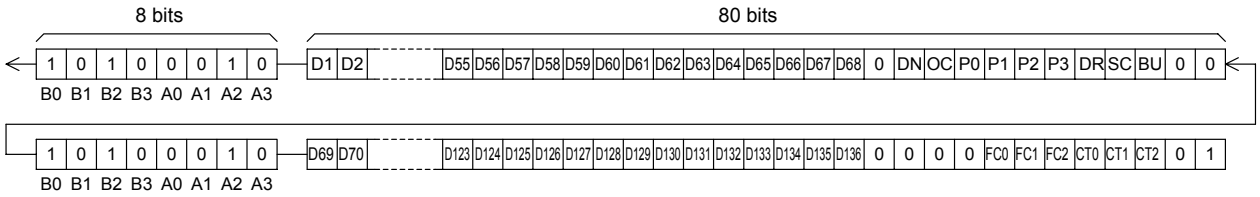
- CCB address ..... "45H"
- D1 to D272 ..... Display data
- DN ..... 264-/272-segment display switching control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DR ..... 1/2-bias drive or 1/3-bias drive switching control data
- SC ..... Segments on/off control data
- BU ..... Normal mode/power-saving mode control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency control data
- CT0 to CT2 ..... Display contrast control data

Serial Data Transfer Example

• When 201 or more segments are used
All 320 bits of serial data must be sent.



• When fewer than 201 segments are used
Either 160 or 240 bits of serial data must be sent, depending on the number of segments to be used. However, the serial data shown below (the D1 to D136 display data and the control data) must always be sent.



Control Data Functions

1. DN: 264-/272-segment display switching control data
   This control data bit selects either the 264- or 272-segment display mode.

DN	Number of display segments	Pin state	
		S67	S68/OSCI
0	Up to 264 segments	"L" (V_{SS})	"L" (V_{SS}) /OSCI
1	Up to 272 segments	S67	S68/OSCI

Note: "L" (V_{SS}) : Low (V_{SS}) level output
S67 : Segment output
"L" (V_{SS}) /OSCI : Low (V_{SS}) level output in internal oscillator operating mode (OC = 0)
External clock input in external clock operating mode (OC = 1)
S68/OSCI : Segment output in internal oscillator operating mode (OC = 0)
External clock input in external clock operating mode (OC = 1)

2. OC: Internal oscillator operating mode/external clock operating mode switching control data
   This control data bit selects either the internal oscillator operating mode or external oscillator operating mode.

OC	Fundamental clock operating Mode	I/O pin (S68/OSCI) state
0	Internal oscillator operating mode	S68
1	External clock operating mode	OSCI

Note: S68: Segment output
OSCI: External clock input

3. P0 to P3: Segment output port/general-purpose output port switching control data
   These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S8/P8 output pins.

Control data				Output pin state							
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8

Note: Sn (n = 1 to 8): Segment output ports
Pn (n = 1 to 8): General-purpose output ports

Note that when the general-purpose output port function is selected, the correspondence between the output pins and the display data will be that shown in the table.

Output pin	Corresponding display data
S1/P1	D1
S2/P2	D5
S3/P3	D9
S4/P4	D13

Output pin	Corresponding display data
S5/P5	D17
S6/P6	D21
S7/P7	D25
S8/P8	D29

For example, if the general-purpose output port function is selected for the S4/P4 output pin, that output pin will output a high level (V_{DD}) when the display data D13 is 1, and a low level (V_{SS}) when the D13 is 0.

4. DR: 1/2-bias drive or 1/3-bias drive switching control data

This control data bit selects either 1/2-bias drive or 1/3-bias drive.

DR	Drive scheme
0	1/3-bias drive
1	1/2-bias drive

5. SC: Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

6. BU: Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode. In this mode, the internal oscillator circuit stops oscillation (the S68/OSCI pin is configured for segment output) if the IC is in the internal oscillator operating mode (OC = 0) and the IC stops receiving external clock signals (the S68/OSCI pin is configured for external clock input) if the IC is in the external clock operating mode (OC = 1). The common and segment output pins go to the V_{SS} level. However, the S1/P1 to S8/P8 output pins can be used as general-purpose output ports under the control of the data bits P0 to P3.

7. FC0 to FC2: Common/segment output waveform frame frequency control data

These control data bits set the frame frequency of the common and segment output waveforms.

Control data			Frame frequency fo [Hz]
FC0	FC1	FC2	
1	1	0	fosc/6144,f_{CK}/6144
1	1	1	fosc/4608,f_{CK}/4608
0	0	0	fosc/3072,f_{CK}/3072
0	0	1	fosc/2304,f_{CK}/2304
0	1	0	fosc/1536,f_{CK}/1536

8. CT0 to CT2: Display contrast control data

These control data bits set the display contrast.

CT0 to CT2: Display contrast settings (7 steps)

CT0	CT1	CT2	LCD drive bias 3/3 voltage $V_{DD}0$ level
0	0	0	$1.00V_{DD} = V_{DD}-(0.05V_{DD}\times0)$
1	0	0	$0.95V_{DD} = V_{DD}-(0.05V_{DD}\times1)$
0	1	0	$0.90V_{DD} = V_{DD}-(0.05V_{DD}\times2)$
1	1	0	$0.85V_{DD} = V_{DD}-(0.05V_{DD}\times3)$
0	0	1	$0.80V_{DD} = V_{DD}-(0.05V_{DD}\times4)$
1	0	1	$0.75V_{DD} = V_{DD}-(0.05V_{DD}\times5)$
0	1	1	$0.70V_{DD} = V_{DD}-(0.05V_{DD}\times6)$

Although adjustment of the display contrast can be accomplished by activating the built-in display contrast adjuster circuit, it is also possible by changing the level of the voltage at the V_{DD} pin.

Display Data and Output Pin Correspondence

Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5/P5	D17	D18	D19	D20
S6/P6	D21	D22	D23	D24
S7/P7	D25	D26	D27	D28
S8/P8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136

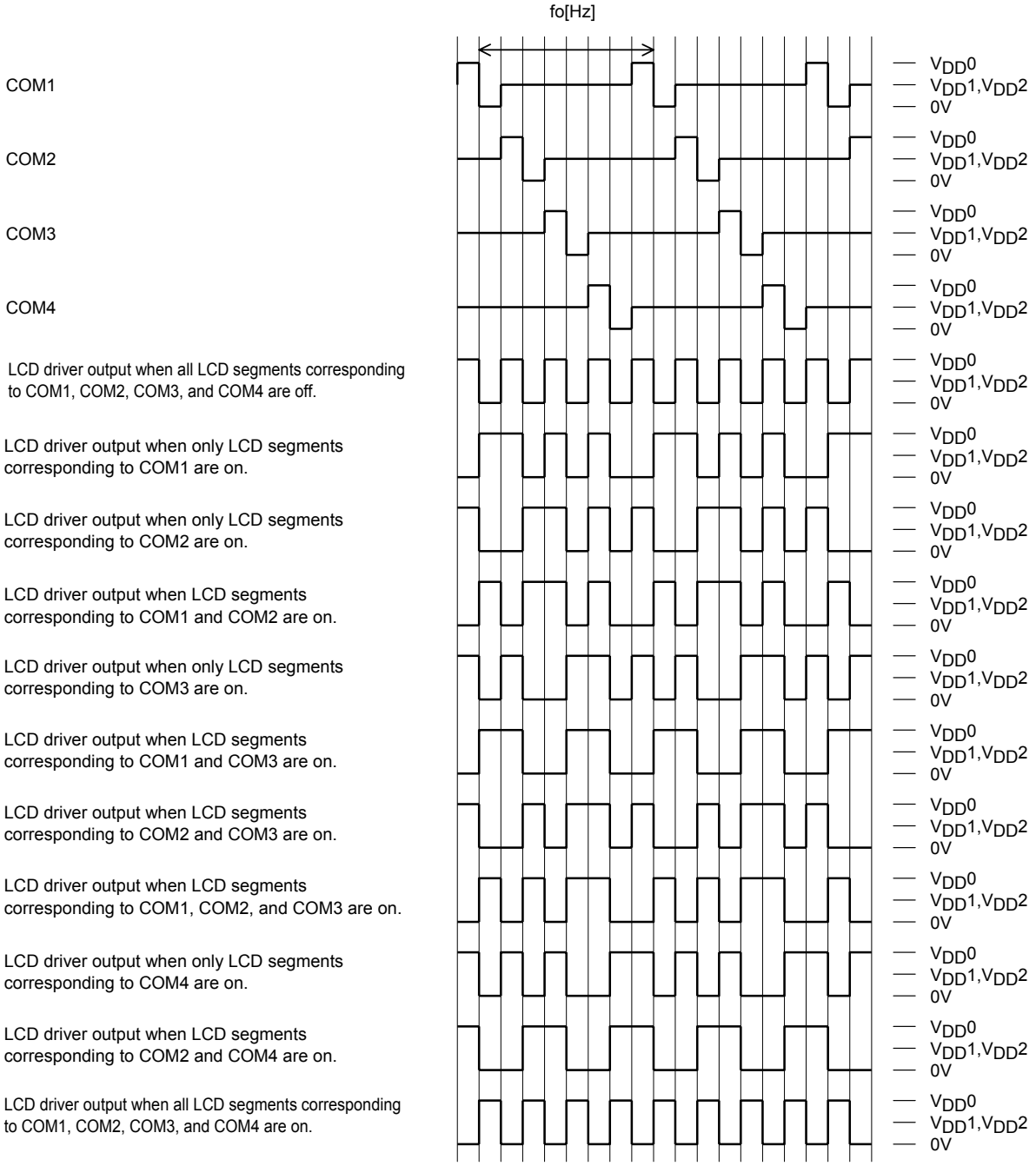
Output pin	COM1	COM2	COM3	COM4
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S67	D265	D266	D267	D268
S68/OSCI	D269	D270	D271	D272

Note: This table assumes that pins S1/P1 to S8/P8 and S68/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

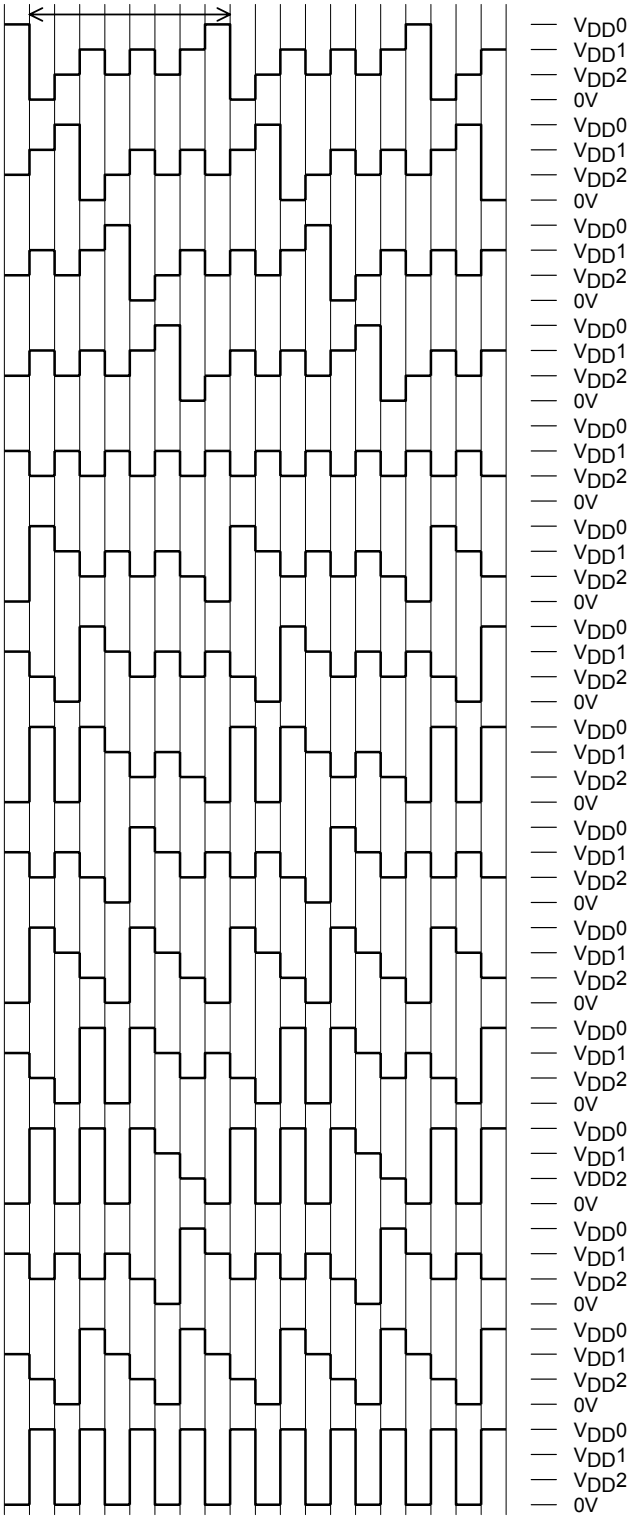
Display data				Output pin (S21) state
D81	D82	D83	D84	
0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

Output waveforms (1/4-Duty 1/2-Bias Drive Scheme)



Control data			Frame frequency fo [Hz]
FC0	FC1	FC2	
1	1	0	fosc/6144,f_{CK}/6144
1	1	1	fosc/4608,f_{CK}/4608
0	0	0	fosc/3072,f_{CK}/3072
0	0	1	fosc/2304,f_{CK}/2304
0	1	0	fosc/1536,f_{CK}/1536

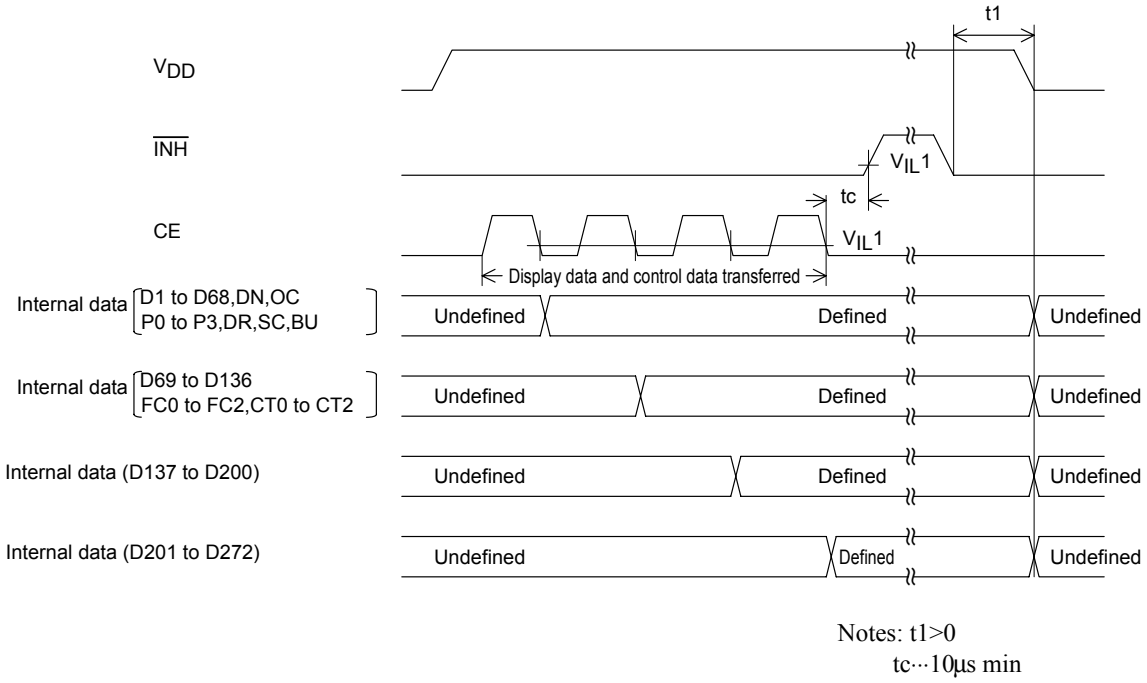
Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)



Control data			Frame frequency fo [Hz]
FC0	FC1	FC2	
1	1	0	fosc/6144,f_{CK}/6144
1	1	1	fosc/4608,f_{CK}/4608
0	0	0	fosc/3072,f_{CK}/3072
0	0	1	fosc/2304,f_{CK}/2304
0	1	0	fosc/1536,f_{CK}/1536

Display Control and the $\overline{INH}$ Pin

Since the LSI internal data (the display data D1 to D272 and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display. (This sets the S1/P1 to S8/P8, S9 to S67, COM1 to COM4, and S68/OSCI pins to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on.
(See Figure 5.)



Notes: t1>0
tc···10μs min

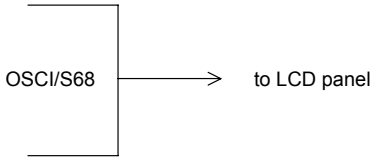
Figure 5

Notes on Controller Transfer of Display Data

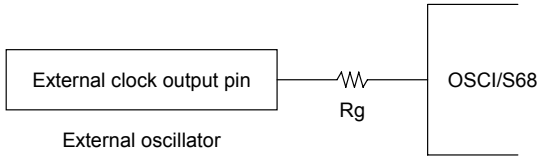
Since the LC75876E and LC75876W transfer the display data (D1 to D272) in four separate transfer operations, we recommend that applications make a point of completing all four data transfers within a period of less than 30ms to prevent observable degradation of display quality.

S68/OSCI Pin Peripheral Circuit

(1) Internal oscillator operating mode (control data OC = 0)
Connect the S68/OSCI pin to the LCD panel when the internal oscillator operating mode is selected.

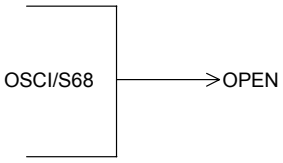


(2) External clock operating mode (control data OC = 1)
When the external clock operating mode is selected, insert a current protection resistor Rg (2.2 to 22kΩ) between the S68/OSCI pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.



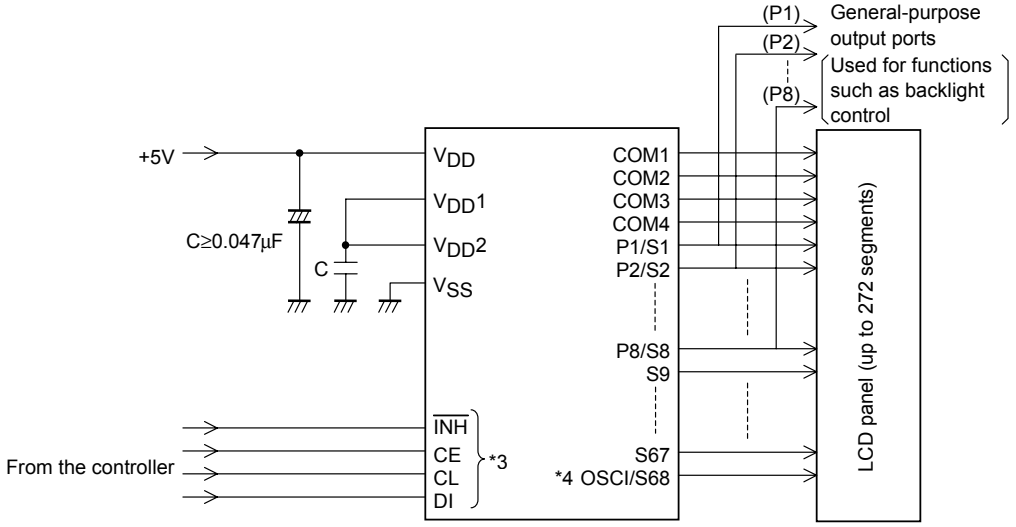
Note: Allowable current value at external clock output pin > $\frac{V_{DD}}{Rg}$

(3) Unused pin treatment
When the S68/OSCI pin is not to be used, select the internal oscillator operating mode (setting control data OC to 0) to keep the pin open.



Sample Application Circuit 1

1/4 Duty, 1/2 Bias

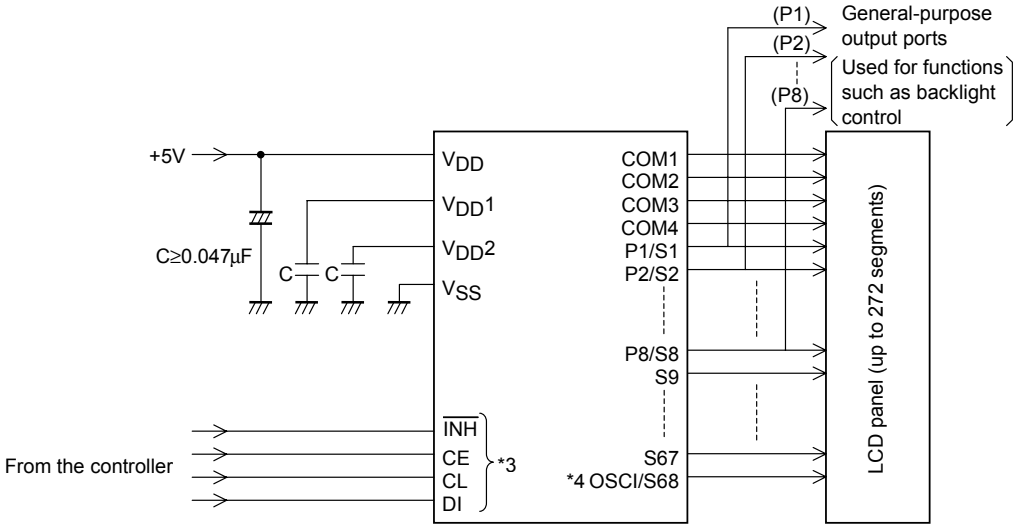


*3: The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3V.

*4: Connect the S68/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg (2.2 to 22kΩ) between the S68/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see "S68/OSCI Pin Peripheral Circuit").

Sample Application Circuit 2

1/4 Duty, 1/3 Bias



*3: The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3V.

*4: Connect the S68/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg (2.2 to 22kΩ) between the S68/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see "S68/OSCI Pin Peripheral Circuit").