

The documentation and process conversion measures necessary to comply with this document shall be completed by 4 March 2018.

INCH-POUND

MIL-PRF-19500/551H  
4 December 2017  
SUPERSEDING  
MIL-PRF-19500/551G  
23 May 2014

## PERFORMANCE SPECIFICATION SHEET

### SEMICONDUCTOR DEVICE, DIODE, SILICON, TRANSIENT VOLTAGE SUPPRESSOR TYPES 1N6461 THROUGH 1N6468, 1N6461US THROUGH 1N6468US, AND 1N6461URS THROUGH 1N6468URS, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

#### 1. SCOPE

1.1 Scope. This specification covers the performance requirements for 500-watt peak pulse, power, silicon, transient voltage suppressor diodes. Three levels of product assurance are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Physical dimensions. See [figures 1, 2, and 3](#).

1.3 Maximum ratings. Maximum ratings are as shown in columns 4, 6, and 7 of the electrical characteristics table herein and as follows:

- a.  $P_R = 2.5 \text{ W}$  ( $T_A = \text{room ambient}$  as defined in the general requirements of 4.5 of [MIL-STD-750](#)). Derate at  $16.7 \text{ mW}/^\circ\text{C}$  for leaded devices and  $50 \text{ mW}/^\circ\text{C}$  for surface mount devices (see [figure 4](#)).
- b.  $P_{PR} = 500 \text{ W}$  (see [figure 5](#)) at  $t_p = 1 \text{ ms}$ .
- c.  $I_{FSM} = 80 \text{ A(pk)}$  at  $t_p = 8.33 \text{ ms}$  ( $T_A = +25^\circ\text{C}$ ).
- d.  $-55^\circ\text{C} \leq T_{op} \leq +175^\circ\text{C}$ ;  $-55^\circ\text{C} \leq T_{STG} \leq +175^\circ\text{C}$  (ambient).

1.4 Primary electrical characteristics. Primary electrical characteristic columns 2 and 4 of the electrical characteristics herein.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.



- \* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.
- \* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".
- \* 1.5.2 Device type. The designation system for the device types of semiconductor covered by this specification sheet are as follows.
- \* 1.5.2.1 First number and first letter symbols. The semiconductors of this specification sheet use the first number and letter symbols "1N".
- \* 1.5.2.2 Second number symbols. The second number symbols for the semiconductor covered by this specification sheet are as follows: "6461", "6462", "6463", "6464", "6465", "6466", "6466", and "6468".
- \* 1.5.3 Suffix symbols. The following suffix symbols are incorporated in the PIN for this specification sheet:

	No second suffix Indicates a through hole mount, axial package. (see <a href="#">figure 1</a> )
US	Indicates a surface mount, square endcap package. (see <a href="#">figure 2</a> )
URS	Indicates a surface mount, 1 round endcap and 1 square endcap package. (see <a href="#">figure 3</a> )

- \* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QML-19500](#).

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

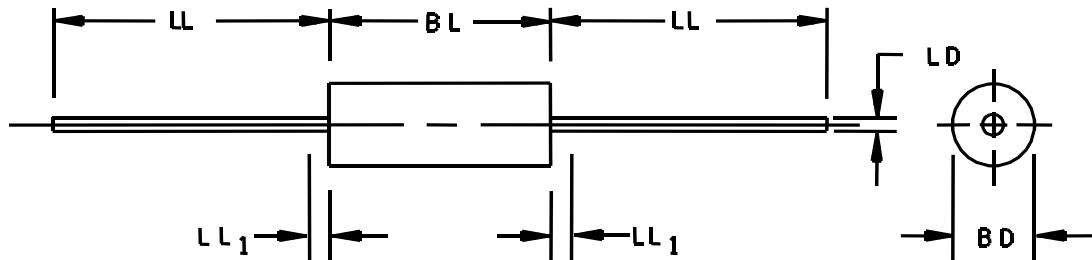
[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

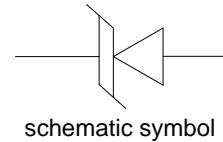
[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



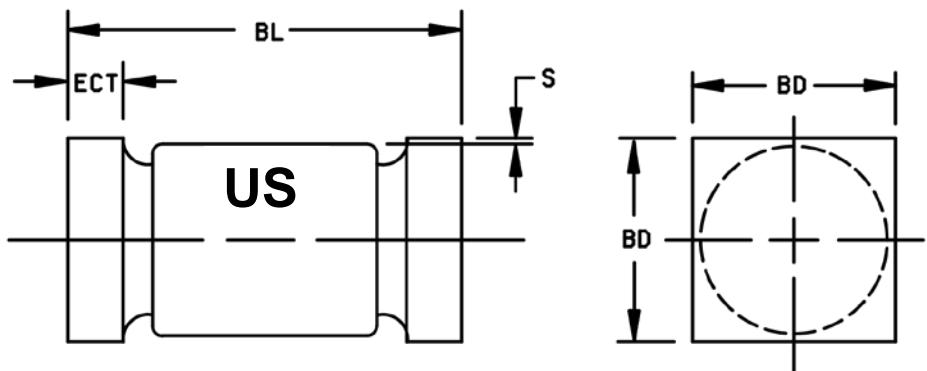
Ltr	Dimensions				Notes	
	Inches		Millimeters			
	Min	Max	Min	Max		
BD	.115	.145	2.92	3.68	3, 4	
BL	.150	.300	3.81	7.62	4	
LD	.037	.042	0.94	1.07	4	
LL	.900	1.300	22.86	33.02		
LL1		.050		1.27	4	



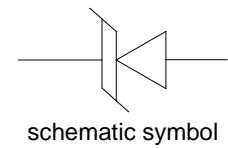
## NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension BD shall be measured at the largest diameter.
4. Dimension BL includes dimension LL<sub>1</sub> region in which the diameter may vary from BD maximum to LD minimum.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

FIGURE 1. Physical dimensions.



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BD	.137	.148	3.48	3.76
BL	.200	.225	5.08	5.72
ECT	.019	.028	0.48	0.71
S	.003		0.08	

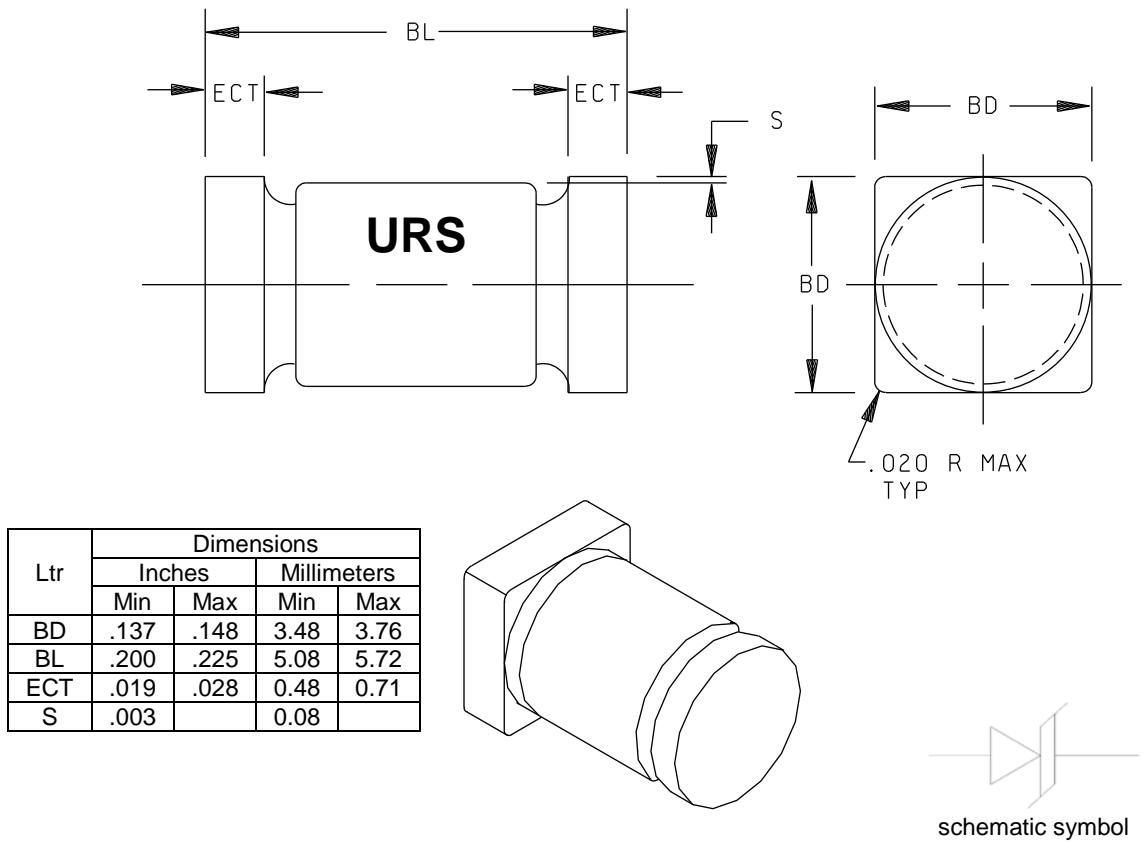


schematic symbol

## NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Referencing to dimension S, minimum clearance of glass body to mounting surface on all orientations.
4. Dimensions are pre-solder dip.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

FIGURE 2. Physical dimensions surface mount devices "US".



## NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimensions are pre-solder dip.
4. One end-cap shall be square and the other end-cap shall be round.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.
6. The cathode shall be connected to the round endcap.

FIGURE 3. Physical dimensions, surface mount devices "URS".

### 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows:

$I_p$ .....Maximum peak pulse current at a specified condition.

$I_{(BR)}$ .....Reverse breakdown current at a specified condition.

TEC .....End-cap temperature.

3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figures 1, 2, and 3](#) herein. The surface mount devices (US and URS) shall be structurally identical to the "non US" version except for lead attachment.

3.4.1 Construction. These devices shall be constructed utilizing metallurgically bonded noncavity double plug construction between both sides of the silicon die and the terminal pins.

3.4.2 Lead finish. Lead finish shall be solderable as defined in [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.3. Metallurgical bond construction. Devices shall be metallurgically bonded, thermally matched, noncavity-double plug construction in accordance with [MIL-PRF-19500](#), and herein.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.5.1 Marking of US and URS versions. For US and URS versions only, all marking may be omitted from the device except for the cathode marking. US and URS devices shall be marked with a cathode band as a minimum, or a minimum of three evenly spaced contrasting color dots around the periphery of the cathode end may be used. At the option of the manufacturer, US and URS devices may include laser marking on an end-cap, to include part number and lot date code for all levels. The prefixes JAN, JANTX, or JANTXV may be abbreviated as J, JX, or JV respectively. (For example: The part number may be reduced to JV6461).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [1.3](#) and [table I](#) herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and [tables I, II, and III](#)).

4.1.1 Sampling and inspection. Sampling and inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein. Lot accumulation period shall be 3 months in lieu of 6 weeks.

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#).

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

\* 4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with [table E-IV](#) of [MIL-PRF-19500](#), and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurement
	JANTX and JANTXV levels
9	Not applicable
11	Not applicable
12	See 4.3.1
13	Not applicable

4.3.1 Burn-in (HTRB) and steady-state operation life (HTRB) conditions. This test shall be conducted with the devices subjected to test conditions in the following order of events and conditions:

- a. Pulse in accordance with 4.5.2b herein 20 times (screening and group B operation life test) and 100 times (group C) at  $T_A$  = room ambient as defined in the general requirements of [MIL-STD-750](#).
- b. Read and record  $I_D$  and  $V_{BR}$  at  $T_A$  = room ambient as defined in the general requirements of [MIL-STD-750](#). Remove defective devices, and record the number of failures.
  - (1) For 96 hours (JANTX and JANTXV) for the screening test.
  - (2) For 340 hours (JANTX and JANTXV) for group B, steady-state operation life test.
  - (3) For 1,000 hours for group C, steady-state operation life test.

Read and record  $I_D$  and  $V_{(BR)}$  at  $T_A$  = room ambient as defined in the general requirements of [MIL-STD-750](#). Devices with  $\Delta I_D > 50$  percent (100 percent for steady-state operation life) of initial value, or 20 percent of column 5 of [table II](#), whichever is greater, or  $\Delta V_{(BR)} = \pm 2$  percent ( $\pm 5$  percent for steady-state operation life) of initial value shall be considered defective. Remove defective devices and record the number of failures.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as herein.

\* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein.

\* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#) and 4.4.2.1 herein.

4.4.2.1 Group B inspection, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1026	$T_A = +125^\circ\text{C}$ , (see 4.3.1).
B5	4081	$R_{\Theta JL} \leq 60^\circ\text{C/W}$ at $L = .375$ inches (9.53 mm), non-surface mount devices; $R_{\Theta JEC} \leq 20^\circ\text{C/W}$ at $L = 0$ inches for surface mount devices.

\* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

4.4.3.1 Group C inspection, table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
*	C2	2036 Axial lead: Test condition A; weight = 12 pounds; $t = 15$ seconds minimum. Test condition E (Lead fatigue not applicable to US diodes).
*	C2	2038 US: Test condition B, weight = 12 pounds; $t = 15$ seconds. Suitable fixtures may be used to pull the end-caps in a manner, which does not aid construction. (See <a href="#">figure 6</a> herein).
C5	4081	$R_{\Theta JL} \leq 60^{\circ}\text{C}/\text{W}$ at $L = .375$ inches (9.53 mm), non-surface mount devices; $R_{\Theta JEC} \leq 20^{\circ}\text{C}/\text{W}$ at $L = 0$ inches for surface mount devices.
C6	1026	$T_A = +125^{\circ}\text{C}$ , (see <a href="#">4.3.1</a> ). Leaded samples from the same lot may be used in lieu of surface mount devices.
C7	4071	$I_{(BR)} = \text{column 3 of } \text{table II}$ , $\alpha V_{(BR)}$ , $T_1 = +25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ ; $T_2 = +125^{\circ}\text{C} \pm 3^{\circ}\text{C}$ ; maximum limits = column 8 of <a href="#">table II</a> . Sample size: 22 devices, $c = 0$ .
C8		See <a href="#">4.5.2.a</a> , ten pulses, sample size: 22 devices, $c = 0$ .

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table III](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Maximum peak pulse current (I<sub>PP</sub>). The peak currents specified in column 7 of [table II](#) shall be applied in the reverse direction while simultaneously maintaining a reverse bias voltage of not less than the applicable voltage specified in column 4 of [table II](#). The clamping voltage ( $V_c$ ) shall be as specified in [4.5.3](#). The peak current shall be applied with a current versus time waveform as follows (one pulse per minute maximum):

- Pulse current shall reach 100 percent of  $I_{PP}$  at  $t \leq 8 \mu\text{s}$  and decay to 50 percent at  $t \geq 20 \mu\text{s}$  for  $t_p = 20 \mu\text{s}$  (see [figure 7](#)).
- Pulse current shall reach 100 percent of  $I_{PP}$  at  $t \leq 10 \mu\text{s}$  and decay to 50 percent at  $t \geq 1 \text{ ms}$  for  $t_p = 1 \text{ ms}$  (see [figure 8](#)).

NOTE: Tolerance on pulse time shall be  $\pm 10$  percent.

4.5.3 Clamping voltage  $V_c$ . The peak pulse clamping voltage shall be measured across the diode in a 1 ms time interval. The response detector shall demonstrate equipment accuracy of  $\pm 3$  percent.

\* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits 2/		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Standby current	4016	DC method; $V_R = V_{RWM}$ (column 4 of <a href="#">table II</a> )	$I_D$		Column 5 of <a href="#">table II</a>	$\mu A$ dc
Breakdown voltage	4022	$t_p \leq 300$ ms, duty cycle $\leq 2$ percent; $I_{(BR)} =$ column 3 of <a href="#">table II</a>	$V_{(BR)1}$	Column 2 of <a href="#">table II</a>		V dc
Forward voltage	4011	$I_F = 1$ A dc	$V_F$		1.5	V (pk)
<u>Subgroup 3</u>		$T_A = -55^\circ C$				
Low temperature operation						
Breakdown voltage	4022	$t_p \leq 300$ ms, duty cycle $\leq 2$ percent; $I_{(BR)} =$ column 3 of <a href="#">table II</a> .	$V_{(BR)2}$	Column 9 of <a href="#">table II</a>		V dc
<u>Subgroup 4</u>						
Clamping voltage (see 4.5.3)		$t_p = 1.0$ ms (see 4.5.2.b) $I_{PP} =$ column 7 of <a href="#">table II</a>	$V_C$		Column 6 of <a href="#">table II</a>	V (pk)
<u>Subgroup 5</u>						
Not applicable						
<u>Subgroup 6</u>						
* Forward surge current	4066	Condition A, One pulse, half sine wave 8.3 ms; $I_F = 0$ , $V_{RWM} = 0$ , $T_A = +25^\circ C$ See <a href="#">table I</a> , subgroup 2	$I_{FSM}$		80	A (pk)
Electrical measurements						
<u>Subgroup 7</u>						
Clamping voltage inverse polarity maximum (see 4.5.3)		$t_p = 1.0$ ms (see 4.5.2.b) except use forward direction current without prior bias voltage	$-V_C$	Column 11 of <a href="#">table II</a>		V (pk)

1/ For sampling plan, see [MIL-PRF-19500](#).2/ Column references are to [table II](#) herein.

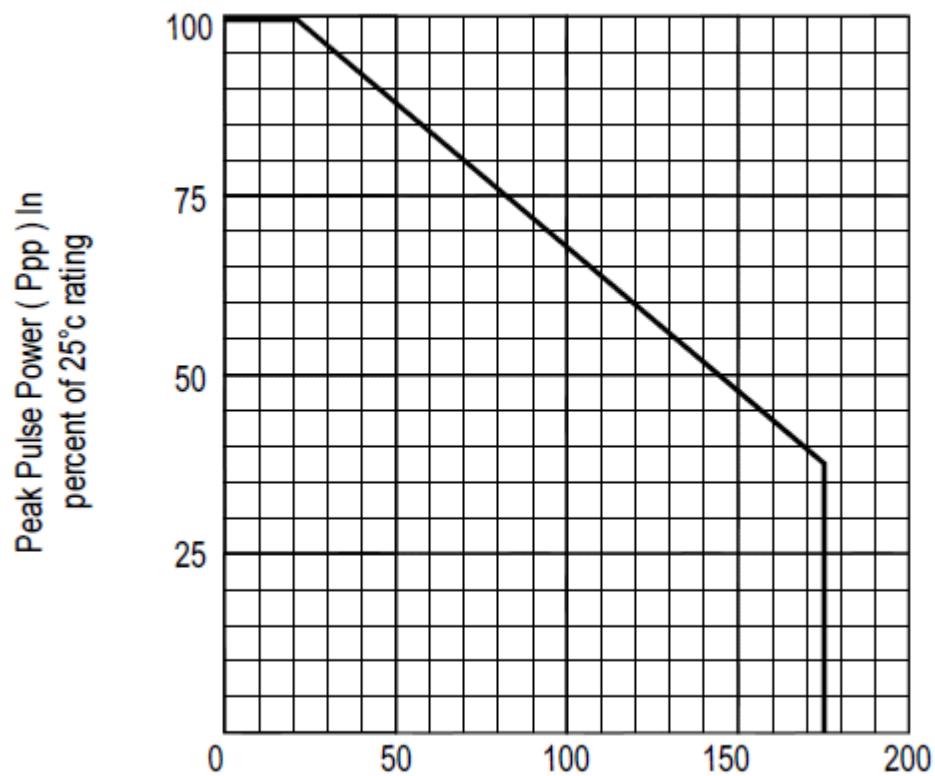
TABLE II. Electrical characteristics. 1/

Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7		Col 8	Col 9	Col 10	Col 11
	$V_{(BR)1}$ at $I_{(BR)}$	$I_{(BR)}$	$V_{RWM}$	$I_D$ at $V_{RWM}$	$V_C$ at $I_{PP}$ for $t_p = 1 \text{ ms}$	$I_{PP}$		$\alpha V_{(BR)}$	$V_{(BR)2}$ Minimum at $I_{BR}$ $T_A = -55^\circ\text{C}$	$(I_{RM})$ Maximum dc current $T_A = +25^\circ\text{C}$	$-V_C$ at $t_p = 1 \text{ ms}$ $A(pk) =$ in accordance with column 7 inverse polarity
						$t_p = 20 \mu\text{s}$	$t_p = 1 \text{ ms}$				
	V dc	mA dc	V (pk)	$\mu\text{A}$ dc	V (pk)	A (pk)	A (pk)	%/°C	V dc	mA	V(pk)
1N6461	5.6	25	5	3,000	9.0	315	56	-0.03, +0.045	5.4	367	-3.5
1N6462	6.5	20	6	2,500	11.0	258	46	+0.060	6.2	304	-3.2
1N6463	13.6	5	12	500	22.6	125	22	+0.085	13.0	139	-3.8
1N6464	16.4	5	15	500	26.5	107	19	+0.085	15.6	63	-3.8
1N6465	27.0	2	24	50	41.4	69	12	+0.096	25.1	39	-3.6
1N6466	33.0	1	30.5	3	47.5	63	11	+0.098	30.2	34	-3.6
1N6467	43.7	1	40.3	2	63.5	45	8	+0.101	40.0	46	-3.5
1N6468	54.0	1	51.6	2	78.5	35	6	+0.103	48.5	20	-3.4

1/ These limits apply to the US and URS device types also.

TABLE III. Group E inspection (all quality levels) for qualification only.

Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
<u>Subgroup 1</u>			
Temperature cycling	1051	500 cycles, condition C, -55°C to +175°C	45 devices, c = 0
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
<u>Subgroup 2</u>			
Life test	1048	1,000 hours. See <a href="#">4.3.1</a>	22 devices, c = 0
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
<u>Subgroups 3, 4 and 5</u>			
Not applicable			
<u>Subgroup 8</u>			
Peak pulse current		See <a href="#">4.5.2</a> . IPP shall be characterized by the supplier and this data shall be available to the Government. Test shall be performed on each low and high voltage device for each structurally identical grouping. Test to failure.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2	
<u>Subgroup 9</u>			
Resistance to glass cracking.	1057	Condition B	



\* FIGURE 4. Derating curve.

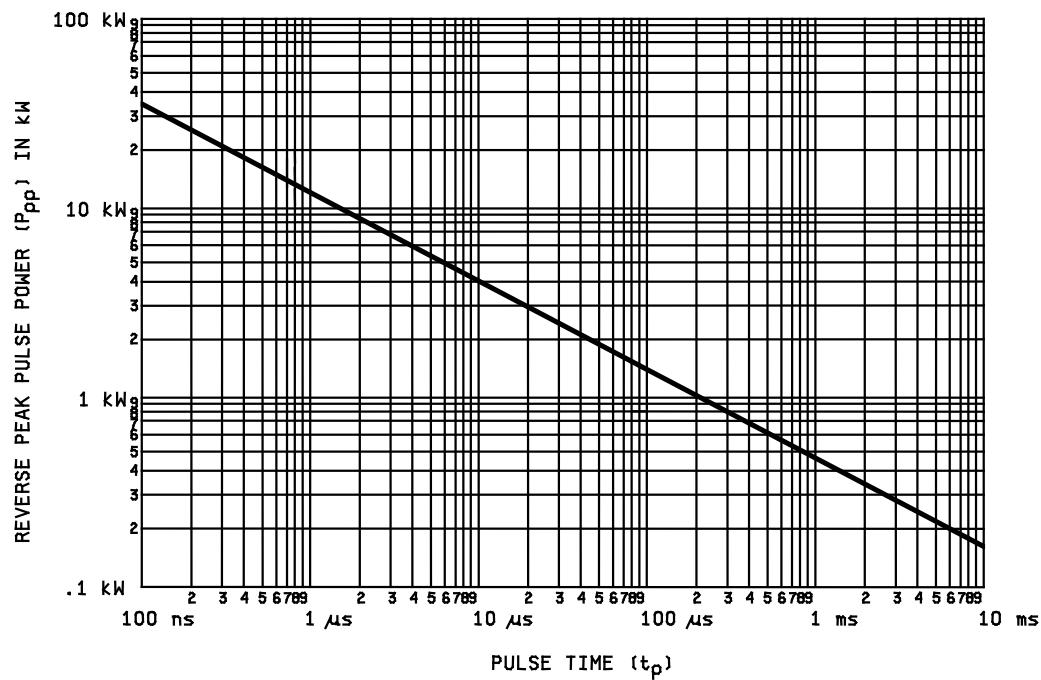


FIGURE 5. Peak pulse power versus pulse time.

MIL-PRF-19500/551H

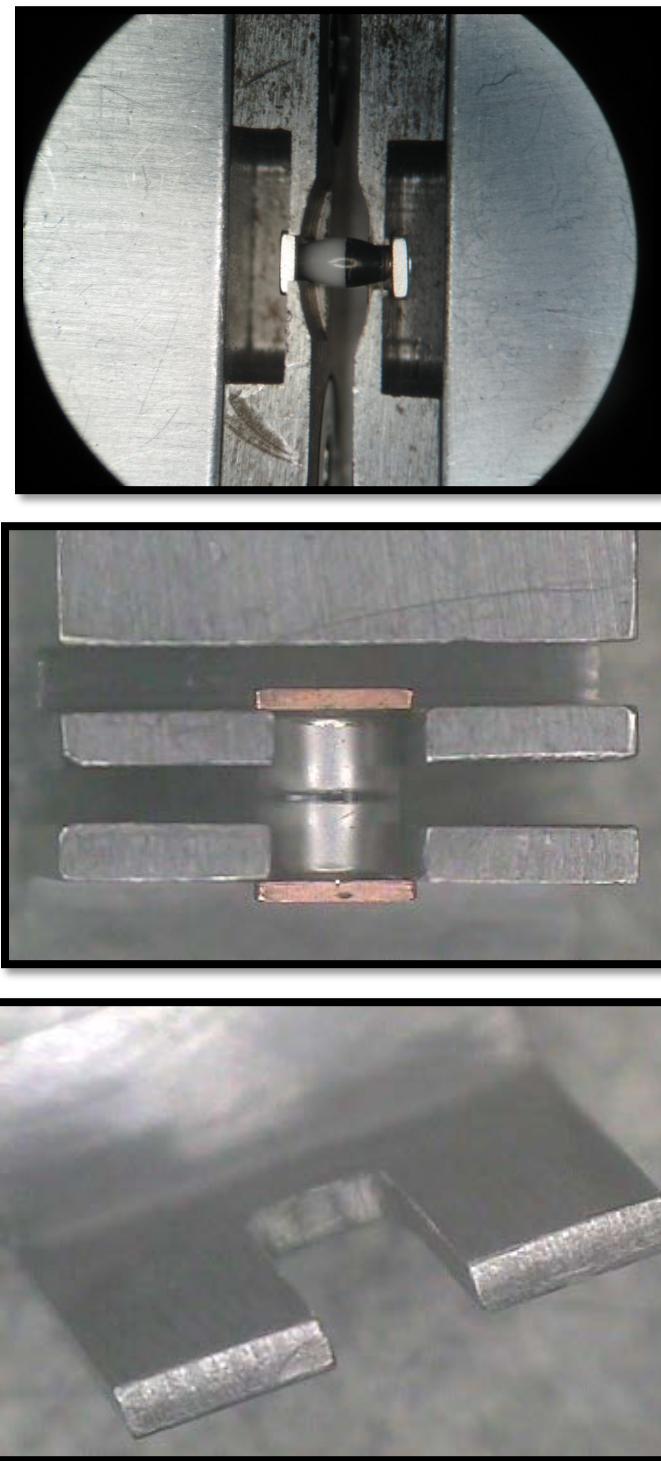


FIGURE 6. URS terminal strength mounting (US suffix shown).

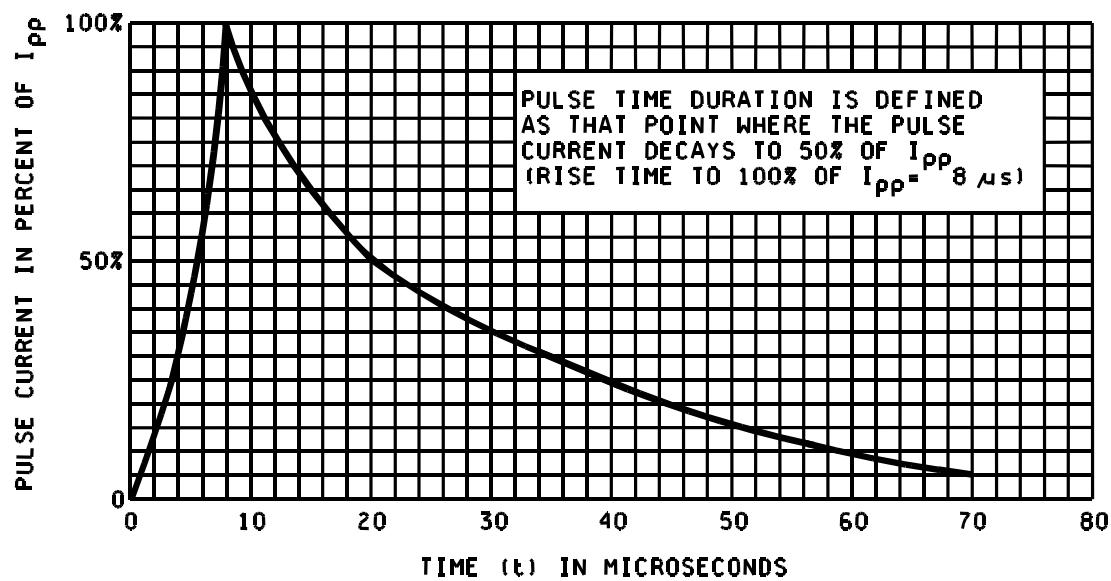


FIGURE 7. Current impulse waveform.

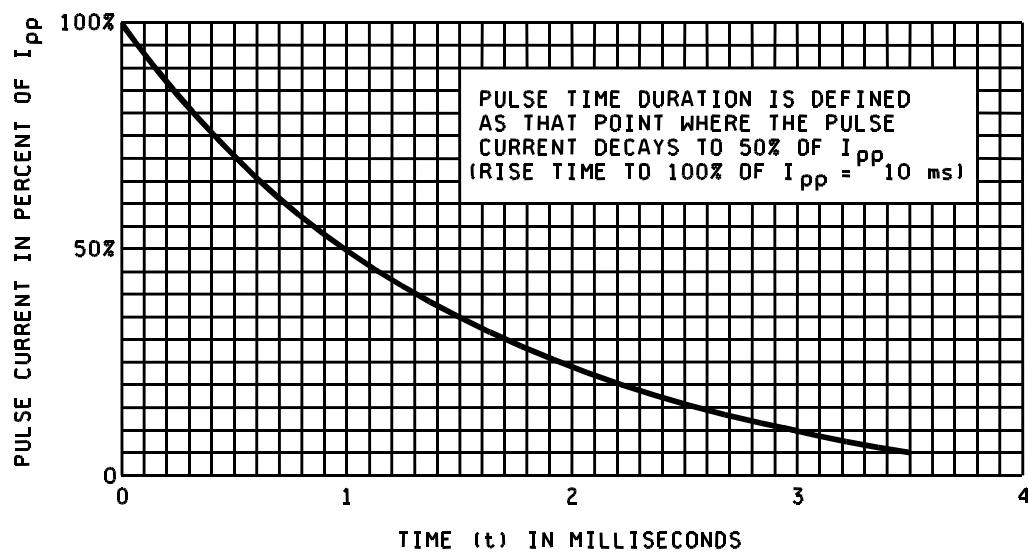


FIGURE 8. Current impulse waveform.

## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

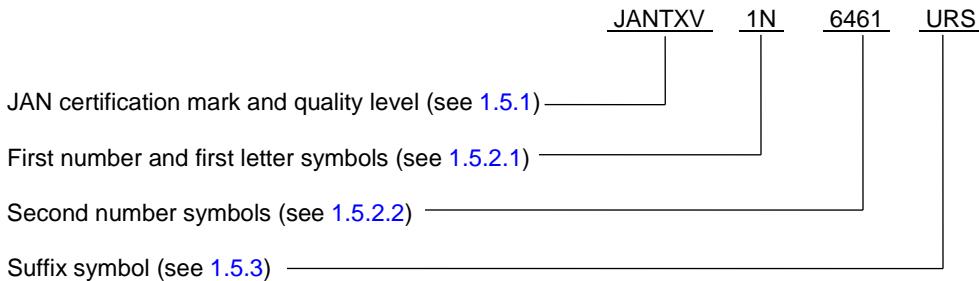
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Lead finish (see 3.4.2).
- c. Packaging requirements (see 5.1).
- d. The complete Part or Identifying Number (PIN), see 1.5 and 6.4 herein.
- e. Destructive physical analysis when requested.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML 19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

\* 6.4 PIN construction example.

\* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



\* 6.5 List of PINs.

\* 6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JAN1N6461 JAN1N6462 JAN1N6463 JAN1N6464 JAN1N6465 JAN1N6466 JAN1N6467 JAN1N6468	JANTX1N6461 JANTX1N6462 JANTX1N6463 JANTX1N6464 JANTX1N6465 JANTX1N6466 JANTX1N6467 JANTX1N6468	JANTXV1N6461 JANTXV1N6462 JANTXV1N6463 JANTXV1N6464 JANTXV1N6465 JANTXV1N6466 JANTXV1N6467 JANTXV1N6468
JAN1N6461US JAN1N6462US JAN1N6463US JAN1N6464US JAN1N6465US JAN1N6466US JAN1N6467US JAN1N6468US	JANTX1N6461US JANTX1N6462US JANTX1N6463US JANTX1N6464US JANTX1N6465US JANTX1N6466US JANTX1N6467US JANTX1N6468US	JANTXV1N6461US JANTXV1N6462US JANTXV1N6463US JANTXV1N6464US JANTXV1N6465US JANTXV1N6466US JANTXV1N6467US JANTXV1N6468US
JAN1N6461URS JAN1N6462URS JAN1N6463URS JAN1N6464URS JAN1N6465URS JAN1N6466URS JAN1N6467URS JAN1N6468URS	JANTX1N6461URS JANTX1N6462URS JANTX1N6463URS JANTX1N6464URS JANTX1N6465URS JANTX1N6466URS JANTX1N6467URS JANTX1N6468URS	JANTXV1N6461URS JANTXV1N6462URS JANTXV1N6463URS JANTXV1N6464URS JANTXV1N6465URS JANTXV1N6466URS JANTXV1N6467URS JANTXV1N6468URS

\* 6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:

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Navy - EC  
Air Force - 85  
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Preparing activity:

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\* Review activities:  
Air Force - 19

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