R2A20057BM

Lithium-Ion Battery Switching Charger IC with Auto Load Current Distribution

R03DS0069EJ0100
Rev.1.00
Mar 1, 2013

This is a target specification. Some specs are subject to change.

Description

R2A20057BM is a semiconductor integrated circuit designed for Lithium-ion battery charger control IC. Built-in Input current limitation circuit compliant with USB requirements and dual output (system and battery) control circuit allows to supply the system power and the battery charging power simultaneously from input power.

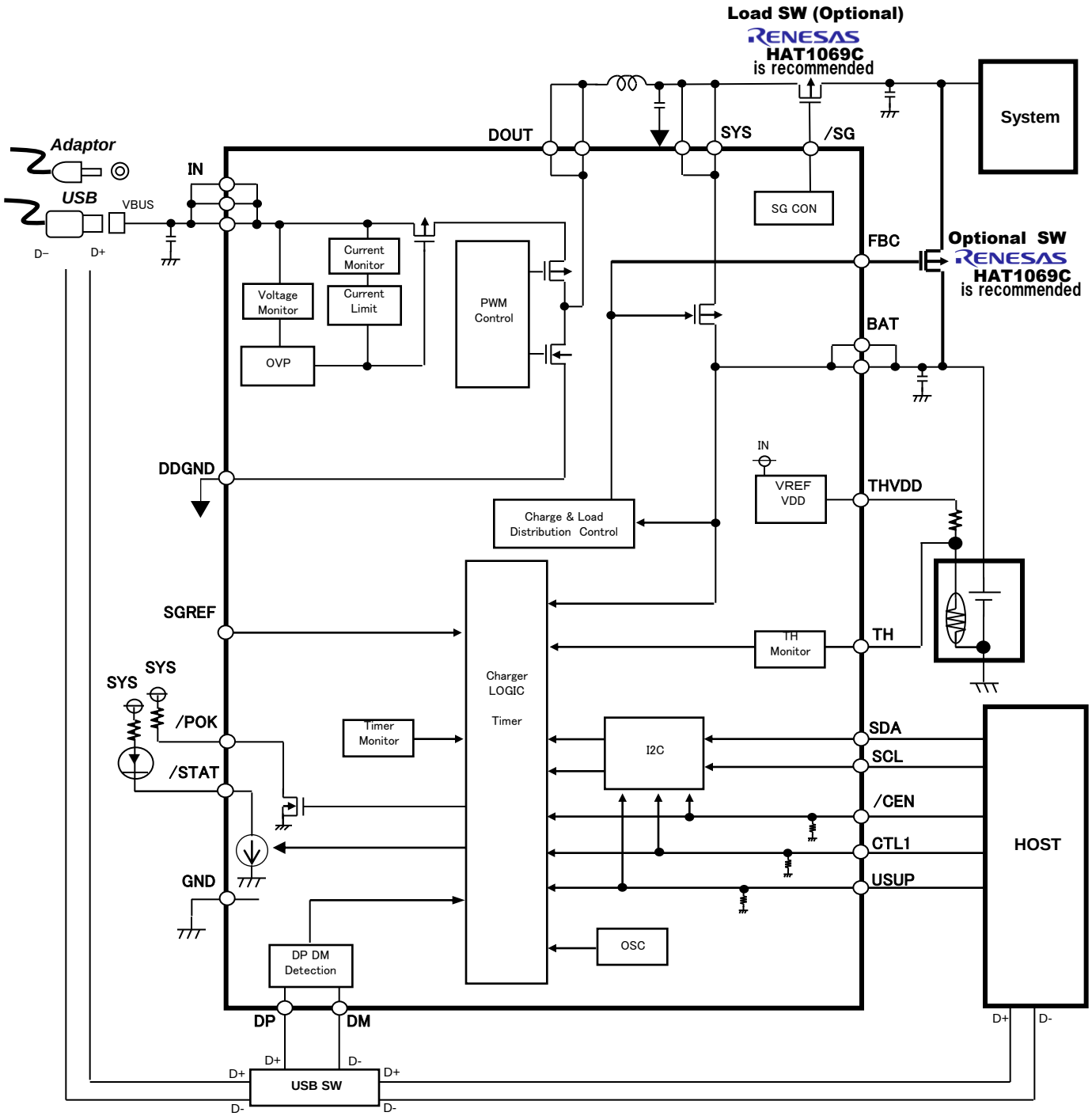
Features

- Allows to USB charging
  - Automatic DPDM detection and automatic input current limitation setup
    (USB battery charging 1.2 and VBUS divided port)
  - Input current limitation is programmable
    I^2C 100mA/500mA/1000mA/1500mA/2100mA/Limitless/Suspend
    External control signal (CTL and USUP) 100mA/500mA/Suspend
  - Weak battery charge function
- High precision charge control voltage : 4.2V+/-21mV (+/-0.5%),4.35V+/-22mV (+/-0.5%)
- Auto load current distribution control
  - Auto power management between system load and battery charge within input current limitation
  - Built-in low Ron path switch (30mohm)
  - System output voltage Switching regulation:battery voltage + 0.3V
- Compliance with JEITA guideline
  - Thermistor I/F detects battery temp. to control CC/CV parameters by built-in charge profile
- I2C interface
  - Adjustable charging parameters
- Protection function
  - Input UVLO/OVLO - Battery over voltage detection - Timer
  - Chip temperature detection - Thermal shutdown
- Recharge function
- Gate control for system Load SW (/SG)
- Input power OK output (/POK)
- Charge status output (/STAT)

Application

- Digital Still Camera
- Digital Video Camera
- Mobile Phone
- PDA/PND
- Tablet/Note PC
- Portable Audio Player
- Portable Game Machine

Block Diagram



①“IN”terminal Capacitor is “ Effective value=4μF” and over. Capacitor is located adjacent to IN terminal.

②Recommended operating inductance condition

Murata：LQM2HPN2R2MGO 2.2uH、1300mA

③If do not use recommended operating inductance condition, please contact us.

Pin function

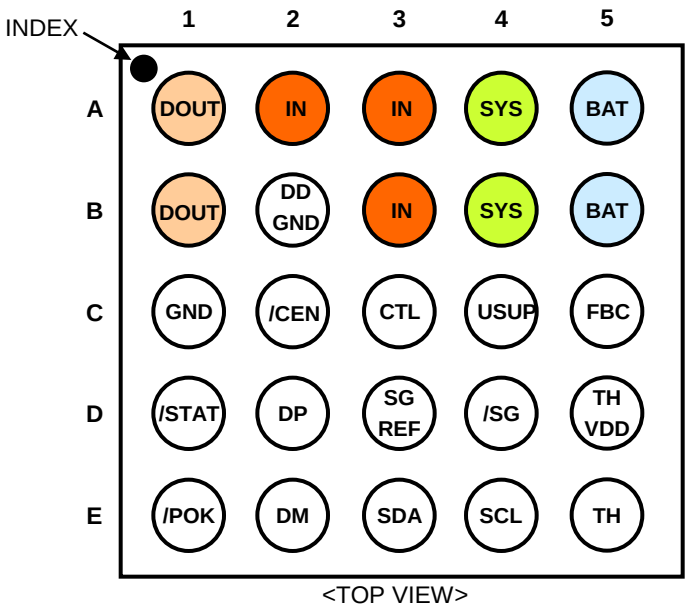
No.	Pin layout No.	Terminal name	I/O	Function
1,2,3	A2,A3,B3	IN	I	Power input (Each IN terminal must be shortcircuited on the board)
4,5	A1,B1	DOUT	O	Switching node (Each DOUT terminal must be shortcircuited on the board)
6,7	A4,B4	SYS	O	System power output (Each SYS terminal must be shortcircuited on the board)
8,9	A5,B5	BAT	I/O	Battery connection terminal (Each BAT terminal must be shortcircuited on the board)
10	C1	GND	GND	GND
11	B2	DDGND	GND	Power GND for DCDC converter
12	D4	/SG	O	Gate control terminal for system Load SW (option)
13	D3	SGREF	I	Reference voltage output terminal for /SG control voltage
14	C5	FBC	O	Optional SW Gate control
15	D5	THVDD	O	Regulated voltage output for the thermistor (2.0V)
16	E5	TH	I	Thermistor input
17	E1	/POK	O	Input power OK output (Open Drain)
18	D1	/STAT	O	Charge status output (Under charge : ON, Error : Blink
19	E3	SDA	I/O	Serial data input/output
20	E4	SCL	I	Serial clock input
21	C2	/CEN	I	Charge enable
22	C3	CTL	I	Input current limitation terminal
23	C4	USUP	I	USB suspend terminal
24	D2	DP	I	USB DP port input
25	E2	DM	I	USB DM port input

/CEN	Charge function
L	Enable
H	Disable

USUP	USB suspend
L	Disable
H	Enable

CTL	SDP input current limit
L	100mA
H	500mA

Pin configuration



<TOP VIEW>

Absolute maximum ratings

(Ta=25degC, unless otherwise specified.)

Symbol	Items		Ratings	Unit
Vmax	Input voltage	IN	−0.3～25	V
		Other Pin	−0.3～6.5	V
IINmax	Input current	IN	2.5	A
		IN (peak) ※1	4.0	A
Iomax	Output current	SYS	3.0	A
		SYS (peak) ※1	4.0	A
		BAT	3.0	A
		BAT (peak) ※1	4.0	A
		THVDD	1.0	mA
Iosmax	Output sink current	/STAT, /POK	20.0	mA
Topr	Operating temperature range		−30～85	°C
Tstg	Storage temperature range		−40～125	°C
Tj	Junction temperature		−30～125	°C
Pd	Power dissipation *2		2.12	W

*1 Within 200µs

*2 This value is at 75mm x 75mm x 1mm of FR4 board with 4 layers at Ta=25 degC.
It depends on the board condition.

Recommended operating condition

(Ta=25degC, unless otherwise specified.)

Symbol	Items	Min.	Max.	Unit
Vin	IN input voltage	4.5	5.5	V
IIN	IN input current		2.0	A
ISYS	SYS output current		2.5	A
IBAT	BAT output current		2.5	A
ICHG	Charge current		2.0	A
Tj	Junction temperature	−30	125	°C

Electrical Characteristics

【 Input voltage detection 】

(Ta=25degC and Vin=5V, unless otherwise specified.)

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
VIN detection voltage	UVLO	VIN voltage rising (250mV Hysteresis)	3.1	3.3	3.5	V
/POK detection time*1	TDGLH1	VIN:0V→5V, /POK=Lo		64		ms
Input over voltage protection (OVP)	VOVP	VIN voltage rising (110mV Hysteresis)	6.1	6..3	6.5	V
OVP detection time *1	TDGLH2	VIN voltage rising		32		μ s
OVP release detection time *1	TDGLL	VIN voltage rising		64		ms

【 Circuit current 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
BAT discharge current1	ISB1	VBAT=4.2V SYSTEM NoLoad			7.5	μ A
BAT discharge current 2	ISB2	VIN=5V,VBAT=4.2V Charge completion, SYSTEM NoLoad			7.5	μ A
BAT discharge current 3	ISB3	VBAT=3.2V Charge error, SYSTEM NoLoad		20	30	μ A
Standby current	ISB	VIN=5V, USB suspend,DCDC=OFF, after USB detection			1.5	mA
Circuit current	ICC	VIN=5V, Charger off SYSTEM NoLoad		12	20	mA

【 Auto load current distribution and Input current limitaition 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
ON Resistance between BAT and SYS	RONBS	VIN=0V, BAT=4.2V, ISYS=200mA		30	60	mΩ
VSYS reguration voltage1	VSYSRG1	BAT=3.6V SYSTEM NoLoad, ICHG=100mA	BAT +0.25	BAT +0.3	BAT +0.35	V
VSYS reguration voltage2 (Auto load current distribution control)	VSYSRG2	USB 500mA Mode VIN=5V, VBAT=3.7V	BAT +0.10	BAT +0.15	BAT +0.20	V
VSYS reguration voltage3 (Supply from IN and BAT)	VSYSRG3	USB 100mA Mode, ISYS=200mA VIN=5V, VBAT=3.7V	BAT −0.05	BAT −0.1	BAT −0.15	V
Input current limitation*1	ILIM0	USB 100mA Mode	80	90	100	mA
	ILIM1	USB 500mA Mode	450	475	500	mA
	ILIM2	USB 1000mA Mode	800	900	1000	mA
	ILIM3	USB 1500mA Mode	1200	1350	1500	mA
	ILIM4	ADP 2100mA Mode	1700	1900	2100	mA

*1:Design guarantee

Electrical Characteristics

【 Battery voltage detection 】

(Ta=25degC and Vin=5V, unless otherwise specified.)

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Charge control voltage(4.35V)	VCHG435	ICHG=1mA	4.328	4.350	4.372	V
Charge control voltage (4.20V)	VCHG420	ICHG=1mA	4.179	4.200	4.221	V
Charge control voltage (4.15V)	VCHG415	ICHG=1mA	4.10	4.15	4.20	V
Charge control voltage (4.10V)	VCHG410	ICHG=1mA	4.05	4.10	4.15	V
Charge control voltage (4.05V)	VCHG405	ICHG=1mA	4.00	4.05	4.10	V
Charge control voltage (4.00V)	VCHG400	ICHG=1mA	3.95	4.00	4.05	V
Charge start voltage	VSTART	VBAT voltage rising(100mV Hysteresis)	1.40	1.50	1.60	V
Quick charge start voltage	VQCHGON	VBAT voltage rising(100mV Hysteresis)	2.90	3.00	3.10	V
Recharge start voltage	VRECHG	VBAT voltage falling(100mV Hysteresis)	3.65	3.75	3.85	V
Overvoltage detection1	VOV1	VBAT voltage rising, VCHG=4.35V	4.42	4.50	4.58	V
Overvoltage detection1	VOV2	VBAT voltage rising, VCHG=4.20V	4.27	4.35	4.43	V

【 Charge current detection 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Quick charge current(1.0C)	ICHG1C	VBAT=3.5V	450	500	550	mA
Quick charge current(0.5C)	ICHG05C	VBAT=3.5V	200	250	300	mA
Trickle charge current(0.2C)	IPCHG02C	VBAT=2.5V	70	100	130	mA
Trickle charge current(0.1C)	IPCHG01C	VBAT=2.5V	35	50	65	mA
Charge complection(0.2C)	IFC02C	CV control	70	100	130	mA
Charge complection(0.1C)	IFC01C	CV control	35	50	65	mA
Charge complection(0.05C)	IFC005C	CV control	10	25	40	mA

【 Timer 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Oscillation frequency*1	FOSC		57.6	64.0	70.4	kHz
Trickle charge timer*1	TPCHG		54	60	66	Min
Quick charge timer*1	TCHG		270	300	330	Min
Weak Battery charge timer*1	TWEAK		36	40	44	Min

*1:Design guarantee

Electrical Characteristics

【 Chip temperature detection 】

(Ta=25degC and Vin=5V, unless otherwise specified.)

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Chip temperature detection*1	TREG	Junction temperature, 10℃Hysteresis		110		℃
Chip temperature reset detection*1	TRGRST	Junction temperature		125		℃
Thermal shutdown temperature*1	TSD	Junction temperature		150		℃

【 Thetmistor detection 】 Type 10kΩ *2

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
THVDD output voltage	VTHVDD	IO=0mA	1.90	2.00	2.10	V
Thermistor connection detect voltage	THCON	Target Battery TEMP -21.5degC	84.7	87.4	89.76	%
Temperature protection detect voltage1	THMVL	Target Battery TEMP 2.5degC (+/-2.5degC)	68.74	70.93	73.05	%
Temperature protection detect voltage hysteresis1	VTHMVL	Hysteresis TEMP 2.5degC (+/-2.0degC)	15	44	80	mV
Temperature protection detect voltage2	THML	Target Battery TEMP 12.5degC (+/-2.5degC)	59.48	61.85	64.18	%
Temperature protection detect voltage hysteresis2	VTHML	Hysteresis TEMP 2.5degC (+/-2.0degC)	18	47	76	mV
Temperature protection detect voltage3	THMH	Target Battery TEMP 42.5degC (+/-2.5degC)	32.98	34.87	36.84	%
Temperature protection detect voltage hysteresis3	VTHMH	Hysteresis TEMP 2.5degC (+/-2.0degC)	8	40	72	mV
Temperature protection detect voltage4	THMVH	Target Battery TEMP 57.5degC (+/-2.5degC)	23.29	24.71	26.2	%
Temperature protection detect voltage hysteresis4	VTHMVH	Hysteresis TEMP 2.5degC (+/-2.0degC)	5	31	55	mV

*1: Design guarantee
*2: TH05-3H103F(10kΩ MITSUBISHI MATERIALS)

Electrical Characteristics

【 Thetmistor detection 】 Type 100kΩ *2

(Ta=25degC and Vin=5V, unless otherwise specified.)

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Thermistor connection detect voltage	THCON	Target Battery TEMP −21.5degC	90	93	96	%
Temperature protection detect voltage1	THMVL	Target Battery TEMP 2.5degC (+/−2.5degC)	73.15	75.70	78.12	%
Temperature protection detect voltage hysteresis1	VTHMVL	Hysteresis TEMP 2.5degC (+/−2.0degC)	17	51	85	mV
Temperature protection detect voltage2	THML	Target Battery TEMP 12.5degC (+/−2.5degC)	61.93	64.85	67.71	%
Temperature protection detect voltage hysteresis2	VTHML	Hysteresis TEMP 2.5degC (+/−2.0degC)	20	59	98	mV
Temperature protection detect voltage3	THMH	Target Battery TEMP 42.5degC (+/−2.5degC)	29.03	31.27	33.63	%
Temperature protection detect voltage hysteresis3	VTHMH	Hysteresis TEMP 2.5degC (+/−2.0degC)	16	47	78	mV
Temperature protection detect voltage4	THMVH	Target Battery TEMP 57.5degC (+/−2.5degC)	18.18	19.69	21.32	%
Temperature protection detect voltage hysteresis4	VTHMVH	Hysteresis TEMP 2.5degC (+/−2.0degC)	11	32	53	mV

*1: Design guarantee
*2: NCP15WF104F03RC(MURATA)

Electrical Characteristics

(Ta=25degC and Vin=5V, unless otherwise specified.)

【 DCDC conveter 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
PWM frequency*1	PWMOSC	IO=0mA		2.0		MHz
Efficiency*1	PEF	BAT=3.8V ISYS=500mA		90		%

【 CTL, USUP terminal 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Input High voltage	VINH1		1.4			V
Input Low voltage	VINL1				0.3	V
Input High current	IIH1	VINH1=2.8V			50	μ A
Input Low current	IIL1	VINL1=0.03V			1	μ A
Pull down resistance	IILR1	VINL1=0.03V		100		kΩ

【 /CEN terminal 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Input High voltage	VINH2		1.4		3.6	V
Input Low voltage	VINL2				0.3	V
Input High current	IIH2	VINH1=2.8V			50	μ A
Input Low current	IIL2	VINL1=0.03V			1	μ A
Pull down resistance	IILR1	VINL1=0.03V		100		kΩ

【 SCL, SDA terminal 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Input High voltage	VINH3		1.4			V
Input Low voltage	VINL3				0.3	V
Output Low voltage (SDA)	VOL1	ISINK=3mA			0.4	V
Input High current	IIH3	VINH2=1.8V			1	μ A
Input Low current	IIL3	VINL=0.03V			1	μ A

*1:Design guarantee

Electrical Characteristics

(Ta=25degC and Vin=5V, unless otherwise specified.)

【 /POK terminal 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Output Low voltage	VOL2	ISINK=5mA			0.4	V

【/STAT terminal 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Common current	ISTAT	SYS=3.7V	1.5	7.5	15	mA

【 TH terminal 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Input voltage range	VINTH		0		THVDD	V

【 Gate On/Off control System Load SW MOSFET 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Low battery detection voltage	VSYSSW OFF	Battery falling	3.2	3.3	3.4	V
Low battery detection voltage hysteresis	VSYSSW OFF_HYS	SGREF=THVDD	100	300	500	mV
SGREF detection voltage	VSYSREF SW		1.7	1.8	1.9	V

Electrical Characteristics

(Ta=25degC and Vin=5V, unless otherwise specified.)

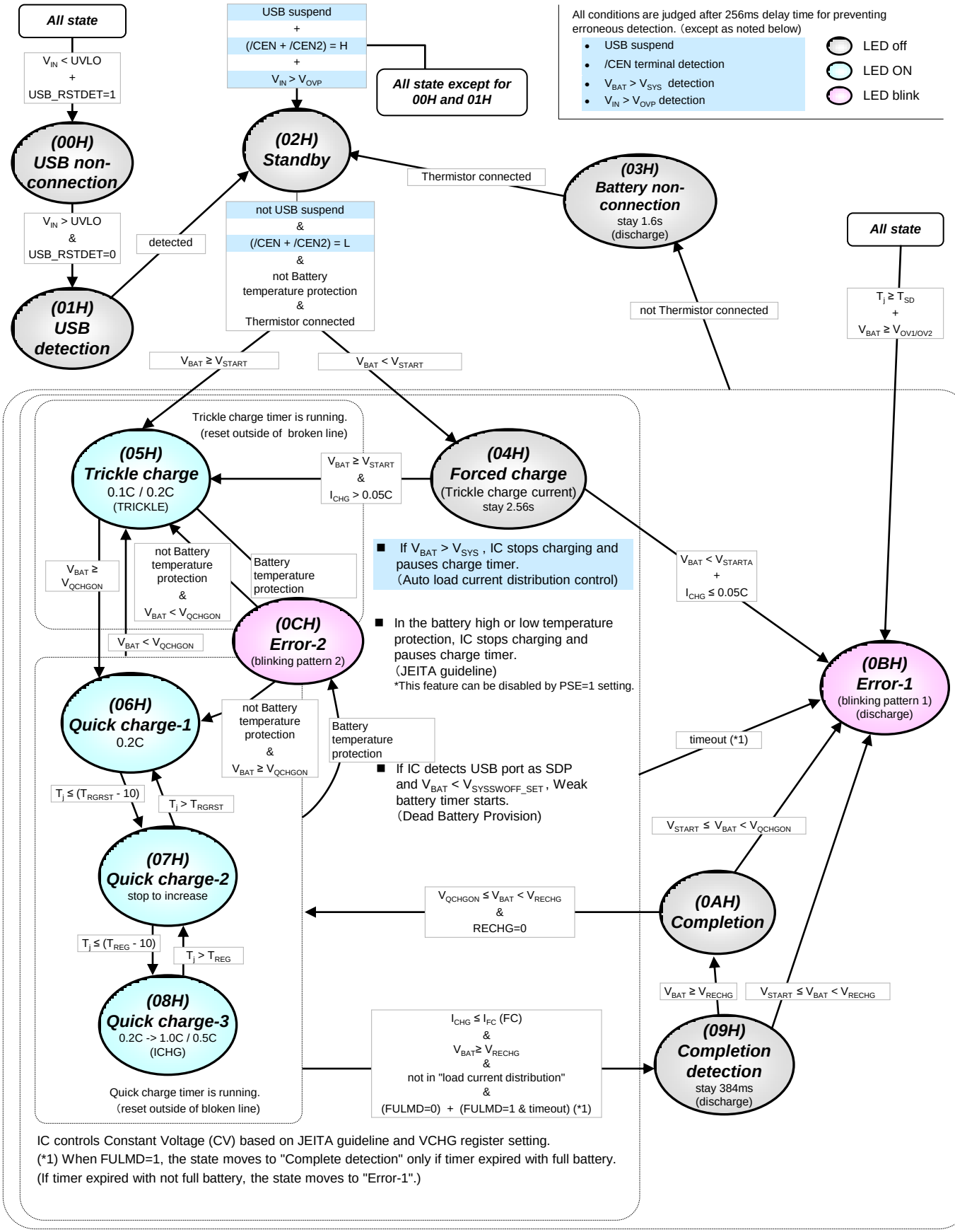
【 DP-DM USB detection 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
DP-DM short resistance	RDPM_SHORT	USB battery charging 1.2		125	200	Ω
DP terminal voltage	VDP_SRC	USB battery charging 1.2	0.5	0.6	0.7	V
DM terminal voltage	VDM_SRC	USB battery charging 1.2	0.5	0.6	0.7	V
DP terminal sink current	IDP_SINK	USB battery charging 1.2	25		175	μ A
DM terminal sink current	IDM_SINK	USB battery charging 1.2	25		175	μ A
Date detection voltage	VDAT_REF	USB battery charging 1.2	0.25		0.40	V

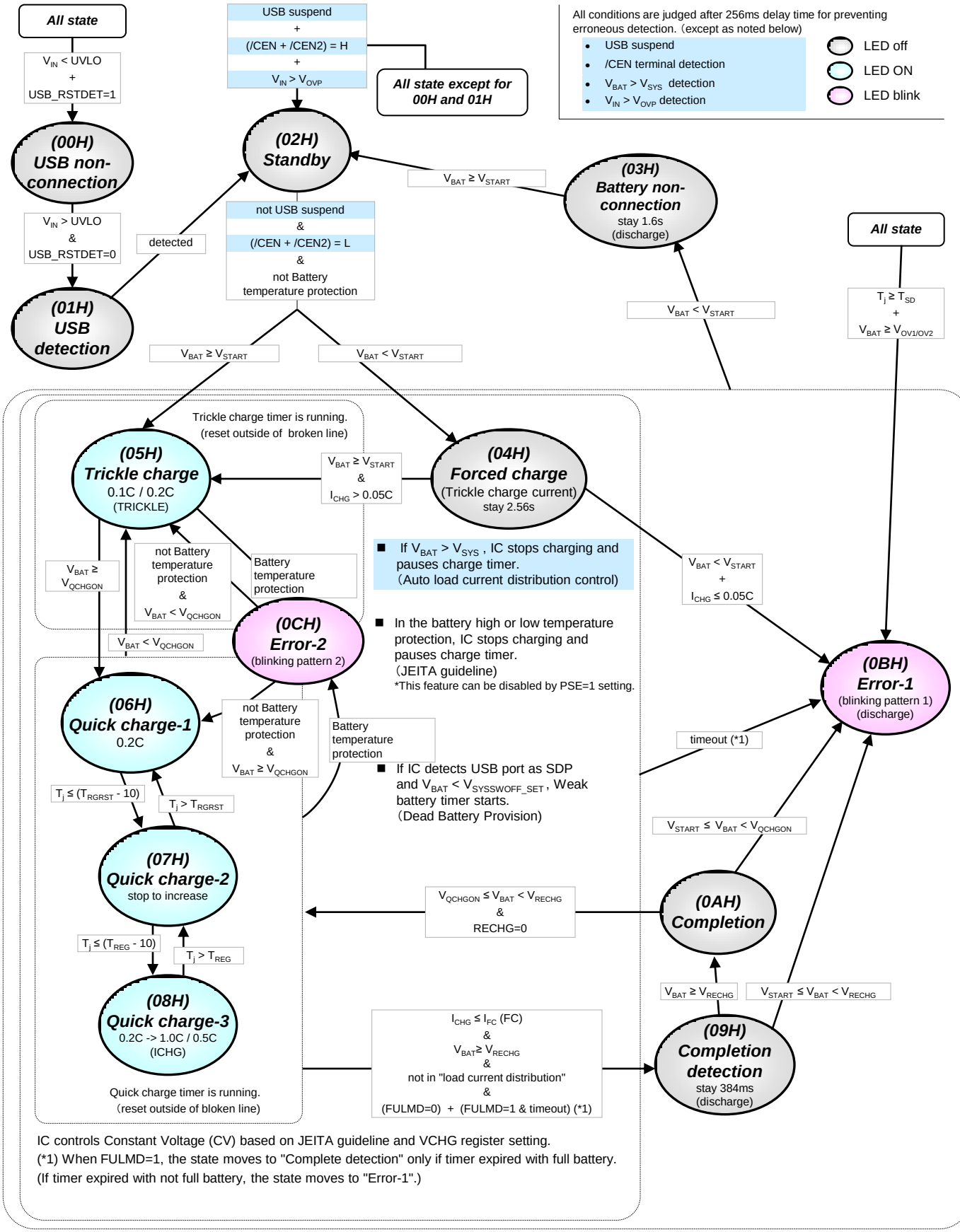
【 Divided Port detection 】

Item	Symbol	Condition	Rate value			Unit
			Min.	Typ.	Max.	
Divided Port Middle voltage	VDIV_MID		1.90	2.00	2.10	V
Divided Port High voltage	VDIV_HIGH		2.55	2.68	2.81	V

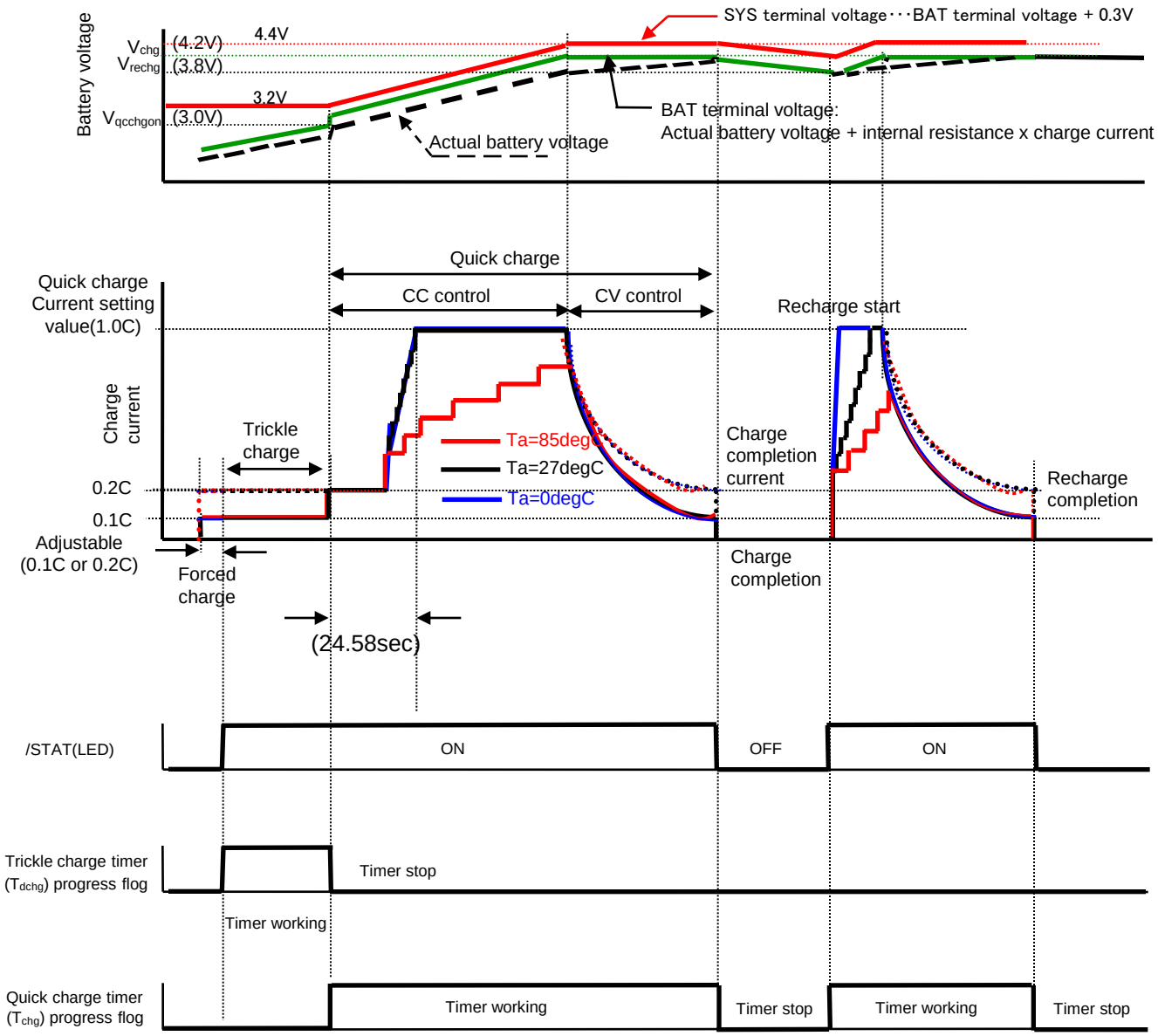
Charge state diagram 1 (register THBATCON = 0 (default setting))



Charge state diagram 2 (register THBATCON = 1)



Charge state diagram

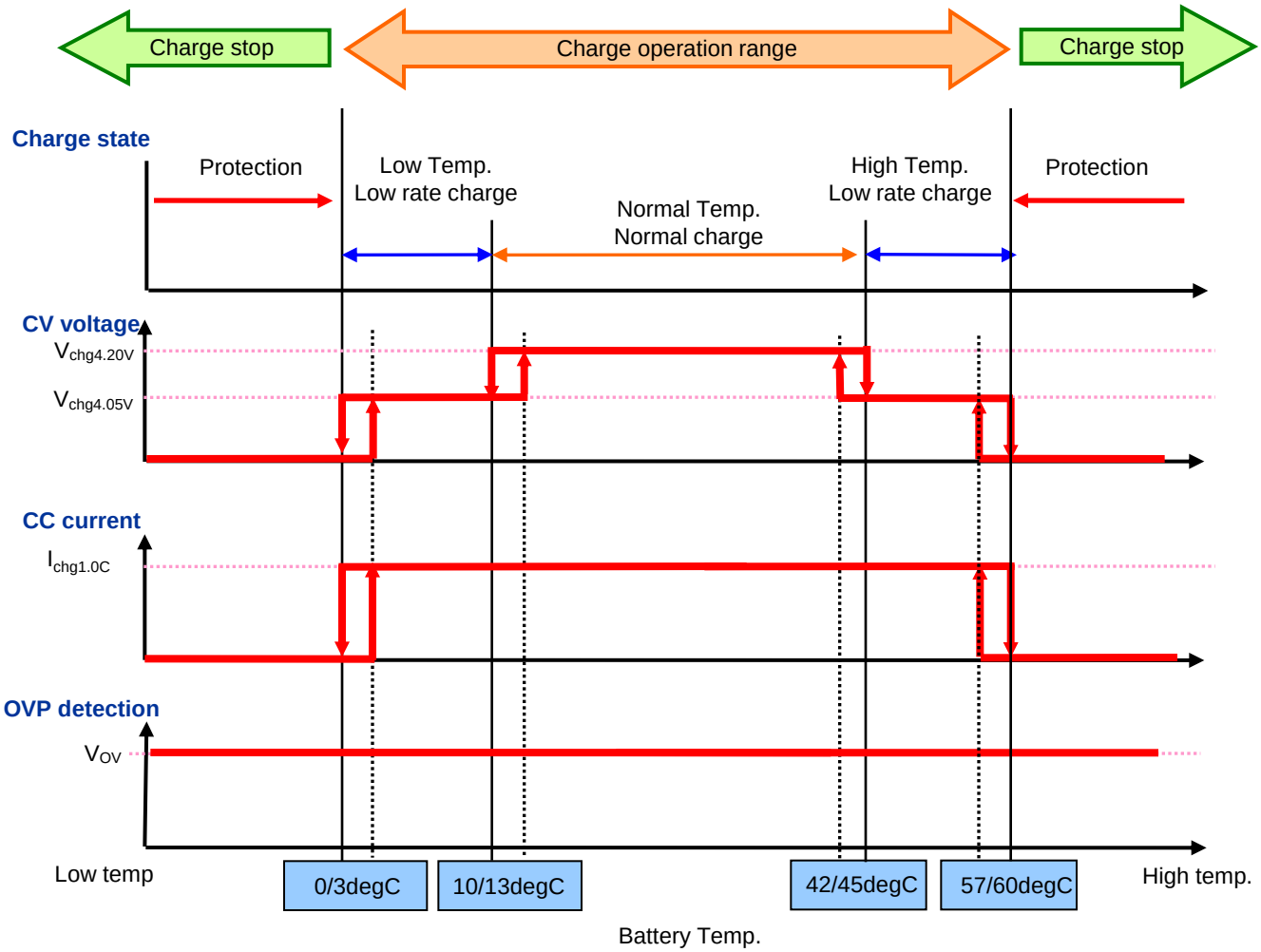


Note:
During quick charge, junction temperature is monitored to limit charge current value between 0.2C-1.0C so that the junction temperature may not exceed Ttreg.

Function description

Battery temperature detection

IC controls CV voltage according to built-in charge profile by detecting battery temperature via thermistor I/F.



There is the delay time(64ms x 4times) for preventing erroneous detection before judging the battery temperature.

When PSE control (ADR=02H) is 'Enable' setting, the charge control voltage changes as the above chart according to JEITA guide line. But when VCHG setting (ADR=00H) is 4.00V, the charge control voltage at low rate charge is also 4.00V.
When PSE control (ADR=02H) is 'Disable' setting, the charge control voltage depends on the VCHG setting (ADR=00H). When THBATCON (ADR=02H) is 'Enable' setting, the battery connection is detected with battery voltage or TH voltage. For details, please read 'Battery connection detection'.
When thermistor is not used, please connect TH terminal with THVDD terminal and set 'PSE control (ADR=02H)' to 'Disable'.

Resister value for thermistor

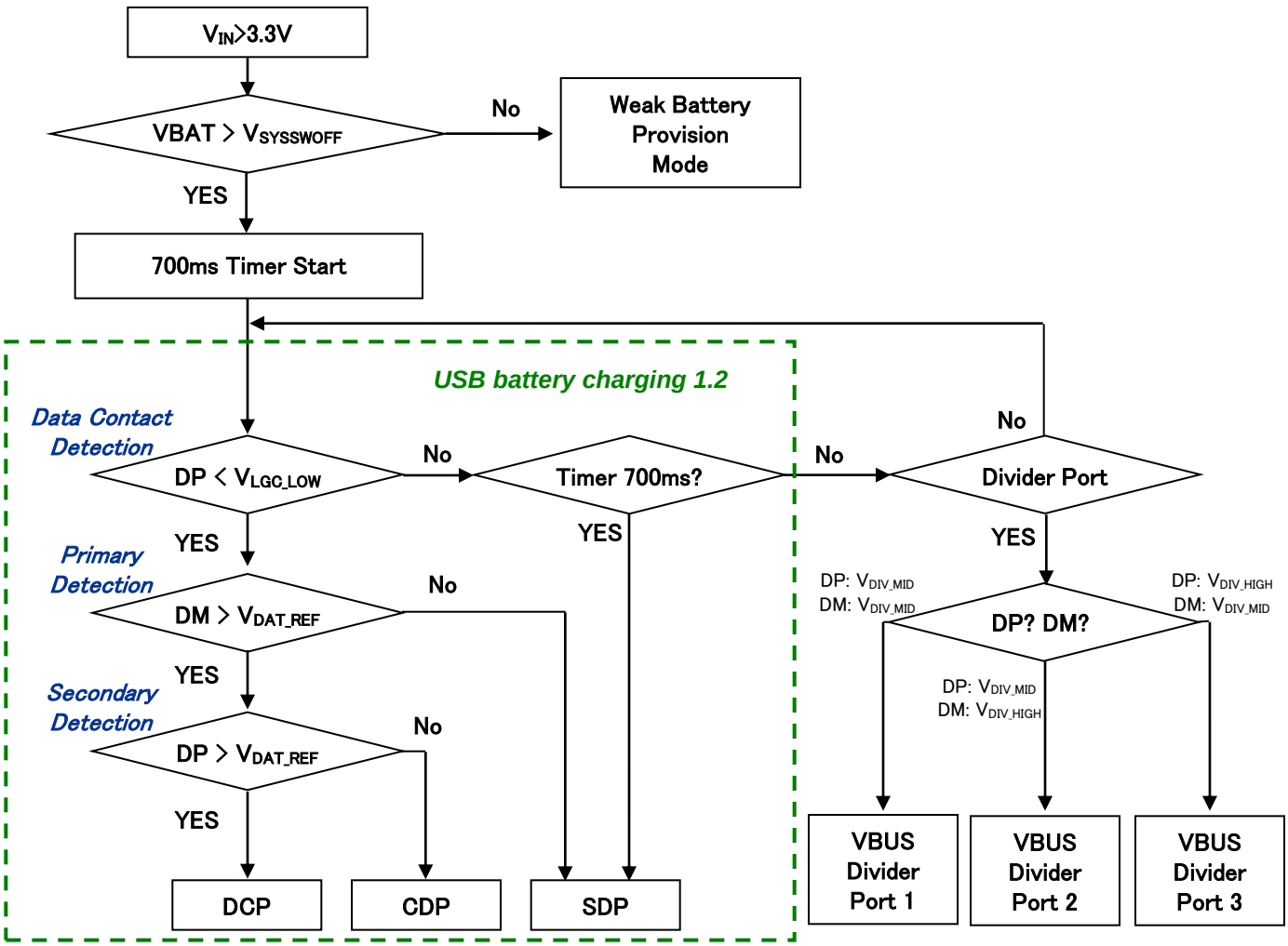
TEMP. (deg.C)	R (Kohm)
2.5	311.6
5.0	272.5
12.5	184.5
15.0	162.7

TEMP. (deg.C)	R (Kohm)
40.0	50.7
42.5	45.5
55.0	27.1
57.5	24.5

* : NCP15WF104F03RC (Murata)

USB charging port detection

[USB charging port detection flow chart]



Function description

・ Input current limit is automatically set after the detection.

NO.	Port	Current limit (mA)
1	SDP(Standard Downstream Port)	100 or 500 *1
2	CDP(Charging Downstream Port)	1500
3	DCP(Dedicated Charging Port)	1500
4	VBUS Divided Port 1	500
5	VBUS Divided Port 2	1000
6	VBUS Divided Port 3	2100

*1 It depends on CTL terminal setting

CTL	SDP Current limit (mA)
Low	100
High	500

・The detection result is stored to the registers.

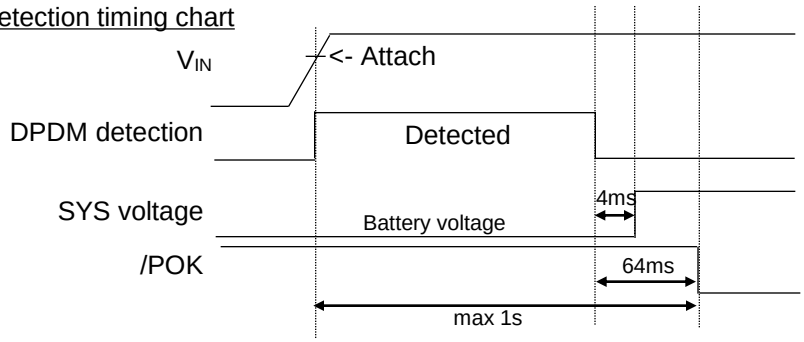
04H DP DM register (Read only)

Bit5	Bit4	Bit3	DP/DM
0	0	0	SDP(Standard Downstream Port)
0	0	1	CDP(Charging Downstream Port)
0	1	0	DCP(Dedicated Charging Port)
0	1	1	DP Port Error(DP < 3V)
1	0	0	VBUS Divided Port 1
1	0	1	VBUS Divided Port 2
1	1	0	VBUS Divided Port 3
1	1	1	DM Port Error(DM < 3V)

・VBUS Divided Port is detected by the input voltage of DP,DM.

Port	DP (V)	DM (V)	Current limit (mA)
VBUS Divided Port 1	2.00	2.00	500
VBUS Divided Port 2	2.00	2.68	1000
VBUS Divided Port 3	2.68	2.00	2100

DPDM detection timing chart



DP and DM terminal become Hi-Z (open) after USB detection.

Function description

Dead Battery Provision (DBP)

When VBAT < Vsysswoff_set (low battery detection voltage), the beaviors for each USB port are as follows:

< SDP (Standard Downstream Port) >
- SG terminal is 'H'.
- Trickle charge or quick charge starts.
- DP terminal outputs VDP_SRC (Typ. 0.6V)
- When Tweak (Typ. 40 min) pasts and VBAT is still lower than Vsysswoff, this IC shifts suspend mode. Tweak timer can be stopped by changing 'Timer control (ADR=01H)' setting to 'Reset' or 'Count Stop'. Changing the input current limit setting also prevents suspend mode from starting.
- When VBAT > Vsysswon (Vsysswoff + Vsysswoff_hys) , the USB detection is done.
- DP and DM terminals become Hi-Z (open) after USB detection.

< CDP (Charging Downstream Port), DCP (Dedicated charging Port)>
- SG terminal is 'H'.
- Trickle charge or quick charge starts.
- DP terminal outputs VDP_SRC (Typ. 0.6V)
- Tweak timer (Typ. 40 min) doesn't count up. But the each charging timer (trickle or quick charge timer) counts up.
- When VBAT > Vsysswon (Vsysswoff + Vsysswoff_hys), IC stops VDP_SRC output, and then it carries out "Secondary Detection".
- DP and DM terminals become Hi-Z (open) after USB detection.
- DPDM detection register (ADR=05H) indicates "SDP" during USB detection (including DBP).

< Divided port 1, 2, 3>
- SG terminal is 'H'.
- Trickle charge or quick charge starts.
- DP and DM terminals become Hi-Z (open) after USB detection.

SGREF terminal setup

The low battery detection voltage (Vsysswoff) is used for the following.
- Detection weak batteyr after 'Forced charge (04H)'
- On/off function for MOSFET for System load SW'

SGREF terminal voltage (VSGREF) can set the low battery detection voltage(Vsysswoff).

[SGREF detection voltage (Typ. 1.8V) < VSGREF]
- The internal setting is selected.
  Vstsswoff = Vsysswoff_in (Typ. 3.3V) , Hysteresis voltage = Vsyssw_in_hys (Typ. 300mV)

We recommend SGREF connected with THVDD when using internal setting.

[VSGREF = GND]
- Low battery detection doesn't operate.
  Please connect SGREF with GND when not use this function.

Function description

Gate control for system Load SW (/SG)

This function controls '/SG' terminal.
'/SG' terminal is connected with LoadSW (recommended Renesas AT1069C) between SYS terminal and SYSTEM, and controls power supply to SYSTEM ON/OFF.
And '/SG' terminal can be used for the control of USB SW because this terminal becomes 'H' (OFF) during USB detection.

1. '/SG' = 'H' ('OFF') during USB detection.

2. This function can be selected for 'Enable' or 'Disable' by SGCTL (ADR=02H).

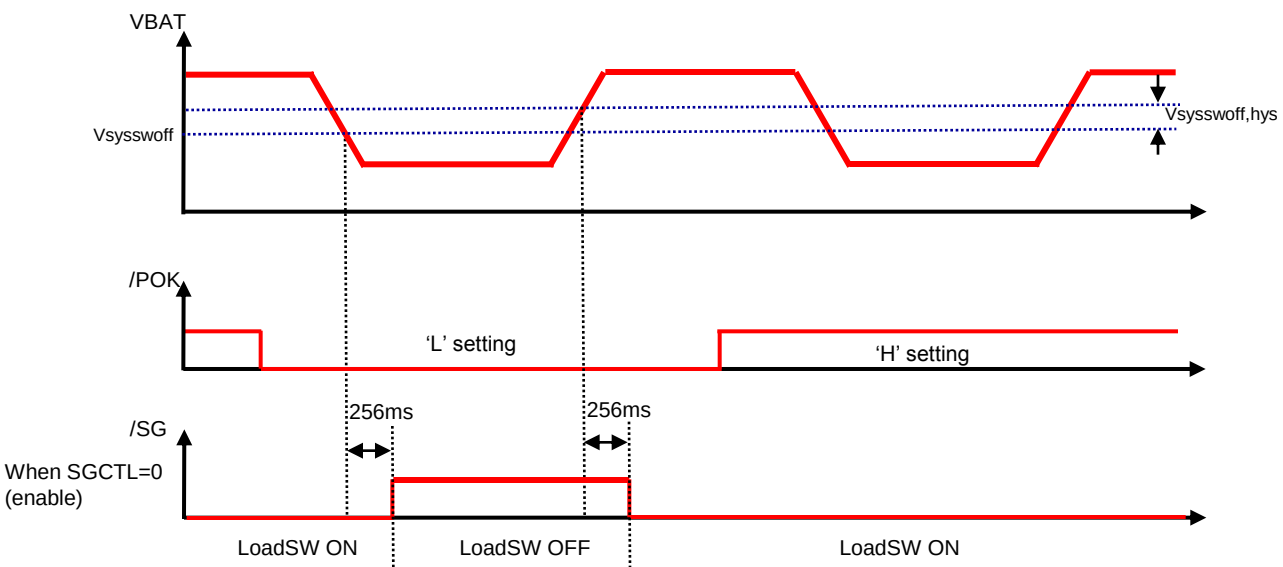
3. When the battery voltage is low and IC is charging it, all current can be used for charging by stopping current supply for SYSTEM with LoadSW off. (After USB detection & SGCTL: Enable)

[/SG control in each condition about IN and BAT (Except for USB detection and SGCTL: Disable)]

(1) IN : connect , BAT : connect
IC is charging weak battery (VBAT < VSYSSWOFF) OFF ('H')
else ON ('L')
(2) IN : connect , BAT : non-connect ON ('L')
(3) IN : non-connect , BAT : connect ON ('L')
(4) IN : non-connect , BAT : non-connect IC and SYSTEM are not operated

Charging OPEN battery is regarded as ' the function during USB detection' and '/SG' is 'H'(OFF).

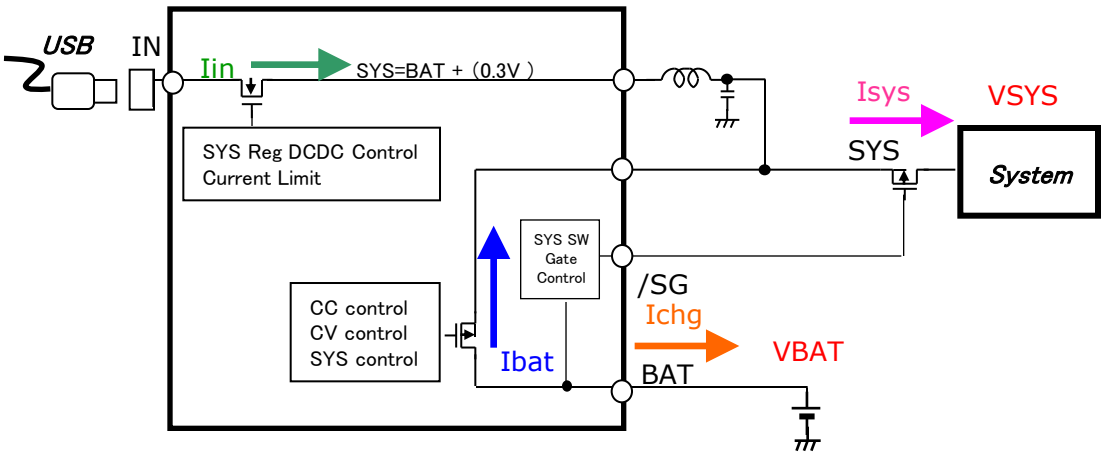
Timing of /SG output



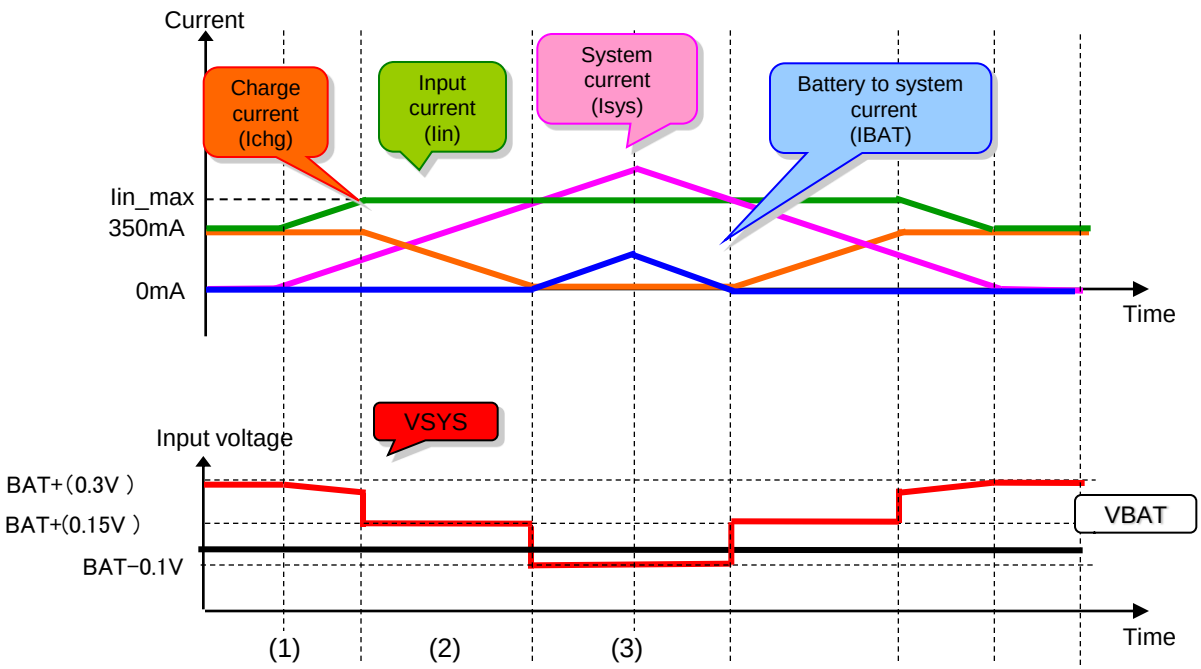
Function description

Input current limitation / Control between SYS and BAT

- USB detection (USB battery charging 1.2)
- Input current limitation(100mA/500mA/1000mA/1500mA/2100mA/limitless/Suspend) can be set by I2C.
-The current limit is dropped for protection as the list when SYS is shorted.
-When the total sum of the charge current and the system current is under the input limit current,
-IC switches the system power supply and the battery charge seamlessly within input current limitation.



Example of power control between the system supply and the battery charge
Conditions : IN=5.0V is connected, Iin_max=500mA, Ichg=350mA, Chargeable battery is connected



(1) IC charges the battery at Ichg=350mA and supplies the system current(Isys) within Iin_max=500mA.

(2) When the system current(Isys) increases and the total sum of Isys and Ichg reaches Iin_max, IC reduces the charge current. (the power not used by the system charges the battery)

(3) When the system current (Isys) increases more and Isys exceeds Iin_max, VSYS falls to Vbat-V_{SYSR} and the battery supplies the load current to system through the Path SW. (IC attempts to sustain the system voltage no matter what causes it to drop.)

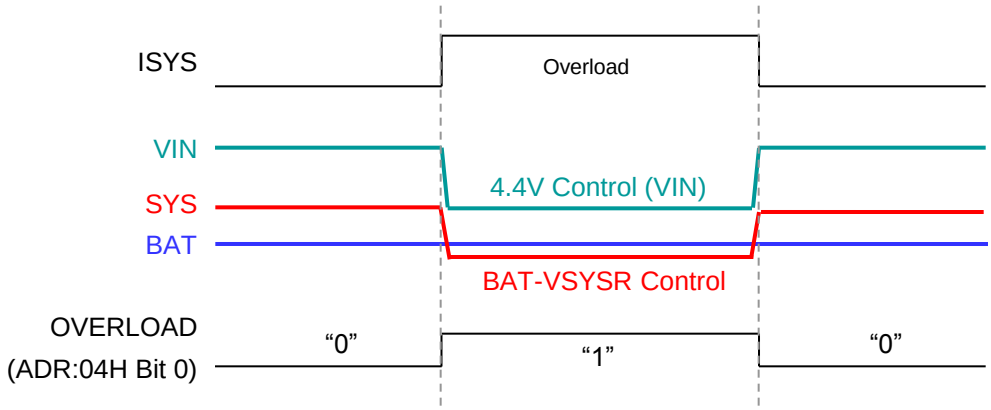
Function description

Over load detection

When IN voltage drops below 4.4V, the input current is controlled as the current at the time regardless of the current limit setting.
The OVERLOAD register (ADR:04H Bit 0) indicate “1”, only when 1500mA or 2100mA input current limitation is selected by DP/DM detection. (not including CTL3 setting)

This IC detects lack of current capability of power supply and prevents exceeded current from flowing into IN terminal.

Operation of Over load detection

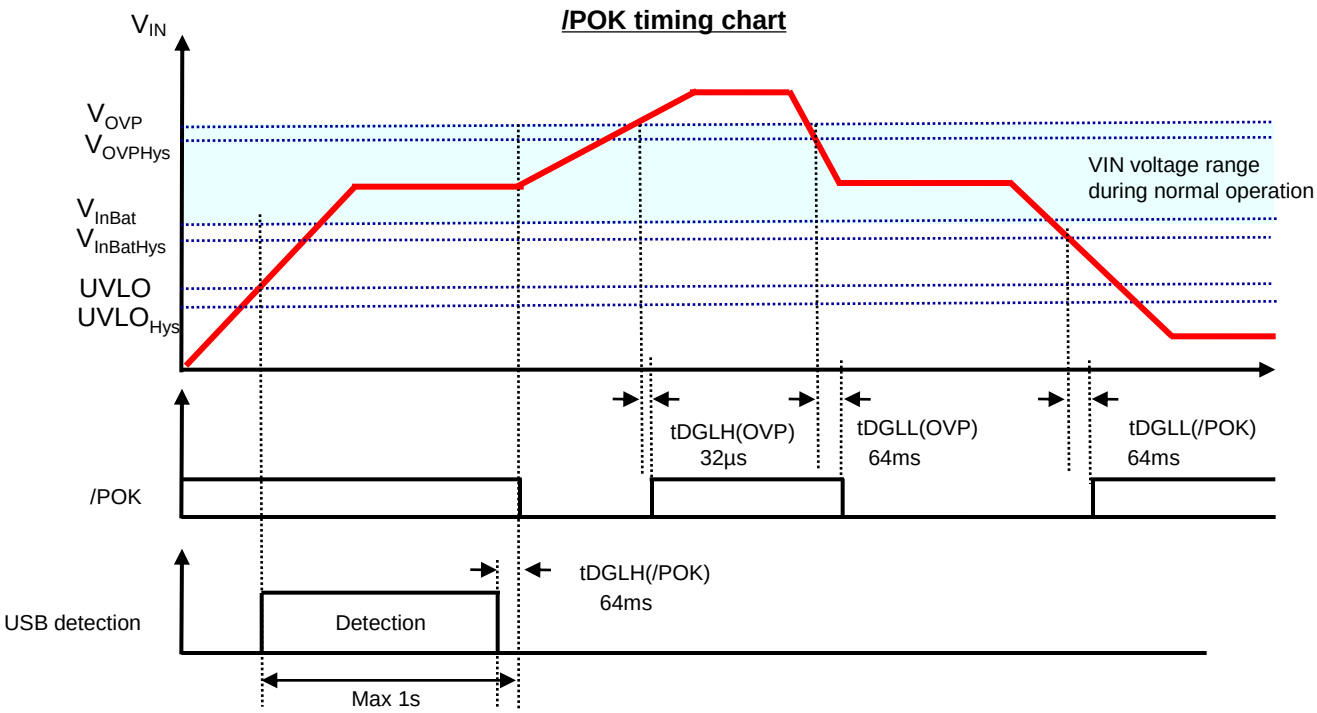


Input voltage detection

$V_{UVLO} \leq V_{IN} \leq V_{OVP}$ and $V_{IN} \geq V_{BAT}+V_{InBat}$: Power supply from IN to SYS and charging are available. /POK =L.

$V_{OVP} \leq V_{IN}$ or USB suspend mode : Power supply from IN to SYS and charging are not available. /POK=H.

/POK timing chart



Battery connection detection

Battery connection detection method is selectable by THBATCON register setting. (ADR:02H)

-THBATCON=0 : Battery is detected by thermistor. (higher than -21.5 deg C.)
-THBATCON=1 : Battery is detected by its voltage. (VBAT > 1.5V)

Combination of THBATCON and PSE register setting.

		PSE		note
		0	1	
THBATCON	0	Condition A	Banned	
	1	Condition B	Condition C	

[Condition A]
IC detects battery connection by thermistor, and charges battery with internal temperature profile.

[Condition B]
IC detects battery connection by voltage, and charges battery with internal temperature profile.

[Condition C]
IC detects battery connection by voltage, and charges battery without internal temperature profile.

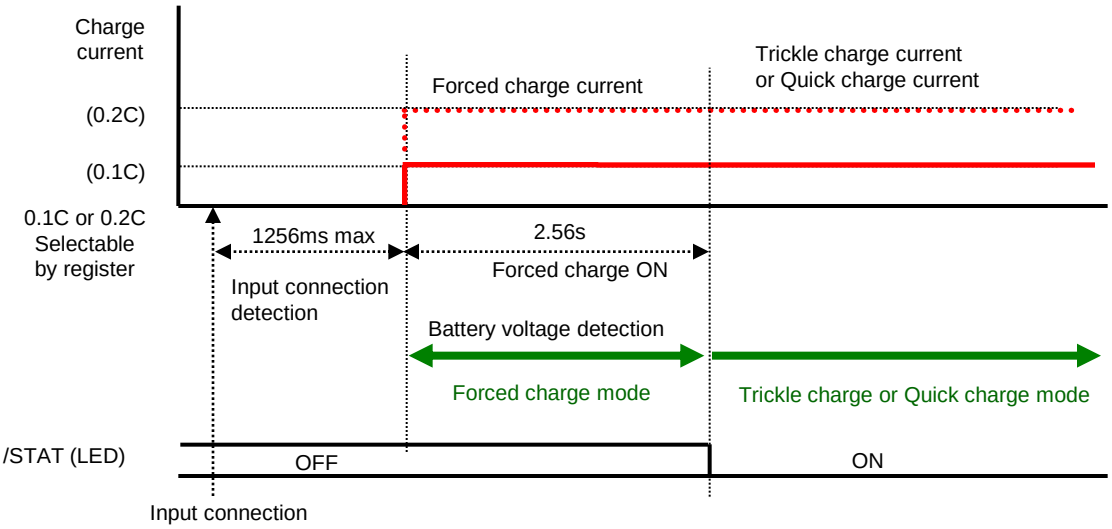
[Banned]
Do not use this setting.

Function description

Forced charge

After input power detection, forced charge starts for canceling the cutoff state of battery due to over-discharge. The forced charged current is same as the trickle charge current setting. Register (ADR=00H Bit6) is available for changing setting.
Charging starts for opened battery or low battery ($V_{BAT} < V_{start}$) by this function.
Please refer to Battery connection detection.

Timing from input detection to charge start



Trickle charge (0.1C constant current charge)

After input detection and battery detection, trickle charge is started when VBAT < $V_{qcchgon}$ (Typ. 3.0V).
- When detecting VBAT ≥ $V_{qcchgon}$, the state moves to quick charge mode.
- Trickle charge timer starts simultaneously with trickle charge starts.
- After trickle charge timer expires, the state moves to charge error mode 1 if VBAT < $V_{qcchgon}$.
- When detecting VBAT ≥ V_{ov} (Typ. 4.35V), the state moves to charge error mode 1.

Trickle charge setting is selectable by register (ADR=00H Bit4,5).

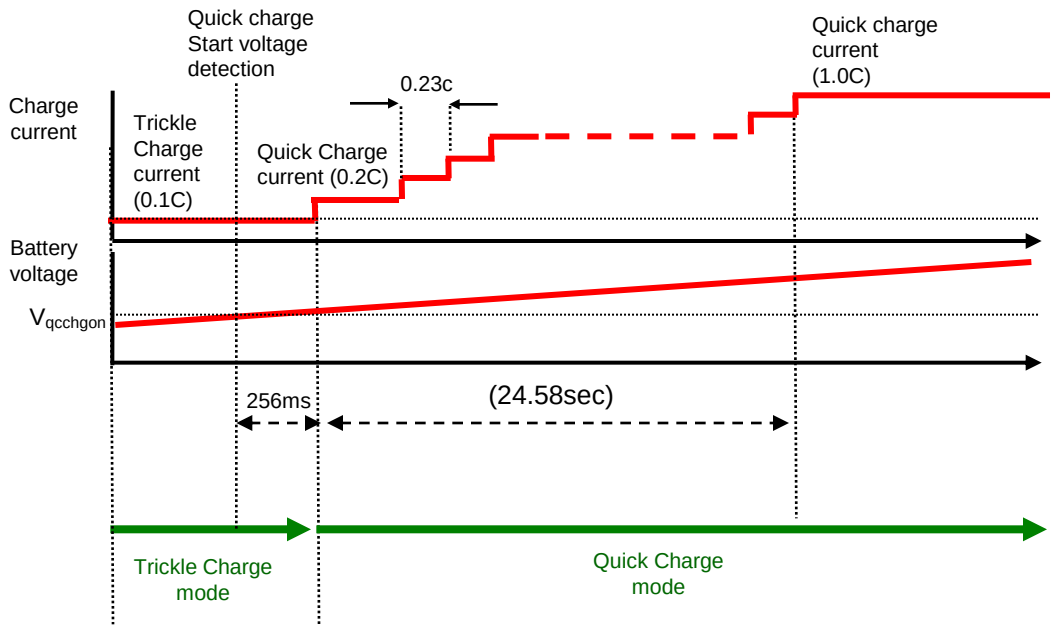
Quick charge (1.0C constant current charge)

Quick charge is started after detecting VBAT ≥ $V_{qcchgon}$.
- When detecting VBAT=Vchg, the state moves to CV (constant voltage) charge mode.
- Quick charge timer starts simultaneously with quick charge starts.
- When detecting VBAT < (V_{chgon} – hysteresis voltage) (Typ. 2.9V) , the state moves to trickle charge mode.
- When detecting VBAT ≥ V_{ov} (Typ. 4.35V), , the state moves to charge error mode 1.

During quick charge, this IC monitors junction temperature and control the current between 0.2C and 1.0C not to exceed T_{treg}.
The quick charge current is selectable by register (ADR=00H Bit 0)

Function description

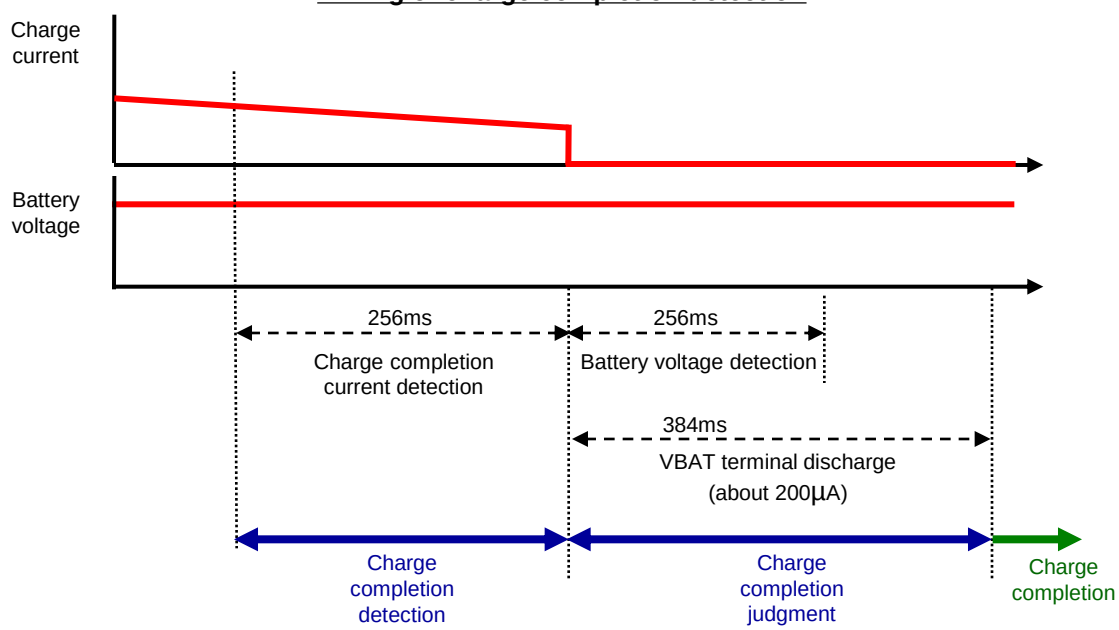
Timing to Quick charge(1.0C)



Constant voltage charge

When detecting VBAT=Charge Control voltage under quick charge, constant voltage charge is started.
- When the charge current falls to charge completion current or less under constant voltage charge, the state moves to charge completion detection mode. If VBAT≥V_{rechg} (Typ. 3.8V), the state moves to charge completion state.
- When V_{start} ≤ VBAT < V_{rechg}, the state moves to error mode.
- When VBAT < V_{start}, the state moves to Battery non-connection mode.
- The state movement is judged 384ms after charge completion current detection.
- The charge control voltage is selectable by register (ADR=00H Bit 1,2,3)

Timing of charge completion detection

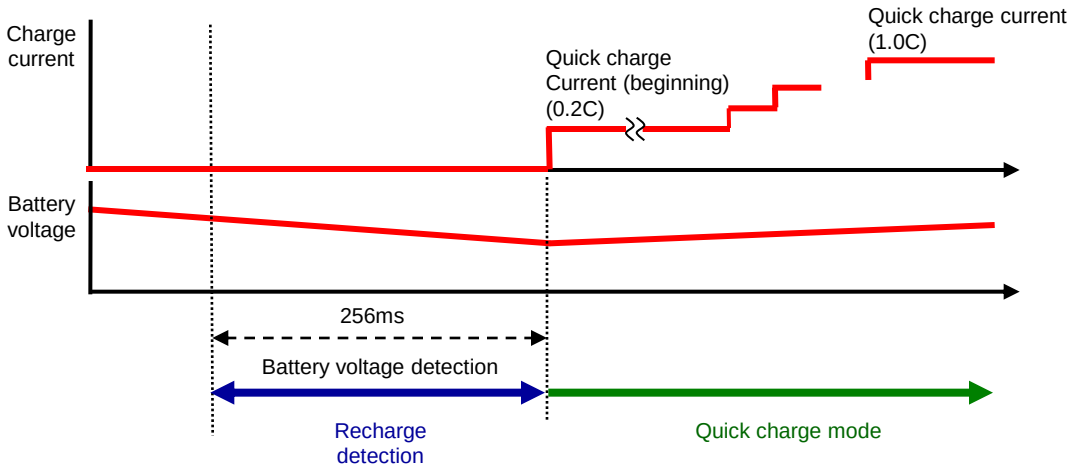


Function description

Recharge function

After charge completion, battery voltage continues to be monitored.
When VBAT < V_{rechg}, recharge is started.
Quick charge timer also starts to operate simultaneously with recharge start.

Timing of recharge judgment



/STAT Terminal functions

/STAT terminal function is switchable by INTR register setting (ADR:02H).

INTR=0: /STAT terminal is LED driver which is controlled according to below table.

Mode	LED	Blink cycle	Note
USB non-connection	OFF	–	
USB detection	OFF	–	
Standby	OFF	–	
Battery non-connection	OFF	–	
Forced charge	OFF	–	
Trickle charge	ON	–	
Quick charge-1	ON	–	
Quick charge-2	ON	–	
Quick charge-3	ON	–	
Completion detection	OFF	–	
Completion	OFF	–	
Error 1	Blink1	128ms	ON DUTY 50%
Error 2	Blink2	1024ms	ON DUTY 50%

INTR=1: /STAT terminal become "Low" when 06H register value are changed. (Interrupt function)
By reading 06H register, /STAT terminal become "High".

Function description

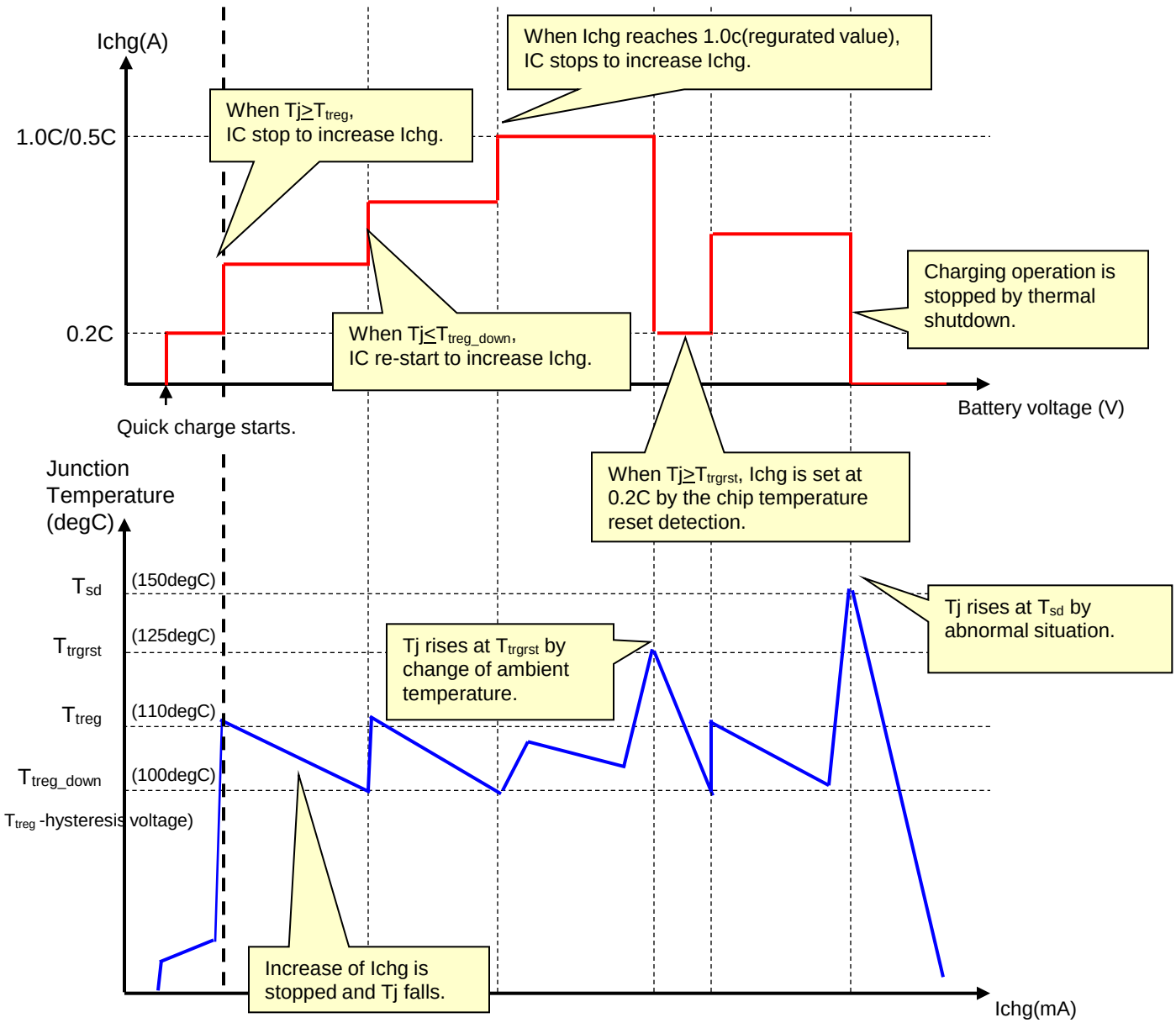
Chip temperature detection

During quick charge, junction temperature is monitored to limit charge current between 0.2C to 1.0C so that junction temperature may not exceed Ttreg.

Thermal shutdown

When junction temperature reaches Tsd(default: 150degC) under charge, IC stops to supply from IN to SYS and the state moves to error mode.

Chip temperature detection and Thermal shutdown



Register Map

•Register Map

☒ : Unassigned bits are always 0.

ADRESS		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	R/W	THM100K	TRICKLE	FC		VCHG			ICHG
01H	R/W	USBMD	TIMER			CTL3			/CEN2
02H	R/W		RST_USBDET	INTR	THBATCON	SGCTL	FULMD	RECHG	PSE
03H	R/W		IOCP			ICHG_1C			
04H	R	GDBAT	VBATH	NOBAT	FULL	TOUT	TSD	POK	OVERLOAD
05H	R	TOUT_WKB	TOUT_DCD	DP DM		TEMP			
06H	R					STAT3	STAT2	STAT1	STAT0

•04H About State Register (Read only)

	0	1
OVERLOAD	Not overload	Overload
POK	Not detect VIN	Detect VIN
TSD	Junction TEMP is normal	Thermal shut down
TOUT	Within the time limit	Time out (Stop charger IC)
FULL	Not fully charged battery	Fully charged battery
NOBAT	Battery detected	No battery
VBATH	Battery voltage normal	Battery voltage is over detection
GDBAT	Weak Battery	Good Battery

When charge stop, FULL=0 and TOUT=0.
When USB suspend, TOUT=0, FULL=0, VBATH=0 and NOBAT=1.

•04H About Temp Register (Read only)

Bit2	Bit1	Bit0	TEMP
0	0	0	TEMP protection works (low)
0	0	1	Low rate charge current (low)
0	1	0	Normal charge
0	1	1	Low rate charge current (High)
1	0	0	TEMP protection works (High)
1	0	1	No thermistor

•05H About DPDM Register (Read only)

Bit5	Bit4	Bit3	Detected port type by DP/DM
0	0	0	SDP（Standard Downstream Port）
0	0	1	CDP（Charging Downstream Port）
0	1	0	DCP（Dedicated Charging Port）
0	1	1	DP Port Error (DP < 3V)
1	0	0	VBUS Divided Port 1
1	0	1	VBUS Divided Port 2
1	1	0	VBUS Divided Port 3
1	1	1	DM Port Error (DM < 3V)

Bit6	DCD Timer
TOUT_DCD	Time out

Bit7	DBP Timer
TOUT_WKB	Time out

Register Map

•06H About Charge state Register (Read only)

Bit3	Bit2	Bit1	Bit0	MODE
0	0	0	0	USB non-connection
0	0	0	1	USB detection
0	0	1	0	Standby
0	0	1	1	Battery non-connection
0	1	0	0	Forced charge
0	1	0	1	Trickle charge
0	1	1	0	Quick charge-1
0	1	1	1	Quick charge-2
1	0	0	0	Quick charge-3
1	0	0	1	Completion detection
1	0	1	0	Completion
1	0	1	1	Error 1
1	1	0	0	Error 2

■ADDRESS 00H Register **☆Default setting**

Quick charge current		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ICHG	0.5C	—	—	—	—	—	—	—	0
	1.0C☆	—	—	—	—	—	—	—	1

Charge voltage		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCHG	4.00V	—	—	—	—	0	0	0	—
	4.05V	—	—	—	—	0	0	1	—
	4.10V	—	—	—	—	0	1	0	—
	4.15V	—	—	—	—	0	1	1	—
	4.20V☆	—	—	—	—	1	0	0	—
	4.35V	—	—	—	—	1	0	1	—

Charge completion current		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FC	0.05C	—	—	0	0	—	—	—	—
	0.1C☆	—	—	0	1	—	—	—	—
	0.2C	—	—	1	0	—	—	—	—

Trickle charge current		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TRICKLE	**0.1C☆**	—	0	—	—	—	—	—	—
	0.2C	—	1	—	—	—	—	—	—

Thermistor resistance		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH100K	**10kΩ☆**	0	—	—	—	—	—	—	—
	100kΩ	1	—	—	—	—	—	—	—

Register Map

■**ADDRESS 01H Register** ☆ **Default setting**

Charge control *1		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
/CEN2	**Enable☆**	–	–	–	–	–	–	–	0
	Disable	–	–	–	–	–	–	–	1

Input current limitation		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTL3	**100mA☆**	–	–	–	–	0	0	0	–
	500mA	–	–	–	–	0	0	1	–
	1000mA	–	–	–	–	0	1	0	–
	1500mA	–	–	–	–	0	1	1	–
	2100mA	–	–	–	–	1	0	0	–
	Limitless	–	–	–	–	1	0	1	–
	USB SUSPEND	–	–	–	–	1	1	1	–

Timer		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TIMER	Disable (no effect) ***6***	–	0	0	0	–	–	–	–
	Enable (normal) ☆	–	0	0	1	–	–	–	–
	Enable (slow mode x2) ***3***	–	0	1	0	–	–	–	–
	Enable (slow mode x3) ***4***	–	0	1	1	–	–	–	–
	Enable (slow mode x4) ***5***	–	1	0	0	–	–	–	–
	Enable (count stop) ***6***	–	1	1	1	–	–	–	–

USB control select *2		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBMD	**Depend on Terminal☆**	0	–	–	–	–	–	–	–
	Depend on Registor	1	–	–	–	–	–	–	–

*1 When /CEN=L and CEN2 (register) ="0", Charge operation is enable.

Truth Table about /CEN and /CEN2

/CEN	/CEN2	IC
Low	0	can start charging.
Low	1	stops charging.
High	0	
High	1	

*2 When USBMD=0, Terminal setting (DP, DM, CTL and USUP) is valid.
When USBMD=1, Register (CTL3) is valid.

*3 Slow: 2 times of normal mode
(Trickle charge timer=120min., Quick charge timer=600min., Weak battery timer = 80min.)
*4 Slow: 3 times of normal mode
(Trickle charge timer=180min., Quick charge timer=900min., Weak battery timer = 120min.)
*5 Slow: 4 times of normal mode
(Trickle charge timer=240min., Quick charge timer=1200min., Weak battery timer = 160min.)

*6 Disable: Timers will not expire. (count values are reset to 0)
Count stop: Timers stop counting. (count values are kept)

Register Map

■**ADDRESS 02H Register** ☆**Default setting**

PSE Control		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSE	**Enable ☆**	–	–	–	–	–	–	–	0
	Disable	–	–	–	–	–	–	–	1

Recharge control		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RECHG	**Enable ☆**	–	–	–	–	–	–	0	–
	Disable	–	–	–	–	–	–	1	–

Operation after charge completion		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FULMD	**Stop charge ☆**	–	–	–	–	–	0	–	–
	Continue to charge (inform FULL)	–	–	–	–	–	1	–	–

/SG control		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SGCTL	**Enable☆**	–	–	–	–	0	–	–	–
	Disable	–	–	–	–	1	–	–	–

Battery-connection detection by		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
THBATCON	**Thermistor ☆**	–	–	–	0	–	–	–	–
	Battery voltage	–	–	–	1	–	–	–	–

/STAT terminal function *7		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTR	**LED driver ☆**	–	–	0	–	–	–	–	–
	Interrrupt signal	–	–	1	–	–	–	–	–

USB re-detection *8		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RST_USBDET	**USB (DP/DM) detect ☆**	–	0	–	–	–	–	–	–
	Reset USB (DP/DM) detect	–	1	–	–	–	–	–	–

*7 When INTR=0, /STAT terminal function is
When INTR=1, /STAT terminal function is intterrupt.

*8 When RST_USB=1, the D+D- detecting is in reset.
In this case, /SG terminal is “L”.
When RST_USB=0, the D+D- detecting will restart.
During the D+D- detection, /SG is “H”.
After D+D- detection, /SG output is decided by the SG function.

Register Map

■**ADDRESS 03H Registor** ☆**Default setting**

Charging current *9		Bit7	Bit6	Bit5	Bit4	Bit3	Bit3	Bit2	Bit0
ICHG_1C	400mA	–	–	–	–	0	0	0	0
	500mA ☆	–	–	–	–	0	0	0	1
	600mA	–	–	–	–	0	0	1	0
	700mA	–	–	–	–	0	0	1	1
	850mA	–	–	–	–	0	1	0	0
	1000mA	–	–	–	–	0	1	0	1
	1200mA	–	–	–	–	0	1	1	0
	1500mA	–	–	–	–	0	1	1	1
	1800mA	–	–	–	–	1	0	0	0
	2000mA	–	–	–	–	1	0	0	1

DCDC over current protection *10		Bit7	Bit6	Bit5	Bit4	Bit3	Bit3	Bit2	Bit0
IOCP	**Limitless ☆**	–	0	0	0	–	–	–	–
	1000mA	–	0	0	1	–	–	–	–
	2000mA	–	0	1	0	–	–	–	–
	3000mA	–	0	1	1	–	–	–	–
	4000mA	–	1	0	0	–	–	–	–

*9 Recommended operating inductance condition

Quick charge current Under **1000mA**	**Murata : LQM2HPN2R2MGO** **2.2uH、1300mA**

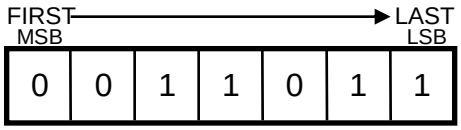
*10 If input current limitation < IOCP, IN current is limited by it.

I²C BUS Line Characteristics

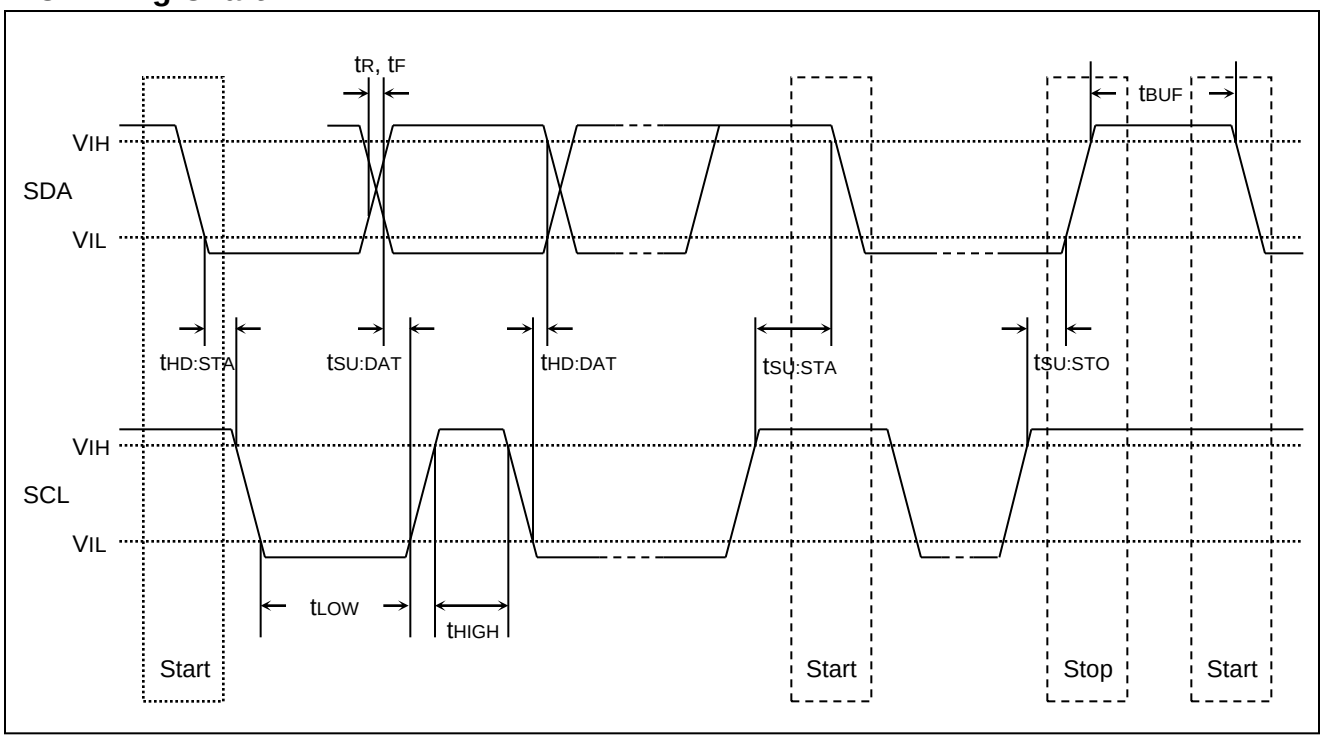
ItemA	Symbol	Min.	Max.	Unit
SCL clock frequency	fSCL	0	400	kHz
Bus free time between STOP condition and START condition	tBUF	1.3	-	µs
START condition hold time (After this period, the first clock pulse is generated)	tHD:STA	0.6	-	µs
SCL low period	tLOW	1.3	-	µs
SCL high period	tHIGH	0.6	-	µs
START condition setup time	tSU:STA	0.6	-	µs
Data hold time	tHD:DAT	0.1	0.9	µs
Data setup time	tSU:DAT	100	-	ns
Rise time (SDA and SCL)	tR	-	300	ns
Fall time (SDA and SCL)	tF	-	300	ns
STOP condition setup time	tSU:STO	0.6	-	µs
Bus line capacitive load	Cb	-	400	pF

Note : Above values are specified by V_{IH}min and V_{IL}max.

■Slave address



I2C Timing Chart

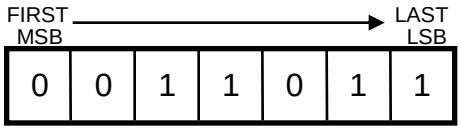


Serial communication format

1. Start condition

Set SDA from High to Low when SCL=High.

2. Slave address:



3. Stop condition

Set SDA from Low to High when SCL=High.

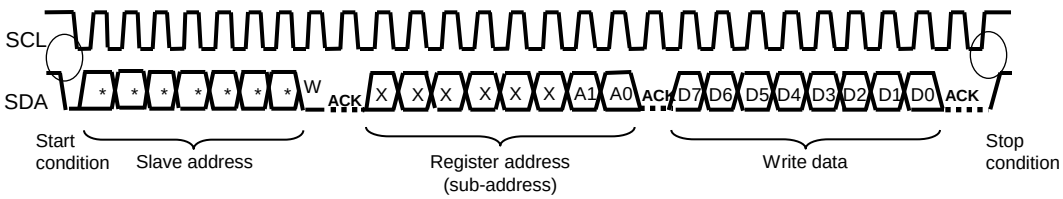
4. Read/Write code

Write code : SDA=Low
Read code : SDA=High

5. Write mode :Data input from Master to R2A20057BM

When Master inputs Slave address(8bit) and Write code after start condition, R2A20057BM responds with an Acknowledge"0".
And then, when Master inputs Register address(8bit), R2A20057BM responds with an Acknowledge"0".
And then, when Master inputs Write data(8bit), R2A20057BM responds with an Acknowledge"0".
Lastly, Master input Stop condition.

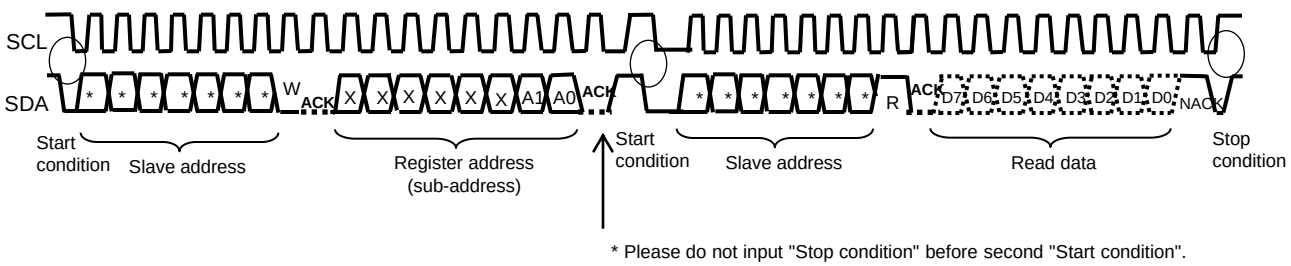
(Solid line: From Master to R2A20057BM, Dotted line: From R2A20057BM to Master)



6. Read mode :Data output from R2A20057BM to Master

When Master inputs Slave address(8bit) and Write code after start condition, R2A20057BM responds with an Acknowledge"0".
And then, when Master inputs Register address(8bit), R2A20057BM responds with an Acknowledge"0".
And then, when Master inputs Start condition, Slave address, and Read code, R2A20057BM responds with an Acknowledge"0" and outputs Read data.
Lastly, Master inputs Acknowledge"1"(or opens bus line) and Stop condition.

(Solid line: From Master to R2A20057BM, Dotted line: From R2A20057BM to Master)



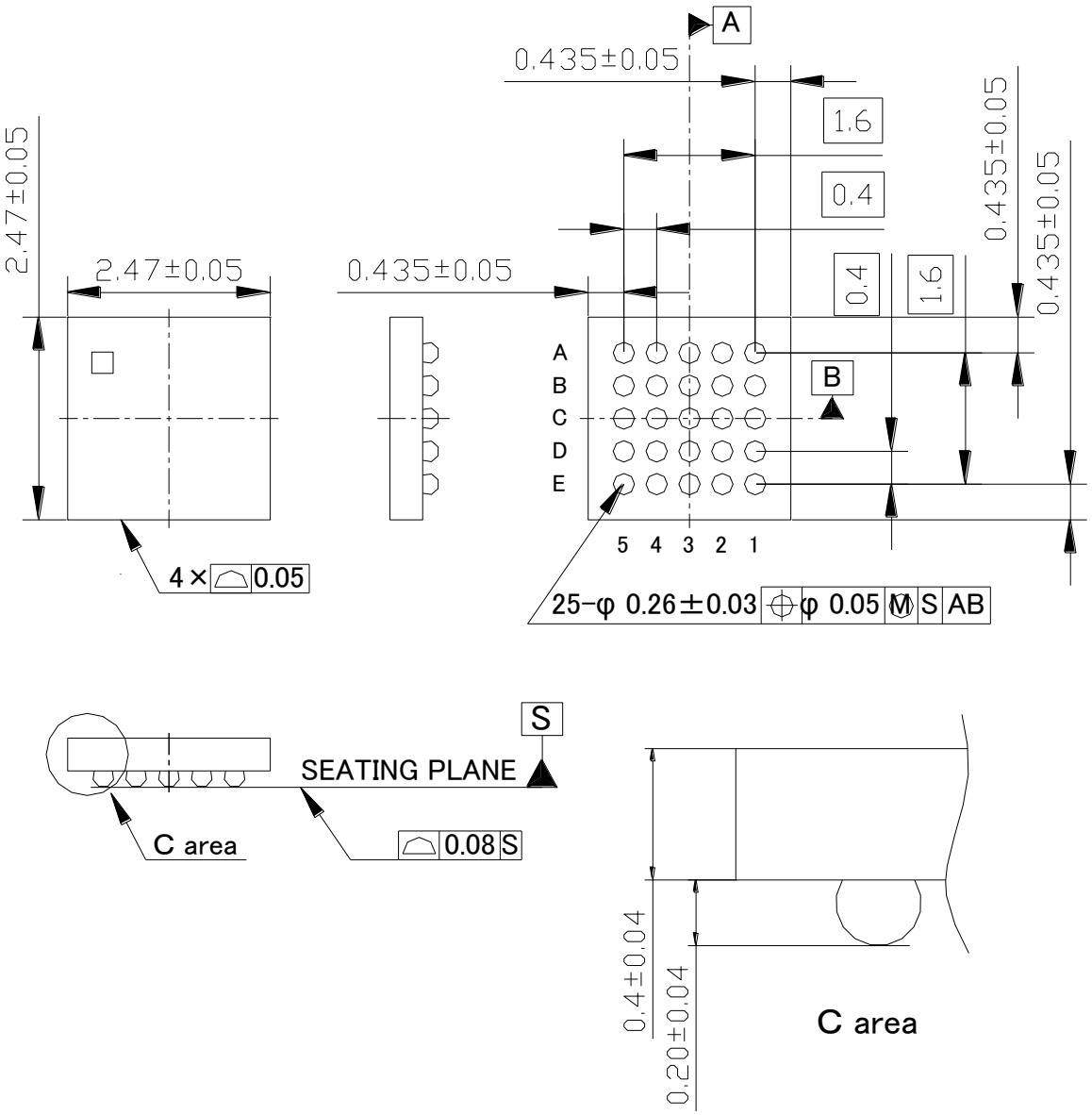
* Please do not input "Stop condition" before second "Start condition".

Lineup

No.	Item	Condition	備考
1	Charge control voltage	VCHG=4.20V	
		VCHG=4.35V	
2	Thermistor	10kΩ	TH05-3H103F (MITSUBISHI MATERIALS)
		100kΩ	NCP15WF104F03RC(MURATA)
3	I2C Slave Adrress	0011011	
		1011011	

Package dimmensions

Unit : mm



Revision History

Rev	発行日	Description	
		Page	Summary
0.50	Dec 10, 2012	—	First Edition issued
1.00	Mar 1, 2013	P4	About IN terminal effective Cap value