Low Cost 24V SLIC For PABX/Key Systems

The Intersil HC5503 low cost SLIC is optimized for use in small Analog or mixed Analog and Digital Key Telephone Systems (KTS) or PBX products. The low component count solution and surface mount package options, enable a small desktop Key System/PBX product to be achieved. The internal power dissipation of the end product is minimized by the low power consumption and minimal power supply voltage requirements of the HC5503.

The HC5503 integrated solution provides higher quality, higher reliability and better performance solution than a transformer, thick film hybrid or discrete analog subscriber interface design.

The HC5503 is designed in a Dielectrically isolated bipolar technology and is inherently latch proof and does not require hot plug or power supply sequencing precautions.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HC5503CB	0 to 75	24 Ld SOIC	M24.3
HC5503CBZ (Note)	0 to 75	24 Ld SOIC (Pb-free)	M24.3
HC5503CBZ96 (Note)	0 to 75	24 Ld SOIC (Pb-free)	M24.3

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

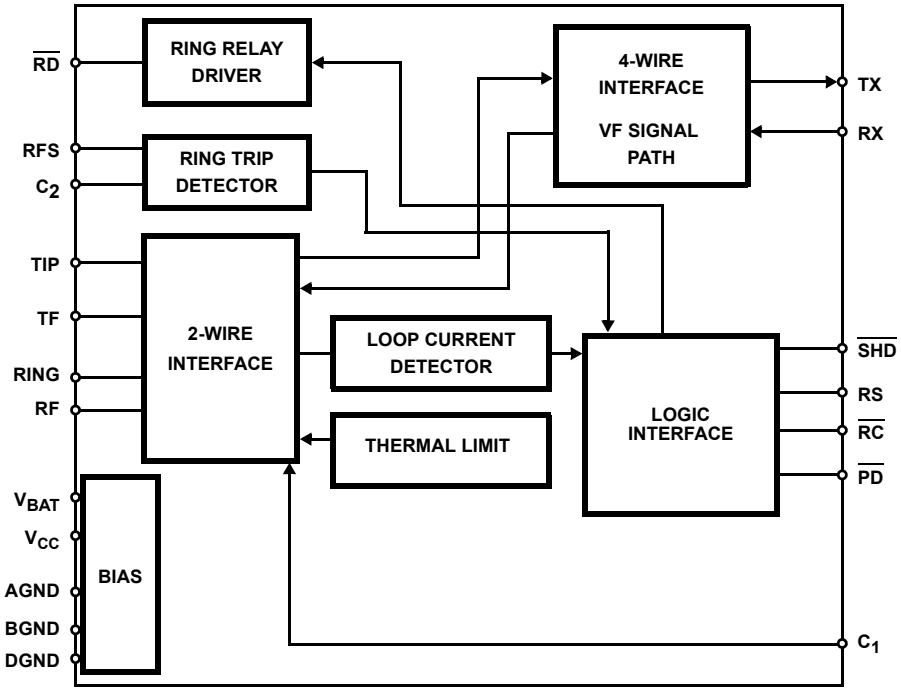
Features

- Wide Operating Battery Range (-21V to -44V)
- Single Additional +5V Supply
- 25mA Short Loop Current Limit
- Ring Relay Driver
- Switch Hook and Ring Trip Detect
- Low On-Hook Power Consumption
- On-Hook Transmission
- ITU-T Longitudinal Balance Performance
- Loop Power Denial Function
- Thermal Protection
- Supports Tip, Ring or Balanced Ringing Schemes
- Low Profile Surface Mount Packaging
- Pin Compatible with Industry Standard HC5504B SLIC
- Pb-free Available

Applications

- Analog Subscriber Line Interfaces in Analog Key Systems and Digital ISDN PABX Systems
- Related Literature
  - AN571, Using Ring Sync with HC-5502A and HC-5504 SLICs

Block Diagram



Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_{BAT}) . . . . . -60 to 0.5V
- (V_{CC}) . . . . . -0.5 to 15V
- (V_{CC} - V_{BAT}) 75V

Relay Drive Voltage (V_{RD}) . . . . . -0.5 to 15V

Operating Conditions

Operating Temperature Range
- HC5503 . . . . . 0°C to 75°C

Relay Driver Voltage (V_{RD}) . . . . . 5V to 12V
Positive Supply Voltage (V_{CC}) . . . . . 4.75V to 5.25V
Negative Supply Voltage (V_{BAT}) . . . . . -22V to -26V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
24 Lead SOIC	75

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 185
Diode Count 36
Die Dimensions . . . . . 137 x 102
Substrate Potential . . . . . Connected
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_{BAT} = -24V, V_{CC} = 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0 (Note 3), V_{CC} = 5V	-	80	100	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0 (Note 4), V_{CC} = 5V	-	180	200	mW
Off Hook I_{VCC}	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = 0°C	-	-	6.0	mA
Off Hook I_{VCC}	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = 25°C	-	-	4.0	mA
Off Hook I_{BAT}	R_L = 600Ω, I_{LONG} = 0 (Notes 3, 4)	-	19	23	mA
Off Hook Loop Current	R_L = 400Ω, I_{LONG} = 0 (Note 3)	-	22.9	-	mA
Off Hook Loop Current	R_L = 400Ω, V_{BAT} = -21.6V, I_{LONG} = 0 (Note 3), T_A = 25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 3)	-	25	30	mA
Fault Currents					
TIP to Ground	(Note 4)	-	27.5	-	mA
RING to Ground		-	70	-	mA
TIP to RING	(Note 4)	-	30	-	mA
TIP and RING to Ground		-	140	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25°C	-	-	25	µA
Ring Trip Detection Period	R_L = 600Ω, (Note 5)	-	2	3	Ring Cycles
Switch Hook Detection Threshold		5	-	10.5	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA

Electrical Specifications Unless Otherwise Specified, V_{BAT} = -24V, V_{CC} = 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Dial Pulse Distortion	(Note 4)	0	-	0.5	ms
Receive Input Impedance	(Note 5)	-	90	-	kΩ
Transmit Output Impedance	(Note 5)	-	10	20	Ω
2-Wire Return Loss	Referenced to 600Ω +2.16μF (Note 4)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 4) IEEE Method $0°C \le T_A \le 75°C$				
2-Wire Off Hook		53	58	-	dB
2-Wire On Hook		53	58	-	dB
4-Wire Off Hook at 1kHz		50	58	-	dB
Insertion Loss 2-Wire to 4-Wire at 3.4kHz V_{TR} to V_O V_O is the Output of the Transhybrid Amplifier	0dBm Input Level, Referenced 600Ω	-	±0.05	±0.2	dB
4-Wire to 2-Wire at 300Hz		-3.8	-4.0	-4.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 4)	-	±0.02	±0.05	dB
Idle Channel Noise, 2-Wire to 4-Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Idle Channel Noise, 4-Wire to 2-Wire	(Note 4)	-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay 2-Wire to 4-Wire, 4-Wire to 2-Wire	(Note 5)	-	-	2	μs
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	30	40	-	dB
Overload Level 2-Wire to 4-Wire (On-hook)	V_{CC} = +5V	2.5	-	-	V_{PEAK}
4-Wire to 2-Wire (Off-hook, R_L = 600Ω)		3.1	-	-	V_{PEAK}
Level Linearity 2-Wire to 4-Wire, 4-Wire to 2-Wire	At 1kHz, (Note 4) Referenced to 0dBm Level +3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB

Electrical Specifications Unless Otherwise Specified, V_{BAT} = -24V, V_{CC} = 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	(Note 4), 30 - 60Hz, R_L = 200Ω				
V_{CC} to 2-Wire		35	-	-	dB
V_{CC} to Transmit		35	-	-	dB
V_{BAT} to 2-Wire		20	-	-	dB
V_{BAT} to Transmit		20	-	-	dB
V_{CC} to 2-Wire	200 - 16kHz, R_L = 200Ω	35	-	-	dB
V_{CC} to Transmit		35	-	-	dB
V_{BAT} to 2-Wire		35	-	-	dB
V_{BAT} to Transmit		35	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	$0V \le V_{IN} \le 2.4V$	-	-	±20	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
$\overline{SHD}$ Output	I_{LOAD} 800µA, V_{CC} = 5V				
Logic '0' V_{OL}		-	0.1	0.4	V
Logic '1' V_{OH}	I_{LOAD} 40µA, V_{CC} = 5V	2.7	-	5.0	V

NOTES:

3. I_{LONG} = Longitudinal Current.
4. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
5. Guaranteed by design, not tested.

Design Information

Line Feed Amplifiers

The line feed amplifiers are high power operational amplifiers and are connected to the subscriber loop through 150Ω of feed resistance as shown in Figure 1. The feed resistors and synthesized impedance via feedback provide a 600Ω balanced load for the 2-wire to 4-wire transmission.

The tip feed amplifier is configured as a unity gain noninverting buffer. A -4V bias (derived from the negative battery (V_{BAT}) in the bias network) is applied to the input of the amplifier. Hence, the tip feed DC level is at -4V. The principal reason for this offset is to accommodate sourcing and sinking of longitudinal noise currents up to 15mA_{RMS} without saturating the amplifier output and to provide sufficient overhead for receive signals. The tip feed amplifier also feeds the ring feed amplifier, which is configured as a unity gain inverting amplifier as seen from the tip feed amplifier. The noninverting input to the ring feed amp is biased at a $V_{BAT}/2$. Looking into this terminal the amplifier has a noninverting gain of 2. Thus, the DC output at ring feed is:

$V_{RF}(DC) = (4 + V_{BAT})$ Volts

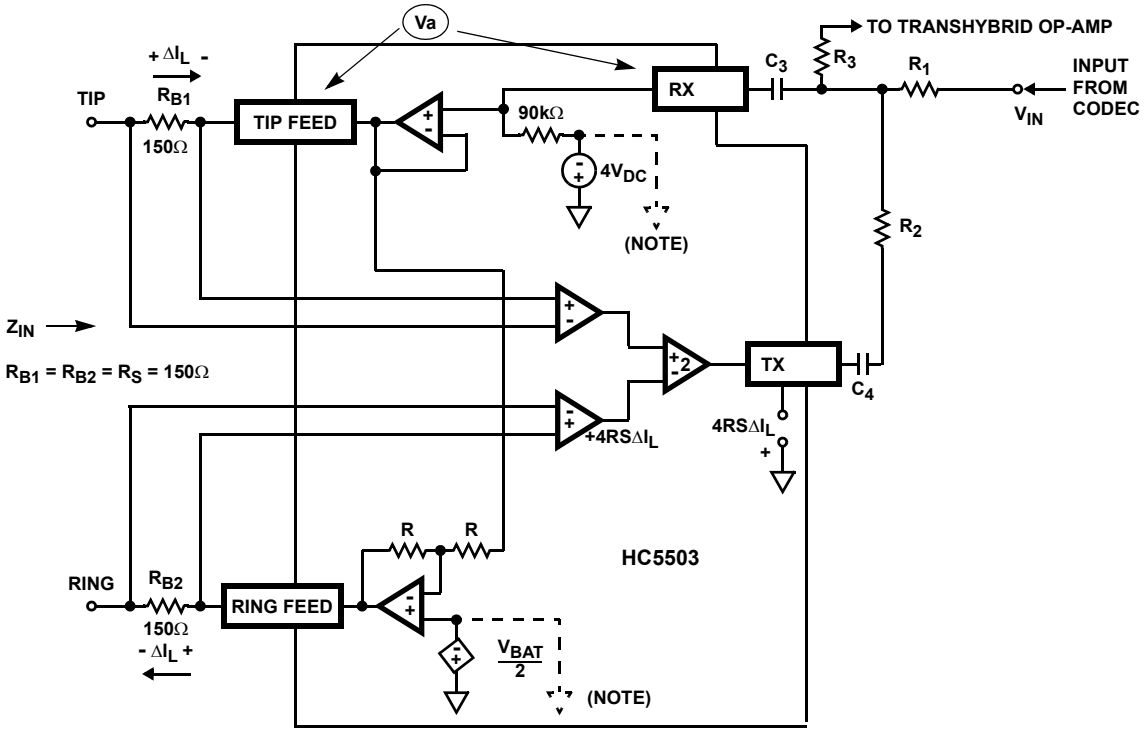
For a -24V battery, V_{RF} = -20V. Hence, the nominal battery feed across the loop provided by the SLIC is 16V. When the subscriber goes off-hook this DC feed causes current (metallic current) to flow around the loop.

The received audio signal RX is fed into the tip feed amplifier and appears at the tip feed terminal. It is also fed through the ring feed amplifier and is inverted. Thus, a differential signal of $2V_{RX}$ appears between tip feed and ring feed. The R_X signal causes AC audio currents to flow around the loop which are then AC coupled to the earpiece of the telephone set.

2-Wire Impedance Matching

The HC5503 is optimized for operation with a -24V battery. Impedance matching to a 600Ω load, is achieved through the combination of the feed resistors (R_{B1}, R_{B2}) and negative feedback through resistor R_2 (reference Figure 1). R_{B1} and R_{B2} are sense resistors that detect loop current and provide negative feedback to synthesize the remaining 300Ω required to match a 600Ω line.

The impedance looking into the tip terminal is 150Ω (R_{B1}) plus the synthesized impedance of the tip amplifier. The synthesized tip impedance is equal to the tip feed voltage Va divided by ΔIL. (Note, the tip feed amplifier is a voltage follower. Thus, the tip feed voltage is equal to the receive input voltage V_{RX}, both are labeled Va.) The synthesized impedance of the ring terminal is calculated the same way and is the ring feed voltage divided by ΔIL. (Note, the ring feed voltage is equal in magnitude to the tip feed voltage, but opposite in phase as a result of the ring feed amplifier gain.)



NOTE: Grounded for AC analysis.

FIGURE 1. IMPEDANCE MATCHING CIRCUITRY

The value of Va, as a result of feedback through R_2 from the T_X output, is given in Equation 1. Equation 1 is a voltage divider equation between resistors R_2 and the parallel combination of resistors; R_1, R_3 and the internal 90kΩ resistor $R_{INTERNAL}$. The Voltage on the transmit out (T_X) is the sum of the voltage drops across resistors R_{B1} and R_{B2} that is gained up by 2 to produce an output voltage at the V_{TX} pin that is equal to $-4R_S\Delta IL$.

$$V_a = \frac{R_1 \| 90k\Omega \| R_3}{R_1 \| 90k\Omega \| R_3 + R_2} \times V_{TX} \quad \text{(EQ. 1)}$$

Where: $V_{TX} = -4R_S\Delta IL = -600\Delta IL$.

To match a 600Ω line, the synthesized tip and ring impedances must be equal to 150Ω. The impedance looking into either the tip or ring terminal is once again the voltage at the terminal (Va) divided by the AC current ΔIL as shown in Equation 2.

$$Z_{Tipfeed} = Z_{Ringfeed} = \frac{V_a}{\Delta I_L} = 150\Omega \quad \text{(EQ. 2)}$$

Substituting the value of 600ΔIL for V_{TX} in Equation 1 and dividing both sides by ΔIL results in Equation 3.

$$\frac{V_a}{\Delta I_L} = \frac{R_1 \| 90k\Omega \| R_3}{R_1 \| 90k\Omega \| R_3 + R_2} \times 600 \quad \text{(EQ. 3)}$$

Setting Va/ΔIL equal to 150Ω and solving for R_2, given that R_1 = 10kΩ, $R_{INTERNAL}$ = 90kΩ and R_3 = 150kΩ the value of R_2 to match the input impedance of 600Ω is determined to be 25.47kΩ. (Note: nearest standard value is 24.9kΩ).

The amount of negative feedback is dependent upon the additional synthesized resistance required for matching. The sense resistors R_{B1} and R_{B2} should remain at 150Ω to maintain the $\overline{SHD}$ threshold listed in the electrical specifications. The additional synthesized resistance is determined by the feed back factor X (Equation 4) which needs to be applied to the transmit output and fed into the RX pin of the HC5503. The feed back factor is equal to the voltage divider between R2 and the parallel combination of R_1, R_3 and $R_{INTERNAL}$, reference Figure 2.

$$FeedbackFactor = X = \frac{R_1 \| 90k\Omega \| R_3}{R_1 \| 90k\Omega \| R_3 + R_2} \quad \text{(EQ. 4)}$$

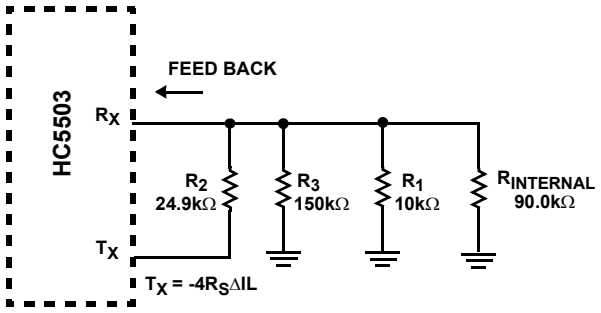


FIGURE 2. FEEDBACK EQUIVALENT CIRCUIT

The voltage that is feed back into the RX pin is equal to the voltage at V_{TX} times the feedback factor (Equation 5).

$$V_a = V_{TX}(X) \quad \text{(EQ. 5)}$$

Where V_{TX} is equal to $-4R_S\Delta IL$ (R_S = 150Ω)

So:

$$X = \frac{V_a}{\Delta I_L 600} \quad \text{(EQ. 6)}$$

But, from Equation 2:

$$\frac{V_a}{\Delta I_L} = 150\Omega \quad \text{(EQ. 7)}$$

Therefore:

$$X = \frac{V_a}{V_{TX}} = \frac{150}{600} = \frac{1}{4} \quad \text{(EQ. 8)}$$

Equation 8 shows that 1/4 of the T_X output voltage is required to synthesize 150Ω at both the Tip feed and Ring feed amplifiers.

To match a 900Ω load would require 300Ω worth of synthesized impedance (300Ω from R_{B1} + R_{B2} and 600Ω from the Tip feed + Ring feed amplifiers).

Setting $V_a/\Delta IL$ equal to 300Ω and solving for R_2 in Equation 3, given that R_1 = 10kΩ, $R_{INTERNAL}$ = 90kΩ and R_3 = 150kΩ the value of R_2 to match the input impedance of 900Ω is determined to be 8.49kΩ (Note: nearest standard value is 8.45kΩ). The feed back factor to match a 900Ω load is 1/2 (300/600).

The selection of the value of 150kΩ for R_3 is arbitrary. The only requirement is that it be large enough to have little effect on the parallel combination between $R_{INTERNAL}$ (90kΩ) and R_1 (10kΩ). R_3 should be greater then 90kΩ.

The selection of the value of 10kΩ for R_1 is also arbitrary. The only requirement is that the value be small enough to offset any process variations of $R_{INTERNAL}$ and large enough to avoid loading of the CODEC's output. A value of 10kΩ is a good compromise.

2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is defined as the output voltage V_{TX} divided by the tip to ring voltage (V_{TR}). Where: V_{TX} = -4R_SΔIL = -600ΔIL and V_{TR} = (RL)ΔIL = 600ΔIL. The 2-wire to 4-wire gain is therefore equal to -1.0, as shown in Equation 9.

$$A_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{-600\Delta I_L}{600\Delta I_L} = -1.0 \quad \text{(EQ. 9)}$$

4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is defined as the output voltage V_{TR} divided by the input voltage, V_{IN}. To determine the 4-wire to 2-wire gain we need to define V_{TR} in terms of V_{IN}. The voltage at V_{TR} is the loop current times the load impedance Z_L.

$$V_{TR} = \Delta I_L \times Z_L = \Delta I_L \times Z_O \quad \text{(EQ. 10)}$$

For optimum 2-wire return loss, the input impedance of the SLIC (Z_O) must equal the load impedance (Z_L) of the line. All Equations going further assume $Z_L = Z_O$.

The loop current ΔIL is the total voltage across the loop divided by the total resistance of the loop. The total voltage across the loop is the sum of the tip feed voltage (V_{TF}) and the ring feed voltage (V_{RF}) where V_{TF} = -V_{RF}. The total resistance is the sum of the sense resistors RB_1 and RB_2 and the load Z_L (Z_L +2R_S). The total loop current is defined in Equation 11.

$$\Delta I_L = \frac{V_{TF} - V_{RF}}{Z_O + 2R_S} = \frac{2(V_{TF})}{Z_O + 2R_S} \quad \text{(EQ. 11)}$$

From Equation 10:

$$\Delta I_L = \frac{V_{TR}}{Z_O} \quad \text{(EQ. 12)}$$

Substituting Equation 12 into Equation 11 and solving for V_{TR}:

$$V_{TR} = \left(\frac{2(V_{TF})}{Z_O + 2R_S}\right) Z_O \quad \text{(EQ. 13)}$$

Using Superposition, the voltage at the receive input R_X is given as:

$$V_{RX} = V_{TF} = \left(\frac{R'_1}{R'_1 + R_2}\right) V_{TX} + \left(\frac{R'_2}{R'_2 + R_1}\right) V_{IN} \quad \text{(EQ. 14)}$$

Where R'_1 is the effective impedance that is formed by the parallel combination of $R_{INTERNAL}$ (90kΩ), R_3 (150kΩ), R_1 (10kΩ) and is equal to 8.49kΩ. R'_2 is the effective impedance that's formed by the parallel combination of $R_{INTERNAL}$ (90kΩ), R_3 (150kΩ), R_2 (24.9kΩ) and is equal to 17.25kΩ.

V_{RX} for the recommended values of R_1 and R_2 is given in Equations 15 and 16. For impedance matching to a load other than 600Ω, recalculate the parallel impedances R'_1, R'_2 and substitute into Equation 15. The 4-wire to 2-wire gain is recalculated by using the Equations below.

$$V_{RX} = V_{TF} = \left(\frac{8.49k\Omega}{8.49k\Omega + 24.9k\Omega}\right) V_{TX} + \left(\frac{17.25k\Omega}{17.25k\Omega + 10k\Omega}\right) V_{IN} \quad \text{(EQ. 15)}$$

$$V_{RX} = V_{TF} = (0.25)V_{TX} + (0.633)V_{IN} \quad \text{(EQ. 16)}$$

Substituting Equation 16 into Equation 13:

$$V_{TR} = \left(\frac{2((0.25)V_{TX} + (0.633)V_{IN})}{Z_O + 2R_S}\right) Z_O \quad \text{(EQ. 17)}$$

From Equation 10:

$$\Delta I_L = \frac{V_{TR}}{Z_O} \quad \text{(EQ. 18)}$$

From Equation 1:

$$V_{TX} = -4RS\Delta I_L \quad \text{(EQ. 19)}$$

Substituting Equation 18 into Equation 19:

$$V_{TX} = -4RS\frac{V_{TR}}{Z_O} \quad \text{(EQ. 20)}$$

Substituting Equation 20 into Equation 17:

$$V_{TR} = \left(-2RS\frac{V_{TR}}{Z_O} + 1.266V_{IN}\right)\frac{Z_O}{Z_O + 2R_S} \quad \text{(EQ. 21)}$$

Assuming R_S = 150Ω and rearranging terms:

$$\left(1 + \frac{300}{Z_O + 300}\right) V_{TR} = \left(\frac{1.266Z_O}{Z_O + 300}\right) V_{IN} \quad \text{(EQ. 22)}$$

The 4-wire to 2-wire gain (Given that: R_1 = 10kΩ, R_2 = 24.9kΩ and R_3 = 150kΩ) for a 600Ω load is:

$$A_{4-2} = \frac{V_{TR}}{V_{IN}} = \left(\frac{1.266Z_O}{Z_O + 600}\right) = 0.633 = -3.96dB \quad \text{(EQ. 23)}$$

The Transversal Amplifier (TA)

Whereas the feed amplifiers perform the 4-wire to 2-wire transmission function, the transversal amplifier acts as the 2-wire to 4-wire hybrid. The TA is a summing amplifier configured to reject common mode signals. It will reject 2-wire common mode signals. R_{B1} and R_{B2} act as loop current sense resistors. The voice signal output of the amplifier is a function of the differential voltages appearing across R_{B1} and R_{B2}.

The transversal amplifier also has a DC output proportional to the metallic current in the loop. The output voltage is given by:

$$V_{TX} = 2(I_{TIP} + I_{RING}) (R_{B1} + R_{B2})$$

This DC level is used as an input to a comparator whose output feeds into the logic circuitry as SH. This signal is used to gate $\overline{SHD}$ output.

Voice signals on the loop are transformed by the TA into ground referenced signals. Since the TA output has a DC offset it is necessary to AC couple the output to any external circuitry. Note, that during 4-wire to 2-wire transmission, the transversal amplifier will have an audio signal at its output proportional to the 4-wire audio receive signal and the loop's equivalent AC impedance. This is called the transhybrid return, and must be cancelled (or balanced) out to prevent an echo effect. Reference the Transhybrid Circuit section for more information.

Loop Current Limiting

The maximum loop length for this application is a 533Ω load across the feed amplifiers ($24V_{SUPPLY}$ - $8V_{OVERHEAD}$)/ $30mA_{MAX}$ loop current). However, on a short loop the line resistance often approaches zero. Thus, a need exists to control the maximum DC loop current that can flow around the loop to prevent an excessive current drain from the system battery. This limit is internally set to 30mA on the HC5503. Figure 3 depicts the feedback network that modifies the V_{RF} voltage as a function of metallic current. Figure 4 illustrates the loop current characteristics as a function of line resistance.

As indicated above, the TA has a DC voltage output directly proportional to the loop current. This voltage level is scaled by R_{19} and R_{18}. The scaled level forms the 'Metallic' input to one side of a Transconductance Amplifier.

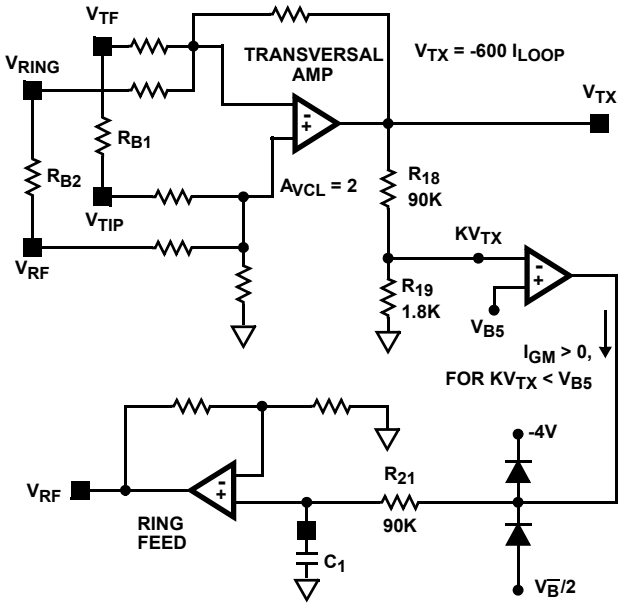


FIGURE 3. DC LOOP CURRENT CHARACTERISTICS

The reference input to this amplifier is generated in the bias network, and is equivalent to 30mA. When the metallic input exceeds the set reference level, the transconductance amplifier sources current. This current will charge C_1 in positive direction causing the V_{RF} (Ring Feed) voltage to approach the V_{TF} (Tip Feed), effectively reducing the battery feed across the loop which will limit the DC loop current. C_1 will continue to charge until an equilibrium level is attained at $I_{LOOP} = I_{LOOP}$mA (Max). The time constant of this feedback loop is set by R_{21} (90kΩ) and C_1 which is nominally 0.33μF.

The V_{RF} voltage level is also modified to reduce or control loop current during ring line faults (e.g., ground or power line crosses), and thermal overload. Figure 8 illustrates this. The thermal and fault current circuitry works in parallel with the transconductance amplifier.

Longitudinal Amplifier

The longitudinal amplifier is an operational amplifier configured as a closed loop differential amplifier with a nominal gain of 0.1. The output is a measure of any imbalance between I_{TIP} and I_{RING}. The transfer function of this amplifier is given by:

$$V_{LONG} = 0.1(I_{TIP} - I_{RING}) 150.$$

The gain factor is much less than one since ring voltage (up to $150V_{PEAK}$) can appear at the Ring or Ring Feed Sense terminals and are attenuated to avoid exceeding the common mode range of the longitudinal amplifier's input.

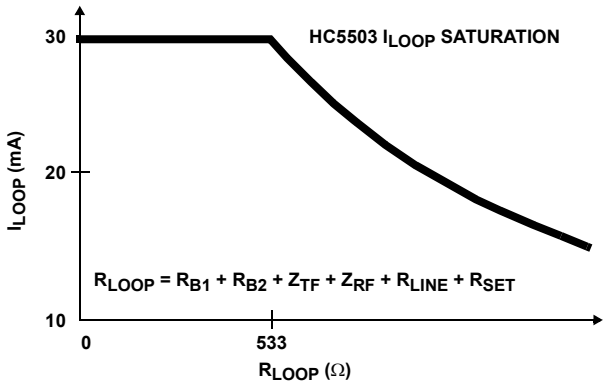


FIGURE 4. DC LOOP CURRENT CHARACTERISTICS

The longitudinal amplifier's principal function is Ring Trip Detection. The output of the amplifier after being filtered by R_{20} and C_2 to attenuate AC signals is fed into a detector whose output inhibits the ring relay driver to remove ringing signals from the line in an off-hook condition, reference Figure 8.

Ringing The Line

The Ring Command ($\overline{RC}$) input is taken low during ringing. This activates the ring relay driver ($\overline{RD}$) output providing the telephone is not off-hook or the line is not in a power denial state. The ring relay connects the ring generator to the subscriber loop. The ring generator output is usually an $80V_{RMS}$, 20Hz signal. The ring signal should not exceed 150V peak. Since the telephone ringer is AC coupled only ring current will flow. This ringing current flows directly into V_{BAT} via a set of relay contacts. The high impedance terminal RFS is provided so that the low impedance V_{RF} node can be isolated from the hot end of the ring path in the battery referenced ring scheme.

The AC ring current flowing in the subscriber circuit will be sensed across R_{B2}, and will give rise to an AC voltage at the output of the longitudinal amplifier. R_{20} and C_2 attenuate this signal before it reaches the ring trip detector to prevent false ring trip. C_2 is nominally set at 1.0μF.

When the subscriber goes off-hook, a DC path is established between the output of the ring generator and the battery ground or V_{BAT} terminal. A DC longitudinal imbalance is established since no tip feed current is flowing through the tip feed resistors. The longitudinal amplifier output is driven negative. Once it exceeds the ring trip threshold of the ring trip detector, the logic circuitry is driven by GK to trip the ring relay establishing an off-hook condition such that $\overline{SHD}$ will become active as loop metallic current starts to flow.

In addition to its ability to be used for tip or ring injected systems, the HC5503 can also be configured for systems utilizing balanced ringing. The main advantage of balanced ringing is that it tends to minimize cross coupling effects owing to the differential nature of the ring tone across the line.

Figure 5 illustrates the sequence of events during ring trip with ring synchronization for a tip injected ring system. Note that owing to the 90 degree phase shift introduced by the low pass filter (R_{20}, C_2) the RS pulse will occur at the most negative point of the attenuated ring signal that is fed into the ring trip detector. Hence, when DC conditions are established for $\overline{SHD}$, the AC component actually assists ring trip taking place. For a ring side injected ring system, the RS pulse should occur at the positive zero crossing of the ring signal as it appears at RFS. If ring synchronization is not used, then the RS pin should be held permanently to a logic high of 5V nominally: ring trip will occur asynchronously with respect to the ring voltage. Ring trip is guaranteed to take place within three ring cycles after the telephone going off-hook.

It is recommended that an RC snubber network is placed across the ring relay contacts to minimize inductive kick-back effects from the telephone ringer. Typical values for such a network are shown in Figure 10.

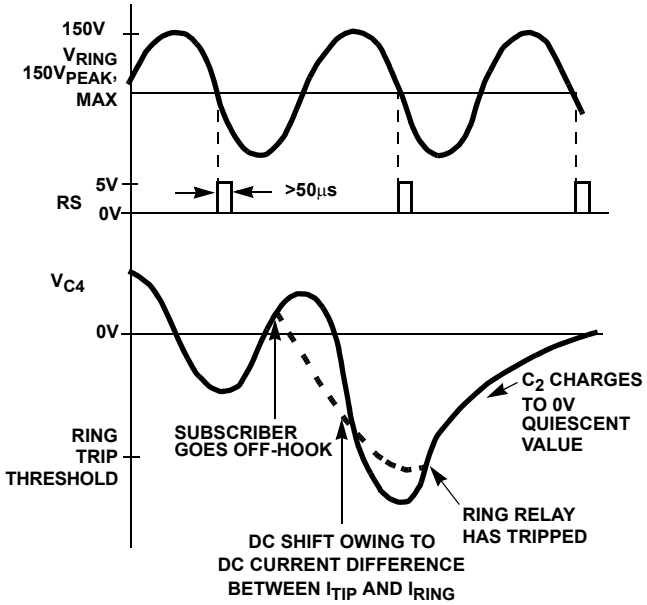


FIGURE 5. RING TIP SEQUENCE

Transhybrid Circuit

The purpose of the transhybrid circuit is to remove the receive signal (R_X) from the transmit signal (T_X), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the 4-wire receive port (R_X) to the 4-wire transmit port (T_X). Figure 6 shows the transhybrid circuit. Because the voltage at R_X is 180 degrees out of phase with the voltage at T_X, the input signal will be subtracted from the output signal if I_1 equals I_2. Node analysis yields the following Equation:

$$I_1 + I_2 = \frac{T_X}{R_4} + \frac{R_X}{R_3} = 0 \quad \text{(EQ. 24)}$$

The voltage at T_X is the product of the 4-wire to 2-wire ($A_{4\text{-}2}$ = 0.633) and 2-wire to 4-wire ($A_{2\text{-}4}$ = -1.0) voltage gains, and is therefore equal to 0.633. The voltage at R_X, when taking into account the negative feedback through R_2,

is the calculated value of 0.633 plus the feedback which is 1/4 T_X (for matching to a 600Ω load, reference Equation 8).

The voltage at R_X is calculated in Equation 25.

$$R_X = 0.633 - \frac{1}{4}(0.633) = 0.474 \quad \text{(EQ. 25)}$$

Substituting the values for T_X and R_X into Equation 24 and setting them equal to each other, the values of R3 and R_4 can then be determined.

$$\frac{0.633}{R_4} = \frac{0.474}{R_3} \quad \text{(EQ. 26)}$$

Setting the value of R_3 to 150kΩ sets the value of R_4 to be 200kΩ.

Notice that the input voltage for the incoming signal (I_1) is taken at R_X, instead of the conventional method at the CODEC (point A, Figure 6). This alternative method is used because the tolerance effects of R_1 on the transhybrid balance are eliminated.

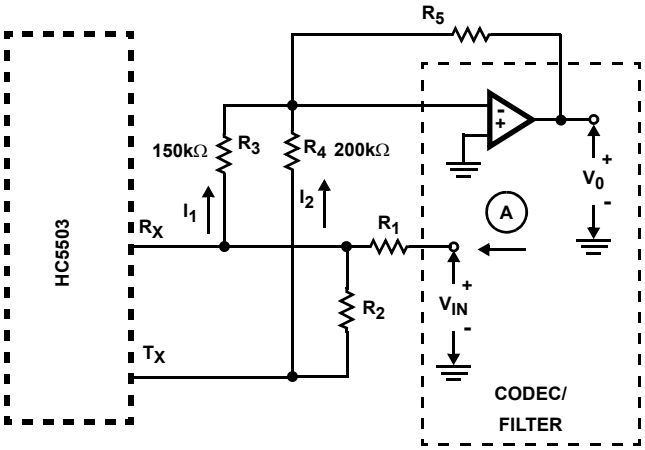


FIGURE 6. TRANSHYBRID CIRCUIT

Power Denial ($\overline{PD}$)

Power denial limits power to the subscriber loop: it does not power down the SLIC, i.e., the SLIC will still consume its normal on-hook quiescent power during a power denial period. This function is intended to “isolate” from the battery, under processor control, selected subscriber loops during an overload or similar fault status.

If $\overline{PD}$ is selected, the logic circuitry inhibits $\overline{RC}$ and switches in a current source to C_1. The capacitor charges up to a nominal -3.5V at which point it is clamped. Since tip feed is always at -4V, the battery feed across the loop is essentially zero, and minimum loop power will be dissipated if the circuit goes off-hook. No signaling functions are available during this mode.

After power denial is released ($\overline{PD}$ = 1), it will be several hundred milliseconds (300ms) before the V_{RF} output reaches its nominal battery setting. This is due to the RC time constant of R_{21} and C_1.

The Logic Network

The logic network utilizes I^2L logic. All external inputs and outputs are LS TTL compatible: the relay driver is an open collector output that can sink 60mA with a V_{CE} of 1V.

Figure 9 is a schematic of the combination logic within the network. The external inputs $\overline{RC}$ (Relay Control) and $\overline{PD}$ (Power Denial) allow the switch controller to ring the line or deny power to the loop, respectively. The Ring Synchronization input (RS) facilitates switching of the ring relay near a ring current zero crossing in order to minimize inductive kickback from the telephone ringer.

Line Fault Protection

The subscriber loop can exist in a very hostile electrical environment. It is often in close proximity to very high voltage power lines, and can be subjected to lightning induced voltage surges. The SLIC has to provide isolation between the subscriber loop and the PBX/Key telephone system.

The most stringent line fault condition that the SLIC has to withstand is that of the lightning induced surge.

The Intersil monolithic SLIC, in conjunction with a simple low cost diode bridge, can achieve up to 450V of isolation between the loop and switch. The level of isolation is a function of the packaging technology and geometry together with the chip layout geometries. One of the principal reasons for using DI technology for fabricating the SLIC is that it lends itself most readily to manufacturing monolithic circuits for high voltage applications.

Figures 10 shows the application circuit for the HC5503. A secondary protection diode bridge is indicated which protects the feed amplifiers during a fault. Most line systems will have primary protection networks. They often take the form of a carbon block or arc discharge device. These limit the fault voltage to less than 450V peak before it reaches the line cards. Thus when a transient high voltage fault has occurred, it will be transmitted as a wave front down the line. ***The primary protection network must limit the voltage to less than 450V.*** The attenuated wave front will continue down the line towards the SLIC. The feed amplifier outputs appear to the surge as very low impedance paths to the system battery. Once the surge reaches the feed resistors, fault current will flow into or out of the feed amplifier output stages until the relevant protection diodes switch on. Once the necessary diodes have started to conduct all the fault current will be handled by them.

If the user wishes to characterize SLIC devices under simulated high voltage fault conditions on the bench, he should ensure that the negative battery power supply has sufficient current capability to source the negative peak fault current and low series inductance. If this is not the case, then the battery supply could be pulled more negative and destroy the SLIC if the total (V_{CC} + V_{BAT}) voltage across it exceeds 75V.

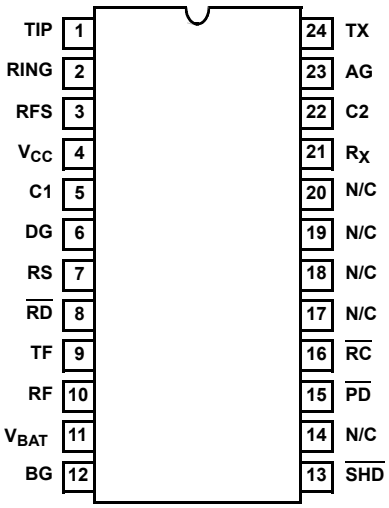
Pin Descriptions

24 PIN SOIC	SYMBOL	DESCRIPTION
1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
2	RING	An analog input connected to the RING (more negative) side of the subscriber loop. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	RFS	Senses ring side of loop for ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
4	V_{CC}	Positive Voltage Source - Most positive supply. V_{CC} is typically 5V.
5	C_1	Capacitor #1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_{BAT}. Typical value is 0.3µF, 16V.
6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5V.
8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
11	V_{BAT}	Negative Voltage Source - Most negative supply. V_{BAT} is typically -24V. Frequently referred to as “battery”.
12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10.5mA and disabled for loop currents less than 5mA.
15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) is not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (R_S) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).
21	R_X	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input deferentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 150Ω of feed resistance on each side of the line.
22	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from nearby power lines and other noise sources. Recommended value is 1.0µF, 20V. This capacitor should be nonpolarized.
23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
14	NC	Used during production testing. For proper operation of the SLIC, this pin should float.
17, 18, 19, 20	NC	No internal connection.

NOTE: All grounds (AG, BG, and DG) must be applied before V_{CC} or V_{BAT}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Pinout

HC5503 (SOIC)
TOP VIEW



Functional Block Diagram

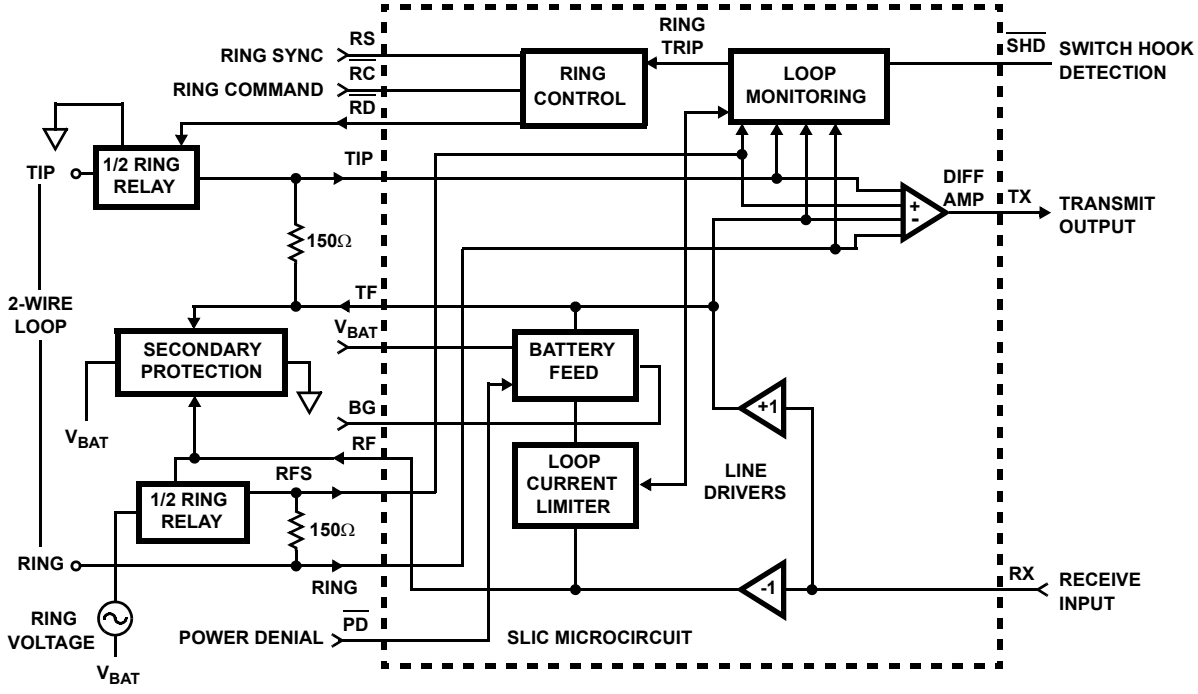


FIGURE 7.

Schematic Diagram

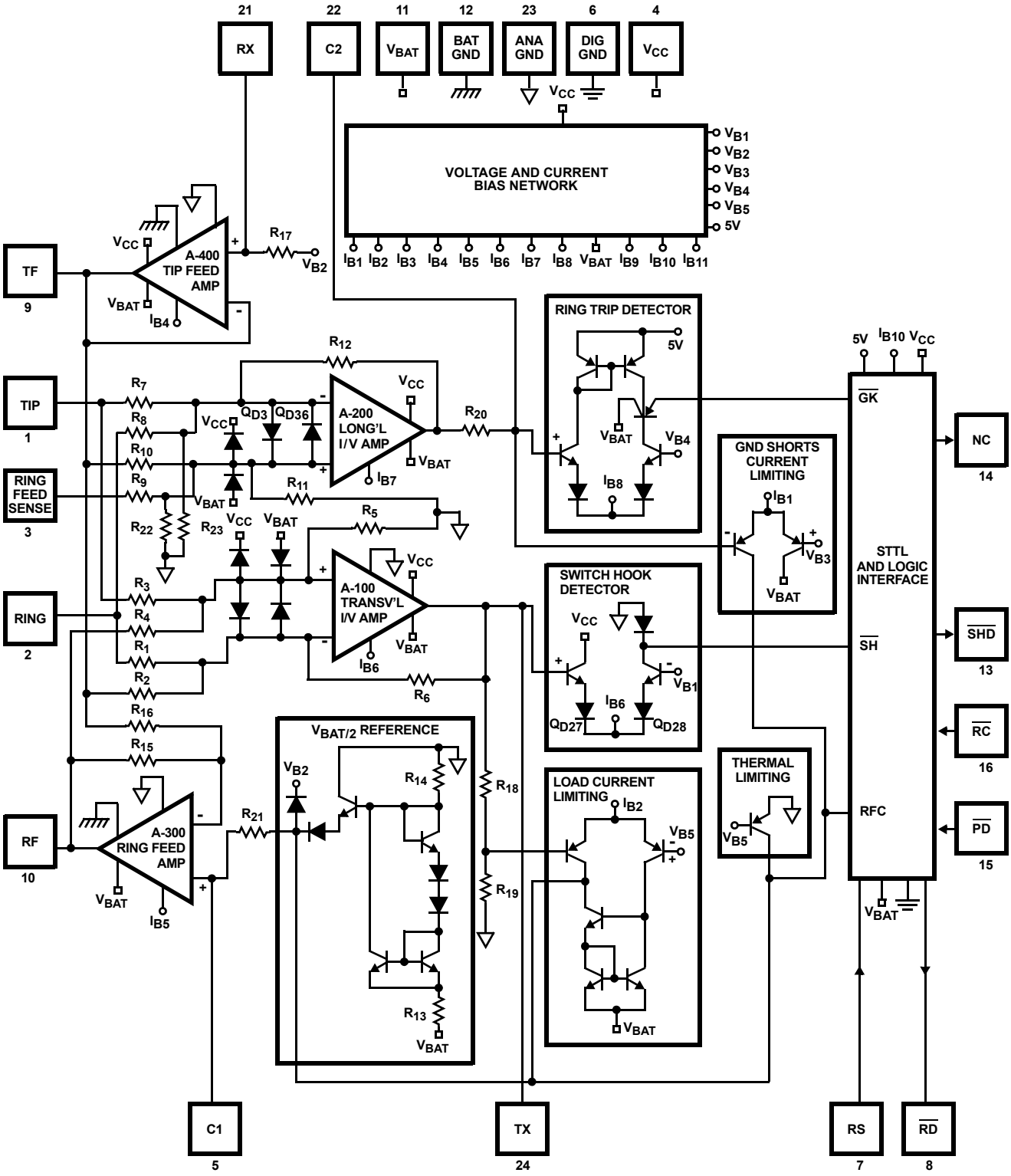


FIGURE 8. FUNCTIONAL SCHEMATIC

Schematic Diagram (Continued)

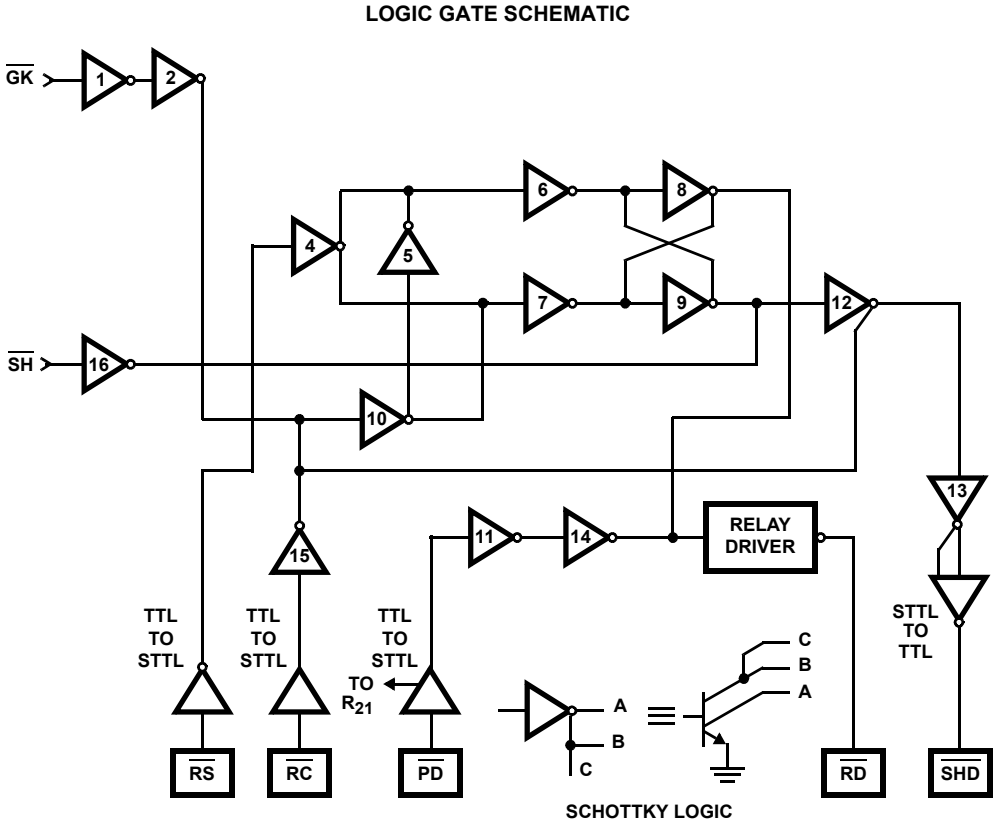


FIGURE 9. LOGIC NETWORK

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

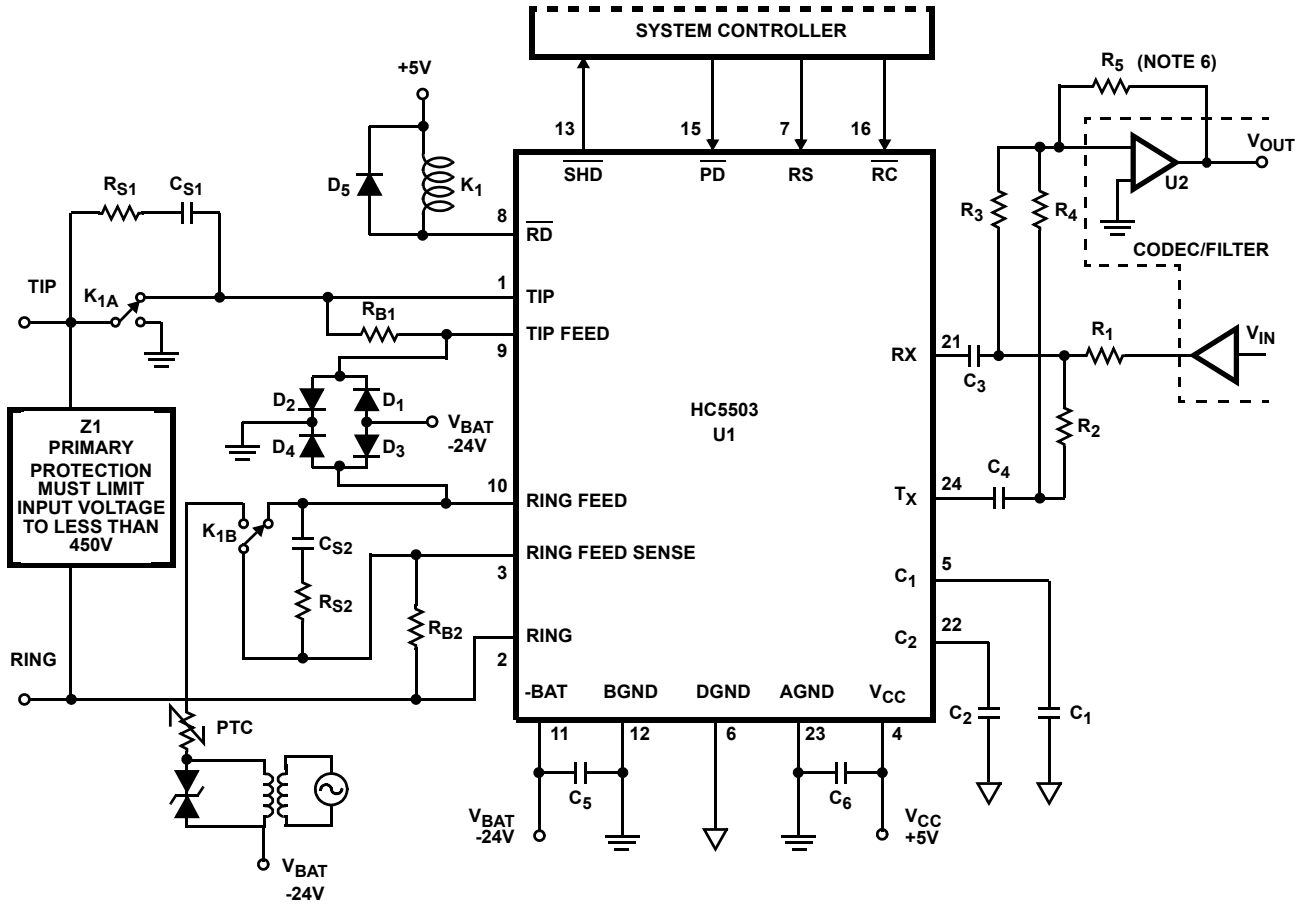
High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $10mA_{RMS}$, $5mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±450 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±450 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±450 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to $10A_{RMS}$	315 (Plastic)	V_{RMS}

Application Circuit



NOTES:

6. R_5 sets the 2-wire to 4-wire gain. R_5 = 150kΩ then A_{2-4} = 0dB. R_5 = 75kΩ then A_{2-4} = -6.0dB.
7. Secondary protection diode bridge recommended is a 2A, 200V type.
8. All grounds (AG, BG, and DG) must be applied before V_{CC} or V_{BAT}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
9. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.

FIGURE 10. -24V APPLICATION CIRCUIT

Typical Component Values:

C_1 = 0.33μF, 20%, 20V.

C_2 = 1.0μF, 10%, 20V.

C_3 = C_4 = 0.47μF, 20%, 30V.

C_5, C_6 = 0.01μF, 30V.

C_{S1} = C_{S2} = 0.1μF, 200V typically, depending on V_{RING} and line length.

R_{B1} = R_{B2} = 150 (1% absolute value).

R_{S1} = R_{S2} = 1kΩ, 1%, 1/4W.

R_1 = 10kΩ, 1%, 1/4W.

R_2 = 24.9kΩ, 1%, 1/4W.

R_3 = R_5 = 150kΩ, 1%, 1/4W.

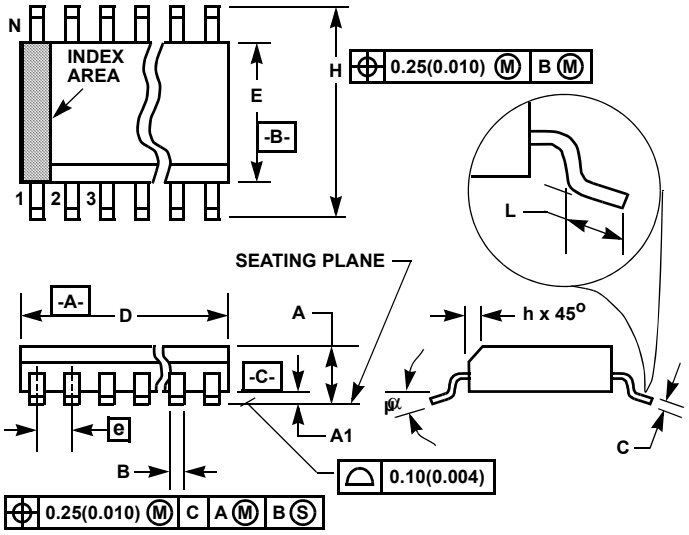
R_4 = 200kΩ, 1%, 1/4W.

D_1, D_2, D_3, D_4, D_5 = 1N40007, 100V, 3A.

Z_1 = 250V to 350V transient protection.

PTC used as ring generator ballast.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 **(JEDEC MS-013-AD ISSUE C)**
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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