

NDF05N50Z, NDD05N50Z

N-Channel Power MOSFET 500 V, 1.5 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- 100% Rg Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	NDF	NDD	Unit
Drain-to-Source Voltage	V_{DS}	500		V
Continuous Drain Current $R_{\theta JC}$	I_D	5.5 (Note 1)	4.7	A
Continuous Drain Current $R_{\theta JC}$, $T_A = 100^\circ\text{C}$	I_D	3.5 (Note 1)	3	A
Pulsed Drain Current, $V_{GS} @ 10\text{ V}$	I_{DM}	20	19	A
Power Dissipation $R_{\theta JC}$	P_D	30	83	W
Gate-to-Source Voltage	V_{GS}	± 30		V
Single Pulse Avalanche Energy, $I_D = 5.0\text{ A}$	E_{AS}	130		mJ
ESD (HBM) (JESD22–A114)	V_{ESD}	3000		V
RMS Isolation Voltage ($t = 0.3\text{ sec.}$, R.H. $\leq 30\%$, $T_A = 25^\circ\text{C}$) (Figure 17)	V_{ISO}	4500		V
Peak Diode Recovery (Note 2)	dV/dt	4.5		V/ns
MOSFET dV/dt	dV/dt	60		V/ns
Continuous Source Current (Body Diode)	I_S	5		A
Maximum Temperature for Soldering Leads	T_L	260		$^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	–55 to 150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

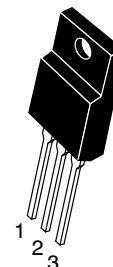
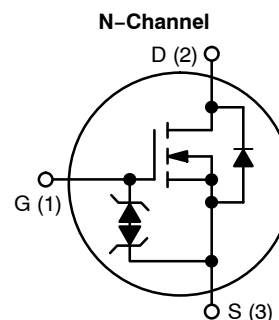
1. Limited by maximum junction temperature
2. $I_S = 4.4\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J = +150^\circ\text{C}$



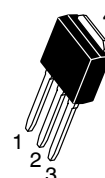
ON Semiconductor®

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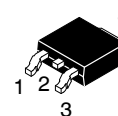
V_{DSS}	$R_{DS(on)} \text{ (MAX) @ } 2.2\text{ A}$
500 V	1.5 Ω



**NDF05N50ZG,
NDF05N50ZH
TO-220FP
CASE 221AH**



**NDD05N50Z-1G
IPAK
CASE 369D**



**NDD05N50ZT4G
DPAK
CASE 369AA**

ORDERING AND MARKING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

NDF05N50Z, NDD05N50Z

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.2 1.5	°C/W
Junction-to-Ambient Steady State	$R_{\theta JA}$	50 38 80	

3. Insertion mounted

4. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	500			V
Breakdown Voltage Temperature Co-efficient	$\Delta BV_{DSS} / \Delta T_J$	Reference to 25°C , $I_D = 1\text{ mA}$		0.6		V/°C
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	25°C 150°C		1 50	μA
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$			±10	μA

ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.2\text{ A}$		1.25	1.5	Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50\text{ μA}$	3.0	3.9	4.5	V
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 2.5\text{ A}$		3.5		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 6)	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	421	530	632	pF
Output Capacitance (Note 6)	C_{oss}		50	68	80	
Reverse Transfer Capacitance (Note 6)	C_{rss}		8	15	25	
Total Gate Charge (Note 6)	Q_g	$V_{DD} = 250\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 10\text{ V}$	9	18.5	28	nC
Gate-to-Source Charge (Note 6)	Q_{gs}		2	4	6	
Gate-to-Drain ("Miller") Charge (Note 6)	Q_{gd}		5	10	15	
Plateau Voltage	V_{GP}			6.5		V
Gate Resistance	R_g		1.5	4.5	8	Ω

RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ Ω}$		11		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(off)}$			24		
Fall Time	t_f			14		

SOURCE-DRAIN DIODE CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	V_{SD}	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$			1.6	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$		255		ns
Reverse Recovery Charge	Q_{rr}	$I_S = 5\text{ A}, di/dt = 100\text{ A/μs}$		1.25		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

6. Guaranteed by design.

TYPICAL CHARACTERISTICS

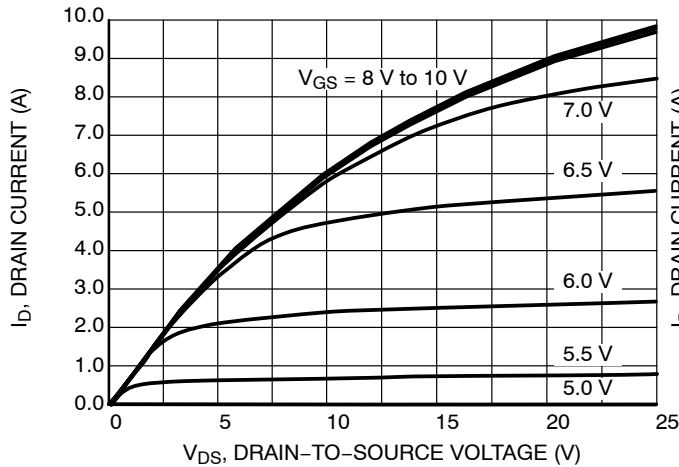


Figure 1. On-Region Characteristics

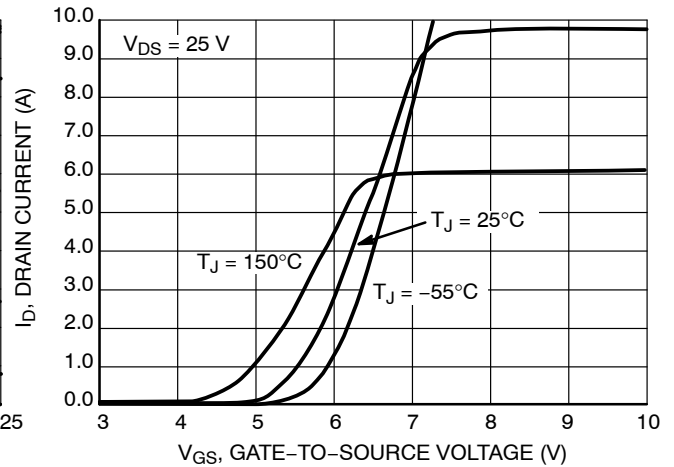


Figure 2. Transfer Characteristics

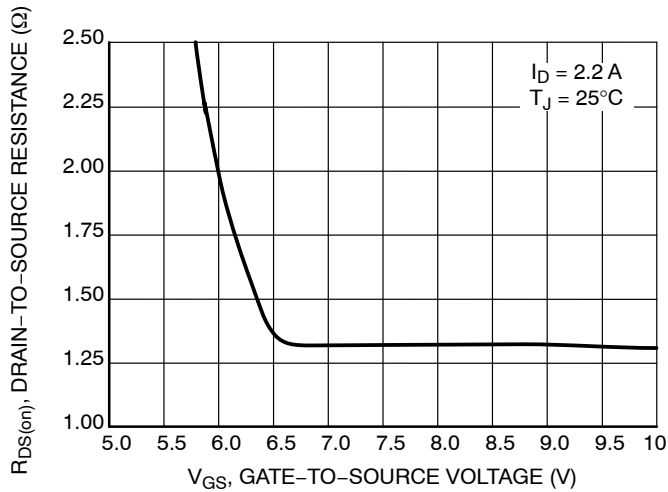


Figure 3. On-Region versus Gate-to-Source Voltage

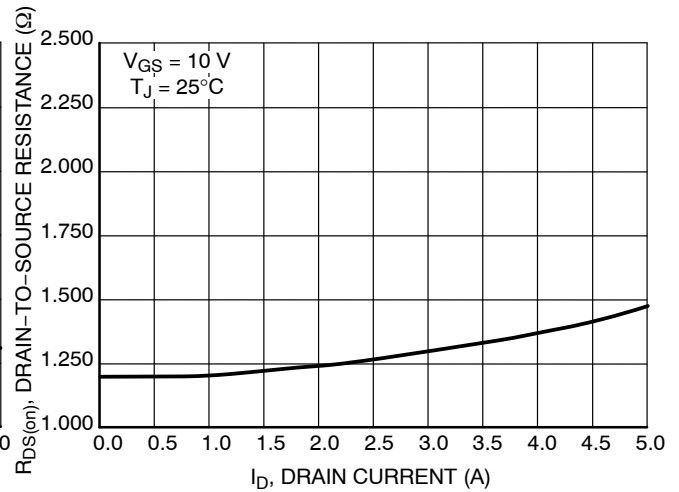


Figure 4. On-Resistance versus Drain Current and Gate Voltage

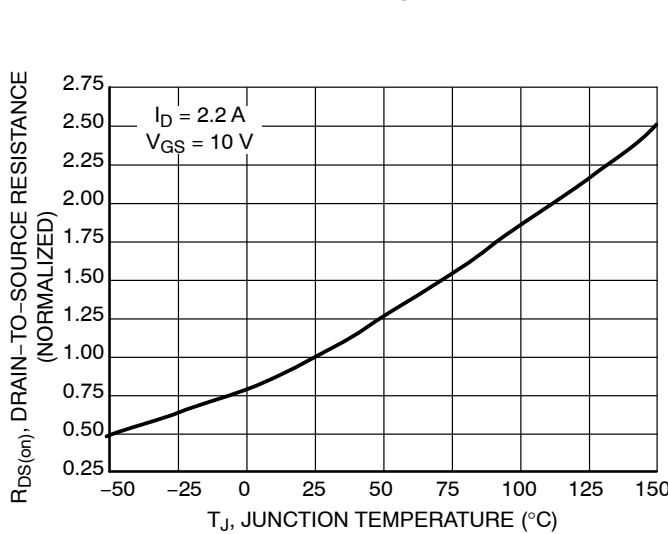


Figure 5. On-Resistance Variation with Temperature

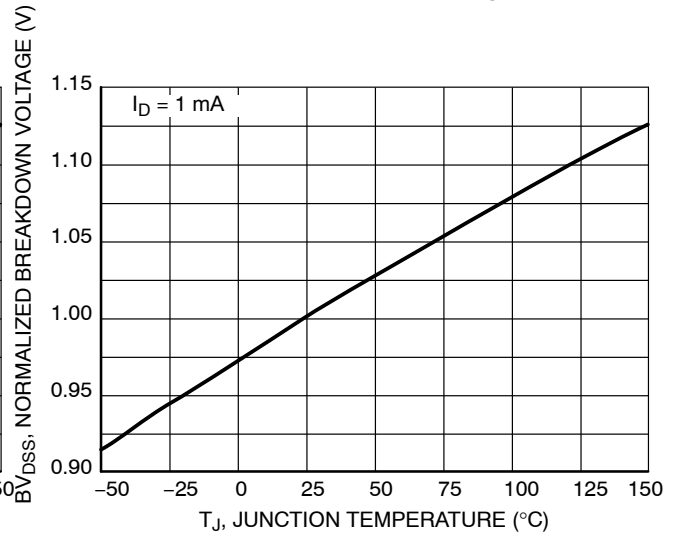


Figure 6. BV_{DSS} Variation with Temperature

TYPICAL CHARACTERISTICS

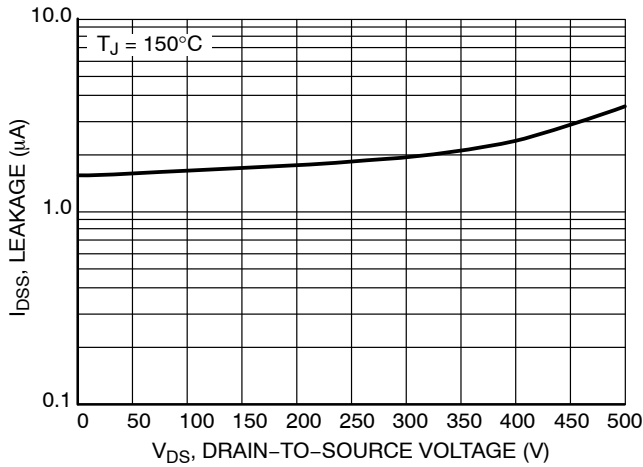


Figure 7. Drain-to-Source Leakage Current versus Voltage

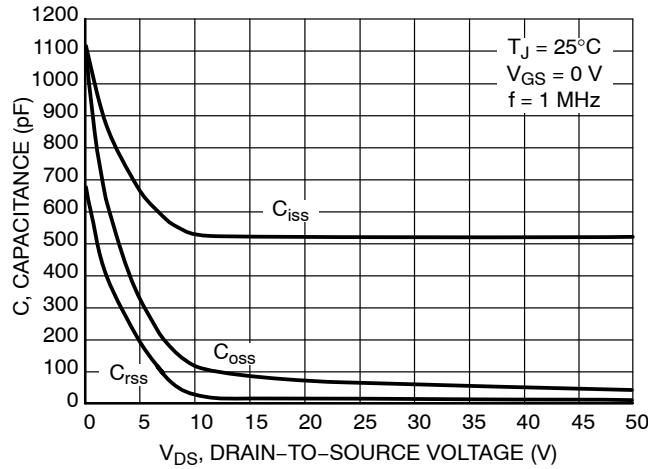


Figure 8. Capacitance Variation

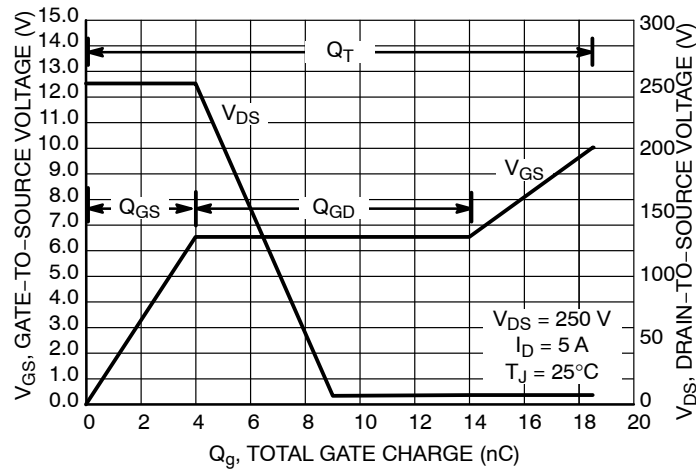


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

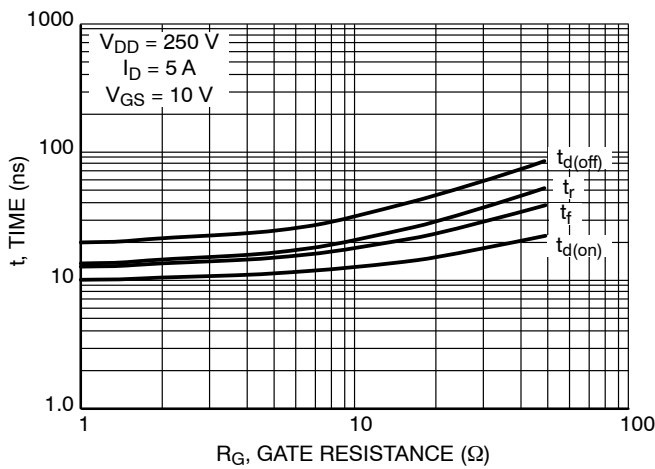


Figure 10. Resistive Switching Time Variation versus Gate Resistance

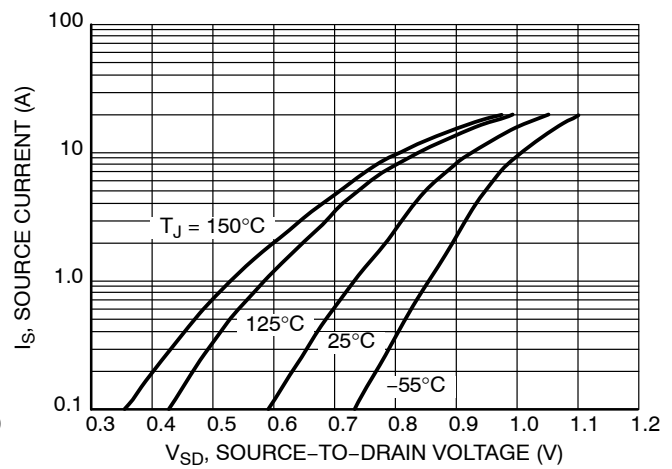


Figure 11. Diode Forward Voltage versus Current

NDF05N50Z, NDD05N50Z

TYPICAL CHARACTERISTICS

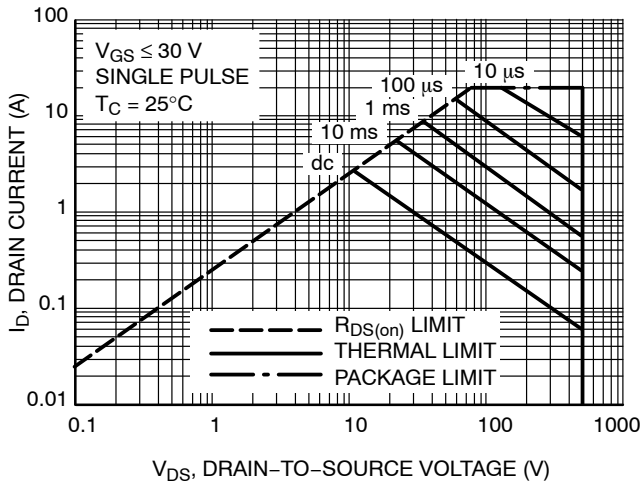


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDF05N50Z

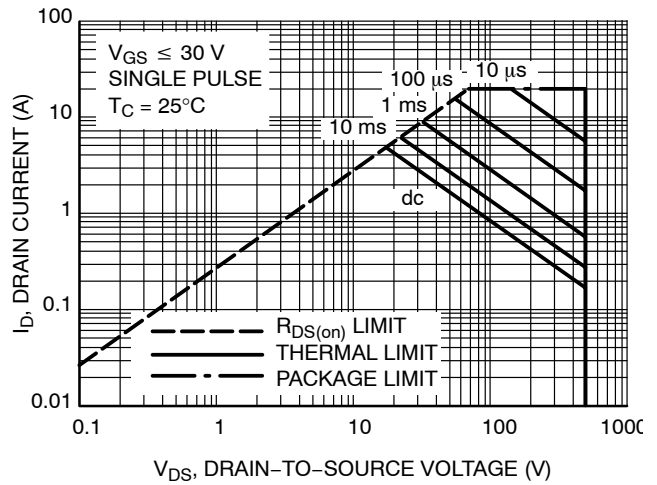


Figure 13. Maximum Rated Forward Biased Safe Operating Area NDD05N50Z

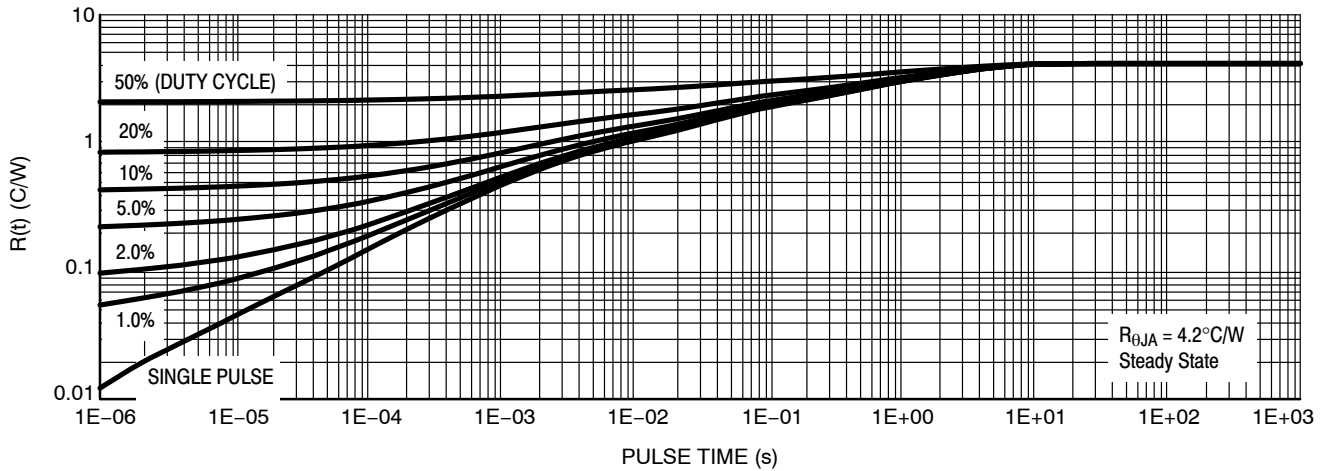


Figure 14. Thermal Impedance (Junction-to-Case) for NDF05N50Z

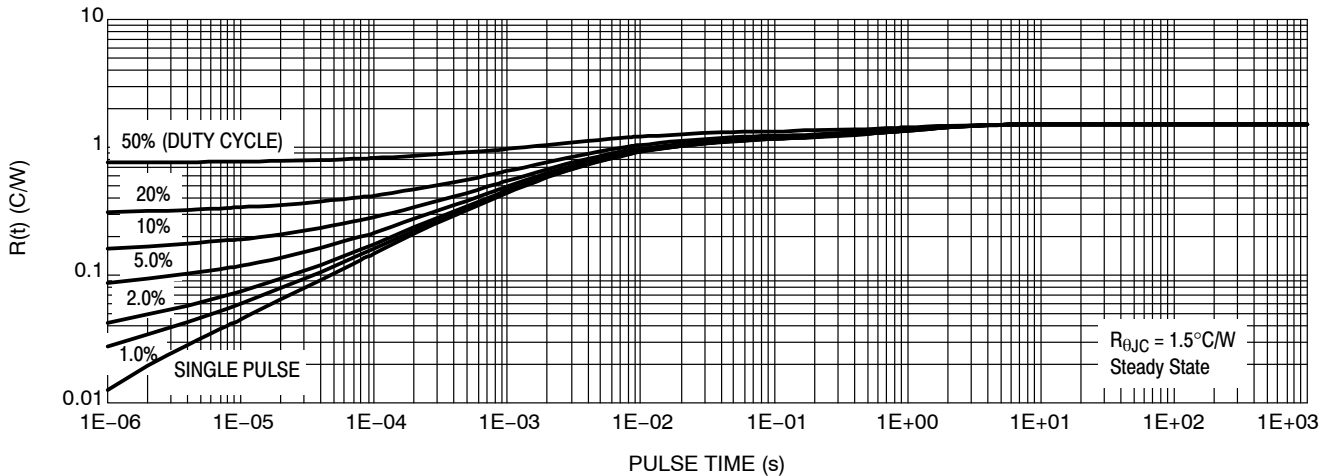


Figure 15. Thermal Impedance (Junction-to-Case) for NDD05N50Z

NDF05N50Z, NDD05N50Z

TYPICAL CHARACTERISTICS

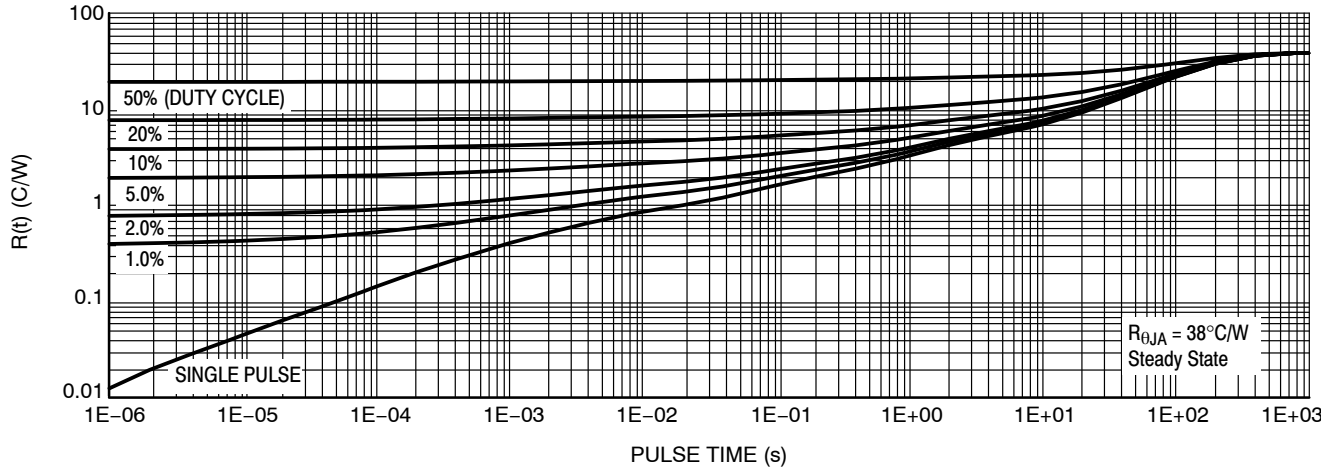


Figure 16. Thermal Impedance (Junction-to-Ambient) for NDD05N50Z

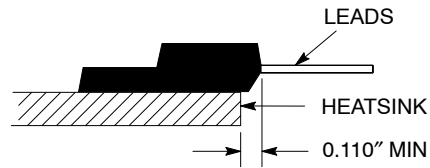


Figure 17. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

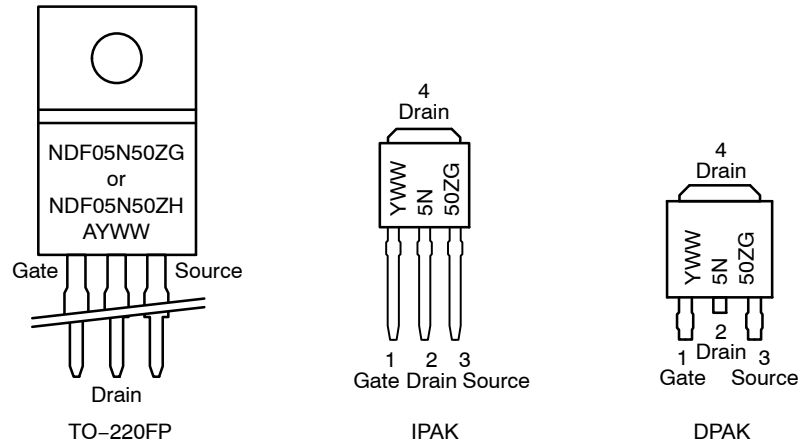
NDF05N50Z, NDD05N50Z

ORDERING INFORMATION

Order Number	Package	Shipping†
NDF05N50ZG	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDF05N50ZH	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDD05N50Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD05N50ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS



A = Location Code
 Y = Year
 WW = Work Week
 G, H = Pb-Free, Halogen-Free Package

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

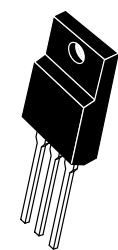


TO-220 FULLPACK, 3-LEAD

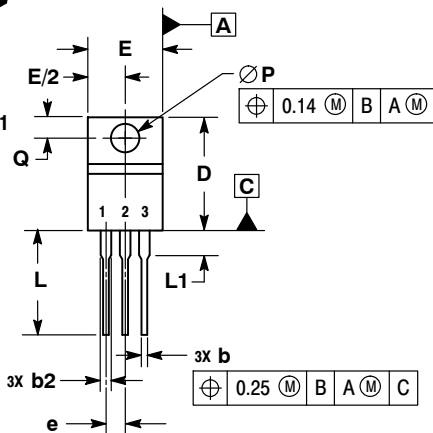
CASE 221AH

ISSUE F

DATE 30 SEP 2014

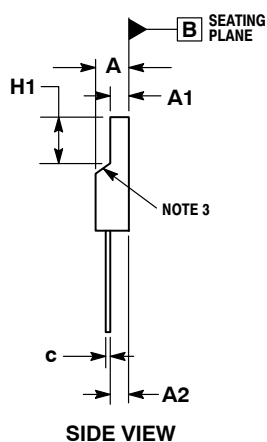
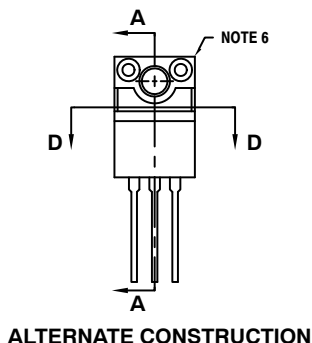


SCALE 1:1



FRONT VIEW

SECTION D-D

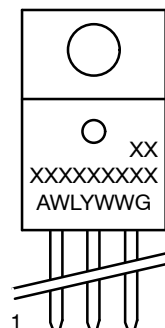


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:

- PIN 1. CATHODE
2. ANODE
3. GATE

DOCUMENT NUMBER: 98AON52577E

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DESCRIPTION: TO-220 FULLPACK, 3-LEAD

PAGE 1 OF 1

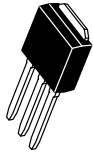
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

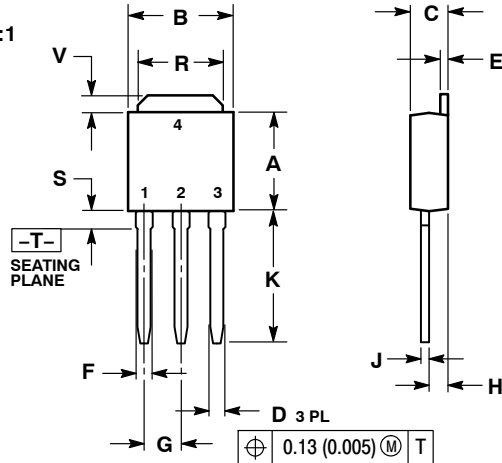
ON



IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

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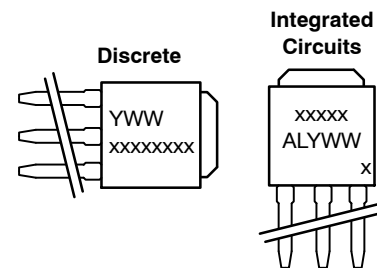


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

MARKING DIAGRAMS

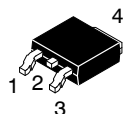
- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



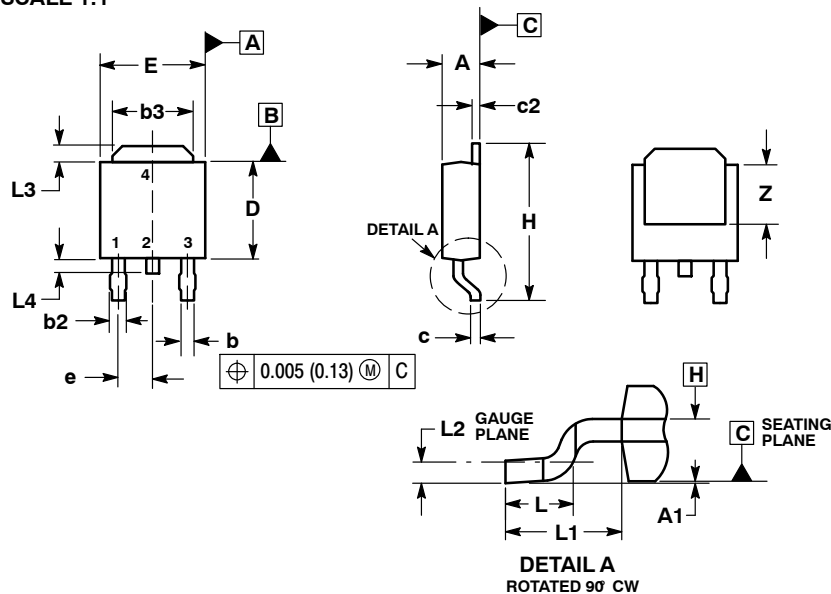
xxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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SCALE 1:1



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

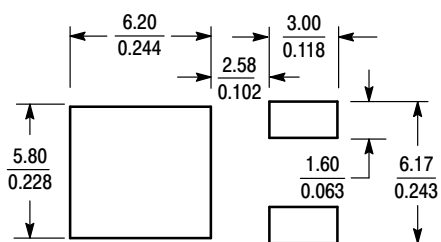
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

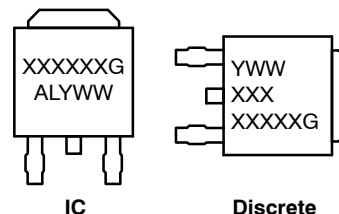
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

GENERIC MARKING DIAGRAM*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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