

PART NUMBER

54ACT11245JT^B

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add vendor CAGE 01295. Change to one part one part number format. Add ground bounce and latch-up immunity tests. Add 10.1 substitution statement. Changes to table I. Editorial corrections throughout. – jak	92-07-09	Monica L. Poelking
B	Change in accordance with NOR 5962-R042-93 - tjr	92-12-29	Monica L. Poelking
C	Change in accordance with NOR 5962-R196-95 – jak	95-09-13	Monica L. Poelking
D	Add device type 03. Add vendor CAGE F8859. Add case outlines X. Add radiation features for device type 01. Update boilerplate to MIL-PRF-38535 requirements. – jak	02-12-18	Thomas M. Hess
E	Add radiation features for device type 03 in section 1.5. Update the boilerplate to include radiation hardness assured requirements for device type 03. Editorial changes throughout. – jak	05-03-15	Thomas M. Hess
F	Update boilerplate to current MIL-PRF-38535 requirements and to include radiation hardness assurance requirements. Add appendix A to document. – LTG	07-05-25	Thomas M. Hess
G	Update dimensions of case outline X to figure 1. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	12-12-19	Thomas M. Hess
H	Update absolute rating maximum supply voltage range in section 1.3 for Vendor cage code F8859 supplying devices.- MAA	17-05-30	Thomas M. Hess
J	Add device with case outline Y for grounded lid for cage code F8859 class V device type 03. Add cage code 3V146 supplier devices. Update boilerplate paragraphs to MIL-PRF-38535 requirements. - MAA	18-08-28	Thomas M. Hess
K	Update boilerplate paragraphs and drawing to current MIL-PRF-38535 requirements. –RDC	23-11-28	Muhammad A Akbar

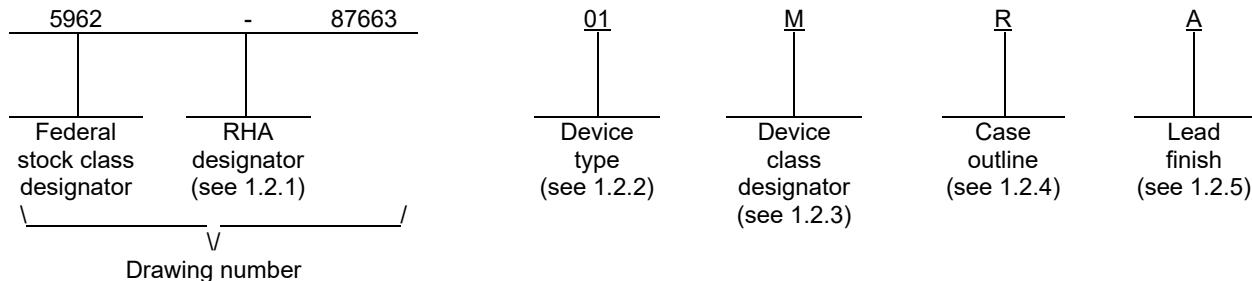


REV																			
SHEET																			
REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30			
REV STATUS OF SHEETS	REV			K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K
PMIC N/A	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14		
STANDARD MICROCIRCUIT DRAWING			PREPARED BY Greg Pitz				DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime												
			CHECKED BY D. A. DiCenzo																
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE			APPROVED BY N. A. Hauck				MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL TRANSCEIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON				REVISION LEVEL K								
			DRAWING APPROVAL DATE 87-08-06																
AMSC N/A			SIZE A				CAGE CODE 67268				SHEET 1 OF 30								

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class B, Q, and M) and space application (device classes S and V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes B, S, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACT245	Octal transceiver with three-state outputs, TTL compatible inputs
02	54ACT11245	Octal transceiver with three-state outputs, TTL compatible inputs
03	54ACT245	Octal transceiver with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
B, S, Q, or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
X	See figure 1	20	Flat pack
Y	See figure 1	20	Flat pack 1/
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

1/ Package case outline Y flat pack with grounded lid.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V _{CC}):	
For device types 01 and 02	-0.5 V dc to +6.0 V dc
For device type 03 (Vendor cage code F8859)	-0.5 V dc to +7.0 V dc
DC input voltage (V _{IN})	-0.5 V dc to V _{CC} + 0.5 V dc
DC output voltage range (V _{OUT})	-0.5 V dc to V _{CC} + 0.5 V dc
Clamp diode current (I _{IK} , I _{OK})	±20 mA
DC output current (I _{OUT})	±50 mA
DC V _{CC} or GND current (I _{CC} , I _{GND})	±200 mA 4/
Storage temperature range (T _{STG})	-65°C to +150°C
Maximum power dissipation (P _D)	500 mW
Lead temperature (soldering, 10 seconds):	
Case outline X	+260°C
All other case outlines except case X	+300°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Junction temperature (T _J)	+175°C
Case operating temperature (T _C)	-55°C to +125°C

1.4 Recommended operating conditions. 2/ 5/

Supply voltage range (V _{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V _{IN})	+0.0 V dc to V _{CC}
Output voltage range (V _{OUT})	+0.0 V dc to V _{CC}
Maximum low level input voltage (V _{IL}):	
V _{CC} = 4.5 V	0.8 V
V _{CC} = 5.5 V	0.8 V
Minimum high level input voltage (V _{IH}):	
V _{CC} = 4.5 V	2.0 V
V _{CC} = 5.5 V	2.0 V
Case operating temperature range (T _C)	-55°C to +125°C
Input rise and fall rate (t _r and t _f) maximum:	
V _{CC} = 4.5 V	10 ns/V
V _{CC} = 5.5 V	8 ns/V
Maximum high level output current (I _{OH})	-24 mA
Maximum low level output current (I _{OL})	24 mA

1.5 Radiation features.

Device type 03:

Maximum total dose available (High dose rate = 50 – 300 Rad (Si)/s) 300 krad(Si) 6/

Heavy ion single event phenomenon(SEP) test:

No single event latchup (SEL) occurs at LET (see 4.4.5.2) ≤ 93 MeV-cm²/mg 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C. Unused inputs must be held high or low.

4/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} or GND pins.

5/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.

6/ Limits obtained during technology characterization/qualification, guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

JESD78 - IC Latch-Up Test.

(Copies of these documents are available online at <https://www.jedec.org>).

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at <https://www.astm.org>).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes B, S, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

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3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1, herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes B, S, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes B, S, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes B, S, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes B, S, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

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TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
High level output voltage 3006	V _{OH1} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	4.5 V	1, 2, 3	4.4		V
	V _{OH2} <u>7/ 8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -50 μA	All All	5.5 V	1, 2, 3	5.4		
	M D P, L, R	01 B, S, Q, V	1	5.4				
				5.4				
				5.4				
	V _{OH3} <u>7/ 8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	4.5 V	1, 2, 3	3.7		
	M D P, L, R	01 B, S, Q, V	1	3.7				
				3.7				
				3.7				
	V _{OH4} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OH} = -24 mA	All All	5.5 V	1, 2, 3	4.7		
Low level output voltage 3007	V _{OL1} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = +50 μA	All All	5.5 V	1, 2, 3	3.85		V
	V _{OL2} <u>7/ 8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = +50 μA	All All	5.5 V	1, 2, 3		0.1	
	M D P, L, R	01 B, S, Q, V	1	3.85				
				3.85				
				3.85				

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/</u> <u>3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Low level output voltage 3007	V _{OL3} <u>7/</u> <u>8/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = +24 mA	All B, S, Q, V	4.5 V	1, 3		0.4	μA
			All M		2		0.5	
			All M		1		0.4	
			M	01 B, S, Q, V	2, 3		0.5	
			D		1		0.4	
			P, L, R				0.4	
	V _{OL4} <u>6/</u>	For all inputs affecting output under test, V _{IN} = V _{IH} = 2.0 V or V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND I _{OL} = +24 mA	All B, S, Q, V	5.5 V	1, 3		0.4	
			All M		2		0.5	
			All M		1		0.4	
			M	01 B, S, Q, V	2, 3		0.5	
			D		1		1.65	
			P, L, R				1.65	
Three-state output leakage current high 3021	I _{OZH} <u>7/</u> <u>8/</u> <u>10/</u>	OE = V _{IH} or V _{IL} V _{IH} = 2.0 V, V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND V _{OUT} = 5.5 V	All B, S, Q, V	5.5 V	1, 2, 3		1.65	μA
			All M		1		0.6	
			All M		2		11.0	
			M	01 B, S, Q, V	1		0.6	
			D		2, 3		11.0	
			P, L, R		1		3.0	
			M, D, P, L, R, F	03 Q, V			10.0	
			M, D, P, L, R, F				20.0	
			M, D, P, L, R, F				5.0	
Three-state output leakage current low 3020	I _{OZL} <u>7/</u> <u>8/</u> <u>10/</u>	OE = V _{IH} or V _{IL} V _{IH} = 2.0 V, V _{IL} = 0.8 V For all other inputs, V _{IN} = V _{CC} or GND V _{OUT} = GND	All B, S, Q, V	5.5 V	1		-0.6	μA
			All M		2		-11.0	
			All M		1		-0.6	
			M	01 B, S, Q, V	2, 3		-11.0	
			D		1		-3.0	
			P, L, R				-10.0	
			M, D, P, L, R, F	03 Q, V			-20.0	
			M, D, P, L, R, F				-5.0	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/ 3/</u> -55°C ≤ T _c ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Positive input clamp voltage 3022	V _{IC+} <u>7/ 8/</u>	For input under test, I _{IN} = 1 mA	All B, S, Q, V	GND	1	0.4	1.5	V
			M		1	0.4	1.5	
			D		1	0.4	1.5	
			P, L, R		1	0.4	1.5	
Negative input clamp voltage 3022	V _{IC-} <u>7/ 8/</u>	For input under test, I _{IN} = -1 mA	All B, S, Q, V	OPEN	1	-0.4	-1.5	V
			M		1	-0.4	-1.5	
			D		1	-0.4	-1.5	
			P, L, R		1	-0.4	-1.5	
Input current high 3010	I _{IH} <u>7/ 8/</u> <u>10/</u>	For input under test, V _{IN} = V _{CC} For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		0.1	μA
					2		1.0	
			All M		1		0.1	
					2, 3		1.0	
			M		1		0.1	
			D		1		0.1	
			P, L, R		1		0.1	
Input current low 3009	I _{IL} <u>7/ 8/</u> <u>10/</u>	For input under test, V _{IN} = GND For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		-0.1	μA
					2		-1.0	
			All M		1		-0.1	
					2, 3		-1.0	
			M		1		-0.1	
			D		1		-0.1	
			P, L, R		1		-0.1	
Control input capacitance 3012	C _{IN}	See 4.4.1c T _c = +25°C	All All	GND	4		10.0	pF
Input/output capacitance 3012	C _{IO}	See 4.4.1c T _c = +25°C	01, 03 All	5.5 V	4		15.0	pF
			02 All	5.0 V	4		24.0	
Power dissipation capacitance	C _{PD} <u>11/</u>	See 4.4.1c T _c = +25°C	01, 03 All	5.0 V	4		85.0	pF
			02 All	5.0 V	4		83.0	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/</u> <u>3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit		
						Min	Max			
Quiescent supply current delta, TTL input levels	ΔI_{CC} <u>7/</u> <u>8/</u> <u>12/</u>	For input under test, V _{IN} = V _{CC} - 2.1 V For all other inputs, V _{IN} = V _{CC} or GND	01 B, S, Q, V	5.5 V	3		1.6	mA		
					1, 2		1.0			
					1, 2, 3		1.6			
					1, 2, 3		1.6			
			All M		1		1.6			
							1.6			
							3.0			
			M	01 B, S, Q, V	5.5 V	1	2.0	μ A		
						2	40.0			
						1	8.0			
			D			2, 3	160.0			
						1	300.0			
							1.0	mA		
			P, L, R				3.0			
							50			
			M, D, P, L, R, F <u>13/</u>	03 Q, V			50	μ A		
							50			
Quiescent supply current, output high 3005	I_{CCH} <u>7/</u> <u>8/</u>	\overline{OE} = GND For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		2.0	μ A		
					2		40.0			
					1		8.0			
					2, 3		160.0			
			M	01 B, S, Q, V		1	300.0			
							1.0	mA		
							3.0			
			P, L, R				50	μ A		
							50			
			M, D, P, L, R, F <u>13/</u>	03 Q, V			50	μ A		
							50			
Quiescent supply current, output low 3005	I_{CCL} <u>7/</u> <u>8/</u>	\overline{OE} = GND For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		2.0	μ A		
					2		40.0			
					1		8.0			
					2, 3		160.0			
			M	01 B, S, Q, V		1	300.0			
							1.0	mA		
							3.0			
			P, L, R				50	μ A		
							50			
			M, D, P, L, R, F <u>13/</u>	03 Q, V			50	μ A		
							50			
Quiescent supply current, outputs three-state 3005	I_{CCZ} <u>7/</u> <u>8/</u>	\overline{OE} = V _{CC} For all other inputs, V _{IN} = V _{CC} or GND	All B, S, Q, V	5.5 V	1		2.0	μ A		
					2		40.0			
					1		8.0			
					2, 3		160.0			
			M	01 B, S, Q, V		1	300.0			
							1.0	mA		
							3.0			
			P, L, R				50	μ A		
							50			
			M, D, P, L, R, F <u>13/</u>	03 Q, V			50	μ A		
							50			

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/</u> <u>3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Low level ground bounce noise	V _{GBL} <u>14/</u> <u>15/</u>	V _{LD} = 2.5 V, I _{OL} = +24 mA See figure 5	All B, S, Q, V	4.5 V	4		2000	mV
High level ground bounce noise	V _{GBH} <u>14/</u> <u>15/</u>	V _{LD} = 2.5 V, I _{OH} = -24 mA See figure 5	All B, S, Q, V	4.5 V	4		2000	mV
Latch-up input/ output over- voltage	I _{CC} (O/V1) <u>16/</u>	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _r ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 10.5 V	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output positive over-current	I _{CC} (O/I1+) <u>16/</u>	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _r ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = +120 mA	All B, S, Q, V	5.5 V	2		200	A
Latch-up input/ output negative over-current	I _{CC} (O/I1-) <u>16/</u>	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _r ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = -120 mA	All B, S, Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I _{CC} (O/V2) <u>16/</u>	t _W ≥ 100 μs, t _{cool} ≥ t _W 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _r ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 9.0 V	All B, S, Q, V	5.5 V	2		100	mA
Truth table test output voltage 3014	<u>7/</u> <u>8/</u> <u>17/</u>	V _{IL} = 0.40 V V _{IH} = 2.40 V Verify output V _{OUT} See 4.4.1	All	4.5 V	7, 8	L	H	
			All	5.5 V	7, 8	L	H	
			M	01 B, S, Q, V	7	L	H	
			D			L	H	
			P, L, R			L	H	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test Conditions <u>2/</u> <u>3/</u> $-55^{\circ}\text{C} \leq T_c \leq +125^{\circ}\text{C}$ $+4.5 \text{ V} \leq V_{CC} \leq +5.5 \text{ V}$ unless otherwise specified	Device type <u>4/</u> and device class	V _{CC}	Group A subgroups	Limits <u>5/</u>		Unit
						Min	Max	
Propagation delay time, data to output, An to Bn and Bn to An 3003	t_{PHL} , t_{PLH} <u>7/</u> <u>8/</u> <u>18/</u> <u>19/</u>	$C_L = 50 \text{ pF}$ minimum $R_L = 500\Omega$ See figure 6	01 B, S, Q, V	4.5 V	9, 11	1.0	8.0	ns
					10	1.0	10.0	
					9, 11	1.0	9.2	
					10	1.0	10.6	
			03 All	4.5 V	9	1.0	8.5	ns
					10, 11	1.0	10.0	
					9	1.0	8.0	
					10, 11	1.0	10.0	
			02 M	4.5 V	9	1.0	9.2	ns
					10, 11	1.0	10.6	
					9	1.0	8.0	
					1.0	8.0	8.0	
			M	4.5 V	9	1.0	8.0	ns
					1.0	8.0	8.0	
					1.0	8.0	8.0	
					1.0	8.0	8.0	
Propagation delay time, output enable, \overline{OE} to An or Bn 3003	t_{PZH} , t_{PZL} <u>7/</u> <u>8/</u> <u>18/</u> <u>19/</u>	$C_L = 50 \text{ pF}$ minimum $R_L = 500\Omega$ See figure 6	01 B, S, Q, V	4.5 V	9, 11	1.0	10.0	ns
					10	1.0	13.0	
					9, 11	1.0	12.0	
					10	1.0	14.1	
			03 All	4.5 V	9	1.0	10.0	ns
					10, 11	1.0	13.0	
					9	1.0	10.0	
					10, 11	1.0	13.0	
			02 M	4.5 V	9	1.0	12.0	ns
					10, 11	1.0	14.1	
					9	1.0	10.0	
					1.0	10.0	10.0	
			M	4.5 V	9	1.0	10.0	ns
					1.0	10.0	10.0	
					1.0	10.0	10.0	
					1.0	10.0	10.0	
Propagation delay time, output disable, \overline{OE} to An or Bn 3003	t_{PHZ} , t_{PLZ} <u>7/</u> <u>8/</u> <u>18/</u> <u>19/</u>	$C_L = 50 \text{ pF}$ minimum, $R_L = 500\Omega$, See figure 6	01 B, S, Q, V	4.5 V	9, 11	1.0	10.0	ns
					10	1.0	12.0	
					9, 10	1.0	12.9	
					11	1.0	14.6	
			03 All	4.5 V	9	1.0	12.0	ns
					10, 11	1.0	13.0	
					9	1.0	10.0	
					10, 11	1.0	12.0	
			02 M	4.5 V	9	1.0	12.9	ns
					10, 11	1.0	14.6	
					9	1.0	10.0	
					1.0	10.0	10.0	
			M	4.5 V	9	1.0	10.0	ns
					1.0	10.0	10.0	
					1.0	10.0	10.0	
					1.0	10.0	10.0	

See footnotes on next sheet.

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TABLE IA. Electrical performance characteristics - Continued.

- 1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table IA herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:
 - a. V_{IC} (pos) tests, the GND terminal can be open. $T_C = +25^\circ C$.
 - b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. $T_C = +25^\circ C$.
 - c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 3/ RHA parts for device type 03 of this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, these devices are only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25^\circ C$.
- 4/ The word "All" in the device type and device class column, means non-RHA limits for all device types and classes. M, D, P, L, R, and/or F in the conditions column are postirradiation limits for those device types and classes specified in the device type and device class column.
- 5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
- 6/ For device classes B, S, Q, and V, this test is guaranteed, if not tested, to the limits specified in table IA.
- 7/ RHA samples do not have to be tested at $-55^\circ C$ and $+125^\circ C$ prior to irradiation.
- 8/ When performing post irradiation electrical measurements for RHA level, $T_A = +25^\circ C$. Limits shown are guaranteed at $T_A = +25^\circ C \pm 5^\circ C$.
- 9/ Transmission driving tests are performed at $V_{CC} = 5.5$ V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = 2.0$ V or 0.8 V.
- 10/ For I_{OZH} and I_{OZL} tests, three-state output conditions are required. For I/O pins, the I_{IH} and I_{IL} measurements shall not be directly performed. These measurements are included in the I_{OZH} and I_{OZL} limits, respectively.
- 11/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$ and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S , n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.
- 12/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits are equal to the number of inputs at a high TTL input level times the ΔI_{CC} maximum limits; and the preferred method and limits are guaranteed.

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TABLE IA. Electrical performance characteristics - Continued.

13/ The maximum limit for this parameter at 100K Rad(si) is 2.0 μ A.

14/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} minimum = ± 24 mA, for example) and 50 pF of load capacitance (see figure 5). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f = 3.5 \pm 1.5$ ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 M Ω impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (figure 5). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

15/ When used in synchronous TTL compatible systems, ground bounce (V_{GBL} and V_{GBH}) = 2,000 mV can be a possible problem.

16/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ± 5 percent.

17/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. The input voltage levels have an allowable tolerance in accordance with MIL-STD-883 already incorporated. For outputs, L < 2.5 V, H \geq 2.5 V. Functional tests at $V_{CC} = 4.5$ V are worst case for RHA specified devices.

18/ Device classes B, S, Q, and V are tested at $V_{CC} = 4.5$ V at $T_C = +125^\circ C$ for sample testing and at $V_{CC} = 4.5$ V at $T_C = +25^\circ C$ for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested. See 4.4.1d.

19/ AC limits at $V_{CC} = 5.5$ V are equal to the limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. Minimum ac limits for $V_{CC} = 5.5$ V are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5$ V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	$T_C =$ temperature $\pm 10^\circ C$	V_{CC}	Effective LET
03	No SEL	+125°C	Bias $V_{CC} = 5.5$ V	LET ≤ 93 MeV-cm 2 /mg

1/ For SEP test conditions, see 4.4.5.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

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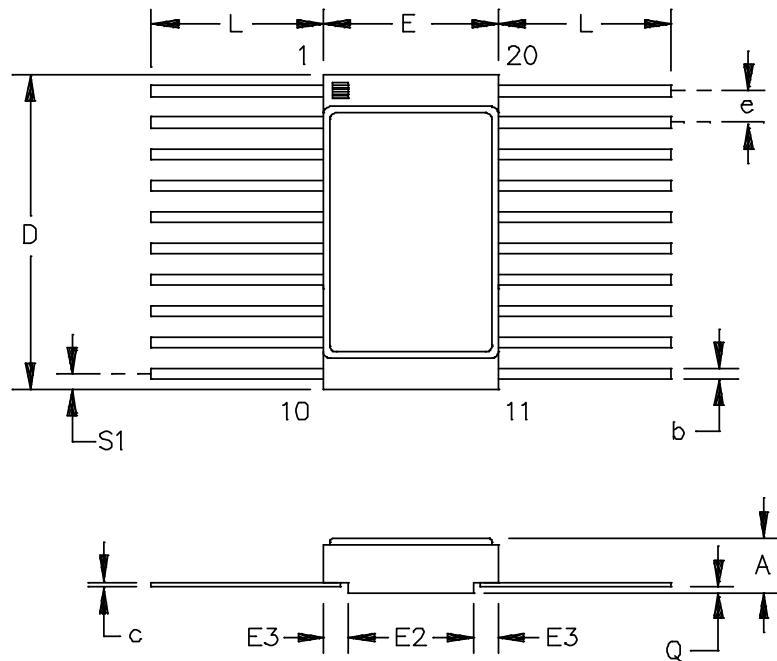
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Case outline X and Y



Symbol	Dimensions					
	Inches			Millimeters		
	Typical	Min	Max	Typical	Min	Max
A		0.075	0.087		1.91	2.21
b		0.015	0.019		0.38	0.48
c		0.003	0.006		0.076	0.152
D		0.505	0.515		12.83	13.08
E		0.275	0.285		6.99	7.24
E2		0.199	0.211		5.05	5.36
E3	0.037			0.95		
e		0.045	0.055		1.14	1.40
L		0.250	0.370		6.35	9.39
Q		0.010	---		0.25	---
S1	0.021			0.55		

Note:

1. Deviation from MIL-STD-1835 REF. F-9, CONFIG. B the dimension c is 0.003 inches minimum instead of 0.004 inches minimum and dimension Q is 0.010 inches Minimum instead of 0.026 inches minimum.
2. Package case outline X flat pack with isolated lid. Package case outline Y flat pack with grounded lid.

FIGURE 1. Case outline X and Y.

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Device types	01, 03	02	
Case outlines	R, S, X, Y and 2	L	3
Terminal number	Terminal symbol		
1	T/R	A0	NC
2	A0	A1	Vcc
3	A1	A2	B3
4	A2	A3	B2
5	A3	GND	B1
6	A4	GND	B0
7	A5	GND	T/R
8	A6	GND	NC
9	A7	A4	A0
10	GND	A5	A1
11	B7	A6	A2
12	B6	A7	A3
13	B5	OE	GND
14	B4	B7	GND
15	B3	B6	NC
16	B2	B5	GND
17	B1	B4	GND
18	B0	Vcc	A4
19	OE	Vcc	A5
20	Vcc	B3	A6
21	---	B2	A7
22	---	B1	NC
23	---	B0	OE
24	---	T/R	B7
25	---	---	B6
26	---	---	B5
27	---	---	B4
28	---	---	Vcc

NC = No internal connection

FIGURE 2. Terminal connections.

All device types			
Inputs		Output	
OE	T/R		
L	L	Bus B data to Bus A	
L	H	Bus A data to Bus B	
H	X	High Z state	

H = High voltage level

L = Low voltage level

X = Irrelevant

Z = High impedance

NOTE: When OE = H, all inputs and outputs are in the Z state.

FIGURE 3. Truth table.

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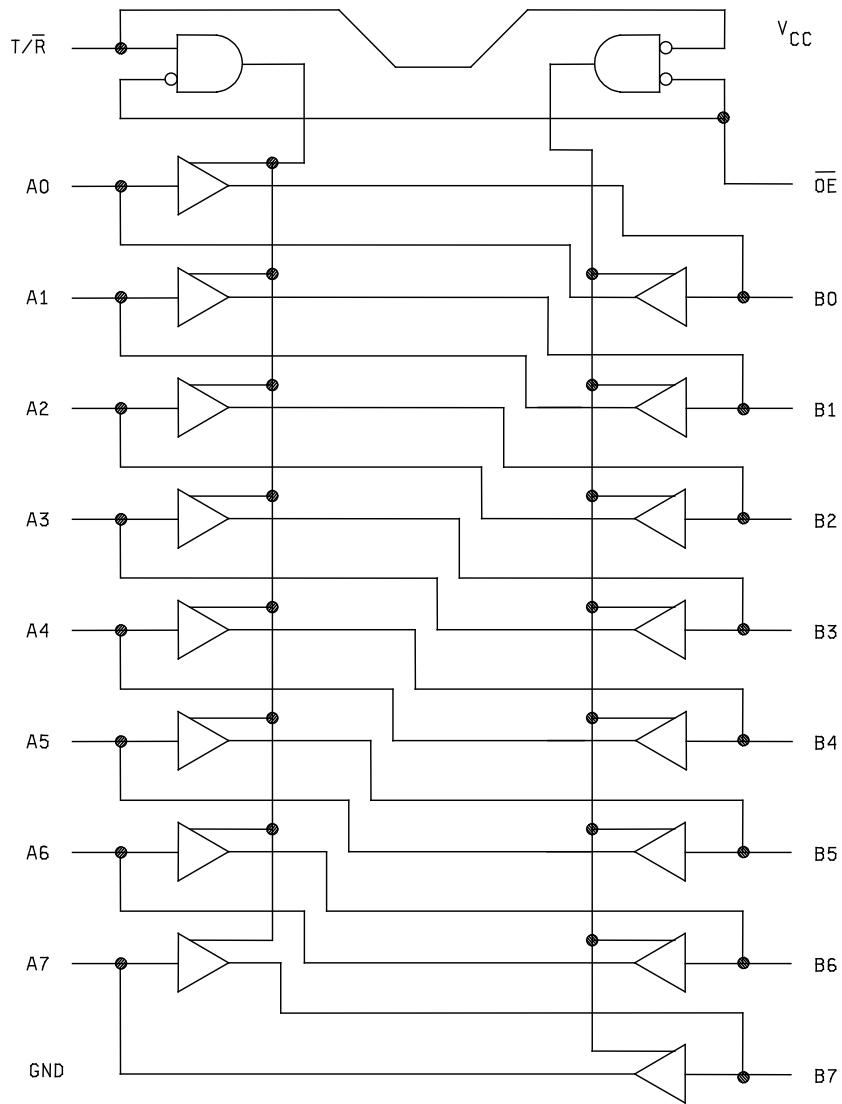


FIGURE 4. Logic diagram.

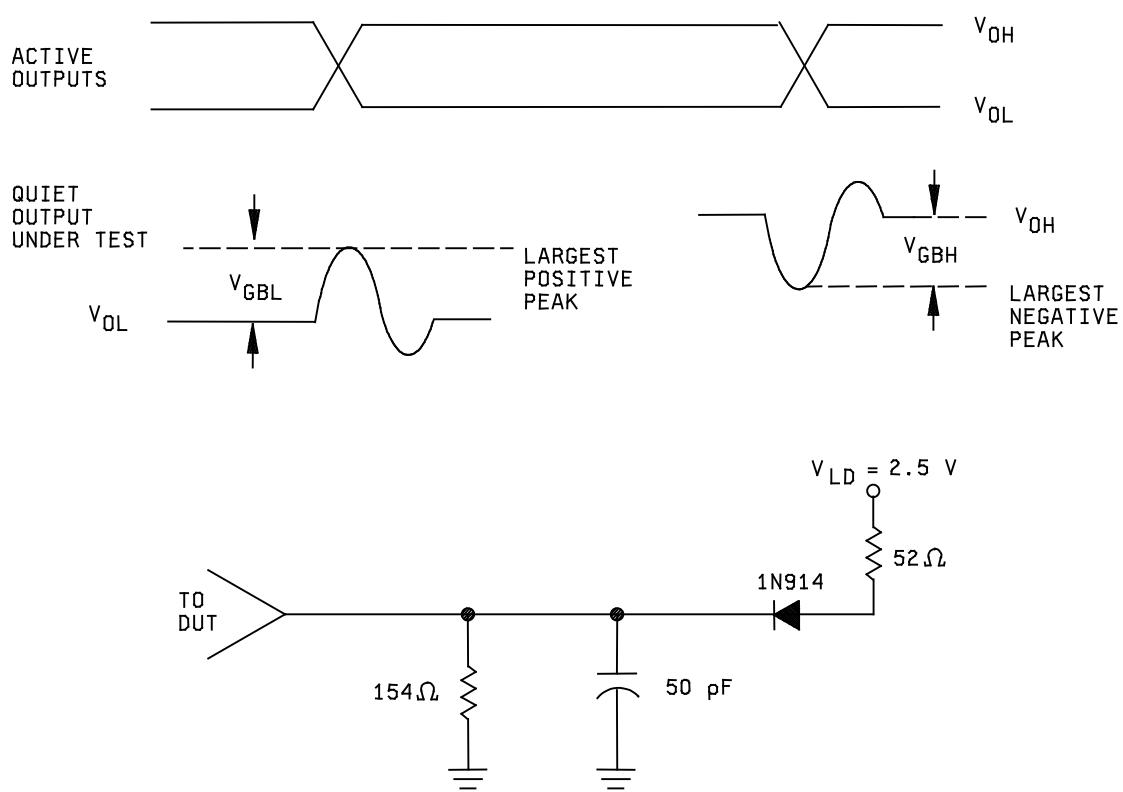
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NOTE: Resistor and capacitor tolerances = $\pm 10\%$.

FIGURE 5. Ground bounce waveforms and test circuit.

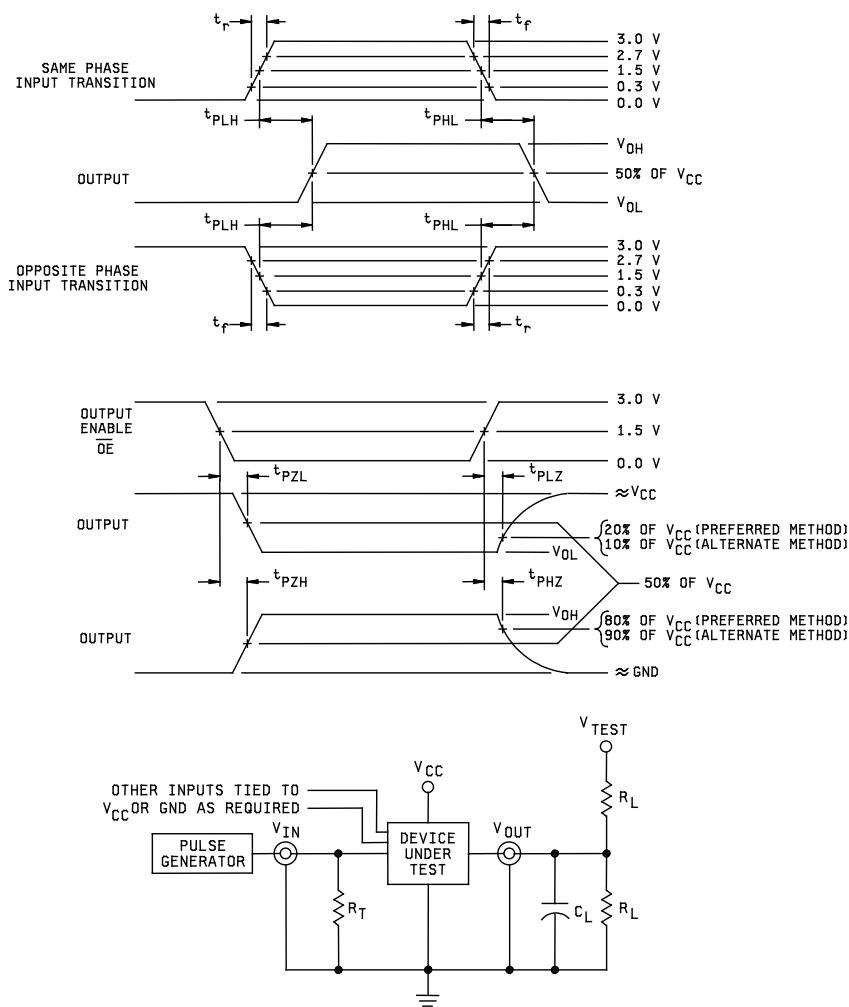
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NOTES:

1. Preferred method - used for device type 02:
 - When measuring t_{PHZ} and t_{PZH} : $V_{TEST} = GND$
 - When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$
 - When measuring t_{PLH} and t_{PHL} : $V_{TEST} = \text{open}$
- Alternate method - used for device types 01 and 03:
 - When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$
 - When measuring t_{PHZ} , t_{PZH} , t_{PLH} , and t_{PHL} : $V_{TEST} = \text{open}$
2. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
3. $R_T = 50\Omega$ or equivalent. $R_L = 500\Omega$ or equivalent.
4. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 3 \text{ ns}$; $t_f \leq 3 \text{ ns}$; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. Outputs are measured one at a time with one output per measurement.

FIGURE 6. Switching waveforms and test circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes B, S, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes B, S, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

- (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- (2) $T_A = +125^\circ\text{C}$, minimum.
- (3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 test requirements of table IIA herein.
- (4) For device class M, unless otherwise specified, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.
- (5) Unless otherwise specified in the QM plan for static burn-in, device class B and S, test condition A, method 1015 of MIL-STD-883, test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table IA of method 1015 for class B devices.
 - (a) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2 \pm 0.5\text{ V}$. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5\text{ V}$. $R1 = 220\Omega$ to $47\text{ k}\Omega$.
 - (b) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC} . Outputs may be open or connected to $V_{CC}/2 \pm 0.5\text{ V}$. Resistors R1 are optional in open outputs and required on outputs connected to $V_{CC}/2 \pm 0.5\text{ V}$. $R1 = 220\Omega$ to $47\text{ k}\Omega$.
 - (c) $V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$, -0.00 V .
- (6) Unless otherwise specified in the QM plan for dynamic burn-in, device classes B and S, test condition D, method 1015 of MIL-STD-883, the following shall apply:
 - (a) Input resistors = 220Ω to $2\text{ k}\Omega \pm 20\text{ percent}$.
 - (b) Output resistors = $220\Omega \pm 20\text{ percent}$.
 - (c) $V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$, -0.00 V .
 - (d) The output enable control pin(s) shall be connected through the resistors in parallel to V_{CC} or GND, as applicable, to enable the outputs. All other inputs shall be connected through the resistors in parallel to a common clock pulse (CP), as applicable. Outputs shall be connected through the resistors to $V_{CC}/2 \pm 0.5\text{ V}$.
 - (e) $CP = 25\text{ kHz}$ to 1 MHz square wave; duty cycle = $50\text{ percent} \pm 15\text{ percent}$; $V_{IH} = 4.5\text{ V}$ to V_{CC} , $V_{IL} = 0\text{ V} \pm 0.5\text{ V}$; $t_r, t_f \leq 100\text{ ns}$.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

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4.2.2 Additional criteria for device classes B, S, Q, and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device classes Q or B shall be as specified in MIL-PRF-38535, appendix B.

4.2.3 Percent defective allowable (PDA).

- a. The PDA for class S or V devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.
- b. Static burn-in I and II failures shall be cumulative for determining the PDA.
- c. The PDA for class B or Q devices shall be in accordance with MIL-PRF-38535 for static burn-in. Dynamic burn-in is not required.
- d. The PDA for class M devices shall be in accordance with MIL-PRF-38535, appendix A for static burn-in and dynamic burn-in.
- e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table IA subgroup 1, are defective and shall be removed from the lot. The verified number of failed devices times 100, divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection for device classes B, S, Q, and V. Qualification inspection for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Latch-up and ground bounce tests are required for device classes B, S, Q, and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground bounce tests, test all applicable pins on five devices with zero failures.
- c. C_{IN} , $C_{I/O}$, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and $C_{I/O}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard JESD20 and table IA herein. For C_{IN} , $C_{I/O}$, and C_{PD} , test all applicable pins on five devices with zero failures.
- d. For device classes B, S, Q, and V, subgroups 9 and 11 tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.
- e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall test all possible input to output logic patterns. For device classes B, S, Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups 1/ (in accordance with MIL-STD-883, method 5005, table IA)	Subgroups 1/ (in accordance with MIL-PRF-38535, table III)			
		Device 2/ class M	Device 2/ class B	Device 2/ class S	Device class Q
Interim electrical parameters, method 5004		1	1	1	1
Static burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Static burn-in II, method 1015 (4.2.1a)	3/	Required 6/	Required 4/	Required 6/	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)		1 2/ , 5/	1 2/ , 5/	1 2/ , 5/	1 2/ , 5/
Dynamic burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Final electrical parameters, method 5004	1, 2, 3, 7, 8, 9 2/	1, 2, 7, 9 2/ , 6/	1, 2, 7, 9 2/	1, 2, 3, 7, 8, 9, 10, 11 2/ , 6/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements, method 5005 (4.4.1)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters, method 5005 (4.4.2)			1, 2, 3, 7, 8, 9, 10, 11 5/		
Group C end-point electrical parameters, method 5005 (4.4.3)	1, 2, 3	1, 2 5/		1, 2, 3 5/	1, 2, 3, 7, 8, 9, 10, 11 5/
Group D end-point electrical parameters, method 5005 (4.4.4)	1, 2, 3	1, 2	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters, method 5005 (4.4.5)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).

3/ The burn-in shall meet the requirements of 4.2.1a herein.

4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.

5/ Delta limits shall be required only on table IA, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.

6/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table IIA).

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TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device types	Delta limits
Supply current	I _{CCH} , I _{CCL} , I _{CCZ}	01 2/	±100 nA
		03	±300 nA
Supply current delta	ΔI _{CC}	03	±0.4 mA
Input current low level	I _{IL}	03	±20 nA
Input current high level	I _{IH}	03	±20 nA
Output voltage low level V _{CC} = 5.5 V I _{OL} = 24 mA	V _{OL}	03	±0.04 V
Output voltage high level V _{CC} = 5.5 V I _{OH} = -24 mA	V _{OH}	03	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ This parameter is not production tested.

4.4.2 Group B inspection. When applicable, the group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady steady-state life tests, the test circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- T_A = +125°C, minimum.
- Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes B, S, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- End-point electrical parameters shall be as specified in table IIA herein.
- For device classes B, S, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

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4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A, and as specified herein.

Device type 03:

- a. Inputs tested high, $V_{CC} = 5.5 \text{ V dc} \pm 5\%$, $V_{IN} = 5.0 \text{ V dc} + 10\%$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.
- b. Inputs tested low, $V_{CC} = 5.5 \text{ V dc} \pm 5\%$, $V_{IN} = 0.0 \text{ V dc}$, $R_{IN} = 1 \text{ k}\Omega \pm 20\%$, and all outputs are open.

4.4.5.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k Rad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at $25^\circ\text{C} \pm 5^\circ\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.5.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 or JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7 \text{ ions/cm}^2$.
- c. The flux shall be between 10^2 and $10^5 \text{ ions/cm}^2/\text{s}$. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be $+25^\circ\text{C}$ for the upset measurements and the maximum rated operating temperature $\pm 10^\circ\text{C}$ for the latch-up measurements.
- f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class B and Q devices will replace device class M devices.

6.1.2.1 Substitution data.

New PIN	Old PIN
5962-8766301MRA	5962-8766301RA
5962-8766301MSA	5962-8766301SA
5962-8766301M2A	5962-87663012A

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6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes B, S, Q, and V. Sources of supply for device classes B, S, Q, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

- a. RHA test conditions of SEP.
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Occurrence of latch-up (SEL).

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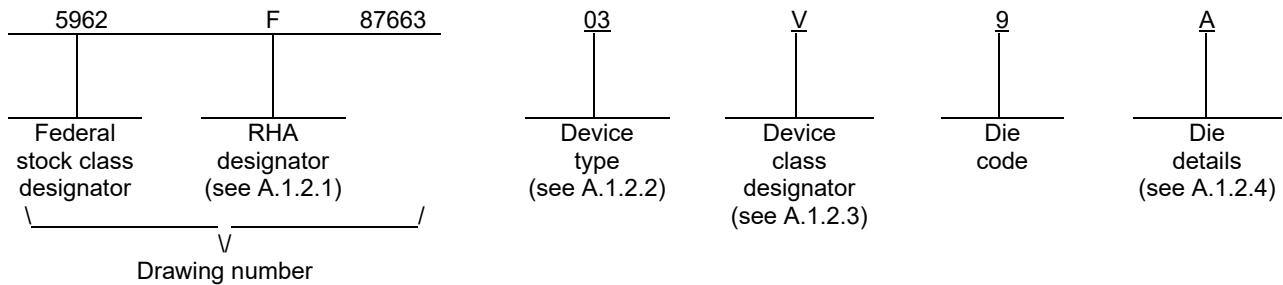
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
03	54ACT245	Octal transceiver with three-state outputs, TTL compatible inputs

A.1.2.3 Device class designator. Device class Q designator will not be included in the PIN and will not be marked on the device since the device class designator has been added after the original issuance of this drawing.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2. APPLICABLE DOCUMENTS

A.2.1 Government specification, standards, and handbooks. The following specification, standard, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

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A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

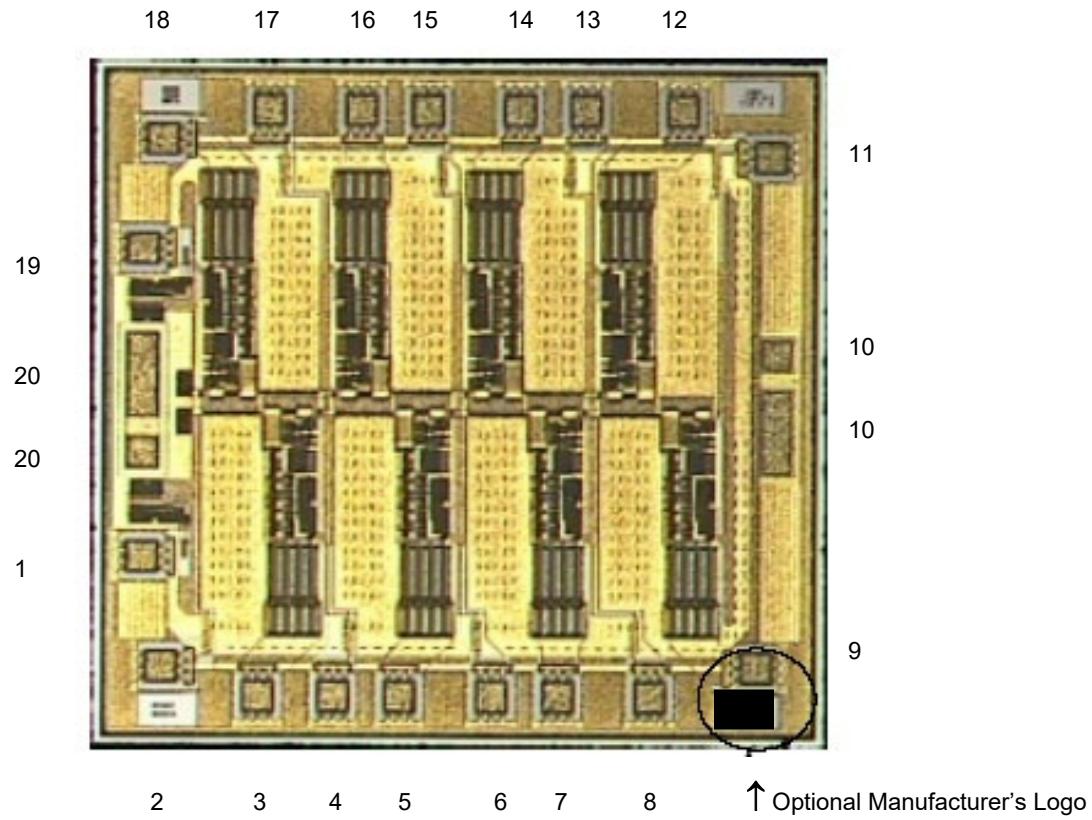
A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0540.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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Pad size: Pad numbers 1 to 9 and 11 to 19: 100 x 100 μm
Pad numbers 10 (GND) and 20 (V_{cc}): 100 x 280 μm

NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1 Die bonding pad locations and electrical functions.

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Die physical dimensions.

Die size: 2408 x 2250 μm
Die thickness: 285 \pm 25 μm

Interface materials.

Top metallization: Al Si Cu 0.85 μm
Backside metallization: None
Glassivation.
Type: P. Vapox + Nitride
Thickness: 0.5 μm – 0.7 μm
Substrate: Silicon

Assembly related information.

Substrate potential: Floating or tied to GND
Special assembly instructions: Bond pad #20 (V_{CC}) first

FIGURE A-1 Die bonding pad locations and electrical functions – Continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-11-28

Approved sources of supply for SMD 5962-87663 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8766301RA	0C7V7	54ACT245DMQB
		QP54ACT245DMQB
5962-8766301SA	0C7V7	54ACT245FMQB
		QP54ACT245FMQB
5962-87663012A	0C7V7	54ACT245LMQB
		QP54ACT245LMQB
5962-8766301MRA	01295	SNJ54ACT245J
	0C7V7	54ACT245DMQB
		QP54ACT245DMQB
	3V146	54ACT245/QRA
5962-8766301MSA	<u>3</u> /	54ACT245
	01295	SNJ54ACT245W
	0C7V7	54ACT245FMQB
		QP54ACT245FMQB
	3V146	54ACT245/QSA
5962-8766301M2A	01295	SNJ54ACT245FK
	0C7V7	54ACT245LMQB
		QP54ACT245LMQB
	3V146	54ACT245/Q2A
5962-8766301BRA	0C7V7	JM54ACT245BRA
		QP54ACT245DMQB
	3V146	54ACT245/BRA
5962-8766301B2A	0C7V7	JM54ACT245B2A
		QP54ACT245LMQB
	3V146	54ACT245/B2A
5962-8766301BSA	0C7V7	JM54ACT245BSA
		QP54ACT245FMQB
	3V146	54ACT245/BSA
5962-8766301SRA	01295	SNV54ACT245J
5962-8766301SSA	01295	SNV54ACT245W
5962-8766301S2A	<u>3</u> /	54ACT245
5962-8766302M3A	3V146	54ACT11245/B3A
5962-8766302MLA	3V146	54ACT11245/BLA
5962-8766303QXA	<u>3</u> /	54ACT245K02Q
5962-8766303QXC	<u>3</u> /	54ACT245K01Q
5962-8766303VXA	<u>3</u> /	54ACT245K02V

See footnotes on next sheet.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 23-11-28

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8766303VXC	<u>3/</u>	54ACT245K01V
5962R8766301BRA	<u>3/</u>	JM54ACT245BRA-R
5962R8766301BSA	<u>3/</u>	JM54ACT245BSA-R
5962R8766301B2A	<u>3/</u>	JM54ACT245B2A-R
5962R8766301SRA	<u>3/</u>	JM54ACT245SRA-R
5962R8766301SSA	<u>3/</u>	JM54ACT245SSA-R
5962R8766301S2A	<u>3/</u>	JM54ACT245S2A-R
5962F8766303QXA	F8859	RHFACT245K02Q
5962F8766303QXC	F8859	RHFACT245K01Q
5962F8766303VXA	F8859	RHFACT245K02V
5962F8766303VYA	F8859	RHFACT245K04V
5962F8766303VXC	F8859	RHFACT245K01V
5962F8766303VYC	F8859	RHFACT245K03V
5962F8766303QRA	F8859	RHFACT245D04Q
5962F8766303QRC	F8859	RHFACT245D03Q
5962F8766303VRA	F8859	RHFACT245D04V
5962F8766303VRC	F8859	RHFACT245D03V
5962F8766303V9A	F8859	ACT245DIE2V

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243
0C7V7	Teledyne e2v, Inc. 765 Sycamore Drive Milpitas, CA 95035
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950

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