Rochester Electronics®

Datasheet

ICL7662

CMOS Voltage Converter

The Harris ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of -4.5V to -20V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

HARRIS SEMICONDUCTOR

ICL7662

February 1994

CMOS Voltage Converter

Features

- **No External Diode Needed Over Entire Temperature Range**
- **Pin Compatible With ICL7660**
- **Simple Conversion of +15V Supply to -15V Supply**
- **Simple Voltage Multiplication (V_{OUT} = (-)nV_{IN})**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **96% Typical Power Efficiency**
- **Wide Operating Voltage Range 4.5V to 20.0V**
- **Easy to Use - Requires Only 2 External Non-Critical Passive Components**

Applications

- **On Board Negative Supply for Dynamic RAMs**
- **Localized μProcessor (8080 Type) Negative Supplies**
- **Inexpensive Negative Supplies**
- **Data Acquisition Systems**
- **Up to -20V for Op Amps**

Description

The Harris ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of -4.5V to -20V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V input.

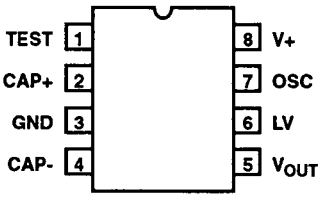
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0V. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

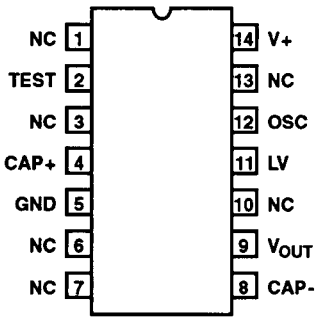
The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10V to +20V), the LV pin is left floating to prevent device latchup.

Pinouts

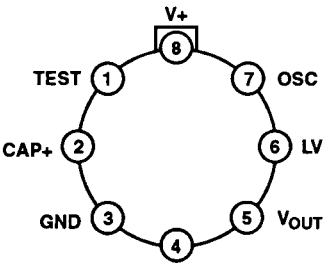
ICL7662 (DIP)
TOP VIEW



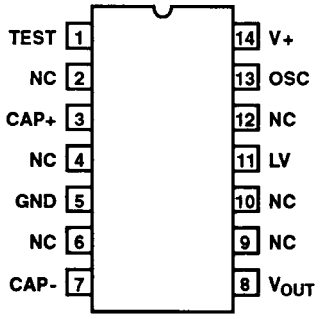
ICL7662CBD AND IBD (SOIC)
TOP VIEW



ICL7662 (CAN)
TOP VIEW



ICL7662CBD-0 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3181.1**

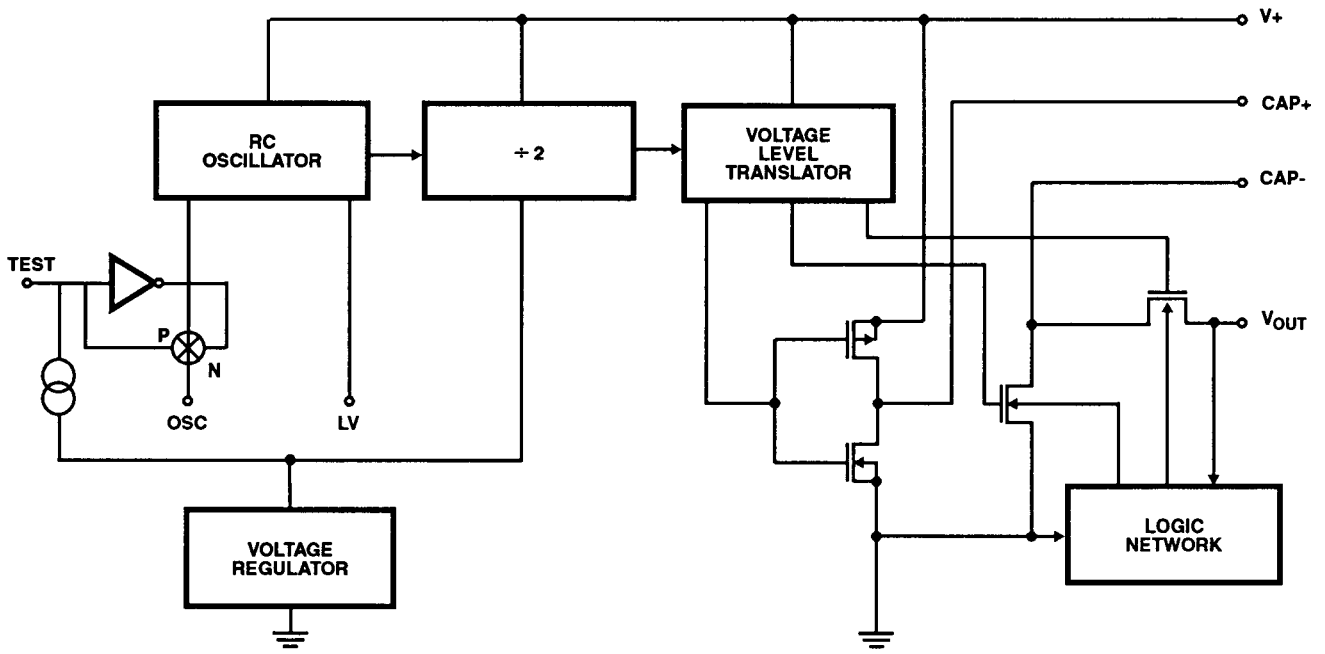
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7662CTV	0°C to +70°C	8 Pin TO-99 Can
ICL7662CPA		8 Lead PDIP
ICL7662CBD-0		14 Lead SOIC
ICL7662CBD		14 Lead SOIC
ICL7662ITV	-40°C to +85°C	8 Pin TO-99 Can
ICL7662IPA		8 Lead PDIP
ICL7662IBD		14 Lead SOIC
ICL7662MTV (Note 1)	-55°C to +125°C	8 Pin TO-99 Can

NOTE:

1. Add /883 to part number if /883B processing is required.

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage 22V
Oscillator Input Voltage..... -0.3V to (V+ +0.3V) for V+ < 10V
..... (V+ -10V) to (V+ +0.3V) for V+ > 10V
(Note 1)
Current Into LV (Note 1) ..... 20µA for V+ > 10V
Output Short Duration ..... Continuous

Power Dissipation (Note 2)
ICL7662CTV, ICL7662ITV, ICL7662MTV..... 500mW
ICL7662CPA, ICL7662IPA..... 500mW
ICL7662CBD, ICL7662CBD-0, ICL7662IBD 500mW
Lead Temperature (Soldering, 10s)..... 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = 15V$, $T_A = +25°C$, $C_{OSC} = 0$, Unless Otherwise Specified. Refer to Figure 1.

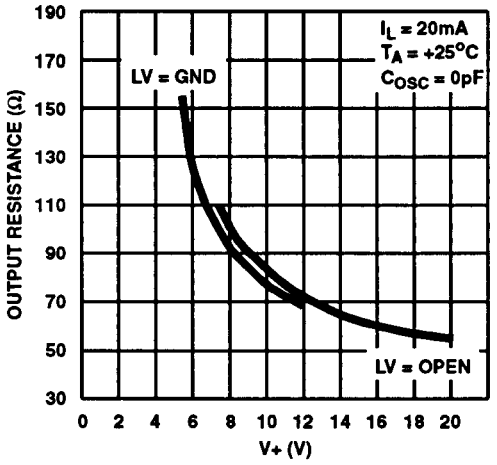
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range - Lo	V+L	$R_L = 10k\Omega$, LV = GND	Min < T_A < Max	4.5	-	11	V
Supply Voltage Range - Hi	V+H	$R_L = 10k\Omega$, LV = Open	Min < T_A < Max	9	-	20	V
Supply Current	I+	$R_L = \infty$, LV = Open	$T_A = +25°C$	-	0.25	0.60	mA
			$0°C < T_A < +70°C$ $-40°C < T_A < +85°C$	-	0.30	0.85	mA
			$-55°C < T_A < +125°C$	-	0.40	1.0	mA
Output Source Resistance	R_O	$I_O = 20mA$, LV = Open	$T_A = +25°C$	-	60	100	Ω
			$0°C < T_A < +70°C$ $-40°C < T_A < +85°C$	-	70	120	Ω
			$-55°C < T_A < +125°C$	-	90	150	Ω
Supply Current	I+	V+ = 5V, $R_L = \infty$, LV = GND	$T_A = +25°C$	-	20	150	µA
			$0°C < T_A < +70°C$ $-40°C < T_A < +85°C$	-	25	200	µA
			$-55°C < T_A < +125°C$	-	30	250	µA
Output Source Resistance	R_O	V+ = 5V, $I_O = 3mA$, LV = GND	$T_A = +25°C$	-	125	200	Ω
			$0°C < T_A < +70°C$ $-40°C < T_A < +85°C$	-	150	250	Ω
			$-55°C < T_A < +125°C$	-	200	350	Ω
Oscillator Frequency	FOSC			-	10	-	kHz
Power Efficiency	P_{EFF}	$R_L = 2K\Omega$	$T_A = +25°C$	93	96	-	%
			Min < T_A < Max	90	95	-	%
Voltage Conversion Efficiency	VoEf	$R_L = \infty$	Min < T_A < Max	97	99.9	-	%
Oscillator Sink or Source Current	I_{OSC}	V+ = 5V (V_{OSC} = 0V to +5V)		-	0.5	-	µA
		V+ = 15V (V_{OSC} = +5V to +15V)		-	4.0	-	µA

NOTES:

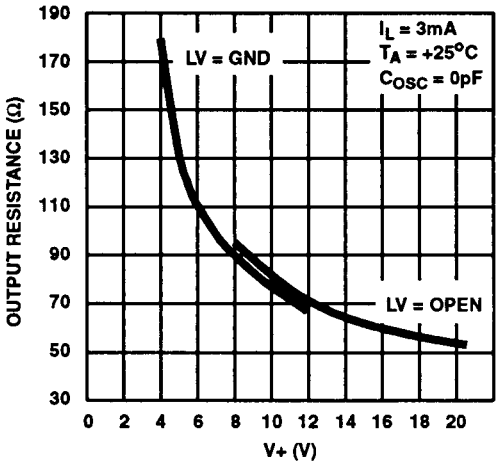
1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660S.
2. Derate linearly above 50°C by 5.5mW/°C.
3. Pin 1 is a Test pin and is not connected in normal use. When the TEST pin is connected to V+, an internal transmission gate disconnects any external parasitic capacitance from the oscillator which would otherwise reduce the oscillator frequency from its nominal value.

Performance Curves (See Figure 1, Test Circuit)

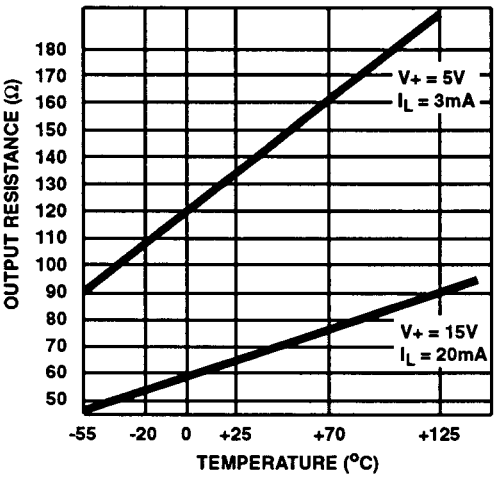
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



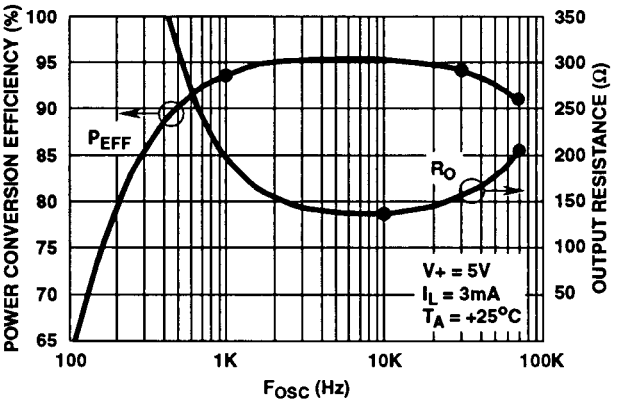
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



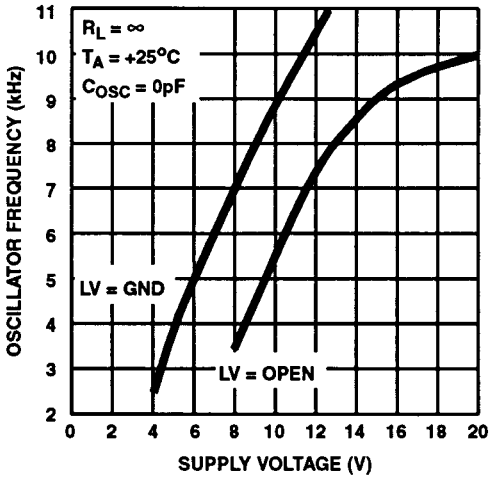
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



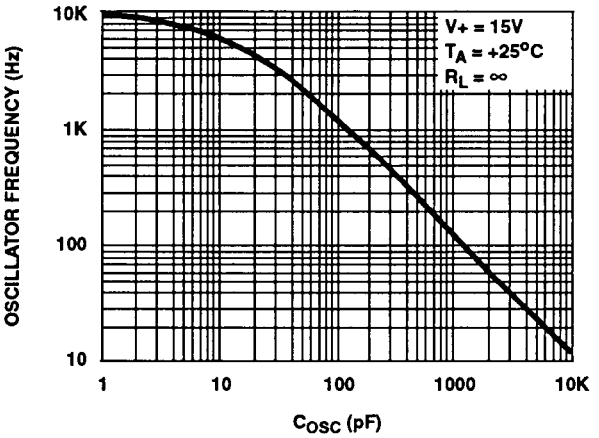
POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



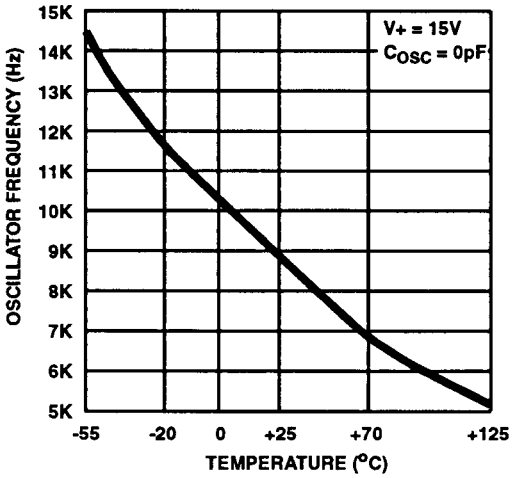
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE



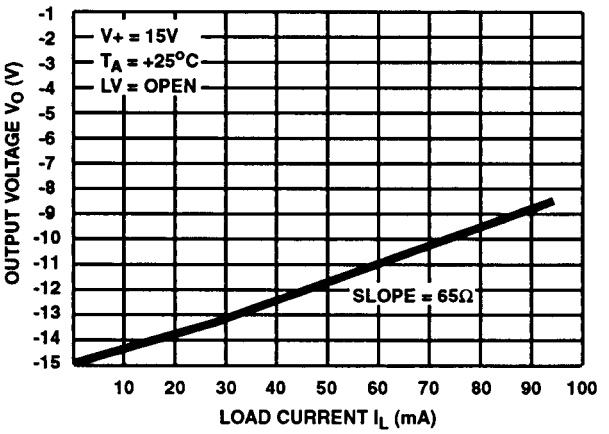
NOTE: All typical values have been characterized but are not tested.

Performance Curves (See Figure 1, Test Circuit) (Continued)

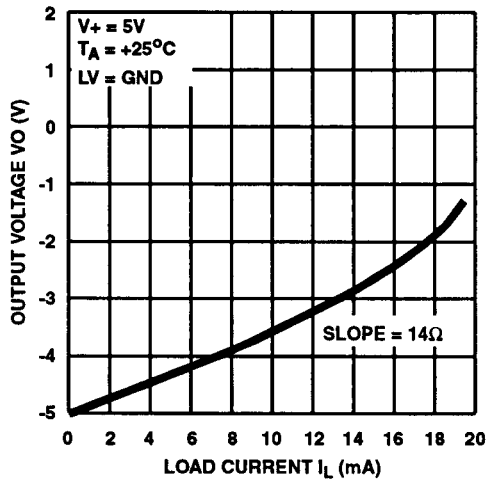
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



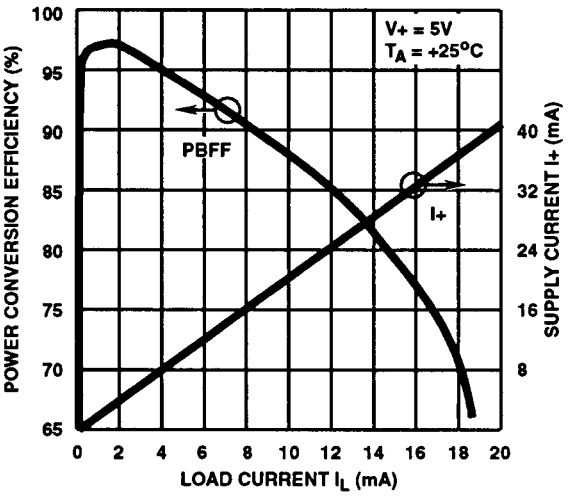
OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



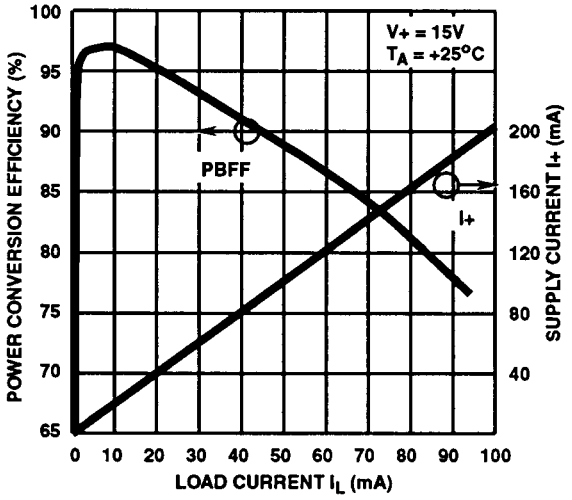
OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



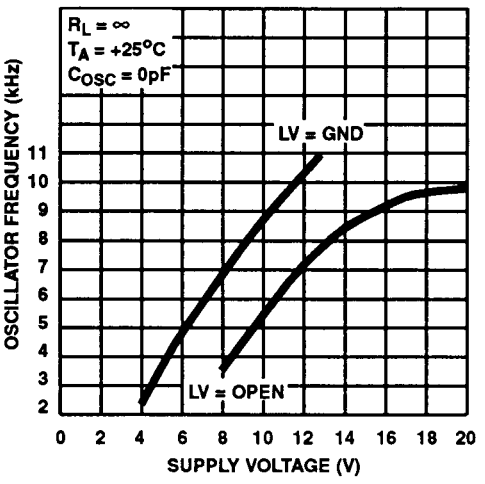
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD



SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

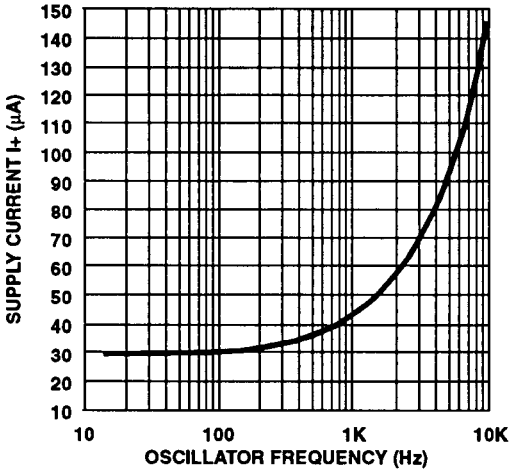


FREQUENCY OF OSCILLATION AS A FUNCTION OF SUPPLY VOLTAGE



Performance Curves (See Figure 1, Test Circuit) (Continued)

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



NOTE 4. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.

Circuit Description

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7662, the 4 switches of Figure 2 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 10V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

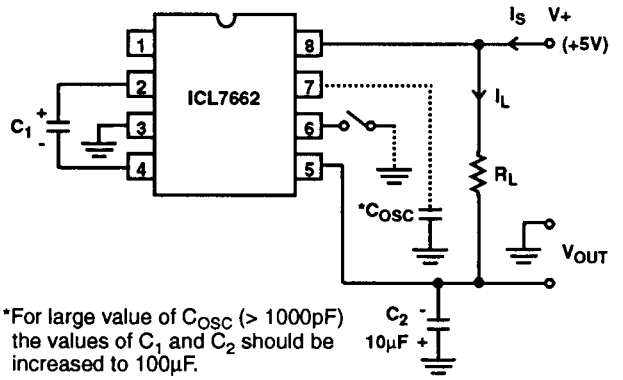


FIGURE 1. ICL7662 TEST CIRCUIT

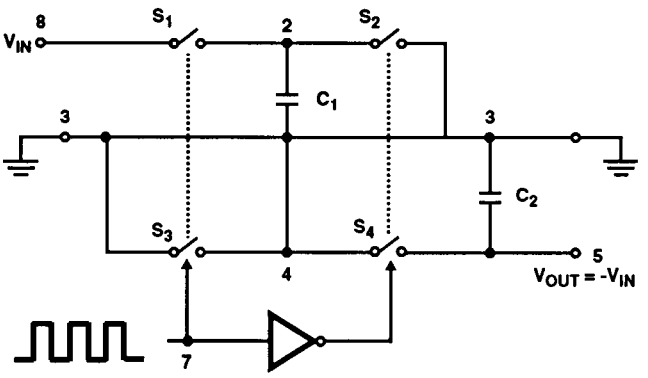


FIGURE 2. IDEALIZED NEGATIVE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's and Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 10V.
3. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7662 and the + terminal of C_2 must be connected to GROUND.
4. If the voltage supply driving the 7662 has a large source impedance (25W - 30W), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
5. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 3 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 10V.

The output characteristics of the circuit in Figure 3A can be approximated by an ideal voltage source in series with a resistance as shown in Figure 3B. The voltage source has a value of -(V+). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C_1 and C_2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESRC_1) + 2(R_{SW2} + R_{SW4} + ESRC_1) + \frac{1}{f_{PUMP} \times C_1} + ESRC_2$$

$$(f_{PUMP} = \frac{f_{OSC}}{2} \quad R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESRC_1 + ESRC_2\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 24Ω at +25°C and 15V, and 53Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C_1)$ component, and low FSR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C_1)$ term, but may have the side effect of a net increase in output impedance when $C_1 > 10\mu F$ and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10kHz and $C = C_1 = C_2 = 10\mu F$:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4\ ESRC_1 + ESRC_2$$

$$R_O \cong 46 + 20 + 5 \times ESR_C\Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

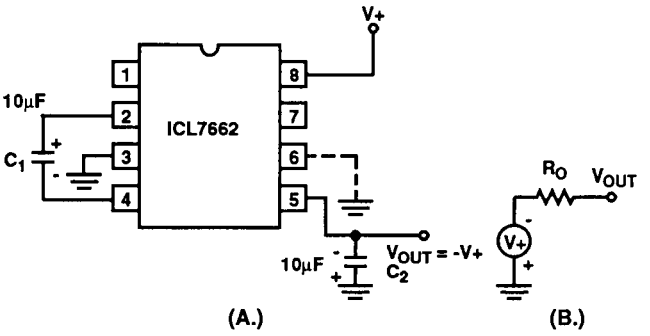


FIGURE 3. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2V, A and B, as shown in Figure 4. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flowing into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is 2 x I_{OUT}, hence the total drop is 2 x I_{OUT} x $ESRC_2V$. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current the load. The drop at B is $I_{OUT} \times t_2/C_2V$. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left(\frac{1}{2 \times f_{PUMP} \times C_2} + 2\ ESRC_2 \times I_{OUT} \right)$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7662 voltage converters may be paralleled (Figure 5) to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7662})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7662 may be cascaded as shown in Figure 6 to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662 R_{OUT} values.

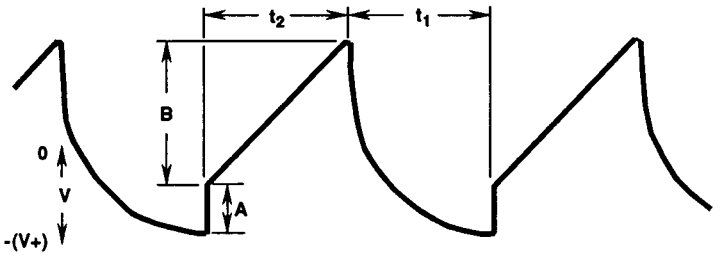


FIGURE 4. OUTPUT RIPPLE

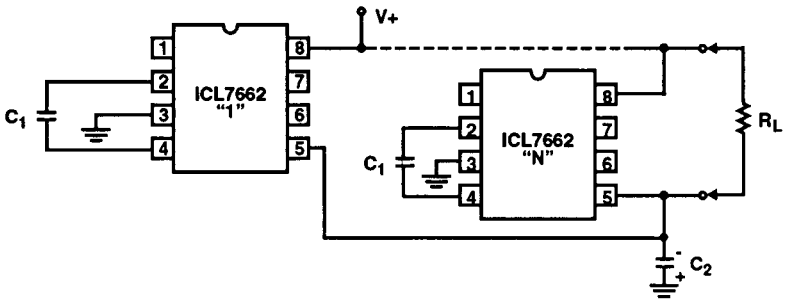


FIGURE 5. PARALLELING DEVICES

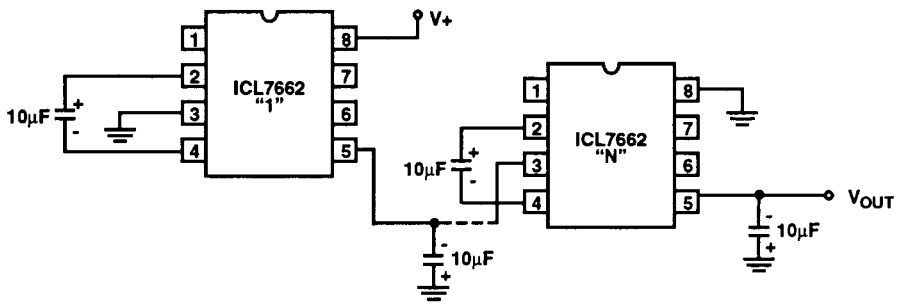


FIGURE 6. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Changing the ICL7662 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1kW resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kW pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, COSC, as shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10mF to 100mF).

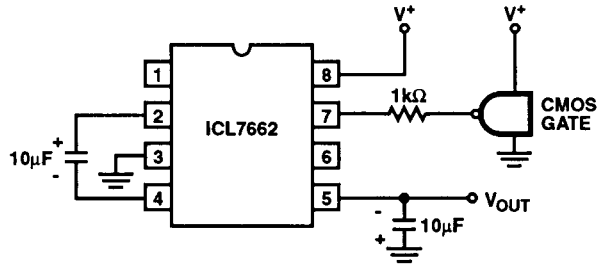


FIGURE 7. EXTERNAL CLOCKING

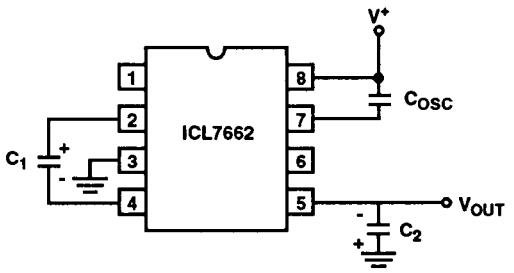
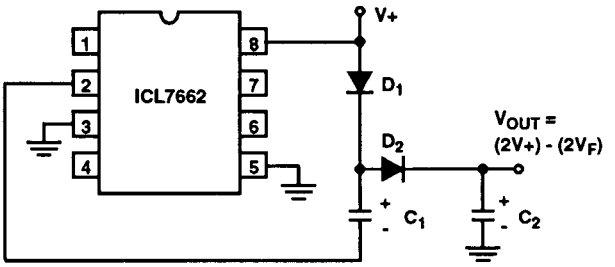


FIGURE 8. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7662 are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode C_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) ($2V_F$) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 15V and an output current of 10mA it will be approximately 70Ω.



NOTE: D_1 and D_2 can be any suitable diode.

FIGURE 9. POSITIVE VOLTAGE DOUBLER

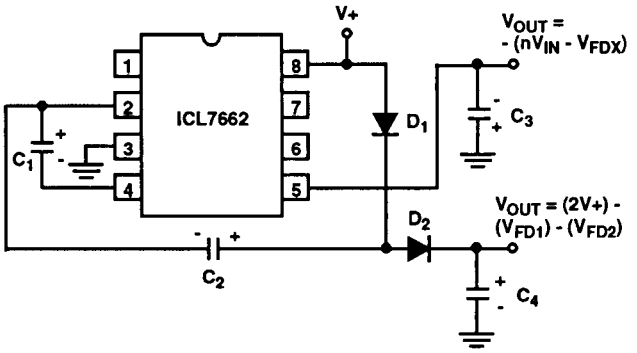


FIGURE 10. COMBINED NEGATIVE CONVERTER AND POSITIVE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 10 combines the functions shown in Figure 3 and Figure 9 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +30V can be converted (via +15V, and -15V) to a nominal -30V, although with rather high series output resistance (~250Ω).

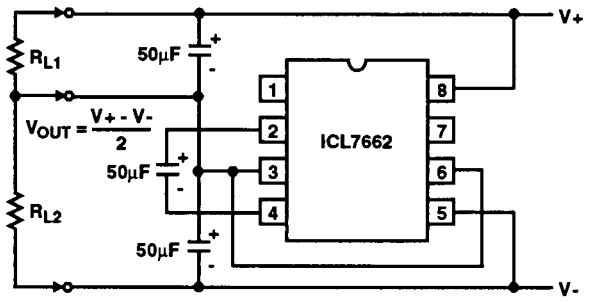


FIGURE 11. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662s output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

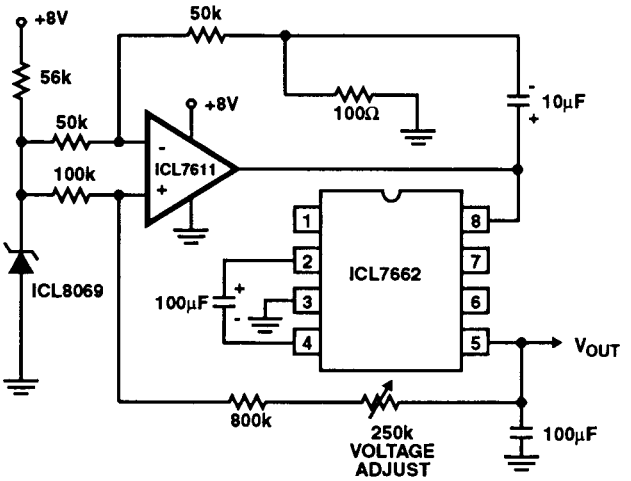


FIGURE 12. REGULATING THE OUTPUT VOLTAGE

Other Applications

Further information on the operation and use of the ICL7662 may be found in A051 "Principles and Applications of the ICL7660 CMOS Voltage Converter".