

**ANALOG
DEVICES****Advanced Video Decoder with 9-Bit ADC,
& Component Input Support****ADV7183****FEATURES**

Analog Video to Digital YUV Video Decoder
 NTSC-(M/N), PAL-(B/D/G/H/I/M/N)
Integrates Two 9-Bit Accurate ADCs
Clocked from a Single 27 MHz Crystal
Dual Video Clocking Schemes
 Line Locked Clock Compatible (LLC)
 Fixed Frequency Oversampling 10-Bit Operation
Adaptive-Digital-Line-Length-Tracking (ADLLT™)
Real Time Clock & Status Information Output
Integrated AGC (Automatic Gain Control) & Clamping
Simplified Digital Interface
On-Board Digital FIFO
Optimised Programmable Video Source Modes
 Broadcast TV
 VCR/Camcorder
 Security/Surveillance
Multiple, Programmable Analog Input Formats:
 CVBS (Composite Video)
 SVHS (Y/C)
 YPrPb or YUV
6 Analog Input Video Channels
2 Line Chroma Comb Filter
Automatic NTSC/PAL Identification
VMI & VIP compliant video pixel port
Digital Output Formats (16-Bit Wide Bus):

YCrCb (4:2:2 or 4:1:1)
 CCIR601/CCIR656 8-Bit
 0.5V to 2.0V pk-pk i/p range
 Differential Gain typ 1%
 Differential Phase typ 1°
Programmable Video Controls
 Pk-White/Hue/Brightness/Saturation/Contrast
CCIR/Square Pixel Operation
Integrated On-Chip Video Timing Generator
Synchronous or Asynchronous Output Timing
Line Locked Clock Output
Close Captioning Passthrough Operation
Vertical Blanking Interval Support
Power Down Mode
2-Wire Serial MPU Interface (I²C Compatible)
+5V Analog +3.3V Digital CMOS Supply Operation
80-Pin LQFP Package

APPLICATIONS

DVD-RAM or DVD-R
 Digital TV's
 Video Conferencing
 Hybrid Analog/Digital Set Top Boxes
 PC Video/Multimedia
 Camcorders
 Security Systems/Surveillance

GENERAL DESCRIPTION

The ADV7183 is an integrated video decoder that automatically recognises and converts a standard analog baseband television signal compatible with world wide standards NTSC or PAL into 4:2:2 or 4:1:1 component video data compatible with 16-bit/8-bit CCIR601/CCIR656 8-Bit standards.

The advanced and highly flexible digital output interface enables performance video decoding and conversion in both frame-buffer based and line locked clock based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics including tape based sources, broadcast sources, security/surveillance cameras and professional systems.

Fully integrated line stores enable real time horizontal and vertical scaling of captured video down to icon size. The 9-bit accurate A/D conversion provides professional quality SNR performance. This allows true 8-bit resolution in the 8-bit output mode.

The 6 analog inputs channel accept standard composite, S-Video and Component YPrPb video signals in an extensive number of combinations. AGC and Clamp Restore circuitry allow an input video signal peak to peak range of 0.5V up to 2V. Alternatively these can be bypassed for manual settings.

The fixed 27 MHz clocking of the ADCs and datapath for all modes allows very precise and accurate sampling and digital filtering. The Line Locked Clock output allows the output data rate, timing signals and output clock signals to be synchronous, asynchronous or line locked even with +/-5% line length variation. The output control signals allow glueless interface connection in almost any application.

The ADV7183 modes are set up over a two wire serial bidirectional port (I²C compatible).

The ADV7183 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7183 is packaged in a small 80 pin LQFP package.

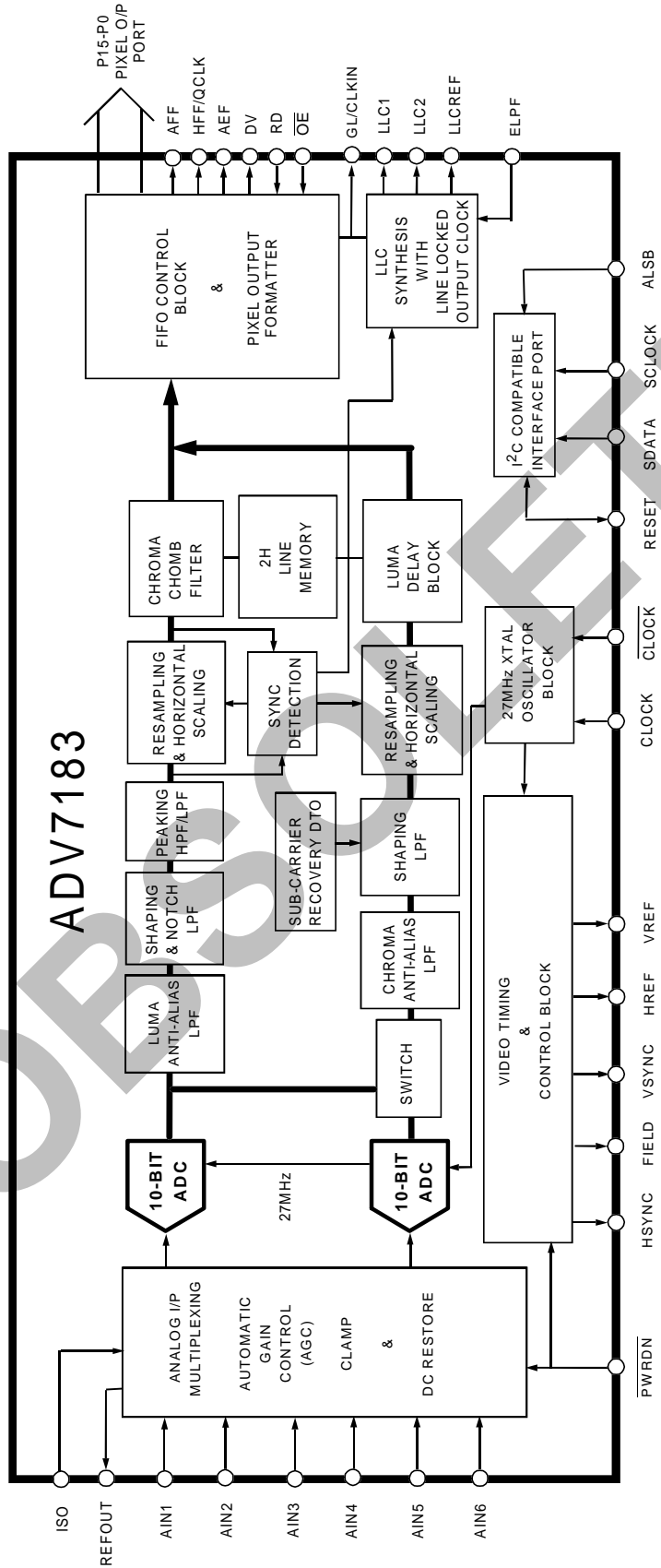
Rev. PrF 09/01

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

* ADV is a Registered Trademark of Analog Devices, Inc.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
 Tel: 617/329-4700 World Wide Web Site: <http://www.analog.com>
 Fax: 617/326-8703 © Analog Devices, Inc.,

ADV7183



ADV7183

FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

| Mnemonic | Input/Output | Function |
|-------------|--------------|--|
| P15-P0 | O | Video pixel output port. 8-Bit Multiplexed YCrCb Pixel Port (P15-P8), 16-Bit YCrCb Pixel Port (P15-P8=Y & P7-P0=Cb,Cr). |
| GPO[0:3] | O | General purpose outputs controlled via I2C. |
| XTAL | I | Input terminal for 27MHz crystal oscillator or connection for external oscillator with CMOS compatible square wave clock signal |
| XTAL1 | O | Second terminal for crystal oscillator; not connected if external clock source is used |
| DVSS1-3 | G | Ground for Digital supply |
| DVDD1-3 | P | Digital Supply Voltage (+3.3V) |
| DVDDIO | P | Digital I/O supply Voltage (+3.3V) |
| DVSSIO | G | Digital I/O ground |
| AVSS | G | Ground for Analog Supply |
| AVDD | P | Analog Supply Voltage (+5V) |
| AVSS1-6 | G | Analog Input Channels ground if single ended mode is selected. These pins should be connected directly to REFOUT in Differential mode is selected. |
| AIN1-6 | I | Video Analog Input Channels |
| SCLOCK | I | MPU Port Serial Interface Clock Input. |
| SDATA | I/O | MPU Port Serial Data Input/Output. |
| ALSB | I | TTL Address Input, it selects the MPU address; MPU address = 88H ALSB = 0, disables I ² C filter MPU address = 8AH ALSB = 1, enables I ² C filter |
| RD | I | Asynchronous FIFO Read Enable signal. A logical high on this pin enables a read from the output of the FIFO. |
| DV | O | DV or Data Valid output signal. In SCAPI/CAPI mode: DV performs a two functions depending on whether SCAPI or CAPI is selected. It toggles high when the FIFO has reached the AFF margin set by the user, and remains high until the FIFO is empty. The alternative mode is where it can be used to control FIFO reads for bursting information out of the FIFO. In API mode DV indicates valid data in the FIFO, which includes both pixel information and control codes. The polarity of this pin is controlled via PDV. |
| OE | I | Output Enable controls pixel port outputs. A logical high will tri-state P19-P0. |
| HREF/HRESET | O | Dual function pin, HREF or Horizontal Reference output signal (enabled when Line Locked Interface is selected , OM_SEL[1:0] = 0,0); this signal is used to indicate data on the YUV output. The positive slope indicates the beginning of a new active line, HREF is always 720 Y samples long. HRESET or Horizontal Reset Output (enabled when SCAPI or CAPI is selected, OM_SEL[1:0] = 0,1 or 1,0) is a signal the indicates the beginning of a new line of video. In SCAPI/CAPI this signal is one clock cycle wide and is output relative to CLKIN. It immediately follows the last active pixel of a line. The polarity is controlled via PHVR. |

PRELIMINARY TECHNICAL DATA

ADV7183

PIN DESCRIPTION

| Mnemonic | Input/Output | Function |
|--------------------|--------------|---|
| <u>VREF/VRESET</u> | O | VREF or Vertical Reference output signal, indicates start of next field). <u>VRESET</u> or Vertical Reset Output is a signal that indicates the beginning of a new field. In SCAPI/CAPI mode this signal is one clock wide and active low relative to CLKIN. It immediately follows <u>HRESET</u> pixel, and it indicates that the next active pixel is the first active pixel of the next field. |
| LLCREF | O | Clock reference output; this is a clock qualifier distributed by the internal CGC for a data rate of LLC2. The polarity of LLCREF is controlled by PLLCREF bit. |
| LLC1/PCLK | O | Dual function pin, Line Locked Clock system output clock (27MHz \pm 5%) or a FIFO output clock ranging from 20-35MHZ. |
| LLC2 | O | Line locked clock system output clock/2 (13.5MHz). |
| ELPF | I | This pin is used for the External Loop Filter that is required for the LLC PLL. |
| <u>RESET</u> | I/O | System Reset, can be configured as an Input or Output signal (the RES bit can be used to control this pin). |
| <u>PWRDN</u> | I | Power Down enable, a logical low will place part in a power down status. |
| REFOUT | O | Internal Voltage Reference Output. |
| CML | O | Common Mode Level for ADC. |
| AEF | O | Almost Empty Flag is a FIFO control signal. It indicates when the FIFO has reached the almost empty margin set by the user (use FFM[4:0]). The ploarity of this signal is controled by PFF bit. |
| HFF/QCLK/GL | I/O | Multi function pin, Half Full Flag (OM_SEL[1:0] = 1,0) is a FIFO control signal which indicates when the FIFO is half full. The QCLK (OM_SEL[1:0] = 0,1) pin function is a qualified pixel output clock when using FIFO SCAPI mode. The GL (OM_SEL[1:0] = 0,0) function (Genlock output) is a signal that contains a serial stream of data which contains information for locking the subcarrier frequency. The ploarity of HFF signal is controled by PFF bit. |
| AFF | O | Almost Full Flag is a FIFO control signal. It indicates when the FIFO has reached the almost full margin set by the user (use FFM[4:0]). The ploarity of this signal is controled by PFF bit. |
| CLKIN | I | CLKIN is an asynchronous FIFO clock. This asynchronous clock is used to output data onto the P19-P0 bus and other control signals. The LLC1 clock can be tied to this pin and the frequency programmed by CLKVAL[17:0]. |
| FIELD | O | ODD/EVEN field output signal. A active state indicates that an even field is being digitized. The polarity of this signal is controlled by PF bit. |
| HS/HACTIVE | O | Dual function pin, HS or Horizontal Sync (OM_SEL[1:0] = 0,0) is a programmable horizontal sync output signal. The rising and falling edges can be controlled by HSB[9:0] and HSE[9:0] in steps of 2 LLC1. The ploarity of HS signal is controled by PHS bit. HACTIVE (OM_SEL[1:0] = 1,0 or 0,1) is an output signal that is active during the active/viewable period of a video line. The active portion of a video line is programmable on the ADV7183. |
| The | | polarity of HACTIVE is controlled by PHS bit. |
| VS/VACTIVE | O | Dual function pin, VS or Vertical Sync (OM_SEL[1:0] = 0,0) is an output signal that indicates a vertical sync with respect to the YUV pixel data. The active period of this signal is six lines of video long. The ploarity of VS signal is controled by PVS bit. VACTIVE (OM_SEL[1:0] = 1,0 or 0,1) is an output signal that is active during the active/viewable period of a video field. The polarity of VACTIVE is controlled by PVS bit. |

PRELIMINARY TECHNICAL DATA

ADV7183

PIN DESCRIPTION

| Mnemonic | Input/Output | Function |
|----------|--------------|---|
| ISO | I | ISO (Input Switch Over) a low to high transition on this input indicates to the decoder core that the input video source has been changed externally and configures the decoder to reacquire the new timing information of the new source. This is useful in applications where external video muxs are used. This input gives the advantage of faster locking to the external muxed video sources. A low to high transition triggers this input. |
| CAPY1-2 | I | ADC Capacitor network. |
| CAPC1-2 | I | ADC Capacitor network. |

OBSOLETE

PRELIMINARY TECHNICAL DATA

ADV7183

ABSOLUTE MAXIMUM RATINGS *

| | |
|--|-----------------------------------|
| V _{AA} to GND..... | 7V |
| Voltage on any Digital Input Pin..... | GND-0.5V to V _{AA} +0.5V |
| Storage Temperature (T _S)..... | -65°C to +150°C |
| Junction Temperature(T _J)..... | +150°C |
| Lead Temperature (Soldering, 10 secs)..... | +260°C |
| Analog Outputs to GND ¹ | GND -0.5 to V _{AA} |

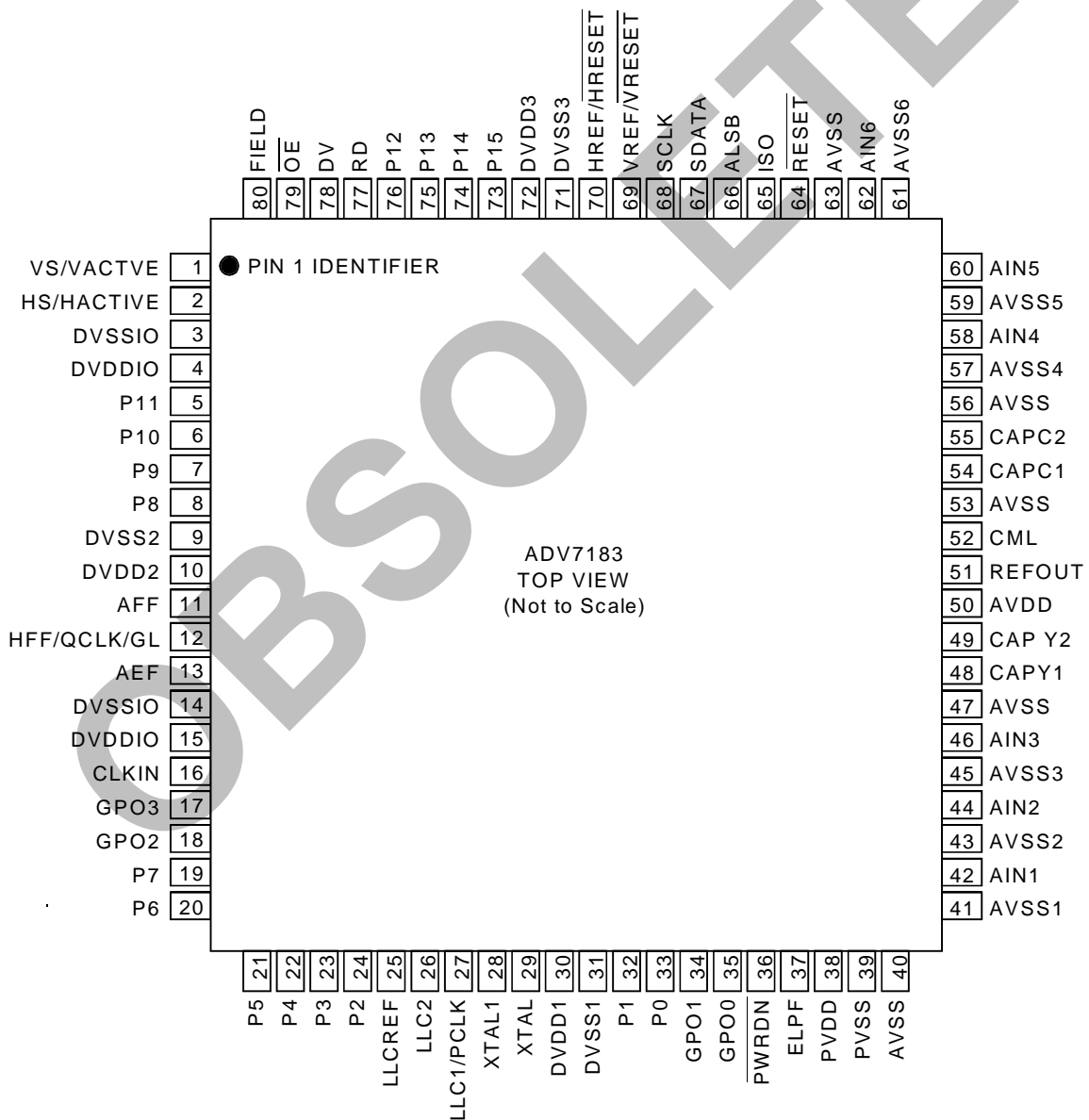
ORDERING GUIDE

| Model Option | Temperature Range | Package |
|--------------|-------------------|---------|
| ADV7183KST | 0°C to 70°C | 80 LQFP |

NOTES

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

¹Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.



ADV7183 PIN FUNCTIONALITY

SPECIFICATIONS¹

($V_{AA} = +5V \pm 5\%$, $V_{DD} = +3.3V \pm 5\%$, $V_{DDIO} = +3.3V \pm 5\%$
 All specifications T_{MIN} to T_{MAX} ² unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|------------------------------------|------|-----------|------|---------|--------------------------------------|
| STATIC PERFORMANCE | | | | | |
| Resolution (each ADC) | | | 9 | Bits | |
| Accuracy (each ADC) | | | | | |
| Integral Nonlinearity | | ± 0.5 | | LSB | |
| Differential Nonlinearity | | ± 0.5 | | LSB | Guaranteed Monotonic |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | 2 | | | V | |
| Input Low Voltage, V_{INL} | | | 0.8 | V | $V_{IN} = 0.4V$ or $2.4V$ |
| Input Current, I_{IN} | -10 | | 10 | μA | |
| Input Capacitance, C_{IN} | | | 10 | pF | |
| DIGITAL OUTPUTS | | | | | |
| Output High Voltage, V_{OH} | 2.4 | | | V | $I_{SOURCE} = 3.2$ mA |
| Output Low Voltage, V_{OL} | | | 0.4 | V | $I_{SINK} = 0.4$ mA |
| High Impedance Leakage Current | | | 10 | μA | |
| Output Capacitance | | | 30 | pF | |
| VOLTAGE REFERENCE | | | | | |
| Reference Range, V_{REFOUT} | | 2.1 | | V | $I_{VREFOUT} = 0\mu A$ |
| POWER REQUIREMENTS | | | | | |
| Digital Power Supply, V_{DD} | 3.15 | 3.3 | 3.45 | V | |
| Analog Power Supply, V_{AA} | 4.75 | 5.0 | 5.25 | V | |
| Digital Supply Current, I_{DD}^3 | | 150 | | mA | CVBS, CCIR-656, $V_{DD} = 3.3V$ |
| Digital Supply Current, I_{DD}^3 | | 154 | | mA | CBVS, PAL Sq Pixel, $V_{DD} = 3.3V$ |
| Analog Supply Current, I_{AA}^4 | | 150 | | mA | CVBS, CCIR-656, $V_{AA} = 5.25V$ |
| Analog Supply Current, I_{AA}^4 | | 150 | | mA | CVBS, PAL Sq Pixel, $V_{AA} = 5.25V$ |
| Power-up Time | | 1 | | field | Sleep mode until powered up |

NOTE

¹ The max/min specifications are guaranteed over this range. The max/min values are typical over $V_{AA} = 4.75V$ to $5.25V$ and $V_{DD}/V_{DDIO} = 3.15V$ to $3.45V$ range

² Temperature Range T_{MIN} to T_{MAX} : $0^{\circ}C$ to $70^{\circ}C$.

³ I_{DD} is total current taken by DVDD & DVDIO supply pins.

⁴ I_{AA} is total analog current taken by AVDD supply pins.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ADV7183

VIDEO PERFORMANCE SPECIFICATIONS¹ ($V_{AA} = +5V \pm 5\%$, $V_{DD} = +3.3 \pm 5\%$, $V_{DDIO} = +5V/3.3 \pm 5\%$ All specifications T_{MIN} to T_{MAX} ² unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|--|-----|------|-----|-------|---|
| NON-LINEAR SPECIFICATIONS | | | | | |
| Differential Phase | | 1 | | deg | CVBS, Comb/No Comb |
| Differential Gain | | 1 | | % | CVBS, Comb/No Comb |
| Luma Non-Linearity | | 1 | | % | |
| Chroma Non-Linear Gain | | 1 | | % | |
| NOISE SPECIFICATIONS | | | | | |
| SNR (Pedestal) | | 60 | | dB | CVBS |
| SNR (Ramp) | | 57 | | dB | CVBS |
| Analog Front End Channel Crosstalk | | 63 | | dB | S-Video/ YUV, single ended |
| Analog Front End Channel Crosstalk | | 63 | | dB | S-Video/ YUV, differential ended |
| LOCK TIME AND JITTER SPECIFICATIONS | | | | | |
| Horizontal Lock Time | | 50 | | lines | TV / VCR mode |
| Horizontal Recovery Time | | 50 | | lines | |
| Horizontal Lock Range | | ±5 | | % | |
| Line Length Variation Over Field | | ±1 | | % | VCR mode/ Surveillance mode |
| Line Length Variation Over Field | | ±1 | | % | TV mode |
| HLock Lost Declared | 10 | | | HSync | TV mode, No. of missing HSyncs |
| HLock Lost Declared | | 20 | | HSync | VCR/Surveillance mode, No. of missing HSyncs |
| Vertical Lock Time | | 2 | | VSync | First Lock into video signal |
| VLock Lost Declared | | 1 | | VSync | All modes, No. of missing VSyncs |
| F _{SC} Subcarrier Lock Range | | ±400 | | Hz | NTSC/PAL |
| Color Lock Time | | 50 | | lines | HLock to Color Lock Time |
| LLC Clock Jitter (Short Time Jitter) | | 1 | | ns | RMS Clock Jitter |
| LLC Clock Jitter (Frame Jitter) | | 37 | | ns | RMS Clock Jitter |
| CHROMA SPECIFIC SPECIFICATIONS | | | | | |
| Hue Accuracy | | 1 | | deg | |
| Color Saturation Accuracy | | 1 | | % | |
| Color Gain Control Range | | -6 | 18 | dB | S-Video, YUV, Overall CGC Range(analog and digital) |
| Analog Color Gain Range | | -6 | 6 | dB | S-Video, YUV |
| Digital Color Gain Range | | 0 | 12 | dB | CVBS, S-Video, YUV |
| LUMA SPECIFIC SPECIFICATIONS | | | | | |
| Luma Brightness Accuracy | | 1.0 | | % | Video Input Range = 1.0Vp-p |
| Luma Contrast Accuracy | | 1.0 | | % | Video Input Range = 1.0Vp-p |

NOTE

¹ The max/min specifications are guaranteed over this range. The max/min values are typical over $V_{AA} = 4.75V$ to $5.25V$ and $V_{DD}/V_{DDIO} = 3.15V$ to $3.45V$ range

² Temperature Range T_{MIN} to T_{MAX} : $0^{\circ}C$ to $70^{\circ}C$.
Specifications subject to change without notice.

TIMING SPECIFICATIONS¹

(V_{AA} = +5V ± 5%, V_{DD} = /3.3V ± 5%, V_{DDIO} = +3.3V ± 5%)
 All specifications T_{MIN} to T_{MAX}² unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|---|-----|------|-----|-------|--------------------------------|
| SYSTEM CLOCK AND CRYSTAL Nominal Frequency | | 27 | | MHz | |
| I ² C PORT | | | | | |
| SCL Clock Frequency | 0 | | 400 | kHz | |
| SCL min pulse width high, t ₁ | 0.6 | | | μs | |
| SCL min pulse width low, t ₂ | 1.3 | | | μs | |
| Hold Time (Start Condition), t ₃ | 0.6 | | | μs | |
| Setup time (Start Condition), t ₄ | 0.6 | | | μs | |
| Data Setup Time, t ₅ | 100 | | | ns | |
| SCL/SDA Rise Time, t ₆ | | | 300 | ns | |
| SCL/SDA Fall Time, t ₇ | | | 300 | ns | |
| Setup Time (Stop Condition), t ₈ | | 0.6 | | μs | |
| RESET FEATURE | | | | | |
| Reset Pulse Input Width | tdb | | | μs | |
| CLOCK OUTPUTS | | | | | |
| LLC1 Cycle Time, t ₉ | | 37 | | ns | CCIR601 mode 27MHz |
| LLC1 Cycle Time, t ₉ | | 33.9 | | ns | PAL Square Pixel mode 29.5MHz |
| LLC1 Cycle Time, t ₉ | | 40.8 | | ns | NTSC Square Pixel mode 24.5MHz |
| LLC1 min low period, t ₁₀ | | 18 | | ns | CCIR601 mode 27MHz |
| LLC1 min high period, t ₁₁ | | 18 | | ns | CCIR601 mode 27MHz |
| LLC1 falling to LLCREF falling, t ₁₂ | | 4 | | ns | |
| LLC1 falling to LLCREF rising, t ₁₃ | | 6 | | ns | |
| LLC1 rising to LLC2 rising, t ₁₄ | | 3 | | ns | |
| LLC1 rising to LLC2 falling, t ₁₅ | | 2 | | ns | |
| CLKIN Cycle Time, t ₁₈ | | 37 | | ns | SCAPI & CAPI modes |
| DATA AND CONTROL OUTPUT | | | | | |
| Data Output Hold Time, t ₁₇ | | 8 | | ns | LLC mode |
| Data Output Access Time, t ₁₆ | | 28 | | ns | LLC mode |
| Data Output Access Time, t ₁₉ | | 20 | | ns | SCAPI & CAPI modes |
| Data Output Hold Time, t ₂₀ | | 10 | | ns | SCAPI & CAPI modes |
| Propagation Delay to HiZ, t ₂₁ | | 5 | | ns | |
| Max Output Enable access Time, t ₂₂ | | 8 | | ns | |
| Min Output Enable access Time, t ₂₃ | | 5 | | ns | |

NOTE

¹ The max/min specifications are guaranteed over this range. The max/min values are typical over V_{AA} = 4.75V to 5.25V and V_{DD}/V_{DDIO} = 3.15V to 3.45V range

² Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.

Specifications subject to change without notice.

ADV7183

ANALOG FRONT END SPECIFICATIONS¹ ($V_{AA} = +5V \pm 5\%$, $V_{DD} = +3.3 \pm 5\%$, $V_{DD} = +5V/3.3 \pm 5\%$,
 All specifications T_{MIN} to T_{MAX} ² unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|--------------------------|-----|------|-----|-----------|--|
| CLAMP CIRCUITRY | | | | | |
| External Clamp Capacitor | | 0.1 | | μF | Clamp switched off |
| Input Impedance | | 500 | | $k\Omega$ | |
| Voltage Clamp Level | | 1.4 | | V | Signal already clamped (fine clamping) |
| Clamp Source Current | | +4 | | μA | |
| Clamp Sink Current | | -4 | | μA | Signal already clamped (fine clamping) |
| Clamp Source Current | | +0.9 | | mA | Aquire mode (fast clamping) |
| Clamp Sink Current | | -0.8 | | mA | Aquire mode (fast clamping) |

NOTE

¹ The max/min specifications are guaranteed over this range. The max/min values are typical over $V_{AA} = 4.75V$ to $5.25V$ and $V_{DD}/V_{DDIO} = 3.15V$ to $3.45V$ range

² Temperature Range T_{MIN} to T_{MAX} : $0^{\circ}C$ to $70^{\circ}C$.
 Specifications subject to change without notice.

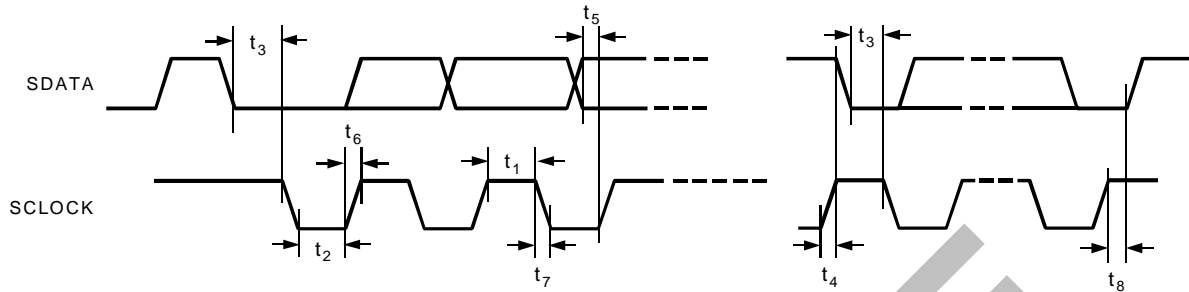


Figure 2. MPU Port Timing Diagram

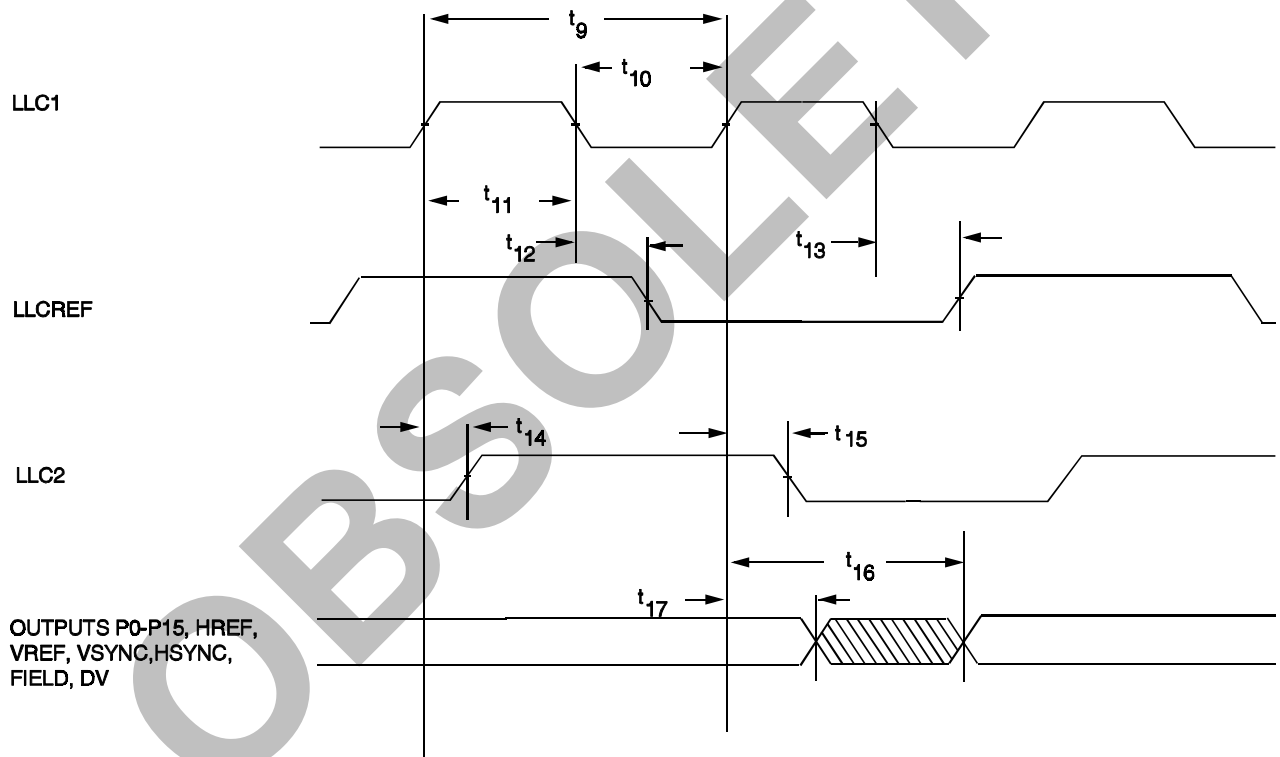


Figure 3. LLC Clock, Pixel Port & Control Outputs Timing Diagram

ADV7183

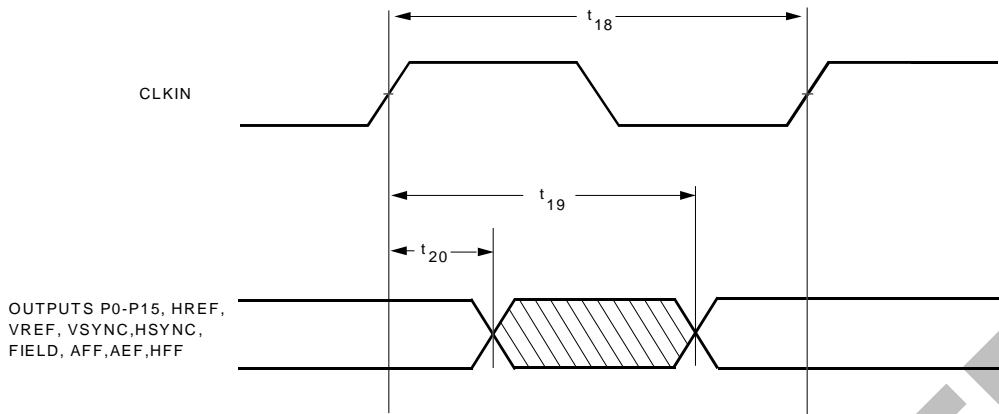


Figure 4. Pixel Port & Control Outputs in CAPI & SCAPI mode Timing Diagram

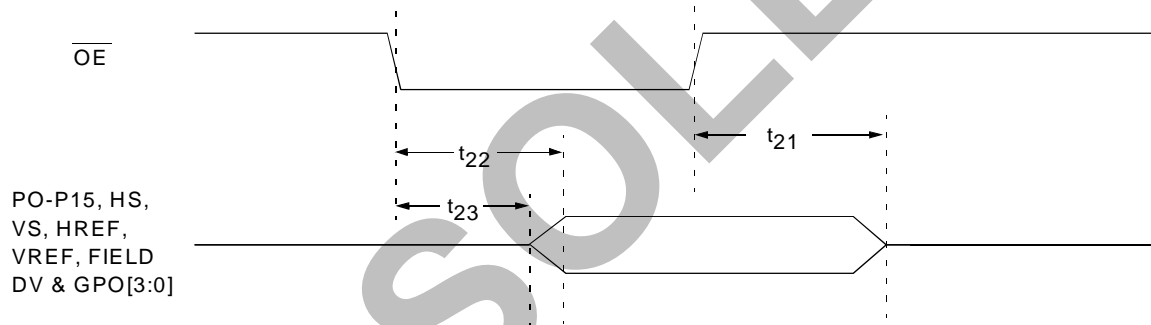


Figure 5 OE Timing Diagram

FUNCTIONAL DESCRIPTION

ANALOG INPUT PROCESSING

The ADV7183 has 6 analog video input channels. These 6 channels can be arranged in a variety of configurations to support up to 6 CVBS input signals, 3 S-Video inputs signals and 2 YCrCb component analog video inputs signals. The INSEL[3:0] control the input type and channel selected. The analog front-end includes 3 clamp circuits for DC restore. There are 3 Sample and Hold Amplifiers prior to the ADC which are used to enable simultaneous sampling of up to 3 channels in a YCrCb input mode. There are 2 9-bit ADC's used for sampling. The entire analog front-end is fully differential which ensures that the video is captured to the highest quality possible, this is very important in highly integrated systems like a video decoder. The block diagram below shows the analog front-end section on the ADV7183.

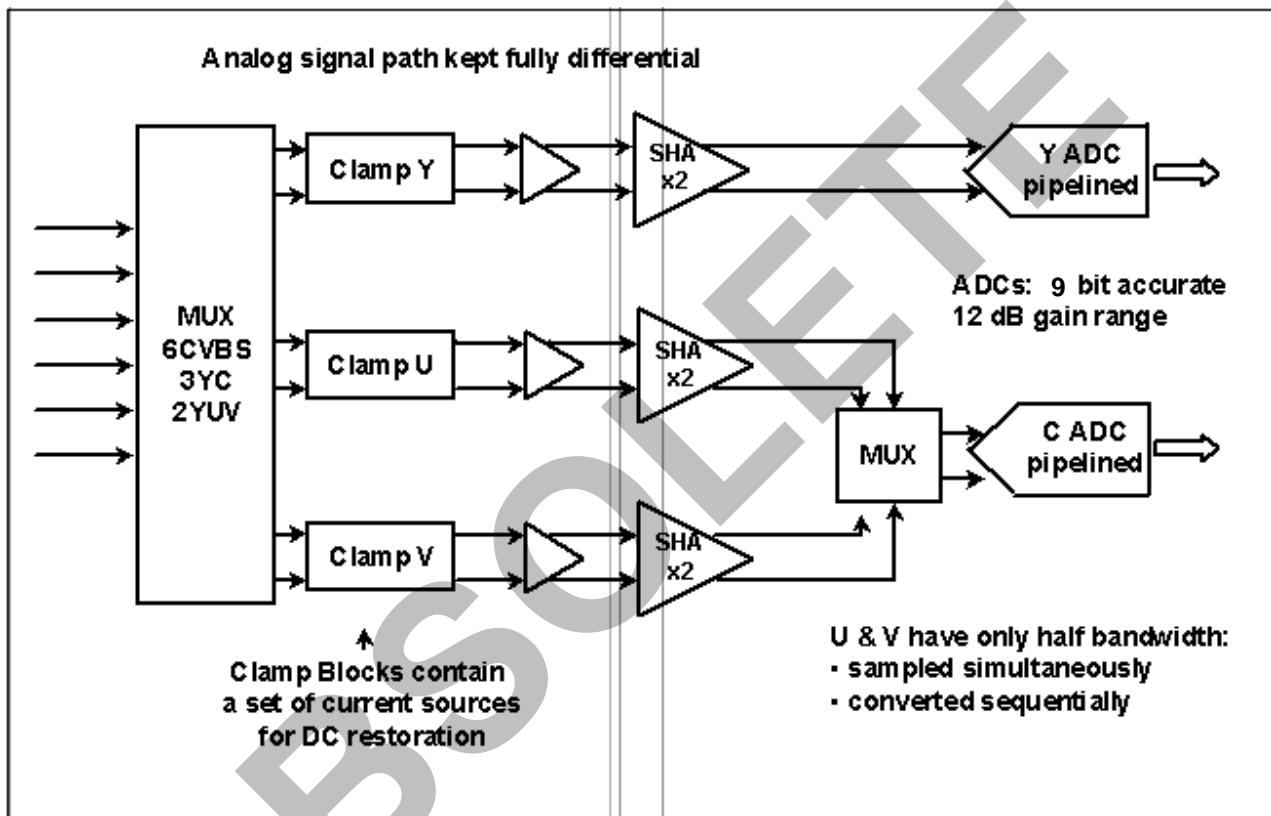


Figure XX. Analog Front-end Block Diagram

CLAMPING

The Clamp control on the ADV7183 consists of a digitally controlled analog current and voltage clamp and a digitally controlled digital clamp circuit. The coupling capacitor on each channel is used to store and filter the clamping voltage. A digital controller controls the Clamp up and down current sources which charge the capacitor on every line. There are four current sources used in the current clamp control, 2 large current sources are used for Course Clamping and two small current sources are used for Fine Clamping. The Voltage Clamp if enabled is only used on startup or if a channel is switched, this clamp pulls the video into the mid range of the ADC, this result in faster clamping and faster lock in time for the decoder. The fourth clamp controller is fully digital and clamps the ADC output data, this results in extremely accurate clamping, it also has the added advantage of being fully digital which result in very fast clamp timing and makes the entire clamping process very robust in terms of handling large amount of Hum which can be present on real world video signals.

In S-Video mode there are 2 clamp controllers used to control the Luminance clamping and the Chrominance clamping separately. Also in YCrCb component input mode there are 2 clamp controllers used to control the Luminance clamping and the CrCb clamping separately, there is however individual current clamps on the Cr & Cb inputs.

User programmability is built into the clamp controllers which enable the Current and Digital clamp controllers to be setup to user defined conditions. Refer to Analog Clamp Control Register(14H), Digital Clamp Control Register(15H) & Digital Color Clamp offset Register(15H & 16H) for control settings.

ADV7183

ANALOG TO DIGITAL CONVERTERS

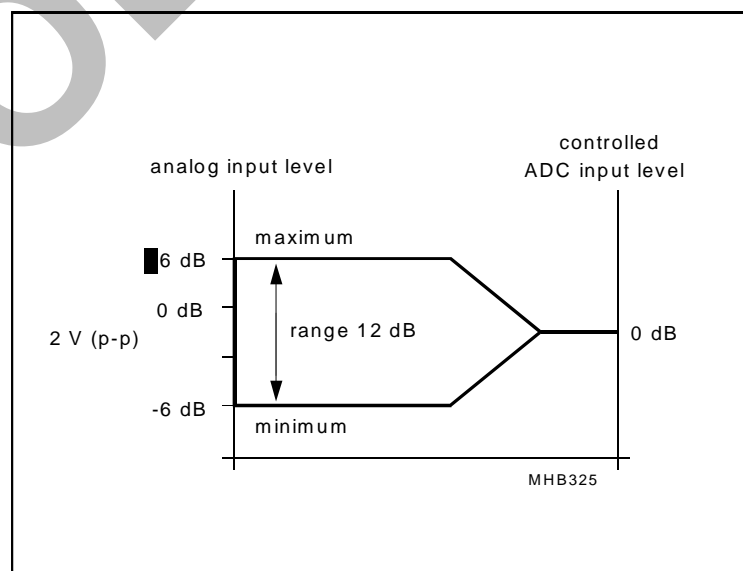
There are two 10-bit ADC used in the ADV7183. These ADC run off a 27MHz input clock. An integrate bandgap generates the required reference voltages for the converters. If the deocder in configured in CVBS mode the 2nd ADC can be switched off to reduce power consumption, see PSC[1:0].

AUTOMATIC GAIN CONTROL

The AGC control block on the ADV7183 is a digitally based systems. This controller ensures that the input video signal (CVBS, S-Video or YCrCb) is scaled to its correct value such that the YCrCb digital output data matches the correct gain of the video signal. The AGC has an analog input video range of 0.5Vp-p to 2.0Vp-p which gives a -6dB to +6dB gain range, Figure xx below demonstrates this range. This AGC range will compensate for video signals that have been incorrectly terminated or have been attenuated due to cable loss etc. There are 2 main control blocks one for the Luminance channel and one for the Chrominance channel.

The Luminance Automatic Gain Control has 8 modes of operation:

- 1) Manual AGC mode where gain for luminance path is set manually using LGM[11:0].
- 2) Blank Level to Sync tip used to set luminance gain, manual MIRE[2:0] controls max the value through Luminance channel. There is no override of this mode when White Peak mode is detected.
- 3) Blank Level to Sync tip used to set luminance gain, manual MIRE[2:0] controls max the value through Luminance channel. There is override of this mode when White Peak mode is detected. White peak mode is activated when the input video exceeds the max luminance range for long periods, this mode is designed to prevent clipping of the input video signal.
- 4) Blank Level to Sync tip used to set luminance gain, MIRE[2:0] is automatically controlled to set the max the value through luminance channel. There is no override of this mode when White Peak mode is detected.
- 5) Blank Level to Sync tip used to set luminance gain, manual MIRE[2:0] is automatically controlled to set the max the value through luminance channel. There is override of this mode when White Peak mode is detected. White peak mode is activated when the input video exceeds the max luminance range for long periods, this mode is designed to prevent clipping of the input video signal.
- 6) The Active video
- 7) The
- 8) The luminance channel gain is Frozen at it present value.



The Chrominance Automatic Gain Control has 4 modes of operation:

- 1) Manual AGC mode where gain for chrominance path is set manually using CGM[11:0].
- 2) Luminance gain used for chrominance channel.
- 3) Chrominance automatic gain based on color burst amplitude.
- 4) Chrominance gain frozen at its present setting.

Both the luminance and chrominance AGC controllers have programmable time constant which allows the AGC to operate in 4 modes, Slow, Medium, Fast & Video quality controlled.

The max IRE (MIRE [2:0]) control can be used to set the max input video range that can be decoded. Figure xx shows the selectable range.

| MIRE [2 : 0] | Function | |
|--------------|-----------|------------|
| | PAL (IRE) | NTSC (IRE) |
| 0 0 0 | 133 | 122 |
| 0 0 1 | 125 | 115 |
| 0 1 0 | 120 | 110 |
| 0 1 1 | 115 | 105 |
| 1 0 0 | 110 | 100 |
| 1 0 1 | 105 | 100 |
| 1 1 0 | 100 | 100 |
| 1 1 1 | 100 | 100 |

Figure XX. MIRE control

ADV7183

LUMINANCE PROCESSING

Figure xx shows the luminance datapath. The 10-bit data from the Y ADC is applied to an Anti Aliasing Low Pass filter which is designed to bandlimit the input video signal such that aliasing does not occur. This filter dramatically reduces the design on an external analog anti-aliasing filter, this filter need only remove components in the input video signal above 22Mhz. The data then passes through a Shaping or Notch filter.

When in CVBS mode a Notch filter must be used to remove the unwanted chrominance data the lays around the subcarrier frequency. A wide variety of programmable Notch filters for both PAL & NTSC are available. The YSFM[4:0] control the selection of these filters, refer to figure xx to figure xx for a plots of these filters. If S-Video or Component mode is selected a Notch filter is no required, the ADV7183 offers 18 possible shaping filters(SVHS1-18) with as range of low pass filter responses from 0.5Mhz up to 5.75MHz, YSFM[4:0] control the selection of these filters please refer to figure xx to figure xx for filter plots.

The next stage in the luminance processing path is a Peaking filter, this filter offers a sharpness function on the Luminance path. The degree of sharpness can be selected using YPM[2:0]. If no sharpness is required this filter can be by-passed.

The luminance data is then passed through a resampler to correct for line length variations in the input video. This resampler is designed to always output 720 pixels per line for standard PAL or NTSC. The resampler used on the ADV7183 is of very high quality as it uses 128 phases to resample the video, giving 1/128 pixel resolution. The resampler is controlled by a sync detection block which calculates line length variations on the input video. The final stage in the luminance path before it is applied to an output formatter block is a 2 line delay store which is used to compensate for delays in the Chroma data path when Chroma Comb filter is selected.

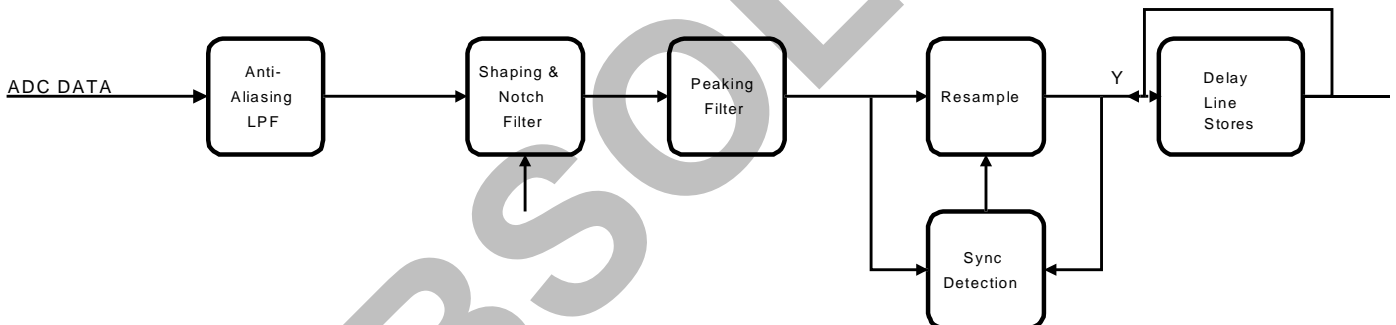


Figure XX. Luminance processing path

LUMINANCE SHAPING FILTER PLOTS

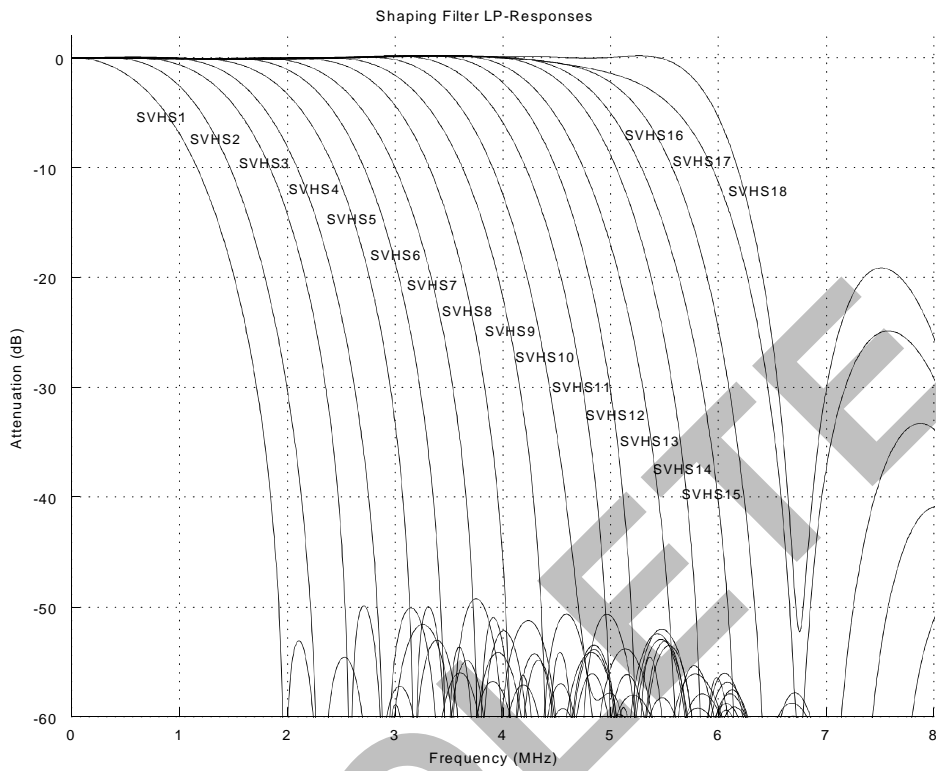


Figure xx. Luminance SVHS1-18 shaping filter responses

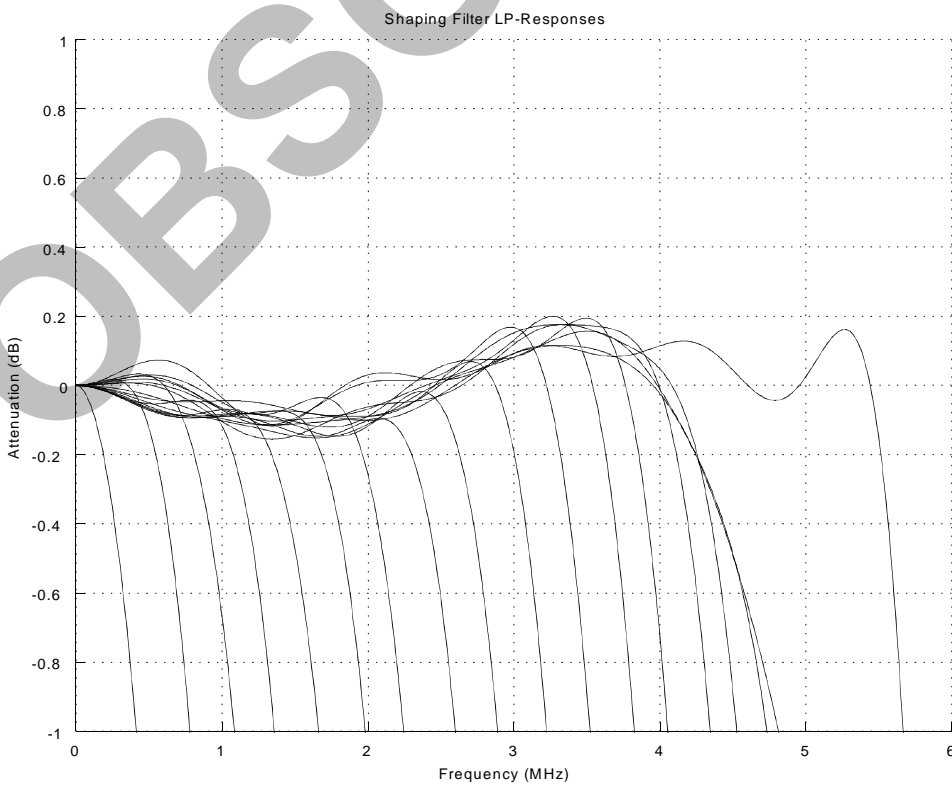


Figure xx. Luminance SVHS1-18 shaping filter responses (closeup)

ADV7183

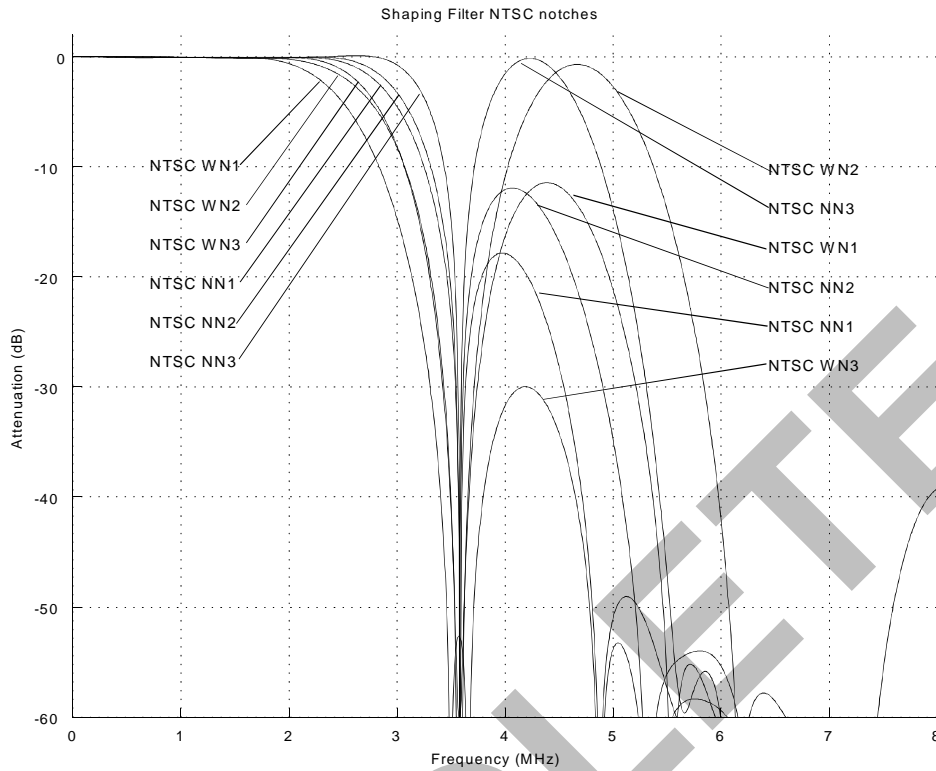


Figure xx. Luminance NTSC Narrow/Wide Notch shaping filter

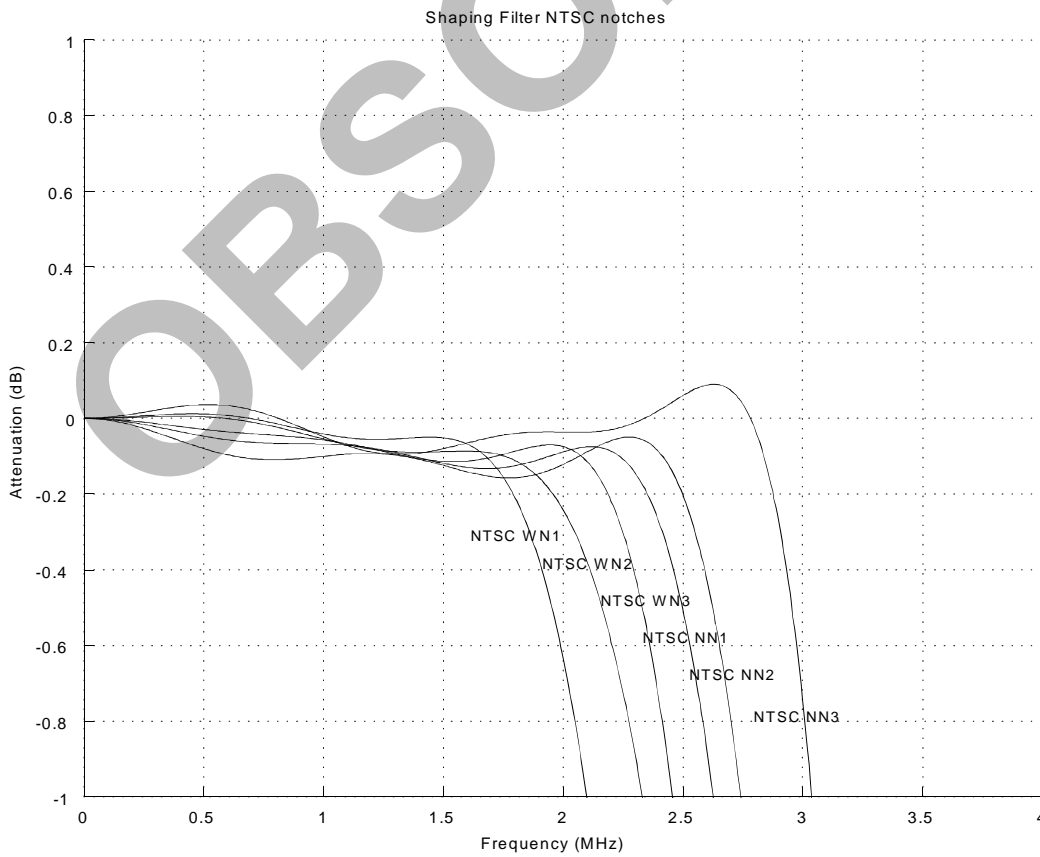


Figure xx. Luminance NTSC Narrow/Wide Notch shaping filter responses (closeup)

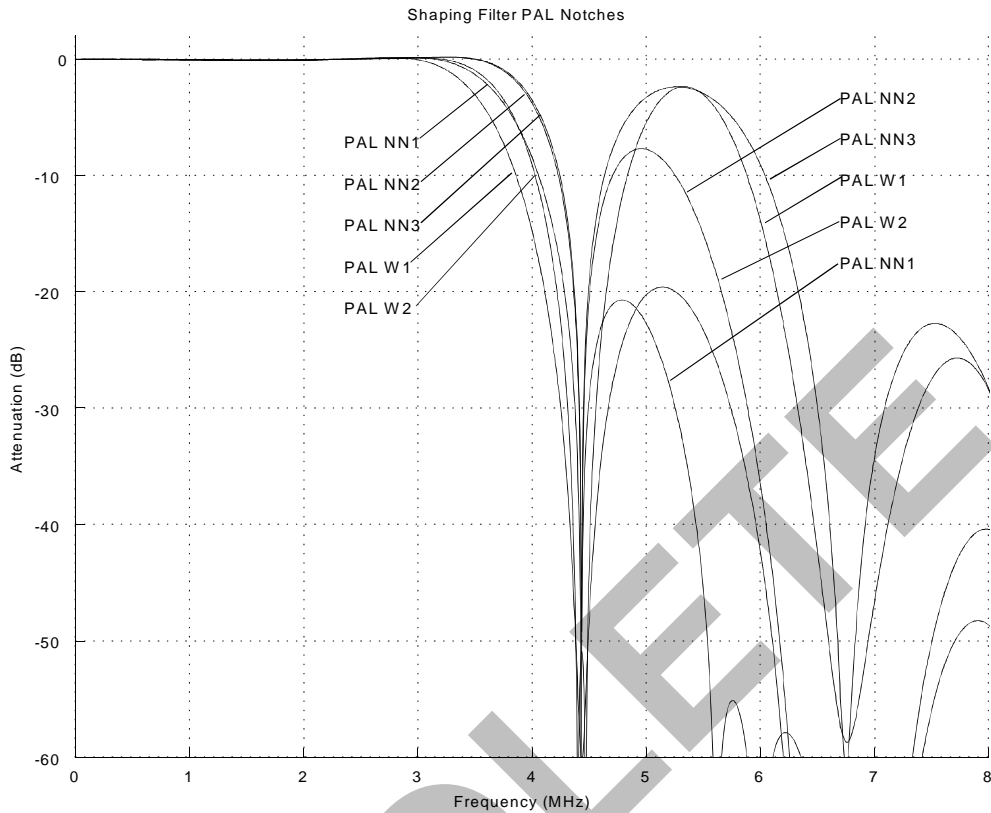


Figure xx. Luminance PAL Narrow/wide Notch shaping filter responses

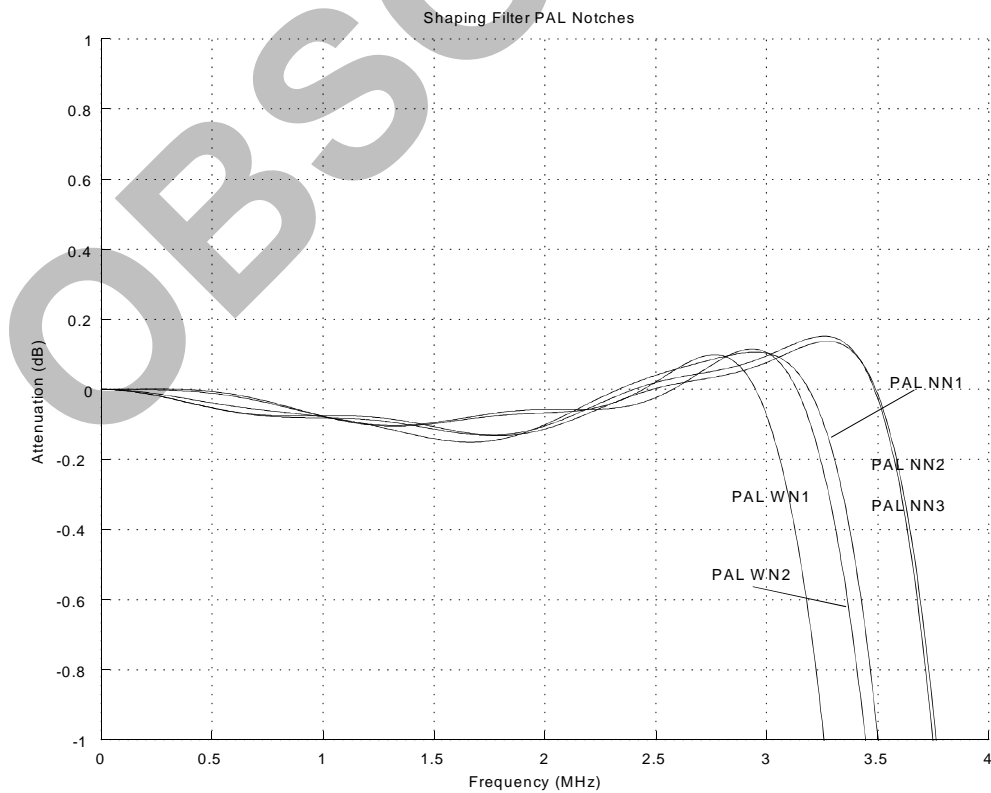


Figure xx. Luminance PAL Narrow?Wide Notch shaping filter responses (closeup)

ADV7183

LUMINANCE PEAKING FILTER PLOTS

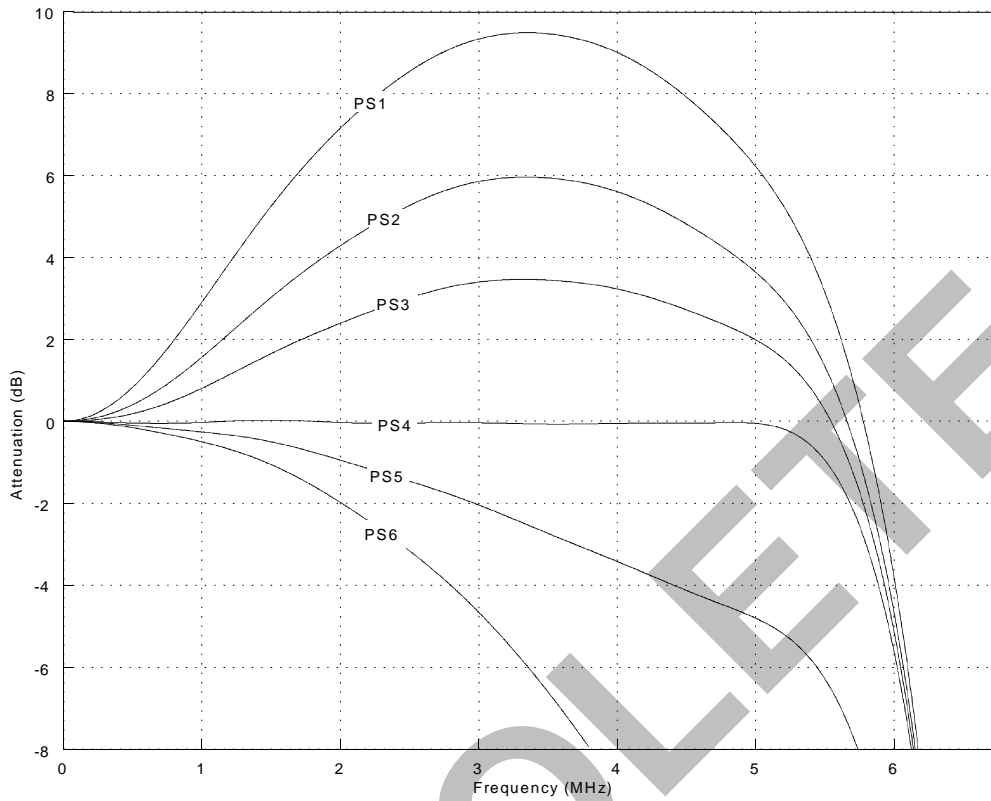


Figure xx. Luminance Peaking filter responses in S-Video (SVHS17 selected)

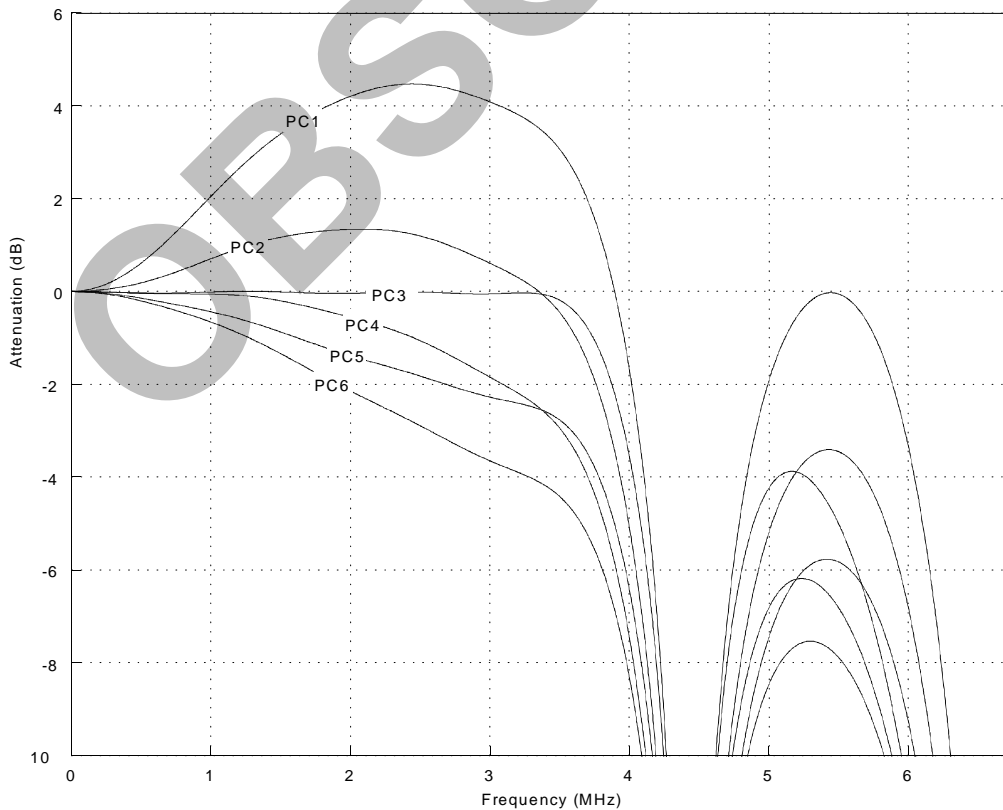


Figure xx. Luminance Peaking filter responses in CVBS (PAL NN3 selected)

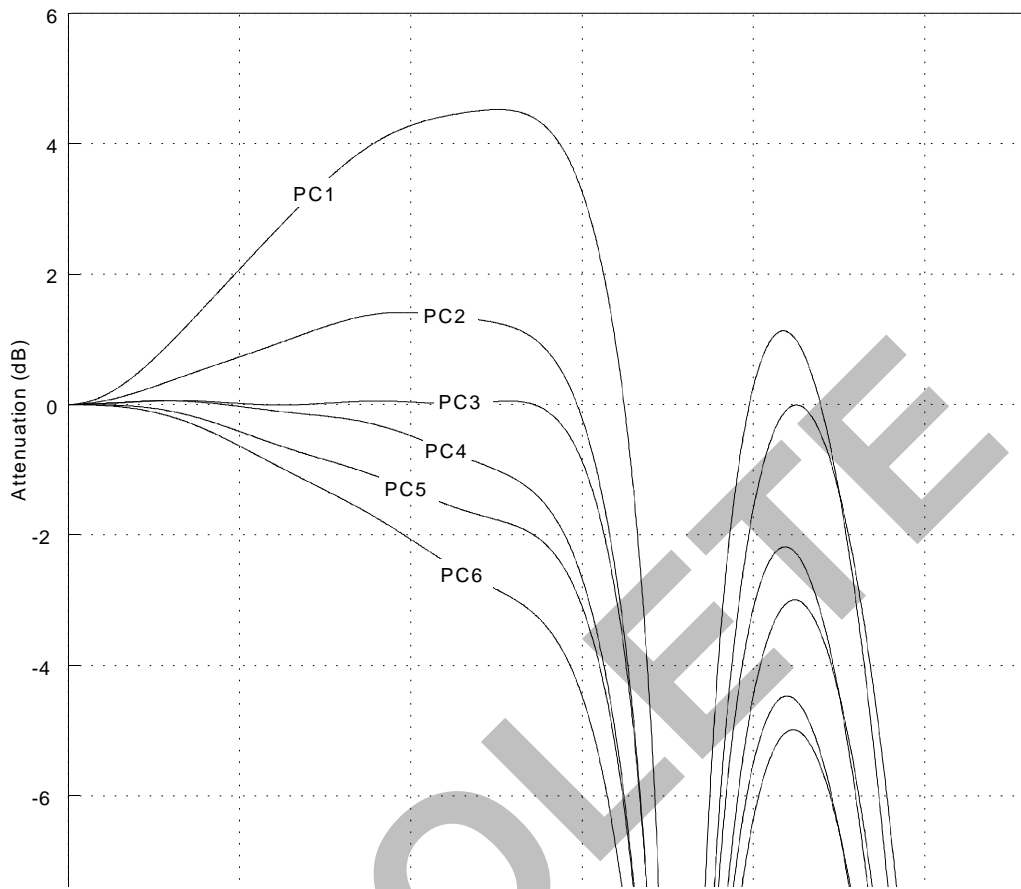


Figure xx. Luminance Peaking filter responses in CVBS (NTSC NN3 selected)

ADV7183

CHROMINANCE PROCESSING

Figure xx shows the chrominance datapath. The 10-bit data from the Y ADC (CVBS mode) or the C ADC (S-video) is first demodulated. The demodulation is achieved by multiplying by the locally generated quadrature subcarrier, where the sign of the cos subcarrier is inverted from line to line according to the PAL switch, and then lowpass filtering is applied to removed components at twice the subcarrier frequency. For NTSC, the phase of the locally generated subcarrier during colour burst is the same as the phase of the colour burst. For PAL, the phase of the colour burst changes from line to line, relative to the phase during active video, and the phase of the locally generated subcarrier is the average of these two values.

The chrominance data is then passed through a anti aliasing filter which is a bandpass filter to removed the unwanted luminance data. This anti aliasing filter dramatically reduces the external anti aliasing filter requirements as it has only to filter components above 25Mhz. In component mode the demodulation block is by-passed.

The next stage of processing is a Shaping filter which can be used to limit the chrominance bandwidth too between 0.5Mhz and 3Mhz, the CSFM[2:0] can be used to select these responses. It should be noted that in CVBS mode a filter or no greater than 1.5Mhz should be selected as CVBS video is typically bandlimited to below 1.5Mhz. In S-Video mode a filter of up to 2Mhz can be used. In Component mode a filter of up to 3 Mhz can be used as component video has higher bandwidth than CVBS or S-Video.

The chrominance data is then passed through a resampler to correct for line length variations in the input video. This resampler is designed to always output 720 pixels per line for standard PAL or NTSC. The resampler used on the ADV7183 is of very high quality as it uses 128 phases to resample the video, giving 1/128 pixel resolution. The resampler is controlled by a sync detection block which calculates line length variations on the input video. The final stage in the chrominance path before it is applied to an output formatter block is Chroma Comb filter.

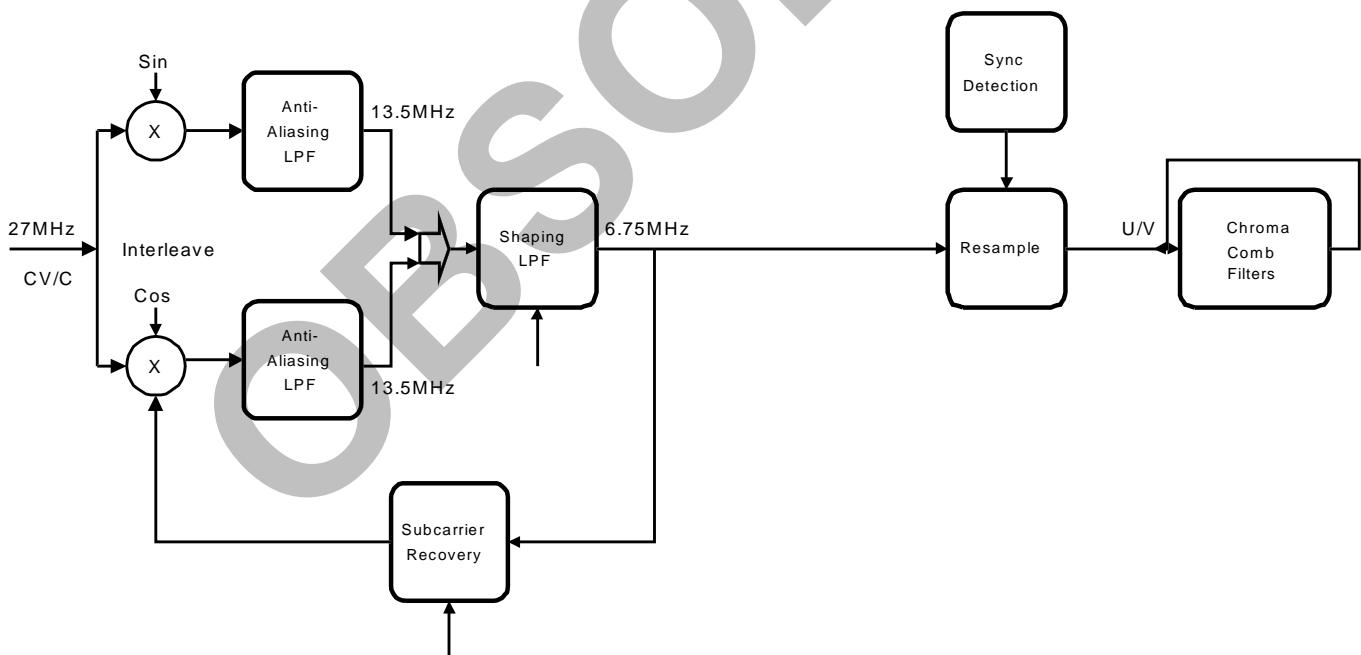


Figure XX. Chrominance processing path

CHROMINANCE SHAPING FILTER L PLOTS

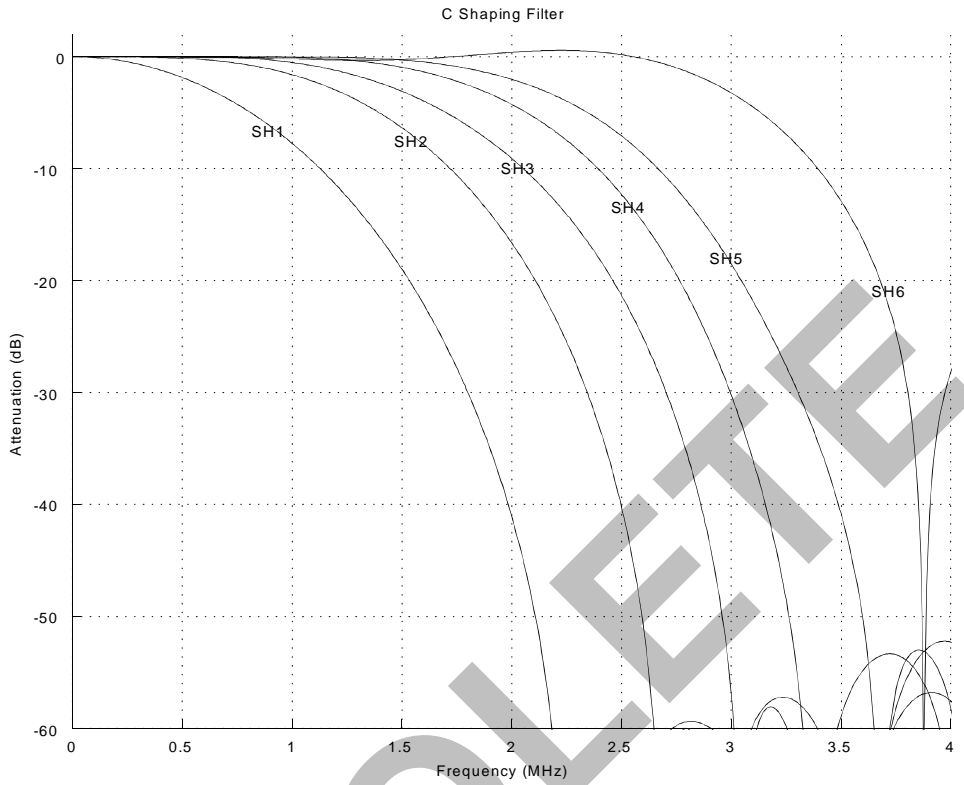


Figure xx. Chrominance shaping filter responses

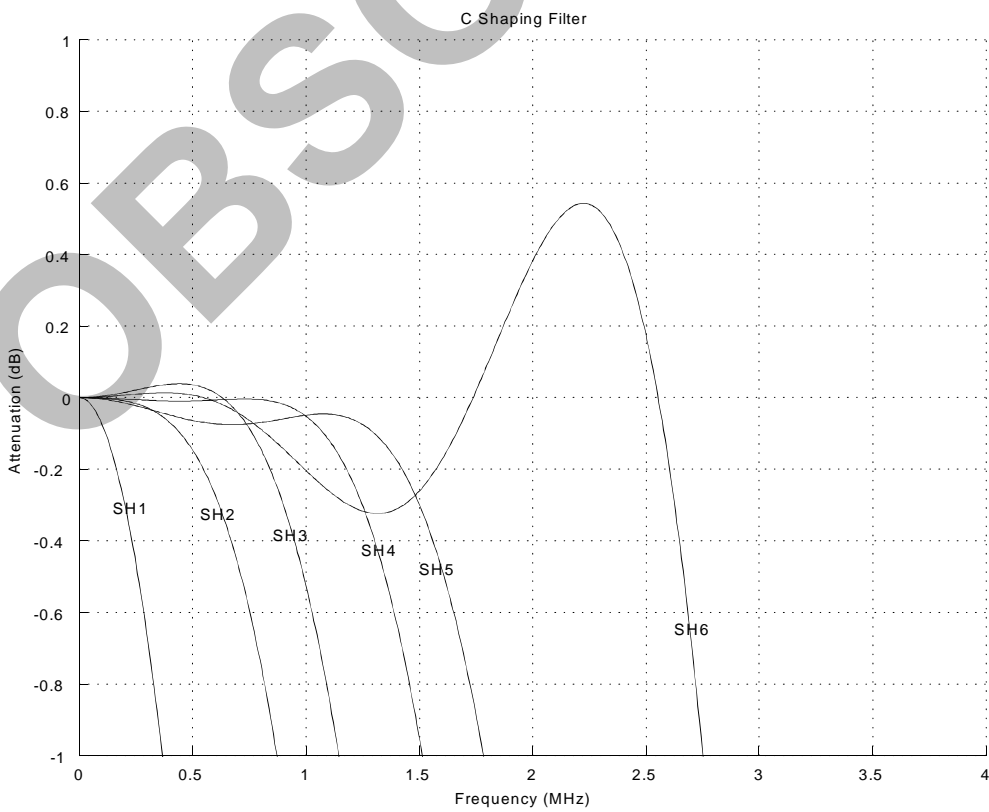
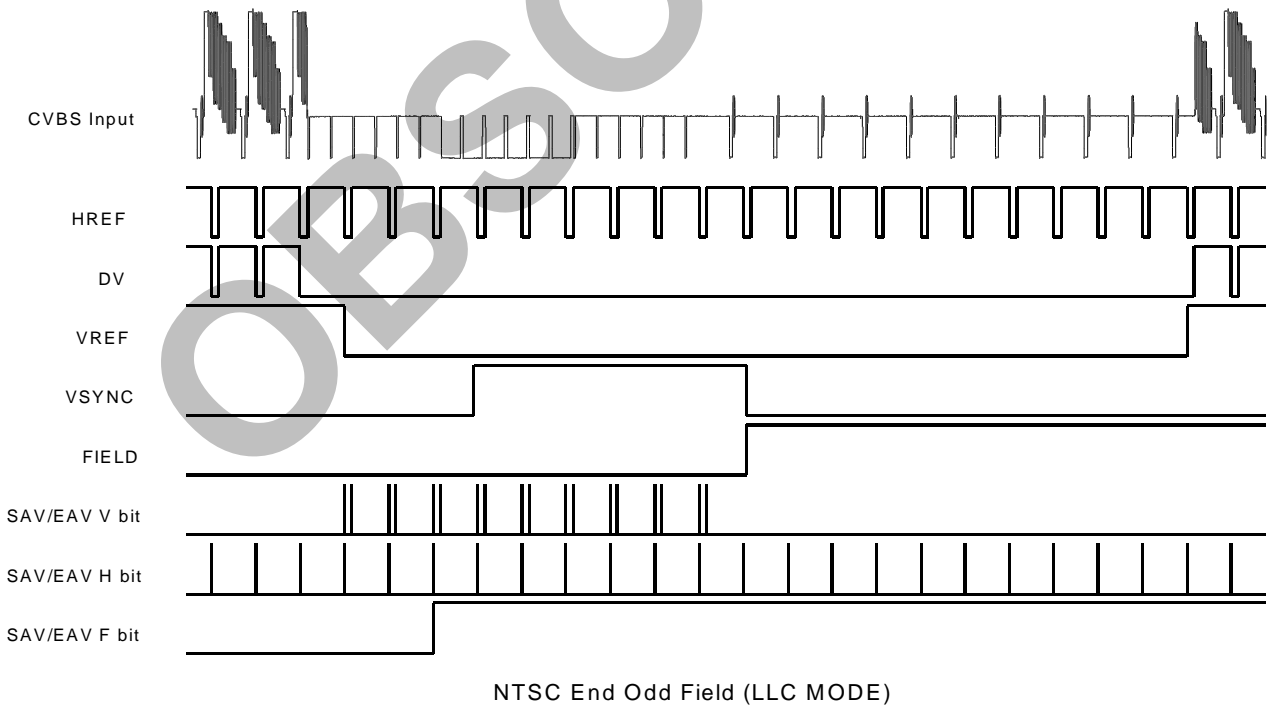
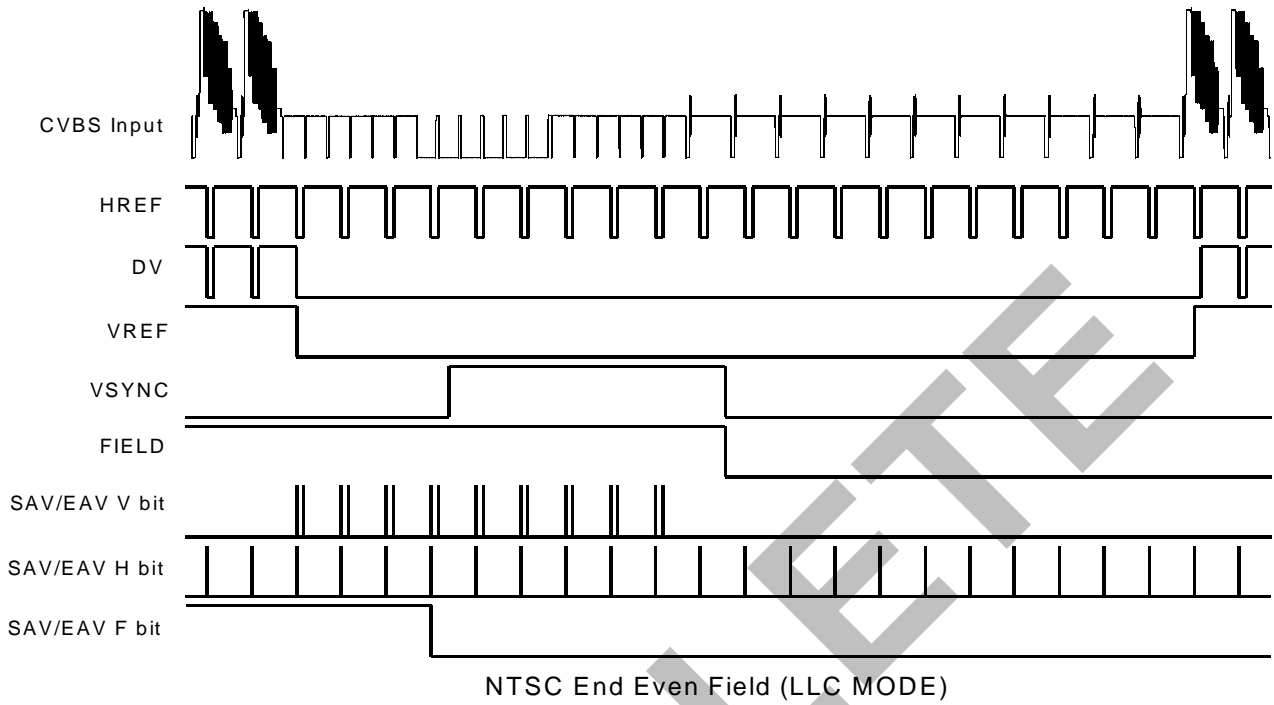


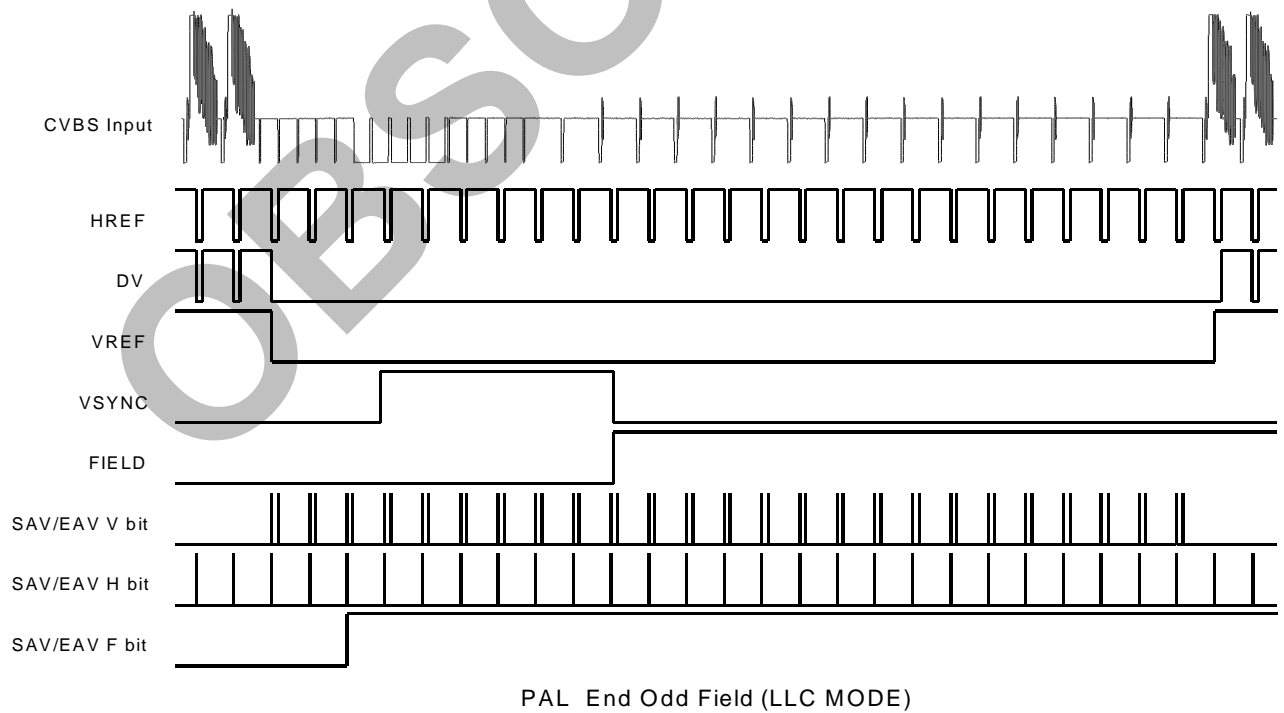
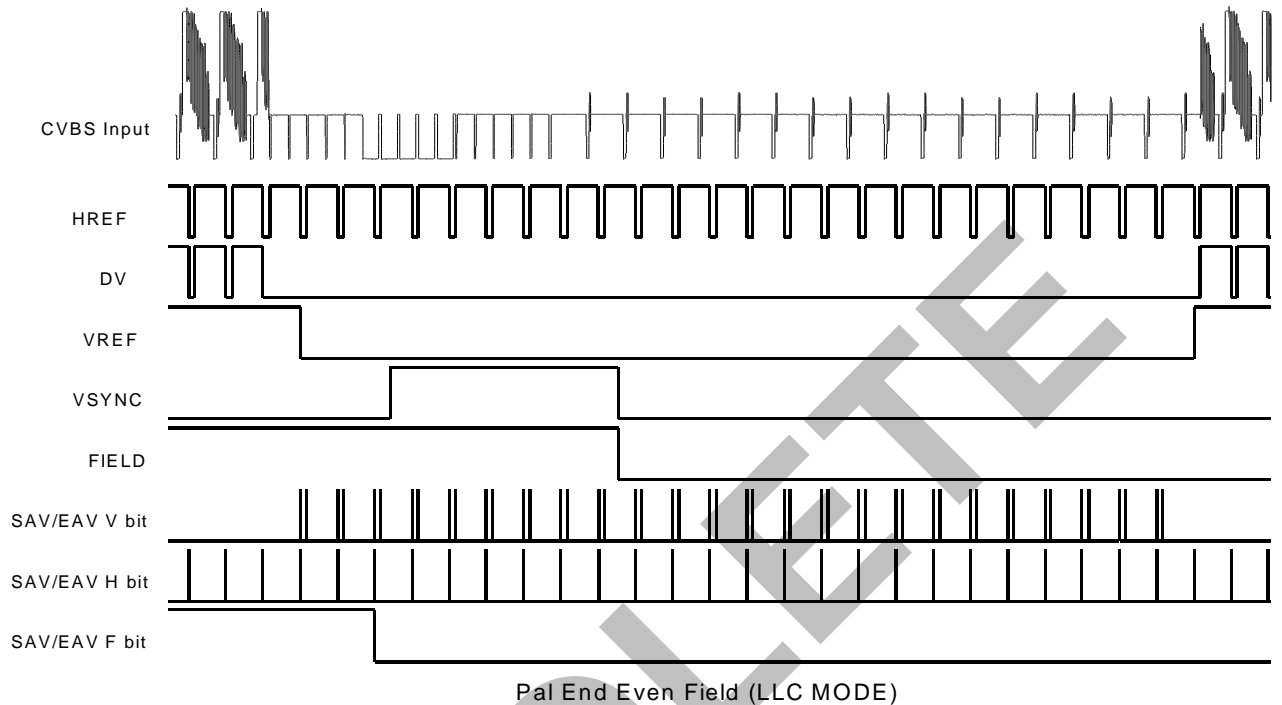
Figure xx. Chrominance shaping filter responses (closeup)

ADV7183

NTSC OUTPUT TIMING DIAGRAMS



PAL OUTPUT TIMING DIAGRAMS



ADV7183

MPU PORT DESCRIPTION.

The ADV7183 support a two wire serial (I^2C Compatible) microprocessor bus driving multiple peripherals. Two inputs Serial Data (SDATA) and Serial Clock (SCLOCK) carry information between any device connected to the bus. Each slave device is recognised by a unique address. The ADV7183 has two possible slave addresses for both read and write operations. These are unique addresses for the device and are illustrated in Figure xx. The LSB sets either a read or write operation. Logic level "1" corresponds to a read operation while logic level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7183 to logic level "0" or logic level "1".

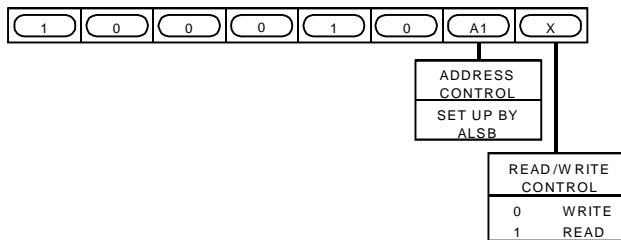


Fig xx. ADV7183 Slave Address

To control the device on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high to low transition on SDATA whilst SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-Bit address + R/W bit). The bits transferred from MSB down to LSB. The peripheral that recognises the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the Start condition and the correct transmitted address. The R/W bit determines the direction of the data. A logic "0" on the LSB of the first byte means that the master will write information

to the peripheral. A logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7183 acts as a standard slave device on the bus. The data on the SDATA pin is 8 bits long supporting the 7-Bit addresses plus the R/W bit. The ADV7183 has 71 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allowing data to be written to or read from from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCLOCK high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7183 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7183 and the part will return to the idle condition.

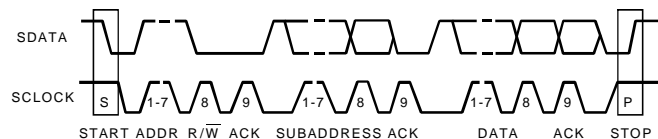


Figure yy. Bus Data Transfer

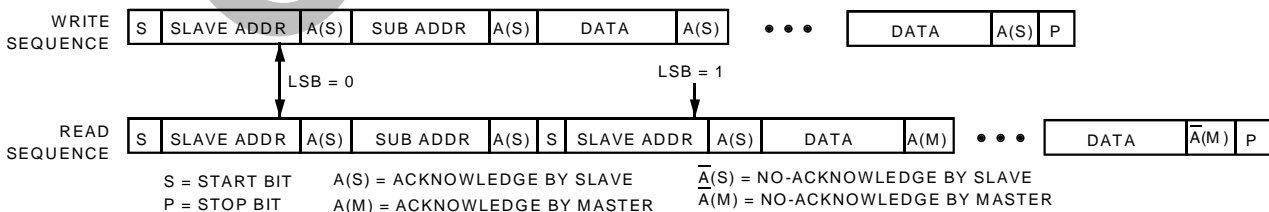


Figure 35 Illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

Figure 36. Write and Read Sequences

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7183 except the Subaddress Register which is a write only register. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the Subaddress Register. Then a read/write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register in terms of its

configuration.

Subaddress Register (SR7-SR0)

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 37 shows the various operations under the control of the Subaddress Register. Zero should always be written to SR7-SR6.

Register Select (SR5-SR0):

These bits are set up to point to the required starting address.

| Register Name | addr (Hex) | | Register Name | addr (Hex) |
|---------------------------|------------|--|------------------------------|------------|
| BASIC BLOCK | | | ADVANCED BLOCK | |
| Input Control | 00 | | Reserved | 1D |
| Video Selection | 01 | | Reserved | 1E |
| Video Enhancement Control | 02 | | Reserved | 1F |
| Output Control | 03 | | Reserved | 20 |
| Extended Output Control | 04 | | Reserved | 21 |
| General Purpose Output | 05 | | Reserved | 22 |
| Reserved | 06 | | Color Subcarrier Control 1 | 23 |
| FIFO Control | 07 | | Color Subcarrier Control 2 | 24 |
| Contrast Control | 08 | | Color Subcarrier Control 3 | 25 |
| Saturation Control | 09 | | Color Subcarrier Control 4 | 26 |
| Brightness Control | 0A | | Pixel Delay Control | 27 |
| Hue Control | 0B | | Manual Clock Control 1 | 28 |
| Default Value Y | 0C | | Manual Clock Control 2 | 29 |
| Default Value C | 0D | | Manual Clock Control 3 | 2A |
| Temporal Decimation | 0E | | Auto Clock Control | 2B |
| Power Management | 0F | | AGC Mode Control | 2C |
| Status Register | 10 | | Chroma Gain Control 1 | 2D |
| Info Register | 11 | | Chroma Gain Control 2 | 2E |
| | | | Luma Gain Control 1 | 2F |
| ADVANCED BLOCK | | | Luma Gain Control 2 | 30 |
| Reserved | 12 | | Manual Gain Shadow Control 1 | 31 |
| Analog Control (internal) | 13 | | Manual Gain Shadow Control 2 | 32 |
| Analog Clamp Control | 14 | | Misc Gain Control | 33 |
| Digital Clamp Control 1 | 15 | | Hsync Position Control 1 | 34 |
| Digital Clamp Control 2 | 16 | | Hsync Position Control 2 | 35 |
| Shaping Filter Control | 17 | | Hsync Position Control 3 | 36 |
| Reserved | 18 | | Polarity Control | 37 |
| Comb Filter Control | 19 | | Reserved | 44 |
| Reserved | 1A | | Reserved | 45 |
| Reserved | 1B | | Reserved | F1 |
| Reserved | 1C | | Reserved | F2 |

Figure 37. Subaddress Register

ADV7183

Table 1.0 Basic Registers

| Register Name | addr (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|------------|-----------|-----------|-----------|-----------|----------|----------|-------------|------------|
| Input Control | 00 | VID SEL.3 | VID SEL.2 | VID SEL.1 | VID SEL.0 | INSEL.3 | INSEL.2 | INSEL.1 | INSEL.0 |
| Video Selection | 01 | ASE | - | BETACAM | 4FSC | DIFFIN | SQPE | VID QUAL.1 | VID QUAL.0 |
| Video Enhancement Control | 02 | - | - | - | COR.1 | COR.0 | YPM.2 | YPM.1 | YPM.0 |
| Output Control | 03 | VBIEN | TOD | OF SEL.3 | OF SEL.2 | OF SEL.1 | OF SEL.0 | OM SEL.1 | OMEL.0 |
| Extended Output Control | 04 | BT656.4 | - | - | - | - | - | - | RANGE |
| General Purpose Output | 05 | HL_EN | BL_C_VBI | GPEH | GPEL | GP0.3 | GP0.2 | GP0.1 | GP0.0 |
| Reserved | 06 | - | - | - | - | - | - | - | - |
| FIFO Control | 07 | FFST | AFR | FR | FFM.4 | FFM.3 | FFM.2 | FFM.1 | FFM.0 |
| Contrast Control | 08 | CON.7 | CON.6 | CON.5 | CON.4 | CON.3 | CON.2 | CON.1 | CON.0 |
| Saturation Control | 09 | SAT.7 | SAT.6 | SAT.5 | SAT.4 | SAT.3 | SAT.2 | SAT.1 | SAT.0 |
| Brightness Control | 0A | BRI.7 | BRI.6 | BRI.5 | BRI.4 | BRI.3 | BRI.2 | BRI.1 | BRI.0 |
| Hue Control | 0B | HUE.7 | HUE.6 | HUE.5 | HUE.4 | HUE.3 | HUE.2 | HUE.1 | HUE.0 |
| Default Value Y | 0C | DEF Y.5 | DEF Y.4 | DEF Y.3 | DEF Y.2 | DEF Y.1 | DEF Y.0 | DEF_AUTO_EN | DEF_VAL_EN |
| Default Value C | 0D | DEF C.7 | DEF C.6 | DEF C.5 | DEF C.4 | DEF C.3 | DEF C.2 | DEF C.1 | DEF C.0 |
| Temporal Decimation | 0E | - | TDR.3 | TDR.2 | TDR.1 | TDR.0 | TDC.1 | TDC.0 | TDE |
| Power Management | 0F | RES | TRAQ | PWRDN | PS CG | PS REF | PDBP | PSC.1 | PSC.0 |
| Status Register | 10 | STATUS.7 | STATUS.6 | STATUS.5 | STATUS.4 | STATUS.3 | STATUS.2 | STATUS.1 | STATUS.0 |
| Info Register | 11 | IDENT.7 | IDENT.6 | IDENT.5 | IDENT.4 | IDENT.3 | IDENT.2 | IDENT.1 | IDENT.0 |

Table 2.0 Advanced Registers

| Register Name | addr (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Reserved | 12 | - | - | - | - | - | - | - | - |
| Reserved | 13 | - | - | - | - | - | - | TIM_OE | - |
| Analog Clamp Control | 14 | - | - | VCLEN | CCLEN | FACL.1 | FACL.0 | FICL.1 | FICL.0 |
| Digital Clamp Control 1 | 15 | DCCM | DCT.1 | DCT.0 | DCTE | DCC0.11 | DCC0.10 | DCC0.9 | DCC0.8 |
| Digital Clamp Control 2 | 16 | DCC0.7 | DCC0.6 | DCC0.5 | DCC0.4 | DCC0.3 | DCC0.2 | DCC0.1 | DCC0.0 |
| Shaping Filter Control | 17 | CSEFM.2 | CSEFM.1 | CSEFM.0 | YSFM.4 | YSFM.3 | YSFM.2 | YSFM.1 | YSFM.0 |
| Reserved | 18 | - | - | - | - | - | - | - | - |
| Comb Filter Control | 19 | - | - | - | COMB_AD | CCM.1 | CCM.0 | - | - |
| Color Subcarrier Control 1 | 23 | - | - | - | CSM | CSMF.27 | CSMF.26 | CSMF.25 | CSMF.24 |
| Color Subcarrier Control 2 | 24 | CSMF.23 | CSMF.22 | CSMF.21 | CSMF.20 | CSMF.19 | CSMF.18 | CSMF.17 | CSMF.16 |
| Color Subcarrier Control 3 | 25 | CSMF.15 | CSMF.14 | CSMF.13 | CSMF.12 | CSMF.11 | CSMF.10 | CSMF.9 | CSMF.8 |
| Color Subcarrier Control 4 | 26 | CSMF.7 | CSMF.6 | CSMF.5 | CSMF.4 | CSMF.3 | CSMF.2 | CSMF.1 | CSMF.0 |

Table 2.1 Advanced Registers Continued

| Register Name | addr (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------------|------------|-----------|-----------|------------|-----------|-----------|-----------|-----------|-----------|
| Pixel Delay Control | 27 | SW_PC | - | CTA.2 | CTA.1 | CTA.0 | - | - | - |
| Manual Clock Control 1 | 28 | FIX27E | CLKMANE | - | - | - | - | CLKVAL.17 | CLKVAL.16 |
| Manual Clock Control 2 | 29 | CLKVAL.15 | CLKVAL.14 | CLKVA5L.13 | CLKVAL.12 | CLKVAL.11 | CLKVAL.10 | CLKVAL.9 | CLKVAL.8 |
| Manual Clock Control 3 | 2A | CLKVAL.7 | CLKVAL.6 | CLKVA5L.13 | CLKVAL.4 | CLKVAL.3 | CLKVAL.2 | CLKVAL.1 | CLKVAL.0 |
| Auto Clock Control | 2B | ACKLM.2 | ACKLM.1 | ACKLM.0 | - | - | - | - | - |
| AGC Mode Control | 2C | - | LAGC.2 | LAGC.1 | LAGC.0 | - | - | CAGC.1 | CAGC.0 |
| Chroma Gain Control 1 | 2D | CAGT.1 | CAGT.0 | - | - | CMG.11 | CMG.10 | CMG.9 | CMG.8 |
| Chroma Gain Control 2 | 2E | CMG.7 | CMG.6 | CMG.5 | CMG.4 | CMG.3 | CMG.2 | CMG.1 | CMG.0 |
| Luma Gain Control 1 | 2F | LAGT.1 | LAGT.0 | - | - | LMG.11 | LMG.10 | LMG.9 | LMG.8 |
| Luma Gain Control 2 | 30 | LMG.7 | LMG.6 | LMG.5 | LMG.4 | LMG.3 | LMG.2 | LMG.1 | LMG.0 |
| Manual Gain Shadow Control 1 | 31 | SGUE | - | - | - | LMGS.11 | LMGS.10 | LMGS.9 | LMGS.8 |
| Manual Gain Shadow Control 2 | 32 | LMGS.7 | LMGS.6 | LMGS.5 | LMGS.4 | LMGS.3 | LMGS.2 | LMGS.1 | LMGS.0 |
| Misc Gain Control | 33 | - | CKE | - | MIRE.2 | MIRE.1 | MIRE.0 | AV_AL | PW_UPD |
| Hsync Position Control 1 | 34 | HSB.9 | HSB.8 | HSE.9 | HSE.8 | - | - | - | - |
| Hsync Position Control 2 | 35 | HSB.7 | HSB.6 | HSB.5 | HSB.4 | HSB.3 | HSB.2 | HSB.1 | HSB.0 |
| Hsync Position Control 3 | 36 | HSE.7 | HSE.6 | HSE.5 | HSE.4 | HSE.3 | HSE.2 | HSE.1 | HSE.0 |
| Polarity Control | 37 | PHS | PHVR | PVS | PLLCR | PF | PDV | PFF | PCLK |
| Resample control | 44 | - | FSC_INV | - | - | - | - | - | - |
| Reserved | 45 | - | - | - | - | - | - | - | - |
| Reserved | F1h | - | - | - | - | - | - | - | - |
| Reserved | F2h | - | - | - | - | - | - | - | - |

PRELIMINARY TECHNICAL DATA

ADV7183

Register 00

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting |
|------------|---------------|--|------|------|------|------|------|------|------|------|---|
| 00hex | Input Control | INSEL [3:0] The INSEL bits allow the user to select an input channel as well as the input format | | | | | | | | | |
| | | | | | | 0 | 0 | 0 | 0 | | CVBS in on AIN1 Composite |
| | | | | | | 0 | 0 | 0 | 1 | | CVBS in on AIN2 |
| | | | | | | 0 | 0 | 1 | 0 | | CVBS in on AIN3 |
| | | | | | | 0 | 0 | 1 | 1 | | CVBS in on AIN4 |
| | | | | | | 0 | 1 | 0 | 0 | | CVBS in on AIN5 |
| | | | | | | 0 | 1 | 0 | 1 | | CVBS in on AIN6 |
| | | | | | | 0 | 1 | 1 | 0 | | Y on AIN1, C on AIN4 S-Video |
| | | | | | | 0 | 1 | 1 | 1 | | Y on AIN2, C on AIN5 |
| | | | | | | 1 | 0 | 0 | 0 | | Y on AIN3, C on AIN6 |
| | | | | | | 1 | 0 | 0 | 1 | | Y on AIN1, U on AIN4, V on AIN5 YUV |
| | | | | | | 1 | 0 | 1 | 0 | | Y on AIN2, U on AIN3, V on AIN6 |
| | | VID_SEL [3:0] The VID_SEL bits allow the user to select the input video standard | | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | | | | | Auto detect PAL (BGHID), NTSC (without pedestal) |
| | | | 0 | 0 | 0 | 1 | | | | | Auto detect PAL (BGHID), NTSC (m) (with pedestal) |
| | | | 0 | 0 | 1 | 0 | | | | | Auto detect PAL (N), NTSC (M) (without pedestal) |
| | | | 0 | 0 | 1 | 1 | | | | | Auto detect PAL (N), NTSC (M) (with pedestal) |
| | | | 0 | 1 | 0 | 0 | | | | | NTSC (M) without pedestal |
| | | | 0 | 1 | 0 | 1 | | | | | NTSC (M) with pedestal |
| | | | 0 | 1 | 1 | 0 | | | | | NTSC 4.43 without pedestal |
| | | | 0 | 1 | 1 | 1 | | | | | NTSC 4.43 with pedestal |
| | | | 1 | 0 | 0 | 0 | | | | | PAL BGHID without pedestal |
| | | | 1 | 0 | 0 | 1 | | | | | PAL N with pedestal |
| | | | 1 | 0 | 1 | 0 | | | | | PAL M without pedestal |
| | | | 1 | 0 | 1 | 1 | | | | | PAL M with pedestal |
| | | | 1 | 1 | 0 | 0 | | | | | PAL combination N |
| | | | 1 | 1 | 0 | 1 | | | | | PAL combination N with pedestal |

:

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | | |
|------------|---|---|------|------|------|------|------|------|------|------|---------------------------------------|----------------------------|--|
| 01hex | Video selection | VID_QUAL [1:0] allows the user to influence the time constant of the system depending on the input video quality. | | | | | | | 0 | 0 | Broadcast quality | | |
| | | | | | | | | | 0 | 1 | TV quality | | |
| | | | | | | | | | | 1 | 0 | VCR quality | |
| | | | | | | | | | | 1 | 1 | Surveillance quality | |
| | SQPE Allows the use to enable/disable the square pixel operation. | | | | | | | | 0 | | Standard mode | | |
| | | | | | | | | | 1 | | Enable square pixel mode | | |
| | DIFFIN Allows the user to select a differential input mode for every entry in the INSEL [3:0] table. | | | | | | | 0 | | | Single ended inputs | | |
| | | | | | | | | 1 | | | Differential inputs | | |
| | FFSC Four Fsc Mode This bit allows the selection of a special NTSC mode where the data is resampled to 4Fsc sampling rate. As a result the LLC will operate at a 4 Fsc rate as well. | | | | 0 | | | | | | Standard Video operation | Only Valid for NTSC input. | |
| | | | | | 1 | | | | | | Select 4 Fsc mode (for NTSC only) | | |
| | BETACAM | | | | 0 | | | | | | Standard video input | | |
| | | | | | 1 | | | | | | Betacam input enable | | |
| | RESERVED | | | | | | | | | 0 | A zero must be written to this bit | | |
| | ASE Automatic Startup Enable When set a change in the INSEL register will automatically be detected and lead the device to enter a video reacquire mode. May be disabled for genlocked video sources. | | | | | | | | | | | | |
| | | | | | | | | | | 1 | INSEL change will not cause reacquire | | |
| | | | | | | | | | | 0 | INSEL change will trigger reacquire | | |

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | |
|------------|---------------------------|--|--|------|------|------|------------------------|------|-----------------------|------|---------------------|--|
| 02hex | Video Enhancement Control | YPM [2:0] Y Peaking Filter Mode .This function allows the user to boost/attenuate luma signals around the colour subcarrier frequency. | | | | | | 0 | 0 | 0 | C=+4.5dB, S=+9.25dB | Used to enhance the picture and improve the contrast C=Composite(2.6Mhz) S=S-Video (3.75Mhz) |
| | | | | | | | | 0 | 0 | 1 | C=+4.5dB, S=+9.25dB | |
| | | | | | | | | 0 | 1 | 0 | C=+4.5dB, S=+5.75dB | |
| | | | | | | | | 0 | 1 | 1 | C=+1.25dB, S=+3.3dB | |
| | | | | | | | | 1 | 0 | 0 | No Change C=+0.S=+0 | |
| | | | | | | | | 1 | 0 | 1 | C=-1.25dB, S=-3dB | |
| | | | | | | | | 1 | 1 | 0 | C=-1.75dB, S=-8dB | |
| | | | | | | | | 1 | 1 | 1 | C=-3.0dB, S=-8dB | |
| | | | COR[1:0] Coring Selection, Controls optional coring of the Y output signal depending on its level. | | | | 0 | 0 | No Coring | | | |
| | | | | | | | 0 | 1 | Truncate if Y<black+8 | | | |
| | | | | | 1 | 0 | Truncate if Y<black+16 | | | | | |
| | | | | | 1 | 1 | Truncate if Y<black+32 | | | | | |
| | Reserved | | | 0 | 0 | 0 | Set to Zero | | | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | | | | |
|------------|--|--|------|------|------|------|------|------|------|------|------------------|--------------------|-------------------------------|---------------------------|--|
| 03hex | Output Control | OM_SEL [1:0] Output Mode Selection. Selects the output mode as in the timing and interface type. | | | | | | | | 0 | 0 | Philips compatible | | | |
| | | | | | | | | | | | 0 | 1 | Broktree API A compatible | | |
| | | | | | | | | | | | | 1 | 0 | Broktree API B compatible | |
| | | | | | | | | | | | | 1 | 1 | Not Valid setting | |
| | OF_SEL [3:0] Allows the user to choose from a set of output formats. | | | | 0 | 0 | 0 | 0 | | | | | Reserved | | |
| | | | | | 0 | 0 | 0 | 1 | | | | | Reserved | | |
| | | | | | 0 | 0 | 1 | 0 | | | | | 16-bit@LLC 4:2:2 CCIR656 | | |
| | | | | | 0 | 0 | 1 | 1 | | | | | 8-bit@LLC 4:2:2 CCIR656 | | |
| | | | | | 0 | 1 | 0 | 0 | | | | | 12-bit@LLC2 4:1:1 | | |
| | | | | | 0 | 1 | 0 | 1 | | | | | 10-bit@LLC 4:2:2 CCIR656 | 10-bit composite in | |
| | | | | | 0 | 1 | 1 | 0 | | | | | 8-bit@LLC 4:2:2 CCIR656 | 10-bit composite in | |
| | | | | | 0 | 1 | 1 | 1 | | | | | Reserved | | |
| | | | | | 1 | 0 | 0 | 0 | | | | | Reserved | | |
| | | | | | 1 | 0 | 0 | 1 | | | | | 8-bit@LLC 4:2:2 CCIR656 | with Debug signals I | |
| | | | | | 1 | 0 | 1 | 0 | | | | | 8-bit@LLC 4:2:2 CCIR656 | with Debug signals II | |
| | | | | | 1 | 0 | 1 | 1 | | | | | Not Used | | |
| | | | | | 1 | 1 | 0 | 0 | | | | | Not Used | | |
| | | | | | 1 | 1 | 0 | 1 | | | | | Not Used | | |
| | | | | 1 | 1 | 1 | 0 | | | | | Not Used | | | |
| | | | | 1 | 1 | 1 | 1 | | | | | Not Used | | | |
| | TOD Tri-State Output Drivers. This bit allows the user to tri-state the output Drivers regardless of the state of the /OE pin. | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | Drivers dependant on /OE pin | | |
| | | | | | | | | | | | | | Drivers tri-stated. | Regardless of /OE pin | |
| | VBI_EN Allows VBI data (lines 1 to 21) to be passed through with only a minimum amount of filtering performed. | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | All lines filtered and scaled | | |
| | | | | | | | | | | | | | Only active video region | | |

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | | |
|------------|---|---|------|------|------|------|------|------|------|------|------------------|-----------------------------|--------------------|
| 04hex | Extended output control | RANGE Allows the user to select the range of output values. Can be CCIR601 compliant or fill the whole accessible number range. | | | | | | | | | 0 | CCIR compliant | |
| | | | | | | | | | | | 1 | Fill whole accessible range | |
| | | | | | | | | | | | 1 | 1 | 0 |
| | Reserved Bits | | | | | | | | | | | | |
| | DDOS [2:0] D Data Output selection. If the 100 pin package is used the 12 additional pins can output additional data. | | | | | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | | | No additional data |
| | BT656-4 Allows the user to select an output mode that is compatible with BT656-4 or BT656-3. | | | | | | | | | | | | |
| | | | | | | | | | | | | BT656-3 compatible | |
| | | | | | | | | | | | | BT656-4 compatible | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | | | |
|------------|------------------------|---|------|------|------|------|------|------|------|------|---------------------------|----------------------|-------------------------------------|--|
| 05hex | General purpose Output | GPO [3:0] These general purpose outputs pins may be programmed by the user but are only available in selected output modes OF_SEL[3:0] and when the output drivers are enabled using GPEL ,GPEH and HL_Enable bits. | | | | | | | | | | Pixel Data Valid off | | |
| | | | | | | | 0 | 0 | 0 | 0 | User Programmable | | | |
| | | GPEL General Purpose enable low This bit enables the output drivers for the general purpose outputs bits 0 and 1. | | | | | | | | | | | HD Test pattern off | |
| | | | | | | 0 | | | | | | | GPO[1:0] tri-stated | |
| | | | | 1 | | | | | | | | | GPO[1:0] enabled | |
| | | GPEH General Purpose enable low This bit enables the output drivers for the general purpose outputs bits 3 and 2. | | | | | | | | | | | | |
| | | | | | | 0 | | | | | | | GPO[3:2] tri-stated | |
| | | | | 1 | | | | | | | | | GPO[3:2] enabled | |
| | | BL_C_VBI Blank Chroma during VBI | | | | | | | | | | | | |
| | | | | 0 | | | | | | | | | Decode and output colour during VBI | |
| | | | | 1 | | | | | | | | | Blank Cr and Cb data during VBI | |
| | | HL_EN Hlock Enable This bit causes the General Purpose output [0] pin to output Hlock instead of GPO [0]. Only available in certain output modes. | | | | | | | | | | | Disabled | General Purpose output (lwr bits) must be enabled GPEL |
| | 0 | | | | | | | | | | GPO[0] pin function | | | |
| | 1 | | | | | | | | | | GPO[0] shows Hlock status | | | |

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | | | |
|------------|-------------------|---|------|------|------|------|------|------|------|------|----------------------|--|----------------------|---------------------|
| 07h | Fifo Control | FFM [4:0] Fifo flag margin The FFM register allows the user to program the location at which the FIFO flag's AEF and AFF. | | | | | | | | | | | | |
| | | | | | | 0 | 0 | 1 | 0 | 0 | User programmable | | | |
| | | FR Fifo reset Setting this bit will cause the FIFO to reset. | | | | | | | | | | | | |
| | | | | | 0 | | | | | | | | Normal operation | |
| | | | | 1 | | | | | | | | | FIFO reset | bit is auto cleared |
| | | AFR Automatic Fifo reset Setting this bit will cause the FIFO to automatically reset at the end of each field of video | | | | | | | | | | | | |
| | | | | | 0 | | | | | | | | No auto reset | |
| | | | | 1 | | | | | | | | | Auto reset | |
| | | FFST Fifo Flag Self Time Set weather the Fifo flags AEF,AFF and HFF are output synchronous to the external CLKIN of the 27Mhz internal clock. | | | | | | | | | | | | |
| | | | | 0 | | | | | | | | | Synchronous to CLKIN | |
| | | 1 | | | | | | | | | Synchronous to 27Mhz | | | |
| 08h | Contrast register | CON[7:0] Contrast Adjust This is the user control for contrast adjustment | | | | | | | | | | | | |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | |
|------------|---------------------|---|------|------|------|------|------|------|------|------|------------------------------|------------------------------|
| 09h | Saturation register | SAT[7:0] Saturation Adjust This allows the user to adjust the saturation of colour output | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 0Ah | Brightness register | BRI[7:0] This register controls the brightness of the video signal. | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 0Bh | Hue Register | HUE[7:0] This register contains the value for the colour hue adjustment. | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Range -90 with h00=0 | The resolution is 1bit=.7 |
| 0Ch | Default Value Y | DEF_VAL_EN Default Value Enable | | | | | | | 0 | | Use programmed value | Y, Cr and Cb values |
| | | | | | | | | | 1 | | Use default value | |
| | | DEF_VAL_AUTO_EN Default Value Auto Enable In the case of lost lock enables/disables default values. | | | | | | | 0 | | Use programmed value | When lock is lost |
| | | | | | | | | | 1 | | Use default value | |
| 0Dh | Default Value C | DEF_C[7:0] Default Value C . Cr and Cb default values are defined in this register. | 0 | 0 | 0 | 1 | 0 | 0 | | | Cr[7:0]={DEF_C[7:4],0,0,0,0} | Cb[7:0]={DEF_C[3:0],0,0,0,0} |
| | | | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | |
|------------|--|---|------|-----------------------|-----------------------|-----------------------|------|------|------|---|------------------|--|
| 0Eh | Temporal Decimation | TDE Temporal Decimation Enable bit allows the user to enable/disable the temporal function. | | | | | | | | 0 | Disabled | Configured using TDC[1:0] and TDR[3:0] |
| | | | | | | | | | | 1 | Enabled | |
| | TDC[1:0] Temporal Decimation Control allows the user to select the suppression of selected fields of video. | | | | | | | 0 | 0 | Suppress frames, start with even field. | | |
| | | | | | | | | 0 | 1 | Suppress frames, start with odd field. | | |
| | | | | | | | | 1 | 0 | Suppress even fields only. | | |
| | | | | | | | | 1 | 1 | Suppress odd fields only. | | |
| | | | | | | | | | | | | |
| | TDR[3:0] Temporal Decimation Rate specifies how many fields/frames as to be skipped before a valid one is output | | | | | | | | | | | AS specified in the TDC[1:0] register |
| | | 0 | 0 | 0 | 0 | Skip no Field/Frame | | | | | | |
| | | 0 | 0 | 0 | 1 | Skip 1 Field/Frame | | | | | | |
| | | 0 | 0 | 1 | 0 | Skip 2 Fields/Frames | | | | | | |
| | | 0 | 0 | 1 | 1 | Skip 3 Fields/Frames | | | | | | |
| | | 0 | 1 | 0 | 0 | Skip 4 Fields/Frames | | | | | | |
| | | 0 | 1 | 0 | 1 | Skip 5 Fields/Frames | | | | | | |
| | | 0 | 1 | 1 | 0 | Skip 6 Fields/Frames | | | | | | |
| | | 0 | 1 | 1 | 1 | Skip 7 Fields/Frames | | | | | | |
| | | 1 | 0 | 0 | 0 | Skip 8 Fields/Frames | | | | | | |
| | | 1 | 0 | 0 | 1 | Skip 9 Fields/Frames | | | | | | |
| | | 1 | 0 | 1 | 0 | Skip 10 Fields/Frames | | | | | | |
| | | 1 | 0 | 1 | 1 | Skip 11 Fields/Frames | | | | | | |
| 1 | | 1 | 0 | 0 | Skip 12 Fields/Frames | | | | | | | |
| 1 | | 1 | 0 | 1 | Skip 13 Fields/Frames | | | | | | | |
| 1 | 1 | 1 | 0 | Skip 14 Fields/Frames | | | | | | | | |
| 1 | 1 | 1 | 1 | Skip 15 Fields/Frames | | | | | | | | |
| | Reserved | | | | | | | | | | | |
| | | 0 | | | | | | | | | Set to Zero | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | | |
|------------|--|---|------|------|------|------|------|------|------|------|-----------------------------|---|-----------------------|
| 0Fh | Power Management | PSC[1:0] Power Save Control allows the a set of different power save modes to be selected . | | | | | | | | | | | |
| | | | | | | | | | 0 | 0 | Full Operation | | |
| | | | | | | | | | | | 0 | 1 | CVBS input only |
| | | | | | | | | | | | 1 | 0 | Digital only |
| | | | | | | | | | | 1 | 1 | Power Save Mode | |
| | | PDBP Power Down Bit Priority There are two ways to shut down the digital core, the Power Down Bit which has higher priority | | | | | | | | | | | |
| | | | | | | | | | 0 | | Pwr. Dwn. Controller by Pin | | |
| | | | | | | | | | 1 | | Pwr. Dwn. Controller by Bit | | |
| | PS_REF Power Save Reference allows the user to enable/disable the internal analog reference. | | | | | | | 0 | | | Reference Functional | | |
| | | | | | | | | 1 | | | Reference in Pwr. Save mode | | |
| | PS_CG Power Save For the LLC Clock Generator | | | | | | | | | | | Clock Generator functional | |
| | | | | | | | | | | | | 1 | CG in Power Save Mode |
| | PWRDN Power Down Disables the input pads and powers down the 27Mhz clock | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | System functional | |
| | | | | | | | | | | | 1 | PowerDown | |
| | TRAQ Timing ReAcquire will cause the part to reaquire the video signal and is the software version of the ISO pin. | | | | | | | | | | | If bit is set will clear its self on the next 27Mhz clk cycle | |
| | | | | | | | | | | | 0 | | Normal Operation |
| | | | | | | | | | | | 1 | | Require Video signal |
| | Reserved | | | | | | | | | | 0 | Reserved Bit set to Zero | |
| 10h | Status Register Read only | Status[7:0] Provides information about the internal status of the decoder. | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | x | | |
| 11h | Info Register Read Only | IDENT[7:0] Provides identification on the revision of the part. | | | | | | | | | | 0=v85a , 3=v85b , 4=v85b3 | |
| | | | x | x | x | x | x | x | x | x | x | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Register Setting | |
|------------|-------------------------|---|------|------|------|------|------|------|------|------------------------|---------------------------|---------------------------|
| 13h | Analog Control Internal | TIM_OE Timing Signals Output Enables the user to force the output drivers for H-SYNC,V-SYNV and Field into an active state regardless of the OE pin and TOD bit. | | | | | | | | | | |
| | | | | | | | | | 0 | | Dependant on OE and TOD | |
| | | | | | | | | | | 1 | | HS,VS,F forced active |
| | | Reserved | | | | | | | | | | |
| | | | 0 | 1 | 0 | 0 | 0 | 1 | | 1 | Set at Default Value | |
| 14h | Analog Clamp Control | FICL[1:0] Fine Clamp Length controls the number of clock cycles for which the slow current is on. | | | | | | | | | | |
| | | | | | | | | | 0 | 0 | I on for 16 clock cycles | |
| | | | | | | | | | | 0 | 1 | I on for 32 clock cycles |
| | | | | | | | | | | 1 | 0 | I on for 64 clock cycles |
| | | | | | | | | | 1 | 1 | I on for 128 clock cycles | |
| | | FACL[1:0] Fast Clamp Length controls the number of clock cycles for which the fast current is on. | | | | | | | | | | |
| | | | | | | | | 0 | 0 | | | I on for 16 clock cycles |
| | | | | | | | | 0 | 1 | | | I on for 32 clock cycles |
| | | | | | | | | 1 | 0 | | | I on for 64 clock cycles |
| | | | | | | | | | 1 | 1 | | I on for 128 clock cycles |
| | | CCLLEN Current Clamp Enable allows the user to switch off the I sources in the analog front end | | | | | | | | | | |
| | | | | | | | | 0 | | | | I sources switched off |
| | | | | | | | | 1 | | | | I sources enabled |
| | | VCLLEN Voltage Clamp Enable bit allows the user to disable the voltage clamp circuitry | | | | | | | | | | |
| | | | | | | 0 | | | | Voltage Clamp disabled | | |
| | | | | | | 1 | | | | Voltage Clamp enabled | | |
| Reserved | | | | | | | | | | | | |
| | | | 0 | 0 | | | | | | | Reserved set to Zero | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | | |
|------------|-------------------------|--|--|------|------|------|------|------|------|------|--------------------------|--|--|---------------------------------------|
| 15h | Digital Clamp Control 1 | DCCO[11:8] Digital Colour Clamp Offset holds upper 4-bits of the digital offset value which gets added to the raw data from the ADC before entering the core. | | | | | | | | | | Only applicable if DCCM is set to manual offset mode | | |
| | | | | | | x | x | x | x | | | | | |
| | | DCFE Digital Clamp Freeze Enable allows the user to freeze the digital clamp loop at any point in time | | | | | | | | | | | | |
| | | | | | 0 | | | | | | | | Digital clamp operational | |
| | | | | | 1 | | | | | | | | Digital clamp frozen | |
| | | DCT [1:0] Digital Clamp Timing determines the time constant of the digital clamping circuitry | | | | | | | | | | | | |
| | | | | 0 | 0 | | | | | | | | Slow (TC: 1 sec) | |
| | | | | 0 | 1 | | | | | | | | Medium (TC: 0.5 sec) | |
| | | | | 1 | 0 | | | | | | | | Fast (TC: 0.1 sec) | |
| | | | | 1 | 1 | | | | | | | | Dependent on VID_QUAL | |
| | | | DCCM[7:0] Digital Colour Clamp Mode sets the mode of operation for the digital clamp circuitry | | | | | | | | | | | Offset correction via DCCO for C only |
| | | | | 0 | | | | | | | | | Automatic digital clamp | |
| | | 1 | | | | | | | | | Manual Offset correction | | | |
| 16h | Digital Clamp Control 2 | DCCO[7:0] Digital Colour Clamp Offset holds the lower 8-bits of the digital offset value which gets added to the raw data from the ADC before entering the core. | | | | | | | | | | | Only applicable if DCCM is set to manual offset mode | |
| | | | x | x | x | x | x | x | x | x | | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | | | |
|------------|------------------------|---|------|--|------|------|------|------|------|------|---------|-------------------|--|---|------------------------|
| 17h | Shaping Filter Control | YSFM[4:0] Y Shaping Filter Mode allows the user to select a wide range of low pass and notch filters. | | | | | | | | | | | | | |
| | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | Auto Wide notch | | | |
| | | | | | | 0 | 0 | 0 | 0 | 0 | 1 | Auto Narrow notch | | | |
| | | | | | | 0 | 0 | 0 | 0 | 1 | 0 | SVHS 1 | | | |
| | | | | | | ~ | ~ | ~ | ~ | ~ | ~ | ~ | | | |
| | | | | | | 1 | 0 | 0 | 0 | 1 | 0 | SVHS 17 | | | |
| | | | | | | 1 | 0 | 0 | 0 | 1 | 1 | PAL NN1 | | | |
| | | | | | | 1 | 0 | 1 | 0 | 0 | 0 | PAL NN2 | | | |
| | | | | | | 1 | 0 | 1 | 0 | 1 | 0 | PAL NN3 | | | |
| | | | | | | 1 | 0 | 1 | 1 | 1 | 0 | PAL WN 1 | | | |
| | | | | | | 1 | 0 | 1 | 1 | 1 | 1 | PAL WN 2 | | | |
| | | | | | | 1 | 1 | 0 | 0 | 0 | 0 | NTSC NN1 | | | |
| | | | | | | 1 | 1 | 0 | 0 | 0 | 1 | NTSC NN2 | | | |
| | | | | | | 1 | 1 | 0 | 1 | 0 | 0 | NTSC NN3 | | | |
| | | | | | | 1 | 1 | 0 | 1 | 1 | 0 | NTSC WN1 | | | |
| | | | | | | 1 | 1 | 1 | 0 | 0 | 0 | NTSC WN2 | | | |
| | | | | | | 1 | 1 | 1 | 0 | 1 | 1 | NTSC WN3 | | | |
| | | | | | | 1 | 1 | 1 | 1 | 1 | 0 | Not Used | | | |
| | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SVHS 18 | | | |
| | | | | CSFM[2:0] C Shaping Filter Mode allows the selection from a range of low pass chrominance filters. | | | | | | | | | | Auto = filter selected based on scaling factor. | |
| | | | | | 0 | 0 | 0 | | | | | | | | Auto selection 1.5Mhz |
| | | | | | 0 | 0 | 1 | | | | | | | | Auto selection 2.17Mhz |
| | | | | | 0 | 1 | 0 | | | | | | | | SH1 |
| | | | | | ~ | ~ | ~ | | | | | | | | ~ |
| | | 1 | 1 | | 0 | | | | | | | SH5 | | | |
| | | 1 | 1 | 1 | | | | | | | SH6 | | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | | |
|------------|-----------------------------|---|----------|------|------|------|------|------|------|------|------------|-------------|--------------------------|-----------------------|
| 19h | Comb Filter Control | Reserved | | | | | | | | 0 | 0 | Set to Zero | | |
| | | CCM[1:0] Chroma Comb Mode selects a primary mode for the filter | | | | | | | | | | | | |
| | | | | | | | 0 | 0 | | | | | No Comb | |
| | | | | | | | 0 | 1 | | | | | 1H | |
| | | | | | | | 1 | 0 | | | | | 2H | |
| | | | | | | | 1 | 1 | | | | | Not Valid, do not use | |
| | | CCMB_AD Chroma Comb Adaptive | | | | 0 | | | | | | | Chroma Comb non-adaptive | |
| | | | | | | 1 | | | | | | | Chroma Comb adaptive | |
| | | | Reserved | | | | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | | | Set to Zero | |
| 23h | Colour Subcarrier Control 1 | CSMF[27:24] Colour Subcarrier Manual Frequency Holds the value used to enable the user support odd subcarrier frequencies | | | | | x | x | x | x | | | | |
| | | | | | | | | | | | | | | |
| | | CSM Colour Subcarrier Manual | | | | 0 | | | | | | | Manual Fsc. Disabled | |
| | | | | | | 1 | | | | | | | User defined Fsc. | Defined in CSFM[27:0] |
| | | Reserved | | | | | | | | | | | | |
| | | | 1 | 1 | 1 | | | | | | Set to One | | | |
| 24h | Colour Subcarrier Control 2 | CSMF[23:16] Colour Subcarrier Manual Frequency Holds the value used to enable the user support odd subcarrier frequencies | | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | | | | |
| 25h | Colour Subcarrier Control 3 | CSMF[15:8] Colour Subcarrier Manual Frequency Holds the value used to enable the user support odd subcarrier frequencies | | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | | | | |
| 26h | Colour Subcarrier Control 4 | CSMF[7:0] Colour Subcarrier Manual Frequency Holds the value used to enable the user support odd subcarrier frequencies | | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | | |
|------------|------------------------|---|------|------|------|------|------|------|------|------|----------------------------|-------------|---------------------------|--|
| 27h | Pixel Delay Control | Reserved | | | | | | | 0 | 0 | 0 | Set to Zero | | |
| | | CTA[2:0] Chroma Timing Adjust allows a specified timing difference between the Luma and Chroma samples | | | | 0 | 0 | 0 | | | | | Not valid setting | |
| | | | | | 0 | 0 | 1 | | | | | | Chroma+2 pixel (early) | |
| | | | | | 0 | 1 | 0 | | | | | | Chroma+1 pixel (early) | |
| | | | | | 0 | 1 | 1 | | | | | | No Delay | |
| | | | | | 1 | 0 | 0 | | | | | | Chroma-1 pixel (late) | |
| | | | | | 1 | 0 | 1 | | | | | | Chroma-2 pixel (late) | |
| | | | | | 1 | 1 | 0 | | | | | | Chroma-3 pixel (late) | |
| | | | | | 1 | 1 | 1 | | | | | | Not valid setting | |
| | | Reserved | | | | | | | | | | | | |
| | | | | | 1 | | | | | | | | Set to One | |
| | | SWPC This bit allows the Cr and Cb samples to be swapped. | | | | | | | | | | | | |
| | | | 0 | | | | | | | | | | No swapping | |
| | | | | | 1 | | | | | | | | Swap the Cr and Cb values | |
| 28h | Manual Clock Control 1 | CLKVAL[17:16] If enabled via CLKMANE then CLKVAL[17:0] determines the fixed output freq. On the LLC, LLC2 and LLCRef pins. | | | | | | | | | | | | |
| | | | | | | | | | | x | x | | | |
| | | Reserved | | | | | | | | | | | | |
| | | | | | 1 | 1 | 1 | 1 | | | | | Set to Default | |
| | | CLKMANE Clock Generator Manual Enable allows the analog clock generator to produce a fixed clock frequency which is not dependent on the video signal | | | | | | | | | | | | |
| | | | 0 | | | | | | | | | | O/p freq set by video | |
| | | | | | 1 | | | | | | | | freq set by CLKVAL[17:0] | |
| | | FIX27E Allows the o/p of fixed 27Mhz crystal clock via LLC, LLC2 and LLCRef o/p pins. | | | | | | | | | | | | |
| 0 | | | | | | | | | | | O/p freq set by clock gen. | | | |
| | | | 1 | | | | | | | | O/p 27Mhz fixed. | | | |
| 29h | Manual Clock Control 2 | CLKVAL[15:8] See above | | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | x | | | |
| 2Ah | Manual Clock Control 3 | CLKVAL[7:0] See above | | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | x | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | |
|------------|--------------------|---|------|------|------|------|------|------|------|-------------|-------------------|--|-------------------------|
| 2Bh | Auto Clock Control | Reserved | | | | | | | | | | | |
| | | | | | 0 | 0 | 0 | 0 | 0 | | | Set to Zero | |
| | | ACLKN[2:0] Automatic Clock Generator Mode influences the mode of operation for the LLC | | | | | | | | | | Only when NOT in manual mode | |
| | | 0 0 0 | | | | | | | | | | Colour Burst line | |
| | | 0 0 1 | | | | | | | | | | Start:line24 colour burst line | |
| | | 0 1 0 | | | | | | | | | | Active Video | |
| | | 0 1 1 | | | | | | | | | | Active Video(<304) PAL | (<264)NTSC |
| | | 1 0 0 | | | | | | | | | | Active Video(<304) PAL | (<256)NTSC |
| | | 1 0 1 | | | | | | | | | | ActiveVideo(<319/320) PAL | (<273/274)NTSC |
| | | 1 1 0 | | | | | | | | | | Invalid | |
| | | 1 1 1 | | | | | | | | | | Invalid | |
| 2Ch | AGC Mode Control | CAGC[1:0] Chroma Automatic Gain Control selects the basic mode of operation for the AGC in the chroma path. | | | | | | | | | | | |
| | | | | | | | | 0 | 0 | | Manual Fixed gain | Use CMG[11:0] | |
| | | | | | | | | | 0 | 1 | | Use luma gain for chroma | |
| | | | | | | | | | 1 | 0 | | Automatic gain | Based on colour burst |
| | | | | | | | | | 1 | 1 | | Freeze chroma gain | |
| | | Reserved | | | | | | | | | | | |
| | | | | | 1 | 1 | | | | | | Set to One | |
| | | LAGC[2:0] Luma Automatic Gain Control selects the mode of operation for the gain control in the luma path | | | | | | | | | | | |
| | | 0 0 0 | | | | | | | | | | Manual Fixed gain | Use LMG[11:0] |
| | | 0 0 1 | | | | | | | | | | AGC no override through white peak. Man IRE control | Blank level to sync tip |
| | | 0 1 0 | | | | | | | | | | AGC auto override through white peak. Man IRE control | Blank level to sync tip |
| | | 0 1 1 | | | | | | | | | | AGC no override through white peak. Auto IRE control | Blank level to sync tip |
| | | 1 0 0 | | | | | | | | | | AGC auto override through white peak. Auto IRE control | Blank level to sync tip |
| | | 1 0 1 | | | | | | | | | | AGC active video with white peak | |
| | | 1 1 0 | | | | | | | | | | AGC active video with average video. | |
| 1 1 1 | | | | | | | | | | Freeze gain | | | |
| Reserved | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | Set to One | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | |
|------------|---|---|------|------|------|------|------|------|------|------|--|---|--|
| 2Dh | Chroma Gain Control 1 | CMG[11:8] Chroma Manual Gain can be used program a desired manual chroma gain or read back the actual used gain value | | | | | | | | | CAGC[1:0] settings will decide what mode CMG[11:0] operates in | | |
| | | Reserved | | | | | x | x | x | x | | | |
| | | | | 1 | 1 | | | | | | Set to One | | |
| | CAGT[1:0] Chroma Automatic Gain Timing allows adjustment of the Chroma AGC tracking speed | | | | | | | | | | | Will only have effect if CAGC[1:0] is set to auto gain (10') | |
| | | 0 | 0 | | | | | | | | | Slow (TC: 2 sec) | |
| | | 0 | 1 | | | | | | | | | Medium (TC: 1 sec) | |
| | | 1 | 0 | | | | | | | | | Fast (TC: 0.2 sec) | |
| | 1 | 1 | | | | | | | | | Dependent on VID_QUAL | | |
| 2Eh | Chroma Gain Control 2 | CMG[7:0] Chroma Manual Gain lower 8-bits ,see CMG[11:8] for description | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | | | |
| 2Fh | Luma Gain Control 1 | LMG[11:8] Luma Manual Gain can be used program a desired manual chroma gain or read back the actual used gain value | | | | | | | | | LAGC[1:0] settings will decide what mode LMG[11:0] operates in | | |
| | | Reserved | | | | | x | x | x | x | | | |
| | | | | 1 | 1 | | | | | | Set to One | | |
| | LAGT[1:0]Luma Automatic Gain Timing allows adjustment of the Luma AGC tracking speed | | | | | | | | | | | Will only have effect if LAGC[1:0] is set to auto gain (001,010,011 or 100) | |
| | | 0 | 0 | | | | | | | | | Slow (TC: 2 sec) | |
| | | 0 | 1 | | | | | | | | | Medium (TC: 1 sec) | |
| | | 1 | 0 | | | | | | | | | Fast (TC: 0.2 sec) | |
| | 1 | 1 | | | | | | | | | Dependent on VID_QUAL | | |
| 30h | Luma Gain Control 2 | LMG[7:0] Luma Manual Gain can be used program a desired manual chroma gain or read back the actual used gain value | | | | | | | | | LAGC[1:0] settings will decide what mode LMG[11:0] operates in | | |
| | | | x | x | x | x | x | x | x | x | | | |

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | |
|------------|---|--|------|------|------|------|------|------|------|------|---|---|--|
| 31h | Manual Gain Shadow Control 1 | LMGS[11:8] Luma Manual Gain Store has dual functions, a desired manual luma gain can be programmed or a readback from the register will return the actual gain used. | | | | | | | | | The function and readback value are dependant on LAGC[2:0] setting. | Gain value will only become active when LAGC[2:0] set to manual fixed gain. | |
| | | Reserved | | | | | x | x | x | x | | | |
| | | | | 1 | 1 | 1 | | | | | Set to One | | |
| | SGUE Surveillance Gain Update Enable enables surveillance mode operation see LMGS[11:0] for details | 0 | | | | | | | | | | Disable LMGS update | |
| | | 1 | | | | | | | | | | Use LMGS update facility | |
| 32h | Manual Gain Shadow Control 2 | LMG[7:0] Chroma Manual Gain lower 8-bits ,see LMG[11:8] for description | | | | | | | | | | | |
| | | | x | x | x | x | x | x | x | x | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | |
|---|---|--|------|------|------|------|------|------|------|------------|---|------------------|--|
| 33h | Misc Gain Control | PW_UPD Peak White Update determines the gain based on measurements taken from the active video, this bit determines the rate of gain change. | | | | | | | | | LAGC[1:0] Must be set to the appropriate mode to enable peak white or average video in the first case | | |
| | | | | | | | | | | 0 | Update gain once per line | | |
| | | | | | | | | | | 1 | Update gain once per field | | |
| | AV_AL Average Brightness Active Lines Allows the selection between two ranges of active video to determine the average brightness | | | | | | | | | 0 | Lines 33-310 | | |
| | | | | | | | | | | 1 | Lines 33-270 | | |
| | | | | | | | | | | | | | |
| | Mire[2:0] Max IRE Sets the max. I/p IRE level dependent on the video standard | | | | | 0 | 0 | 0 | | | | PAL-133 NTSC-122 | |
| | | | | | | 0 | 0 | 1 | | | | PAL-125 NTSC-115 | |
| | | | | | | 0 | 1 | 0 | | | | PAL-120 NTSC-110 | |
| | | | | | | 0 | 1 | 1 | | | | PAL-115 NTSC-105 | |
| | | | | | | 1 | 0 | 0 | | | | PAL-110 NTSC-100 | |
| | | | | | | 1 | 0 | 1 | | | | PAL-105 NTSC-100 | |
| | | | | | | 1 | 1 | 0 | | | | PAL-100 NTSC-100 | |
| | | | | | | 1 | 1 | 1 | | | | PAL-100 NTSC-100 | |
| | | | | | | | | | | | | | |
| Reserved | | | 1 | | | | | | | Set to one | | | |
| CKE Colour Kill Enable allows the optional colour kill function to be switched on or off. | | | | | | | | | | | | | |
| | | | 0 | | | | | | | | Colour Kill disabled | | |
| | | | 1 | | | | | | | | Colour Kill enabled | | |
| Reserved | | | | | | | | | | | | | |
| | | | | | | | | | | 1 | Set to one | | |

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | |
|------------|--------------------------|---|------|------|------|------|------|------|------|------------|---|---|--|
| 34h | Hsync Position Control 1 | Reserved | | | | | | | | | | | |
| | | | | | | 1 | 1 | 1 | 1 | Set to One | | | |
| | | HSE[9:8] HSync End allows the positioning of the HSync output within the video line | | | | | | | | | | HSync ends after HSE[9:0] pixel after falling edge of HSync | |
| | | | | 0 | 0 | | | | | | | | |
| 35h | Hsync Position Control 2 | HSB[9:8] HSync begin allows the positioning of HSync output within the video line | | | | | | | | | HSync starts after HSB[9:0] pixel after the falling edge of HSync | | |
| | | | | | | | | | | | | | |
| | | | 0 | 0 | | | | | | | | | |
| 35h | Hsync Position Control 2 | HSB[7:0] See above, using HSB[9:0] and HSE[9:0] the user can program the position and length of HSync output signal | | | | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | |
| 36h | Hsync Position Control 3 | HSE[7:0] See above. | | | | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | | | |
|------------|----------|--|---|------|------|------|------|------|------|------|---------|-------------|-------------|--|--|
| 37h | Polarity | PCLK Sets the polarity of LLC, LLC2 and QClk | | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | Active High | | | |
| | | | | | | | | | | | | 1 | Active Low | | |
| | | | PFF Sets the polarity of HFF, AEF and AFF | | | | | | | | | | | | |
| | | | | | | | | | | | | 0 | Active High | | |
| | | | | | | | | | | | | 1 | Active Low | | |
| | | PDV Sets the polarity for Data Field | | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | Active High | | | |
| | | | | | | | | | | | 1 | Active Low | | | |
| | | PF sets the field sync polarity | | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | Active High | | | |
| | | | | | | | | | | | 1 | Active Low | | | |
| | | PLLCR sets the LLC Ref Polarity | | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | Active High | | | |
| | | | | | | | | | | | 1 | Active Low | | | |
| | | PVS sets the Vsync Polarity | | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | Active High | | | |
| | | | | | | | | | | | 1 | Active Low | | | |
| | | PHVR sets the Href and Vref sync polarities | | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | Active High | | | |
| | | | | | | | | | | | 1 | Active Low | | | |
| | | PHS sets Hsync Polarity | | | | | | | | | | | | | |
| | | | | | | | | | | | 0 | Active High | | | |
| | | | | | | | | | | | 1 | Active Low | | | |

| Subaddress | Register | Bit Description | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Comment | Note | | |
|------------|------------------|---|------|------|------|------|------|------|------|------|---------------------|---------------------|--------------------------|-------|
| 44h | Resample Control | Reserved Set to Default | | | | | | | | | | | | |
| | | | | | 0 | 0 | 0 | 0 | 0 | 1 | Set to Default | | | |
| | | FSC_INV Colour Subcarrier RTCO Inversion allows the inversion of the GL bit | | | | | | | | | | | | |
| | | | | x | | | | | | | | | NB No Default Value | <v85c |
| | | | 0 | | | | | | | | | | Compatible ADV7190/91/94 | |
| | | | 1 | | | | | | | | | | Compatible with ADV717x | |
| | | Reserved | | | | | | | | | | | | |
| | | | 0 | | | | | | | | Set to zero | | | |
| 45h | Reserved | Reserved Functions | | | | | | | | | | | | |
| | | | | 0 | 0 | 1 | x | x | 0 | 1 | 1 | Default Value | | |
| | | | | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Set to these values | | |
| F1h | Reserved | Reserved Functions | | | | | | | | | | | | |
| | | | | 1 | 1 | 1 | 1 | 0 | 1 | 1 | x | Default values | | |
| | | | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | Set to these values | | | |
| F2h | Reserved | Reserved Functions | | | | | | | | | | | | |
| | | | | 1 | 0 | 0 | 1 | 1 | 1 | 0 | x | Default values | | |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Set to these values | | | |

PRELIMINARY TECHNICAL DATA

ADV7183

POWER ON RESET VALUES

| Register Name | addr (Hex) | Default (Hex) | | Register Name | addr (Hex) | Default (Hex) |
|---------------------------|------------|---------------|--|------------------------------|------------|---------------|
| BASIC BLOCK | | | | ADVANCED BLOCK | | |
| Input Control | 00 | 00 | | Reserved | 1D | xx |
| Video Selection | 01 | 80 | | Reserved | 1E | xx |
| Video Enhancement Control | 02 | 04 | | Reserved | 1F | xx |
| Output Control | 03 | 0C | | Reserved | 20 | xx |
| Extended Output Control | 04 | 0C | | Reserved | 21 | xx |
| General Purpose Output | 05 | 40 | | Reserved | 22 | xx |
| Reserved | 06 | - | | Color Subcarrier Control 1 | 23 | Ex |
| FIFO Control | 07 | 04 | | Color Subcarrier Control 2 | 24 | xx |
| Contrast Control | 08 | 80 | | Color Subcarrier Control 3 | 25 | xx |
| Saturation Control | 09 | 80 | | Color Subcarrier Control 4 | 26 | xx |
| Brightness Control | 0A | 0 | | Pixel Delay Control | 27 | 58 |
| Hue Control | 0B | 0 | | Manual Clock Control 1 | 28 | xx |
| Default Value Y | 0C | 10 | | Manual Clock Control 2 | 29 | xx |
| Default Value C | 0D | 88 | | Manual Clock Control 3 | 2A | xx |
| Temporal Decimation | 0E | 00 | | Auto Clock Control | 2B | A0 |
| Power Management | 0F | 00 | | AGC Mode Control | 2C | CE |
| Status Register | 10 | - | | Chroma Gain Control 1 | 2D | Fx |
| Info Register | 11 | - | | Chroma Gain Control 2 | 2E | xx |
| | | | | Luma Gain Control 1 | 2F | Fx |
| ADVANCED BLOCK | | | | Luma Gain Control 2 | 30 | xx |
| Reserved | 12 | - | | Manual Gain Shadow Control 1 | 31 | 7x |
| Analog Control (internal) | 13 | 45 | | Manual Gain Shadow Control 2 | 32 | xx |
| Analog Clamp Control | 14 | 18 | | Misc Gain Control | 33 | E3 |
| Digital Clamp Control 1 | 15 | 6x | | Hsync Position Control 1 | 34 | 0F |
| Digital Clamp Control 2 | 16 | xx | | Hsync Position Control 2 | 35 | 01 |
| Shaping Filter Control | 17 | 01 | | Hsync Position Control 3 | 36 | 00 |
| Reserved | 18 | - | | Polarity Control | 37 | 00 |
| Comb Filter Control | 19 | 10 | | Reserved | 44 | x1 |
| Reserved | 1A | xx | | Reserved | 45 | xx |
| Reserved | 1B | xx | | Reserved | F1 | Fx |
| Reserved | 1C | xx | | Reserved | F2 | 9x |

ADV7183

APPENDIX 1

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7183 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7183 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VDD and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7183 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7183, the analog output/input traces, and all the digital signal traces leading up to the ADV7183. The ground plane is the board's common ground plane.

Power Planes

The ADV7183 and any associated analog circuitry should have its own power plane, referred to as the analog power plane (VDD). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7183.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7183 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 μF ceramic capacitor decoupling. Each group of VDD pins on the ADV7183 must have at least one 0.1 μF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7183 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7183 should be isolated as much as possible from the analog inputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7183 should be avoided to reduce noise pickup. Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7183 should be located as close as possible to the input connectors to minimize noise pickup and reflections due to impedance mismatch.

The video input signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital Outputs, especially Pixel Data Inputs and clocking signals should never overlay any of the analog signal circuitry and should be kept as far away as possible.

The ADV7183 should have no inputs left floating. Any inputs that are not required should be tied to ground.

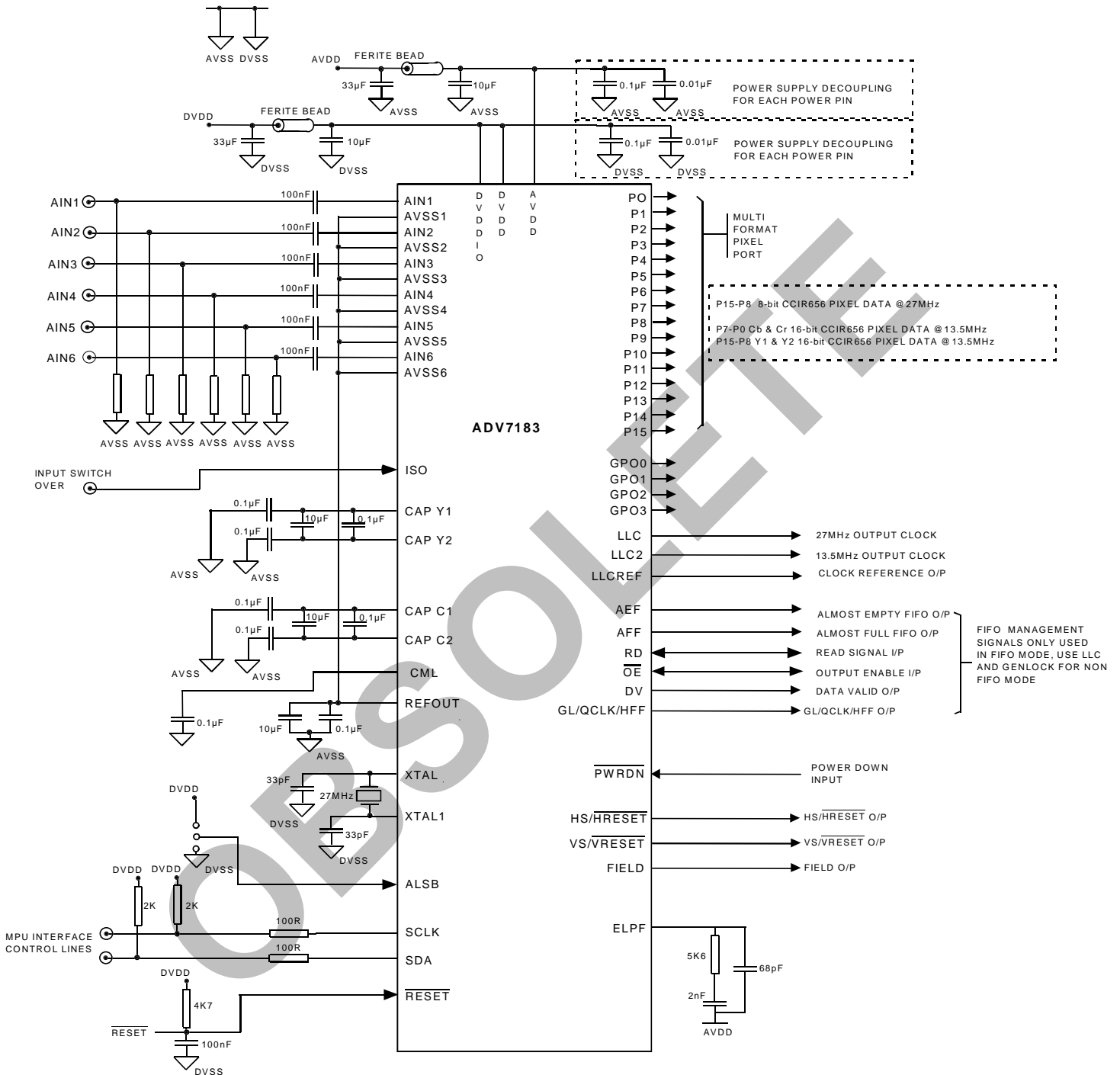


Figure 1. Recommended Circuit Layout

ADV7183

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

