HD63265

Floppy Disk Controller (FDC)

HD63265 is a floppy disk controller (FDC) VLSI circuit which is capable of controlling up to 3.5", 5.25", or 8" floppy disk drives receiving commands from a microprocessor in a 68 or 80-series microcomputer system. Since the FDC has 20 types of high-performance function commands, a floppy disk drive can early be integrated into a system by simple software. In addition, by incorporating a high accuracy VFO circuit and a precompensation circuit, it greatly simplify hardware design. Moreover, since it features a CMOS circuit structure with sleep mode and low power dissipation, it can be used in a wide range of systems from laptop computers to larger systems.

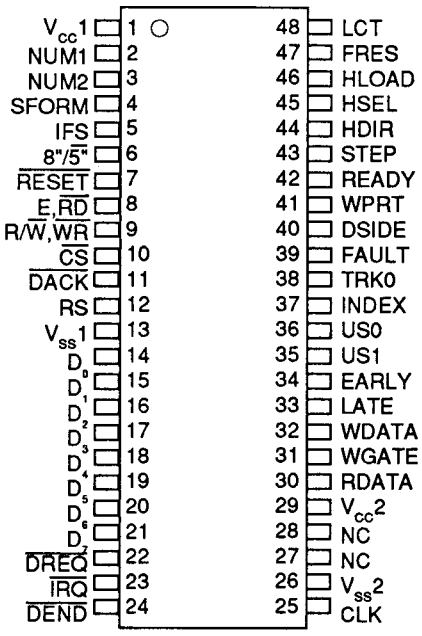
Features

- On-chip high accuracy data separator (adjustment free analog VFO system)
  - No adjustment required
- On-chip write precompensation circuit
  - Delay time programmable in the range from 0 to 750nsec by 62.5nsec increments
  - Delay time independently selectable for inner and outer tracks.
  - Outer to inner switch over programmable in the range of 1 to 255
- Command code compatible with standard FDCs
- Compatible with both 68 and 80-series microprocessors
- Low power dissipation
  - CMOS circuit plus SLEEP command
- Selectable recording
  - FM and MFM
- Serial data transfer rate
  - FM mode : 125, 150, 250 kbps
  - MFM mode : 250, 300, 500 kbps
- Selectable DMA and Non-DMA host data transfers
- Formatting
  - Both IBM and ECMA (ISO) track formats supported
- Error checking
  - 16-bit CRC generator and checker incorporated ($X^{16} + X^{12} + X^5 + 1$)
- Multi-sector and multi-track Read/Write capability
- Data Scan Capability-scans a single sector or an entire cylinder compare byte-for-byte host memory and disk data.
- Multi-drive parallel seek capability
- Stepping rate, head load time, and head unload time programmable
  - Stepping rate programmable by 1 msec increments when using 5" mode
- Drive control range (Max. value)
  - Number of drives : 4
  - Number of heads : 2 heads/drive
  - Number of cylinders : 255 cylinders/drive
  - Number of sectors : 255 sectors/track
- Sector length programmable
  - 128, 256, 512, 1024, 2048, 4096, 8192 bytes/sector

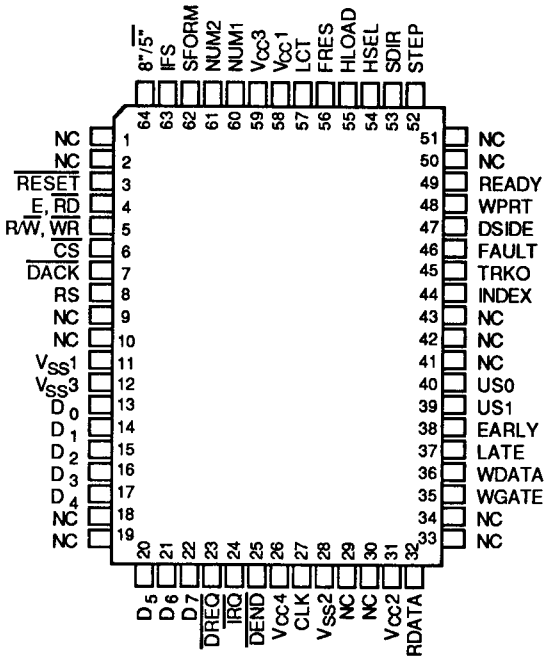
Ordering Information

Type No.	Clock Frequency	Package
HD63265P	16 MHz, 19.2 MHz	48-pin plastic DIP (DP-48)
HD63265FP		64-pin plastic QFP (FP-64)

Pin Arrangement



(DP-48)



(FP-64)

(Top View)

V_{cc}1-V_{cc} 4	+5V
V_{ss}1-V_{ss} 3	Ground
NUM1	Not User Mode 1
NUM2	Not User Mode 2
SFORM	Select Format
IFS	Interface select
8"/5"	8"/5" Mode Select
RESET	Reset
E, RD	Enable, Read
R/W, WR	Read/Write, Write
CS	Chip Select
DACK	DMA Acknowledge
RS	Register Select
D_0	Data Bus 0-7
D_1	
D_2	
D_3	
D_4	
D_5	
D_6	
D_7	
DREQ	DMA Request
IRQ	Interrupt Request
DEND	DMA End

LCT	Low Current
FRES	Fault Reset
HLOAD	Head Load
HSEL	Head Select
HDIR	Head Direction
STEP	Step
READY	Ready
WPRT	Write Protected
DSIDE	Double Sided
FAULT	Fault
TRK0	Track 00
INDEX	Index
US0	Unit Select 0
US1	Unit Select 1
EARLY	Early
LATE	Late
WDATA	Write Data
WGATE	Write Gate
RDATA	Read Data
NC	No Connection
CLK	Clock

Pin Function

Table 1. Pin Functions

Type	Pin No. DP-48	FP-64	Symbol	Pin Name	Input/Output
Power	1	58	$V_{cc}1$	$V_{cc}1$	–
Supply,	13	11	$V_{ss}1$	$V_{ss}1$	–
Clock	29	31	$V_{cc}2$	$V_{cc}2$	–
	26	28	$V_{ss}2$	$V_{ss}2$	–
	25	27	CLK	Clock	Input
		59	$V_{cc}3$	$V_{cc}3$	–
		26	$V_{cc}4$	$V_{cc}4$	–
		12	$V_{ss}3$	$V_{ss}3$	–
MPU	7	3	$\overline{RESET}$	Reset	Input
Interface	8	4	E,$\overline{RD}$	Enable, Read	Input
	9	5	R/$\overline{W}$, $\overline{WR}$	Read/Write, Write	Input
	10	6	$\overline{CS}$	Chip select	Input
	12	8	RS	Register select	Input
	14-21	13-22	D0-D7	Data bus, bits 0-7	Input/Output
	23	24	$\overline{IRQ}$	Interrupt request	Output
DMA	11	7	$\overline{DACK}$	DMA acknowledge	Input
Control	22	23	$\overline{DREQ}$	DMA request	Output
	24	25	$\overline{DEND}$	DMA end	Input
FDD	30	32	RDATA	Read data	Input
Interface	31	35	WGATE	Write gate	Output
	32	36	WDATA	Write data	Output
	33	37	LATE	Late	Output
	34	38	EARLY	Early	Output
	35	39	US1	Unit select 1	Output
	36	40	US0	Unit select 0	Output
	37	44	INDEX	Index	Input
	38	45	TRK0	Track 0	Input
	39	46	FAULT	Fault	Input
	40	47	DSIDE	Double sided	Input
	41	48	WPRT	Write protect	Input
	42	49	READY	Ready	Input
	43	52	STEP	Step	Output
	44	53	HDIR	Head direction	Output
	45	54	HSEL	Head select	Output
	46	55	HLOAD	Head load	Output
	47	56	FRES	Fault reset	Output
	48	57	LCT	Low current	Output

SIGNAL DESCRIPTION

Power Supply, Clock

$V_{cc}1$-$V_{cc}4$, $V_{ss}1$-$V_{ss}3$ (Power Supply): $V_{cc}1$, $V_{cc}3$, $V_{cc}4$, $V_{ss}1$ and $V_{ss}3$ are the power and ground for the logic area (+5 V ±5 %). $V_{ss}1$ and $V_{ss}3$ are connected to ground. $V_{cc}2$ and $V_{ss}2$ are the power and ground for the internal VFO (+5 V ±5 %). $V_{ss}2$ is connected to ground.
CLK (Clock): CLK is the 16 MHz clock input (19.2 MHz for 150 and 300 kbps).

MPU Interface

$\overline{\text{RESET}}$ (Reset): $\overline{\text{RESET}}$ sets the $\overline{\text{DREQ}}$ and $\overline{\text{IRQ}}$ signals high and sets all the other output signals low. It forces D0-D7 into the input state.
E, $\overline{\text{RD}}$ (Enable, Read), R/$\overline{\text{W}}$, $\overline{\text{WR}}$ (Read/Write, Write): The functions of E, $\overline{\text{RD}}$ and R/$\overline{\text{W}}$, $\overline{\text{WR}}$ depend on the IFS input (table 2).

$\overline{\text{CS}}$ (Chip Select): $\overline{\text{CS}}$ selects the chip and enables the read/write of the internal registers.

Table 1. Pin Functions (cont)

Type	Pin No. DP-48	Pin No. FP-64	Symbol	Pin Name	Input/Output
FDC	4	62	SFORM	Select format	Input
Function	5	63	IFS	Interface select	Input
Switching	6	64	8"/$\overline{5"}$	8"/5" mode select	Input
Others	2	60	NUM1	Not-user mode 1	Input
	3	61	NUM2	Not-user mode 2	Input
	27	1, 2	NC	No Connection	
	28	9, 10			
		18, 19			
		29, 30			
		33, 34			
		41-43			
		50, 51			

Table 2. E, $\overline{\text{RD}}$ and R/$\overline{\text{W}}$, $\overline{\text{WR}}$ Function

Signal	IFS		Function
E, $\overline{\text{RD}}$	0	$\overline{\text{RD}}$	Accepts the 80-series Read signal
	1	E	Accepts the 68-series Enable signal
R/$\overline{\text{W}}$, $\overline{\text{WR}}$	0	$\overline{\text{WR}}$	Accepts the 80-series Write signal
	1	R/$\overline{\text{W}}$	Accepts the 68-series Read/Write signal

RS (Register Select): RS selects the internal register on which an MPU read/write is performed (table 3).

D0-D7 (Data Bus): D0-D7 form the bidirectional 8-bit data bus, enabled by read/write.
$\overline{IRQ}$ (Interrupt Request): $\overline{IRQ}$ requests data transfer with the MPU in Non-DMA mode. It informs the MPU that a READ, WRITE, or SEEK command has been completed. When IFS is high, $\overline{IRQ}$ becomes an open drain output.

DMA Control

$\overline{DACK}$ (DMA Acknowledge): $\overline{DACK}$ receives the DMA acknowledge signal from the DMAC during a DMA transfer.
$\overline{DREQ}$ (DMA Request): $\overline{DREQ}$ requests the DMAC to perform a DMA transfer.
$\overline{DEND}$ (DMA End): $\overline{DEND}$ receives the DMA end signal from the DMAC and terminates the DMA transfer .

FDD Interface

RDATA (Read Data): RDATA inputs the read data signal from the FDD.
WGATE (Write Gate): WGATE outputs the write control signal to the FDD.
WDATA (Write Data): WDATA outputs the write data signal to the FDD.
LATE, EARLY (Late, Early): The LATE and EARLY output the write precompensation control signals used to advance or delay the write data before sending it to the FDD.
US1, US0 (Unit Select 1, 0): The US1 and US0 unit select outputs select the FDD.
A maximum of 4 FDDs can be selected by decoding US1 and US0 (table 4).

Table 3. RS Function

RS	Register Selected	Conditions
0	Status Register	Read
	Abort Register	Write
1	Data Register	Read/Write

Table 4. FDD Selection

US1	US0	FDD
0	0	FDD 0
0	1	FDD 1
1	0	FDD 2
1	1	FDD 3

INDEX (Index): INDEX inputs the index signal from the FDD.
TRK0 (Track 0): TRK0 inputs the track 00 signal from the FDD.
FAULT (Fault): FAULT inputs the fault signal from the FDD.
DSIDE (Double Sides): DSIDE inputs the double sided signal from the FDD.
WPRT (Write Protect): WPRT inputs the write protected signal from the FDD.
READY (Ready): READY inputs the ready signal from the FDD.
STEP (Step): The STEP output moves the FDD head.
HDIR (Head Direction): The HDIR output controls the direction of FDD head movement. HDIR = 0 indicates outward direction (towards track 0), while HDIR = 1 indicates inward direction.
HSEL (Head Select): The HSEL output selects the FDD head.
HSEL = 0 selects head 0, while HSEL = 1 selects head 1.
HLOAD (Head Load): The HLOAD output directs the FDD to load the heads onto the disk.
FRES (Fault Reset): The FRES output resets the FDD fault status FF.
LCT (Low Current): The LCT output reduces the FDD write current for inner tracks. After the SPECIFY 1 command is issued, the most outer position of the low current tracks is specified as track 43. For tracks ≧ this track, LCT = 1. A different most outer track position can be specified by the SPECIFY 2 command.

FDC Function Switching

SFORM (Select Format): The SFORM input selects the track format for formatting.
SFORM high selects IBM format, SFORM low selects ECMA (ISO) format. SFORM is needed for formatting only. The FDC can read or write in either format regardless of the SFORM input level.
IFS (Interface Select): The IFS input specifies the host interface. IFS defines the functions of pins 8 and 9 (E, $\overline{RD}$ and R/$\overline{W}$, $\overline{WR}$) as shown in table 2.
IFS = 0 for 80-series interface. IFS = 1 for 68-series interface.
8"/$\overline{5}$" (8"/5" Mode Select): The 8"/$\overline{5}$" input selects the FDD type. It specifies the drive data rate depending on the modulation method selected (table 5).

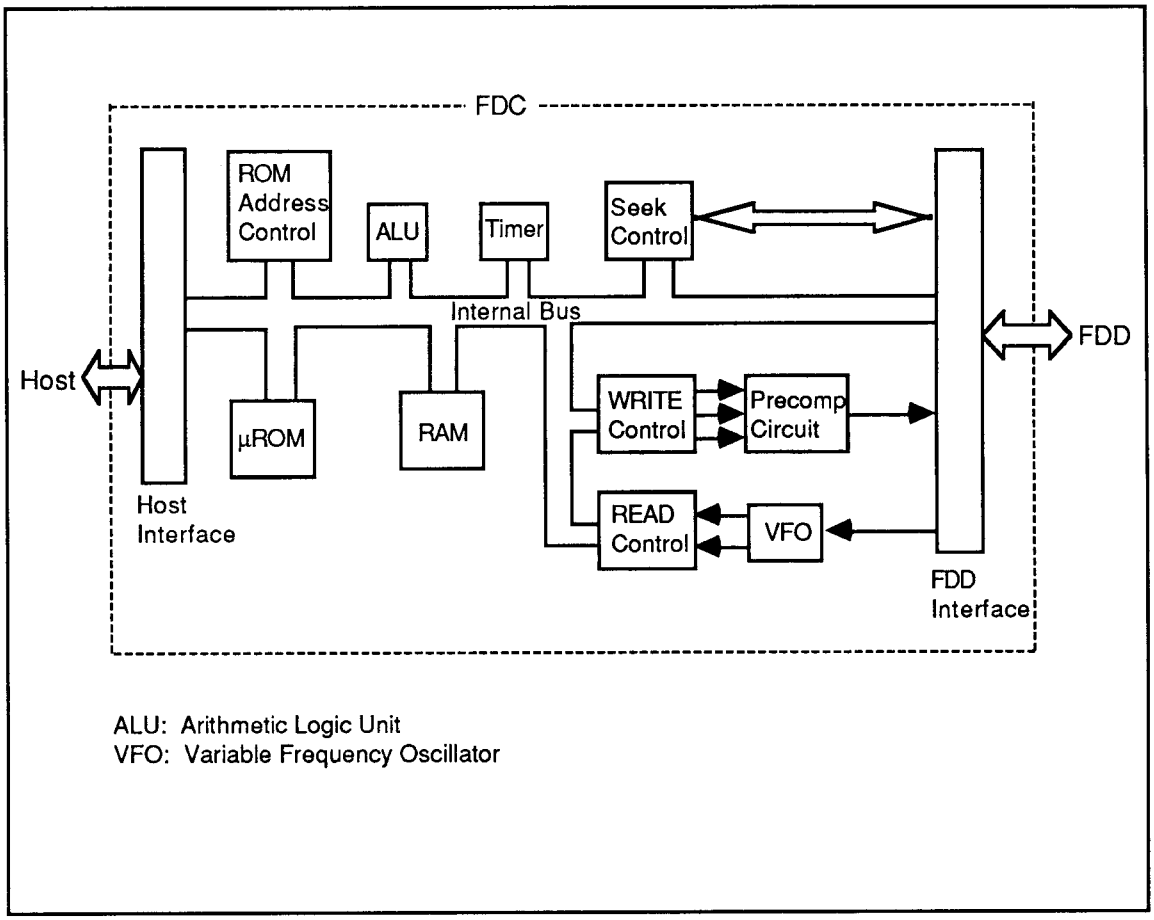
NUM1, NUM2 (Not-User Mode 1, 2): NUM1 and NUM2 are not for user applications. They must be tied to low.
NC (No Connection): NC pins require no connection.

Table 5. Drive Data Rate

8"/$\overline{5}$"	FM	MFM
0	125 kbits/s	250 kbits/s
	150 kbits/s (Note)	300 kbits/s (Note)
1	250 kbits/s	500 kbits/s

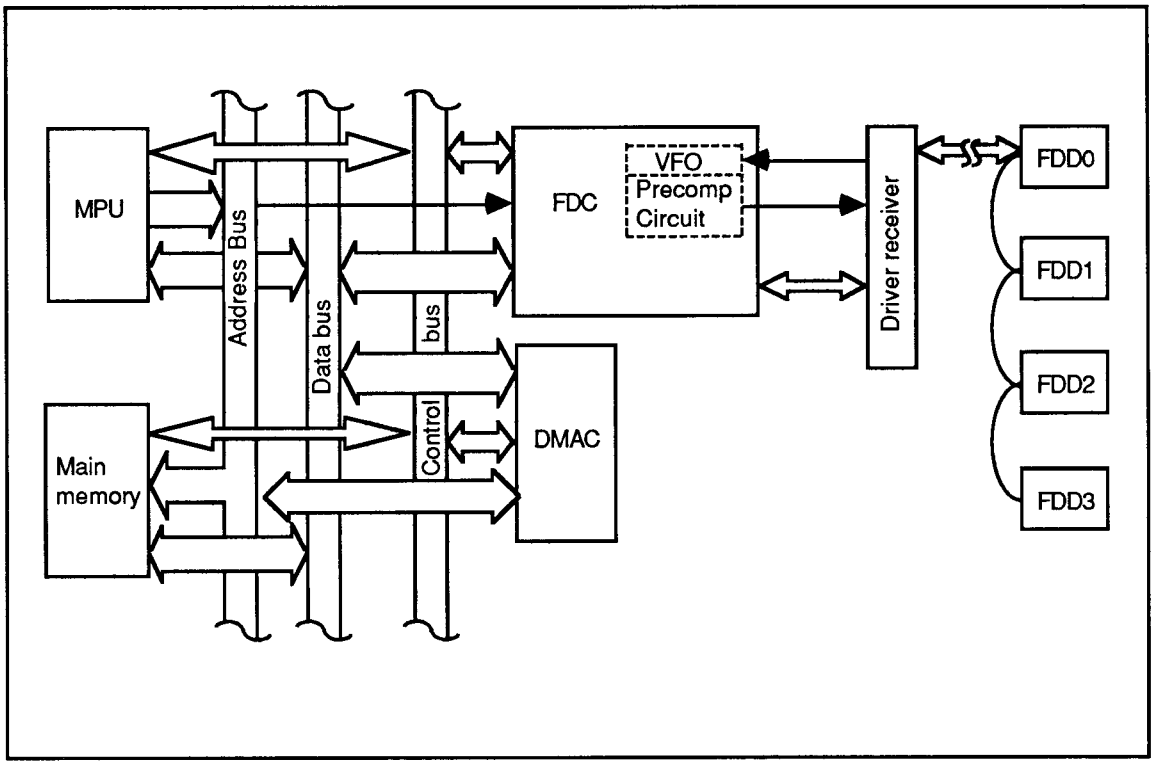
Note: When CLK = 19.2 MHz

FDC Block Diagram



ALU: Arithmetic Logic Unit
VFO: Variable Frequency Oscillator

System Block Diagram



Host Interface

This FDC can easily be interfaced to the 68- as well as the 80-series 8-bit devices. IFS (pin 5) is used for selecting between 68- and 80-series interfaces.

68 Series Interface (IFS = 1)

QFP	DIP
Pin 4	Pin 8: E
Pin 5	Pin 9: R/$\overline{W}$
Pin 24	Pin 23 ($\overline{IRQ}$): Open-drain output

For the 68-series interface only, the data flow direction controlled by R/$\overline{W}$ input (pin 9) is reversed between DMA and Non-DMA transfers (table 6). Here, DMA FDC access is by $\overline{DACK}$ signal (pin 11), and Non-DMA FDC access is by $\overline{CS}$ signal (pin 10). When the FDC is accessed by the $\overline{DACK}$ signal, the RS signal (pin 12) is ignored, and DTR (data register) is always accessed.

80 Series Interface (IFS = 0)

QFP	DIP
Pin 4	Pin 8: $\overline{RD}$
Pin 5	Pin 9: $\overline{WR}$
Pin 24	Pin 23 $\overline{IRQ}$: CMOS output the same as the other output pins

Table 7 shows the data transfer signals.

Table 6. Data Transfer 68-Series

Mode	$\overline{DACK}$	$\overline{CS}$	R/$\overline{W}$	E	Data Transfer Direction
DMA	0	1	0	1	FDC ----------→ Main memory
	0	1	1	1	Main memory ----------→ FDC
Non-	1	0	0	1	Host ----------→ FDC
DMA	1	0	1	1	FDC ----------→ Host

Table 7. Data Transfer 80-Series

Mode	$\overline{DACK}$	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Data Transfer Direction
DMA	0	1	1	0	Main memory ----------→ FDC
	0	1	0	1	FDC ----------→ Main memory
Non-	1	0	1	0	Host ----------→ FDC
DMA	1	0	0	1	FDC ----------→ Host

Internal Registers

The host can access three registers: Data register (DTR), status register (STR), and abort register (ATR). These registers are selected by the RS signal and read/write operations (table 8).

Status Register

The status register (figure 1) is a read-only register which indicates the FDC status and also whether each FDD selected by signals US0 and US1 is currently performing a seek or recalibrate operation.

Bit 7 TXR (Transfer Ready): Bit 7 is set to 1 when DTR is in the read/write enabled state and it is cleared to 0 when data starts to be read or written by the host.

Bit 6 DIR (Data Direction): Bit 6 indicates the data transfer direction between the host and the FDC.

DIR = 0: The host writes data to the FDC.

DIR = 1: The host reads data from the FDC.

Bit 5 NDM (Non-DMA Mode): Bit 5 set to 1 indicates that the FDC transfers data in Non-DMA mode. But even when Non-DMA mode is selected by commands SPECIFY 1 and SPECIFY 2, this bit is cleared to 0, except during the execution of read/write related commands.

Bit 4 BSY (Controller Busy): Bit 4 is set to 1 when the FDC cannot accept the next command because it is decoding or executing a command. A new command, except for the ABORT command, must be issued only when BSY = 0.

Table 8. Register Selection

RS	Read/Write	Selected Register
0	Read	Status Register (STR)
	Write	Abort Register (ATR)
1	Read/Write	Data Register (DTR)

STR

Bit	7	6	5	4	3	2	1	0
Symbols	TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S

Figure 1. Status Register

Bit 0-3 D0S-D3S (Drivers 0-3 Seek): Bits 0-3 are set to 1 when the FDD selected by signals US0 and US1 is executing a SEEK or RECALIBRATE command. Bit 0 corresponds to FDD0 and bit 3 to FDD3. Bits D0S to D3S are 1's when the seek or recalibrate command is issued. Even if all of the step pulses are output, these bits stay as 1's until the SEEK and RECALIBRATE end status information is accepted by the CHECK INTERRUPT STATUS command.

Abort Register

Abort register is a write-only register used exclusively for the ABORT command. ABORT command is issued by writing HEX FF into this register. This command is valid when the $\overline{\text{RESET}}$ signal is inactive regardless of the state of the FDC. Values other than HEX FF written into this register are ignored by the FDC.

Data Register

Data register is a read/write register (actually a stack of registers with only one connected to the data bus at a time) which is used to receive commands and command parameters, transfer data, and read out result parameters.

COMMAND DESCRIPTION

Command Description List

This FDC supports 20 commands listed in Table 9.

READ LONG and WRITE LONG commands become valid only after command SPECIFY 2 has been issued.

Table 9. FDC Commands

Commands	Functions
READ DATA	Reads data from any specified sector (s) except the deleted sector (s)
READ DELETED DATA	Reads data from any specified sector (s) containing a data address mark of F8
READ ERRONEOUS DATA	Reads data from the first sector immediately after the index to the end of track regardless whether there are errors or not
READ ID	Reads the first errorfree ID encountered on a track
WRITE DATA	Writes data to any specified sector (s) using a data address mark of FB
WRITE DELETED DATA	Writes data to any specified sector (s) using a data address mark of F8
WRITE FORMAT	Formats the track where the head is currently positioned
SEEK	Moves the selected FDD's head to a specified track
RECALIBRATE	Moves the selected FDD's head to track 0
COMPARE EQUAL COMPARE LOW OR EQUAL COMPARE HIGH OR EQUAL	Compares the data read from the selected FDD with the data sent from the host according to the chosen command
CHECK DEVICE STATUS	Reads the selected FDD's status
CHECK INTERRUPT STATUS	Reads the interrupt causes
SPECIFY 1 SPECIFY 2*	Specifies the FDC operating mode and sets up the various timers in the FDC
SLEEP *	Sets the FDC to the low power dissipation mode
ABORT *	Software reset command
READ LONG *	Reads the CRC bytes as well as the data from a sector to the host
WRITE LONG*	Writes the CRC bytes as well as the data to a sector from the host

Note: Commands marked with * are newly added commands which are unique to this FDC. Rest of the commands are identical to other standard FDC commands.

Command Code List

Table 10 lists the FDC commands and the corresponding command codes.

Table 10. Command Codes

Commands	Command Codes							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
READ DATA	MT	MM	SD	0	0	1	1	0
READ DELETED DATA	MT	MM	SD	0	1	1	0	0
READ ERRONEOUS DATA	0	MM	0	0	0	0	1	0
READ ID	0	MM	0	0	1	0	1	0
WRITE DATA	MT	MM	0	0	0	1	0	1
WRITE DELETED DATA	MT	MM	0	0	1	0	0	1
WRITE FORMAT	0	MM	0	0	1	1	0	1
SEEK	0	0	0	0	1	1	1	1
RECALIBRATE	0	0	0	0	0	1	1	1
COMPARE EQUAL	MT	MM	SD	1	0	0	0	1
COMPARE LOW OR EQUAL	MT	MM	SD	1	1	0	0	1
COMPARE HIGH OR EQUAL	MT	MM	SD	1	1	1	0	1
CHECK DEVICE STATUS	0	0	0	0	0	1	0	0
CHECK INTERRUPT STATUS	0	0	0	0	1	0	0	0
SPECIFY 1	0	0	0	0	0	0	1	1
SPECIFY 2	0	A	H	0	1	0	1	1
SLEEP	0	0	0	0	1	1	1	0
ABORT	1	1	1	1	1	1	1	1
READ LONG	MT	MM	SD	1	0	0	1	0
WRITE LONG	MT	MM	0	1	0	1	1	0

MT: Multi Track
MT = 1 specifies read/write of multi tracks.

MM: MFM Mode
MM = 0 selects FM mode
MM = 1 selects MFM mode

SD: Skip DDAM
Sector with DDAM (deleted data address mark) is read or skipped depending on whether SD = 0 or 1. When SD = 1, sector with DDAM is skipped.

A: Auto precompensation
When A = 1, auto write precompensation is performed.

H: High speed seek
H = 1 selects high speed seek mode.

Command Functions

READ DATA

The READ DATA command (figure 2) transfers data to the host from the disk. The command parameters specify the location of the data on the disk. Multisector read is automatically performed. Multitrack read can also be performed if specified.

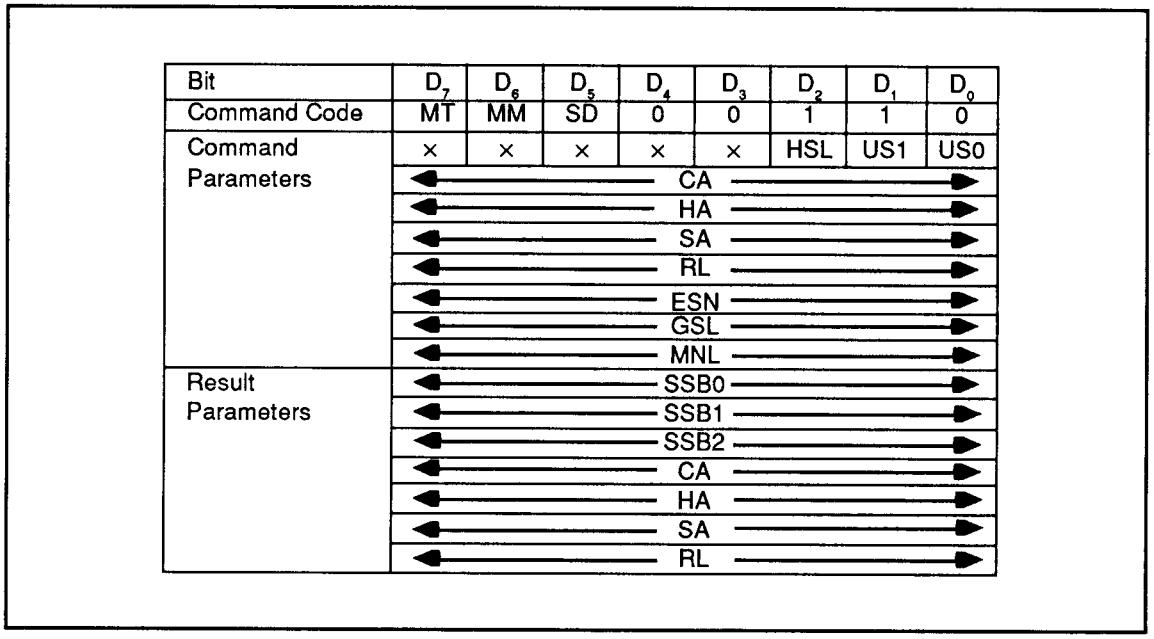


Figure 2. READ DATA Command

READ DELETED DATA

The READ DELETED DATA command (figure 3) is identical to the READ DATA command except that HEX FB and HEX F8 are regarded as the deleted data address mark and the data address mark, respectively.

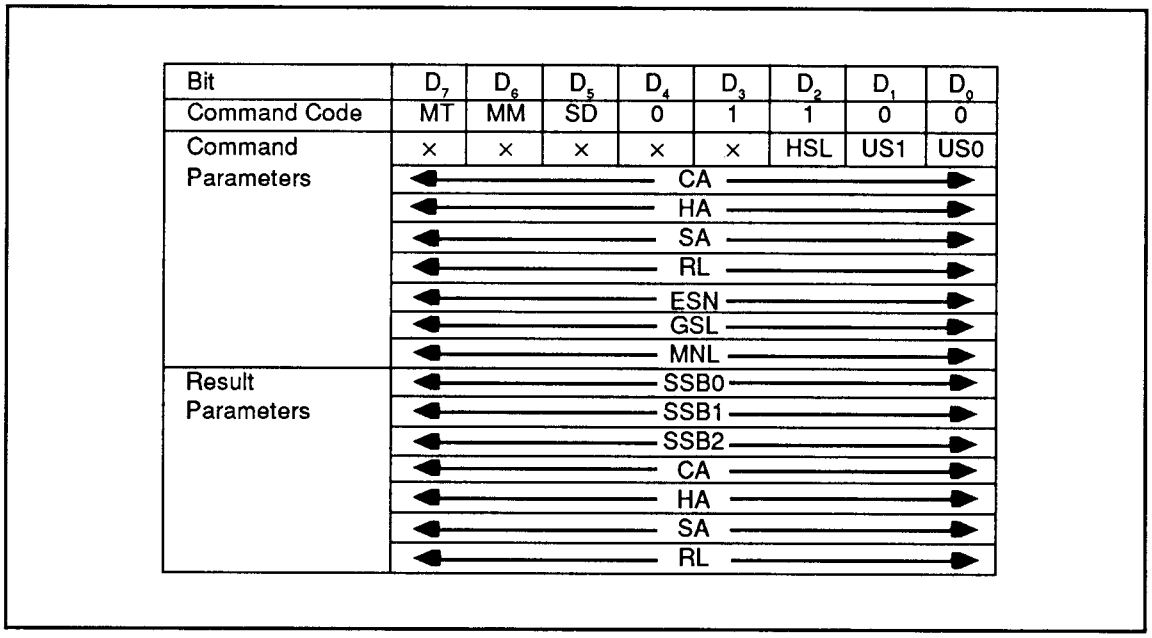


Figure 3. READ DELETED DATA Command

READ ERRONEOUS DATA

The READ ERRONEOUS DATA command (figure 4) reads the data starting from the first sector detected after the index to the end of the track regardless whether there are errors present or not. Sectors are read in the order, they occur after index pulse detection, independent of CA, HA, SA and RL. The SA byte of the command parameters is ignored and HEX 01 is specified in the FDC at the start of the command execution. Multisector read is performed by incrementing SA by 1. Multitrack read cannot be specified.

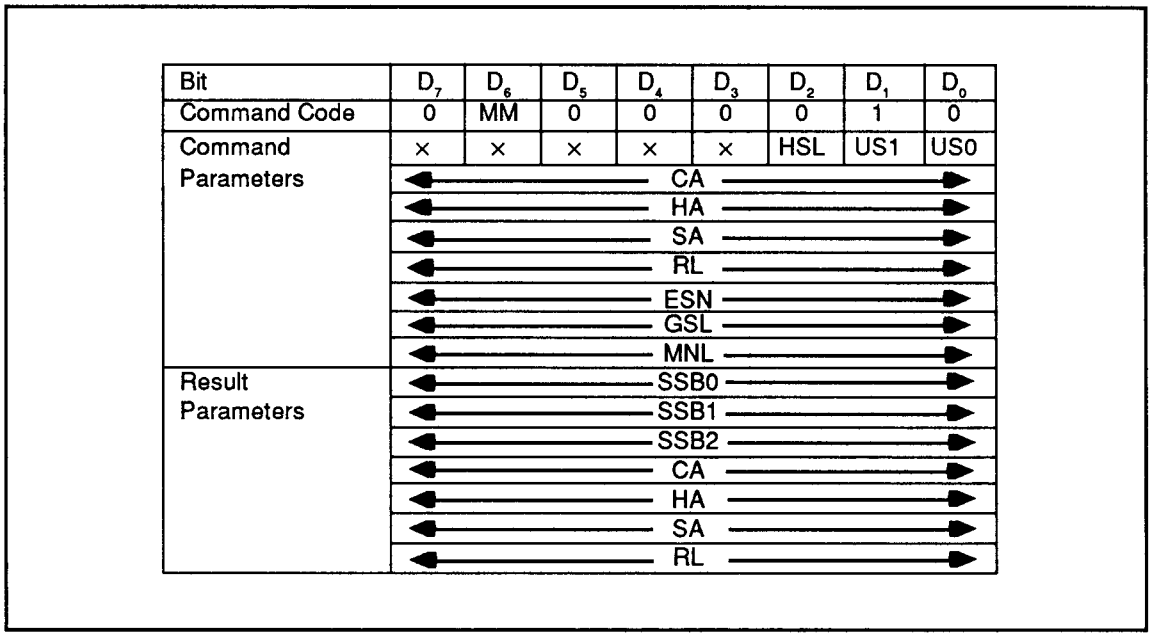


Figure 4. READ ERRONEOUS DATA Command

READ ID

The READ ID command (figure 5) transmits the first error-free ID detected after the command execution has started to the host as result parameters CA, HA, SA, and RL.

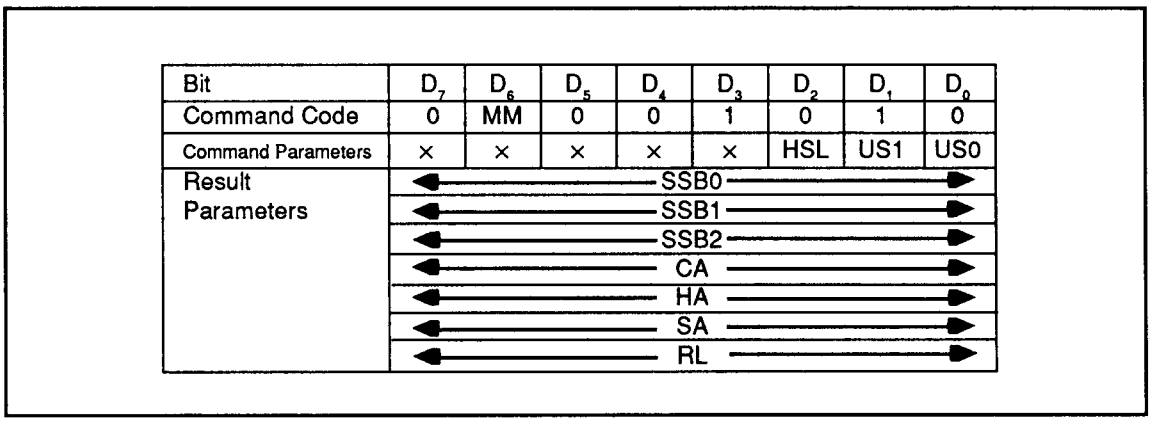


Figure 5. READ ID Command

WRITE DATA

The WRITE DATA command (figure 6) requests the data transfer from the host and writes it to a sector on a track specified by the command parameters at the current head position. Multisector write is automatically performed. Multitrack write can also be performed if specified.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	0	0	0	1	0	1
Command Parameters	×	×	×	×	×	HSL	US1	US0
	← CA →							
	← HA →							
	← SA →							
	← RL →							
	← ESN →							
	← GSL →							
	← MNL →							
Result Parameters	← SSB0 →							
	← SSB1 →							
	← SSB2 →							
	← CA →							
	← HA →							
	← SA →							
	← RL →							

Figure 6. WRITE DATA Command

WRITE DELETED DATA

The WRITE DELETED DATA command (figure 7) is identical to the WRITE DATA command except that the following 1-byte and 4-byte deleted data address marks are written in the FM and MFM mode, respectively.

In FM mode
Data: HEX F8
Clock: HEX C7

In MFM mode
Data: HEX A1, HEX A1, HEX A1, HEX F8
Clock: HEX 0A, HEX 0A, HEX 0A, HEX 03

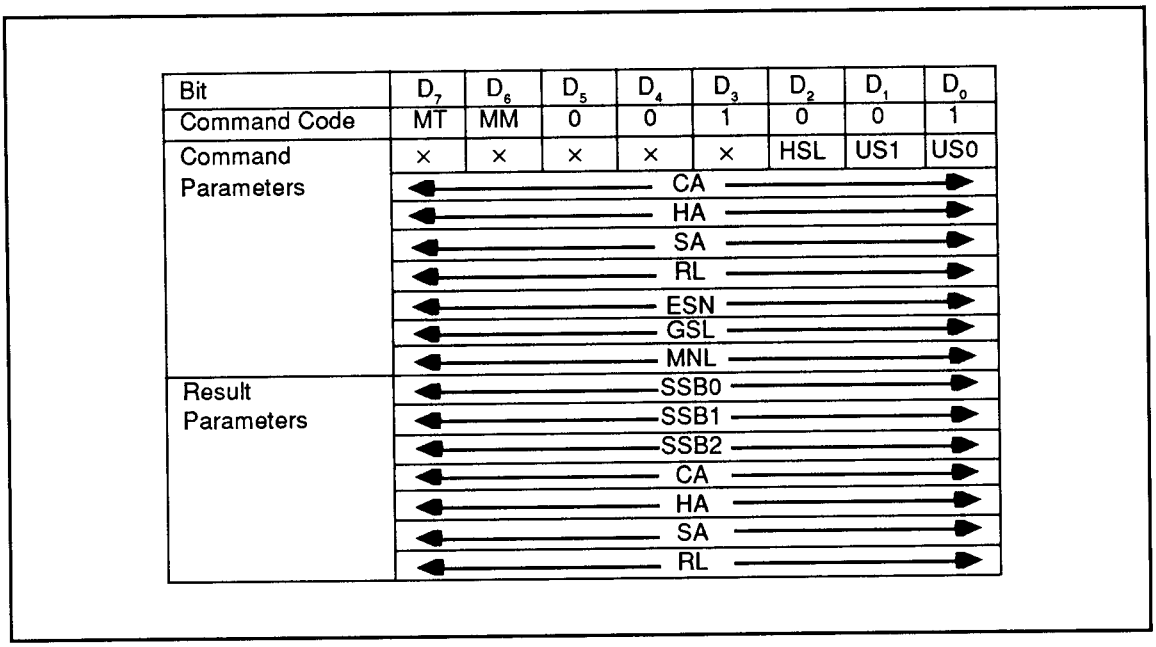


Figure 7. WRITE DELETED DATA Command

WRITE FORMAT

The WRITE FORMAT command (figure 8) formats a single track where the head is currently positioned depending on the SFORM input (pin 4).

SFORM = 1 : IBM format

SFORM = 0 : ECMA (ISO) format

When an index pulse is detected, the write gate signal is activated to begin the formatting operation.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	MM	0	0	1	1	0	1
Command Parameters	×	×	×	×	×	HSL	US1	US0
	← RL →							
	← SCNT →							
	← GP3L →							
	← DUD →							
	← SSB0 →							
	← SSB1 →							
	← SSB2 →							
Result Parameters	← CA →							
	← HA →							
	← SA →							
	← RL →							

Figure 8. WRITE FORMAT Command

SEEK

In the SEEK operation (figure 9), a drive's head is moved onto the track specified by the command parameter's NCN (New Cylinder Number) byte. The stepping rate (step pulse interval) is specified by the SPECIFY command.

RECALIBRATE

The RECALIBRATE command (figure 10) moves a drive's head to track 0. Head movement speed is the stepping rate (step pulse interval) specified by the SPECIFY command.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	1	1	1	1
Command Parameters	×	×	×	×	×	×	US1	US0
	← NCN →							
Result Parameters	—							

Figure 9. SEEK Command

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	0	1	1	1
Command Parameters	×	×	×	×	×	×	US1	US0
Result Parameters	—							

Figure 10. RECALIBRATE Command

COMPARE EQUAL

The COMPARE EQUAL command (figure 11) searches for a sector on disk such that data from the drive is equal to data from the host.

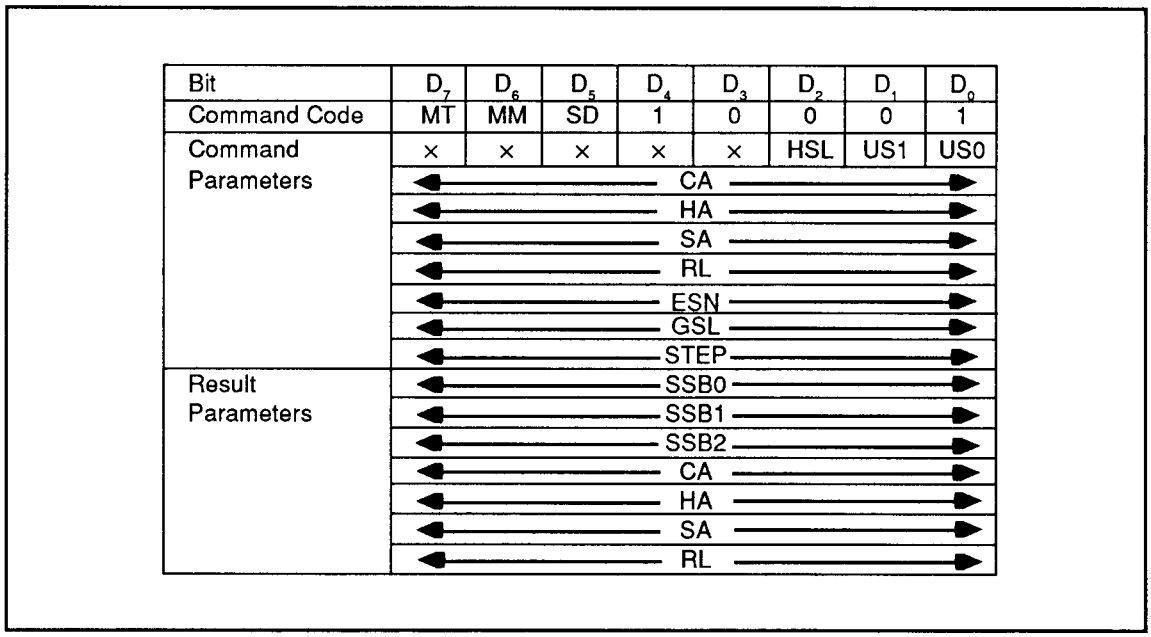


Figure 11. COMPARE EQUAL Command

COMPARE LOW OR EQUAL

The COMPARE LOW OR EQUAL command (figure 12) searches for a sector on disk such that data from the drive is less than or equal to data from the host.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	SD	1	1	0	0	1
Command Parameters	×	×	×	×	×	HSL	US1	US0
	← CA →							
	← HA →							
	← SA →							
	← RL →							
	← ESN →							
	← GSL →							
	← STEP →							
Result Parameters	← SSB0 →							
	← SSB1 →							
	← SSB2 →							
	← CA →							
	← HA →							
	← SA →							
	← RL →							

Figure 12. COMPARE LOW OR EQUAL Command

COMPARE HIGH OR EQUAL

The COMPARE HIGH OR EQUAL command (figure 13) searchs for a sector on disk such that data from the drive is greater than or equal to data from the host.

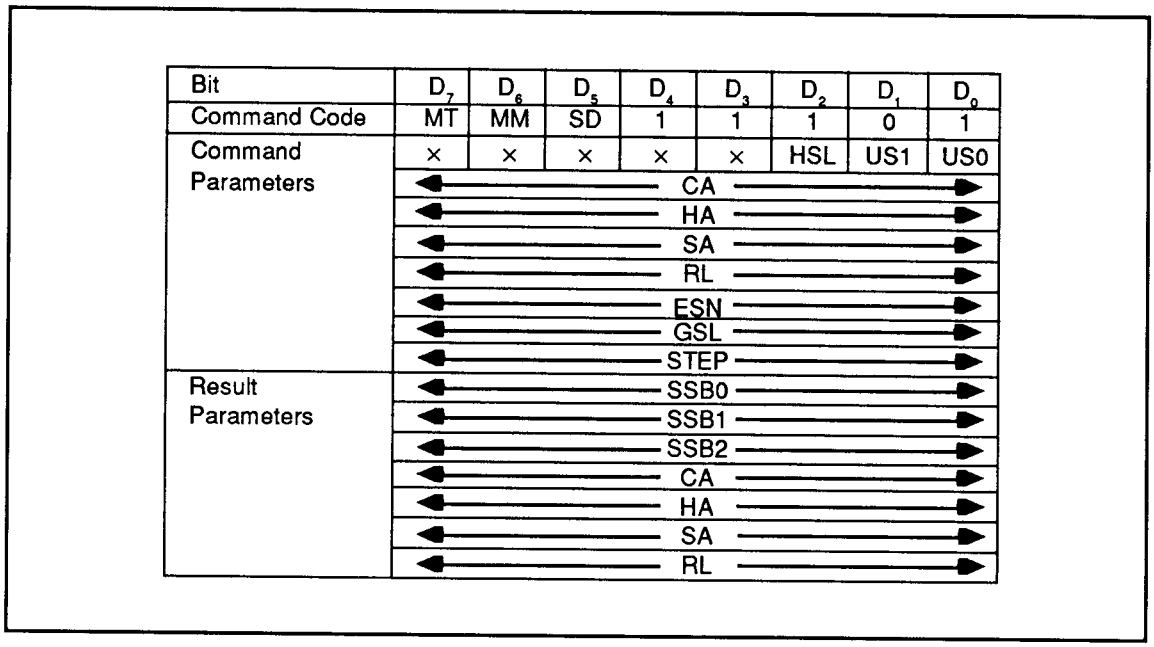


Figure 13. COMPARE HIGH OR EQUAL Command

CHECK DEVICE STATUS

The CHECK DEVICE STATUS command (figure 14) reads the status of a drive and sets it up in SSB3 transfer to the host. HSL, US1 and US0 bits of SSB3 are updated to contain exactly the same values as the respective command parameter values. This command can also be issued for a drive which is performing a seek or recalibrate operation. If the command is issued for a different drive than the one currently selected, then its heads must be immediately unloaded (HLOAD = 0).

CHECK INTERRUPT STATUS

The CHECK INTERRUPT STATUS command (figure 15) transfers to the host the causes of the interrupt request made by the FDC, when the status register value is HEX 8X (command waiting state).

There are two types of interrupt causes:

- SEEK or RECALIBRATE command has ended normally or abnormally
- Ready signal has changed state since last polling

When the FDC does not have the Seek End (SED) or Ready Inversion (CDS) status, issuance of the CHECK INTERRUPT STATUS command is treated as an INVALID command.

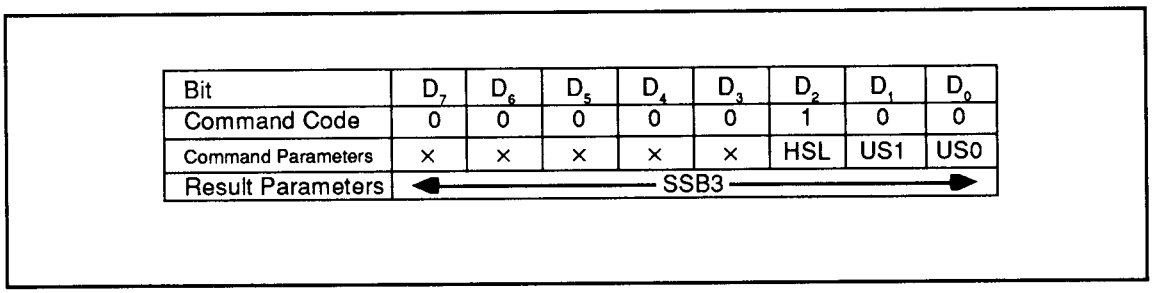


Figure 14. CHECK DEVICE STATUS Command

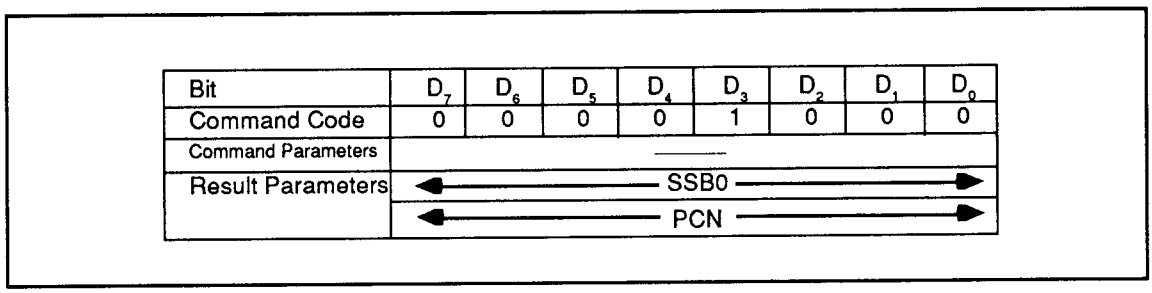


Figure 15. CHECK INTERRUPT STATUS Command

SPECIFY 1

The SPECIFY 1 command (figure 16) specifies the stepping rate, head unload time, head load time, and Non-DMA mode (or DMA mode).

If a SPECIFY 1 command is issued after a SPECIFY 2 command, the auto-precompensation and high-speed seek modes specified under SPECIFY 2 command are reset, and the track position activating the LCT signal is specified as track 43.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	0	0	1	1
Command Parameters	STR				HDUT			
	HDLT							NDM
Result Parameters	—							

Figure 16. SPECIFY 1 Command

SPECIFY 2

The SPECIFY 2 command (figure 17) specifies the stepping rate, head unload time, head load time, Non-DMA mode, low write current starting track position, auto-precompensation mode, high-speed seek mode, precompensation delays for auto precompensation, and precompensation delay change track number. Command parameter 1 is required whenever this command is issued. Command parameter 2 is needed only when command code bit A = 1. When A = 0, the FDC cannot accept this parameter.

Auto-Precompensation Mode: When A = 1, the auto-precompensation mode is selected. In this mode, the write data which has been adjusted for the PC1 or PC0 specified precompensation delays is output (only in MFM mode), with the EARLY (pin 34) and LATE (pin 33) outputs fixed at low level. When A = 0, auto-precompensation is not performed, but the EARLY and LATE precompensation control signals are output (only in MFM mode).

High-Speed Seek Mode: When H = 1, the high-speed seek mode is selected. This mode allows the stepping rate to be set to a value ranging from 1 to 16 ms in 1 ms increments in the 5" mode (8"/$\overline{5}$" = low). In the 8" mode (8"/$\overline{5}$" = high), H has no meaning.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	A	H	0	1	0	1	1
Command Parameter 1	STR				HDUT			
	HDLT							NDM
	LCTK							
Command Parameter 2	PC1				PC0			
	PCDCT							
Result Parameter	———							

Figure 17. SPECIFY 2

SLEEP

The SLEEP command (figure 18) allows the FDC to dissipate lower power.
When the FDC receives this command,

1. HLOAD (Head Load) is set low,
2. US0 and US1 are set high,

and the SLEEP mode is entered. In this mode, no drive polling is performed.
In the SLEEP mode, the FDC's status register is set to HEX 80 indicating that the FDC is in the command waiting state. When the FDC receives a command in the SLEEP mode, it automatically releases the SLEEP mode and executes the command.
Power dissipation can be reduced by halting the FDC clock after saving the status conditions gathered immediately before the SLEEP mode is entered.

ABORT

The ABORT command (figure 19) resets the FDC by software.
Note: This command is issued by writing it into the abort register (ATR), and holding RS = 0.
The abort register can be accessed at any time, irrespective of the FDC state, except when the $\overline{\text{RESET}}$ input signal is active.
When the FDC receives the ABORT command:

1. FRES, HLOAD, STEP, EARLY, LATE, WDATA, and WGATE signals are set to low level.
2. $\overline{\text{DREQ}}$ and $\overline{\text{IRQ}}$ signals are set to high level
3. Status register (STR) is set to HEX 80 and the drive polling starts.

This command cannot reset FDC's cylinder numbers or the values specified by the SPECIFY command. However, when the ABORT command is issued during the execution of a SEEK or RECALIBRATE command, the cylinder number is the value set by the SEEK or RECALIBRATE command, although the remaining step pulses are no longer generated. Thus, in such a case, a RECALIBRATE command must be issued before the next command is issued.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	1	1	1	0
Command Parameters								
Result Parameters								

Figure 18. SLEEP Command

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	1	1	1	1	1	1	1	1
Command Parameters								
Result Parameters								

Figure 19. ABORT Command

READ LONG

The READ LONG command (figure 20) transfers the 2-byte CRC information as well as the data read from a sector to the host.

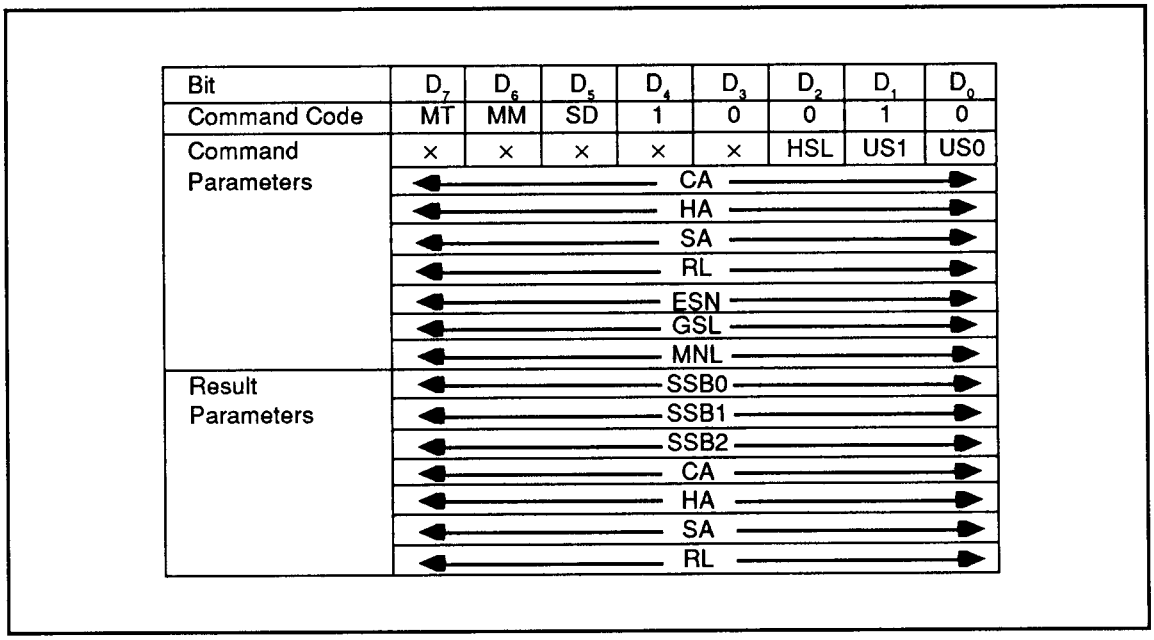


Figure 20. READ LONG Command

WRITE LONG

The WRITE LONG command (figure 21) writes to a disk the 2-byte CRC information as well as the data sent from the host.

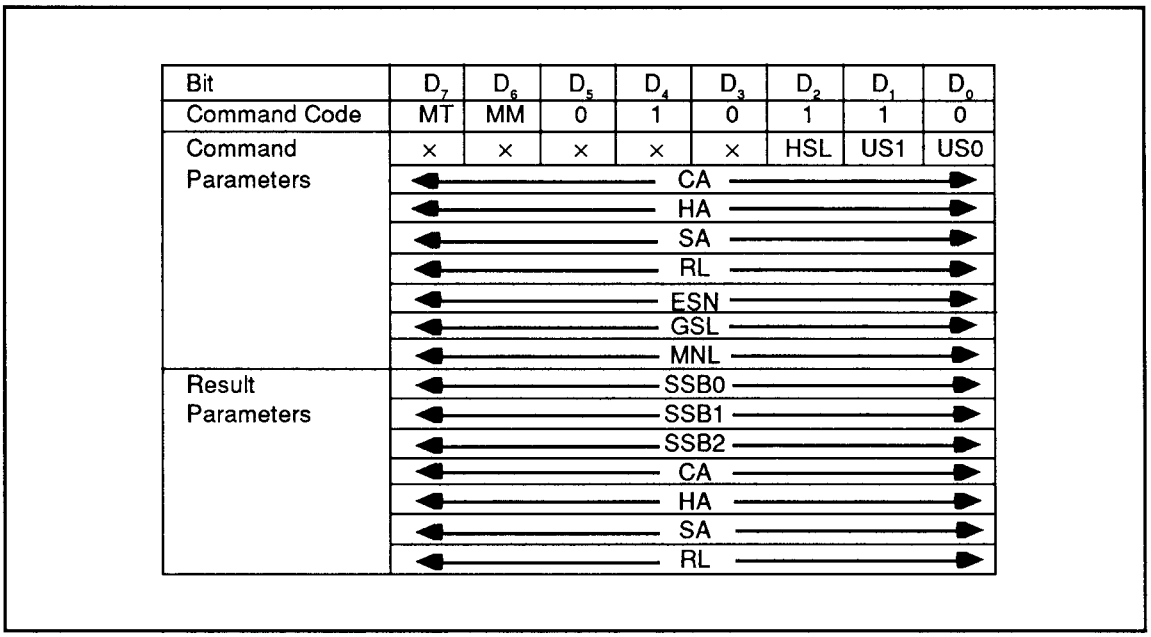


Figure 21. WRITE LONG Command

INVALID

The FDC processes the following cases as an INVALID command (Figure 22):

- Undefined command codes are written into the data register (DTR).
- HEX FF is written into DTR as a command.
- Issuing the CHECK INTERRUPT STATUS command when FDC has no Seek-end or Ready Inversion status informations.

SSB0 of the result parameter is HEX 80.

The following codes are not considered as INVALID commands after the SPECIFY 2 command has been issued:

HEX 10, 13, 14, 15, 17, 18, 1A, 1B, 1C, 1F, 57, 58

Consequently, if any of these codes is written into the FDC as a command, the FDC will malfunction. The ABORT command can be used to bring the FDC to the command waiting state, but the internal RAM contents may be destroyed.

To prevent this a SPECIFFY command followed by the RECALIBRATE command must be issued before any other command is issued. Do not write these codes into FDC as a command at SPECIFY 2 mode.

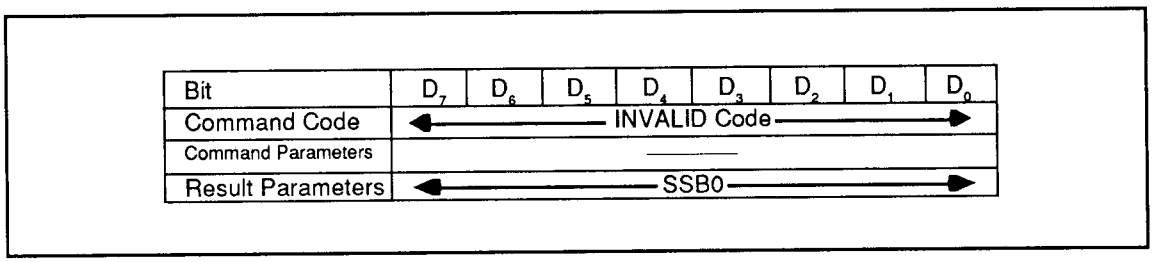


Figure 22. INVALID Command

COMMAND PARAMETERS

HSL-US: Head Select-Unit Select

US0 and US1 bits (figure 23) specify the FDD that performs the command.
HSL specifies the read/write head to be used. When SEEK and RECALIBRATE commands are issued, HSL has no meaning.

CA: Cylinder Address
CA (figure 24) specifies a sector's or track's cylinder address.
CA range: 0 to 255

HA: Head Address

HA (figure 25) specifies a sector's or track's head address as 0 or 1.

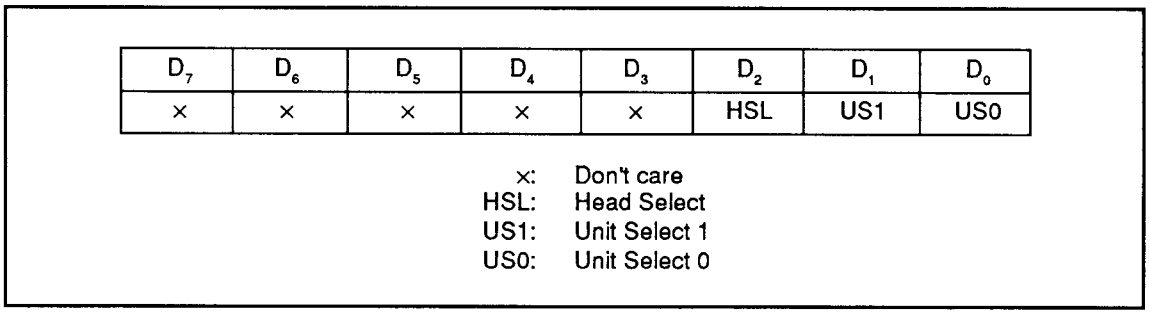


Figure 23. Head Select-Unit Select

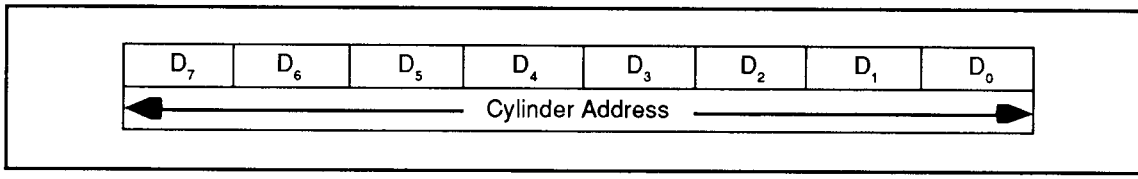


Figure 24. Cylinder Address

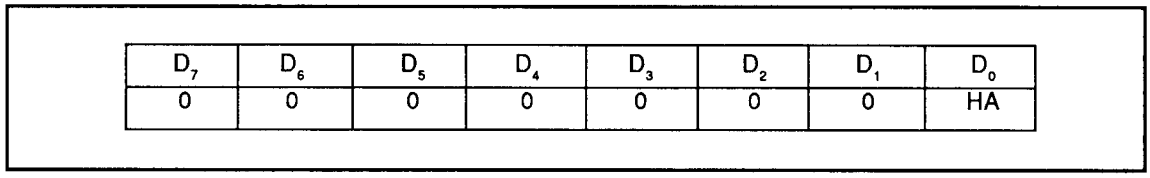


Figure 25. Head Address

SA: Sector Address

SA (Figure 26) specifies a sector's address (sector number).
SA range: 1 to 255

RL: Record Length

RL (figure 27) specifies the sector length using a 3-bit binary code.
Using values 0 to 6, different sector lengths are specified as in table 11.

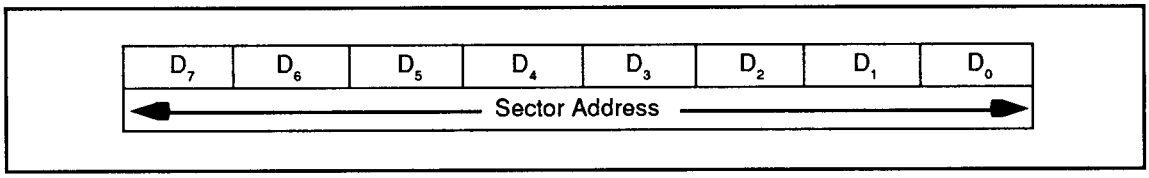


Figure 26. Sector Address

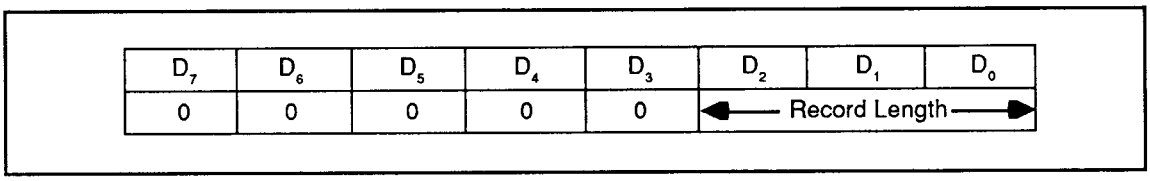


Figure 27. Record Length

Table 11. Record Length

RL	Sector Length
0	128 Bytes/sector
1	256 Bytes/sector
2	512 Bytes/sector
3	1024 Bytes/sector
4	2048 Bytes/sector
5	4096 Bytes/sector
6	8192 Bytes/sector

ESN: End Sector Number

ESN (figure 28) specifies the sector number of the last sector on the track.
This number need not be the same as the actual (physical) last sector number.
Read/Write access starts from the sector specified by SA, continues to and ends with the sector specified by ESN on the same track. However, if $\overline{\text{DEND}}$ signal is received during this time, the access terminates immediately.
ESN range: 1 to 255. However, for COMPARE commands, the range is 1 to 253.

GSL: Gap Skip Length

GSL (figure 29) specifies the number of bytes skipped in between sectors as GAP3.

MNL: Meaning Length

To access part of a sector, MNL (figure 30) specifies the byte count of data to be accessed. This function is valid only for sectors with RL = 0 (128 bytes/sector).
Values from 0 to 255 can be set for MNL. If a value exceeding 128 (HEX 80) is specified, it is treated as 128, and the entire sector is accessed. When sectors with RL ≠ 0 are accessed, MNL has no effect.

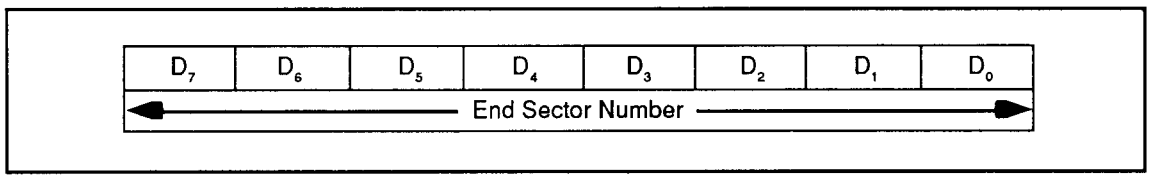


Figure 28. End Sector Number

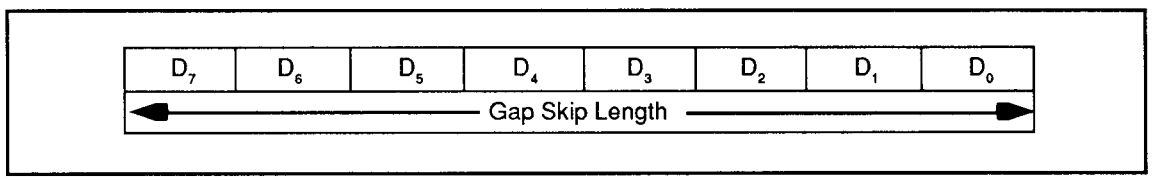


Figure 29. Gap Skip Length

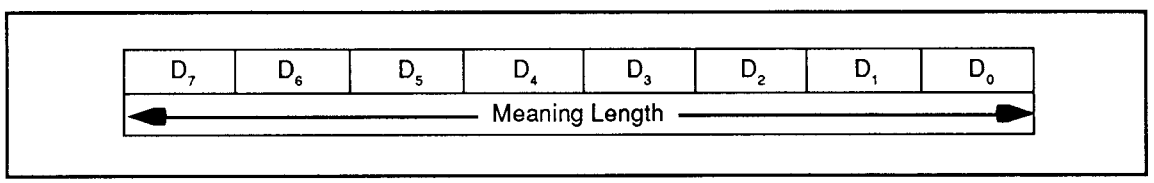


Figure 30. Meaning Length

SCNT: Sector Count

SCNT (figure 31) specifies the sector count for formatting a track.
SCNT range: 1 to 255

GP3L: Gap 3 Length

GP3L (figure 32) specifies in bytes the GAP3 length used in formatting a track.
GP3L range: 1 to 255

DUD: Dummy Data

DUD (figure 33) specifies the dummy data pattern to be written into a sector's data area when formatting.
DUD range: 0 to 255

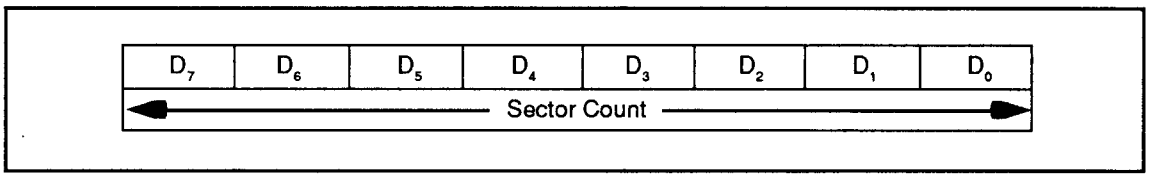


Figure 31. Sector Count

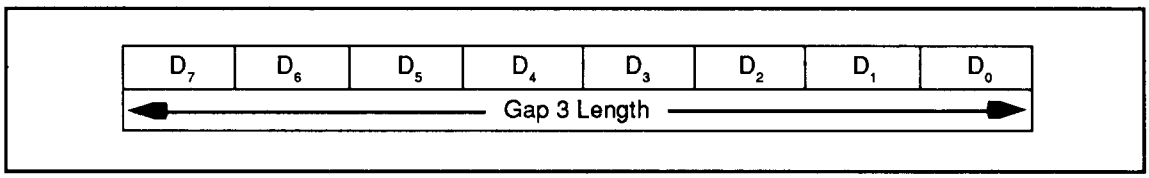


Figure 32. Gap 3 Length

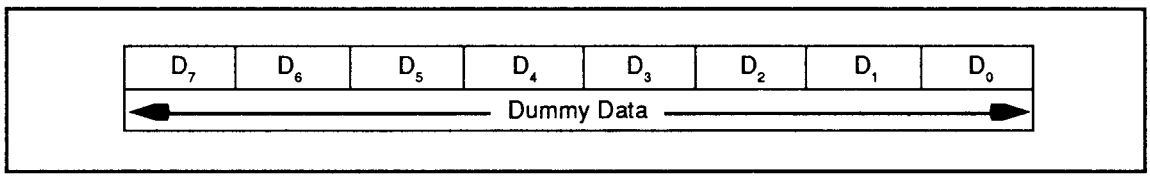


Figure 33. Dummy Data

STEP: Step

STEP (figure 34) specifies the sector increment for incrementing the sectors whose data is to be compared byte-by-byte with the data sent from the host using a COMPARE command.

STEP = 1: Data from contiguous sectors is used for comparison.

STEP = 2: Data from alternate sectors is used for comparison.

NCN: New Cylinder Number

NCN (figure 35) specifies the cylinder number to which the head is to be moved.
NCN range: 0 to 255.

STR-HDUT: Stepping Rate-Head Unload Time

STR-HDUT (figure 36) is a one-byte code in which the upper 4 bits represent STR (stepping rate) and the lower 4 bits represent HDUT (head unload time).

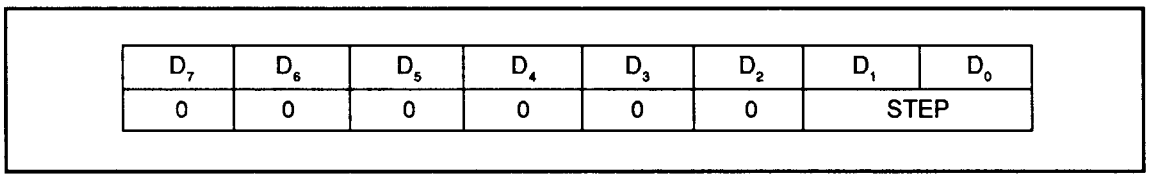


Figure 34. Step

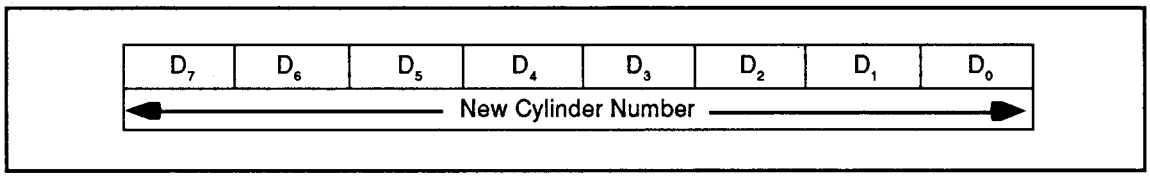


Figure 35. New Cylinder Number

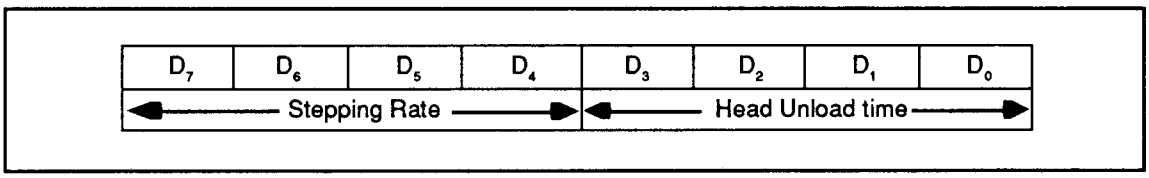


Figure 36. Stepping Rate-Head Unload Time

STR: STR specifies the step pulse interval (stepping rate) for the seek and recalibrate operations. Using values 1 to 15, different stepping rates are specified as in table 12.

Table 12. Stepping Rates

Values (Decimal)	Stepping Rate (ms)	
	8"/$\overline{5"}$ = 1 or high-speed seek mode is selected	8"/$\overline{5"}$ = 0 and high-speed seek mode is not selected
0	16	32
1	15	30
2	14	28
3	13	26
4	12	24
5	11	22
6	10	20
7	9	18
8	8	16
9	7	14
10	6	12
11	5	10
12	4	8
13	3	6
14	2	4
15	1	2

CLK = 16 MHz

HDUT: HDUT specifies the time to wait from the completion of the head-load associated command execution before deactivating the head load signal. Using values 0 to 15, different head unload times are specified as in table 13.

HDLT-NDM: Head Load Time-Non-DMA Mode

The upper 7 bits of HDLT-NDM (figure 37) denote HDLT (head load time) while the lowest bit denotes NDM (Non-DMA mode).

Table 13. Head Unload Times

Set Values (Decimal)	Head Unload Time (ms) 8"/5" = 1	8"/5" = 0
0	0	0
1	16	32
2	32	64
3	48	96
4	64	128
5	80	160
6	96	192
7	112	224
8	128	256
9	144	288
10	160	320
11	176	352
12	192	384
13	208	416
14	224	448
15	240	480

CLK = 16 MHz

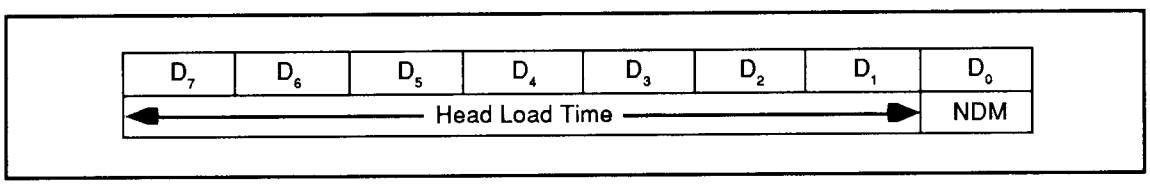


Figure 37. Head Load Time-Non-DMA Mode

HDLT: HDLT specifies the time to wait from setting the head load signal active to start the command execution. When specifying HDLT, an allowance for head settle waiting time should be made also. Using values 0 to 127, different head load times are specified as in table 18.

NDM: NDM specifies if DMA or Non-DMA mode is used for transferring data between the FDC and the host.

NDM = 0: DMA mode
NDM = 1: Non-DMA mode

LCTK: Low Current Track

LCTK (figure 38) specifies the cross-over track number beyond which the LCT signal (pin 48) becomes active in SPECIFY2 mode. With LCTK set to a value ranging from 1 to 255, the LCT signal becomes active for tracks exceeding the LCTK value. With LCTK set to 0, the LCT signal is inactive at every track.

Table 14. Head Load Times

Set Values (Decimal)	Head Load Time (ms) 8"/5" = 1	8"/5" = 0
0	0	0
1	2	4
2	4	8
3	6	12
4	8	16
5	10	20
6	12	24
7	14	28
8	16	32
↓	↓	↓
124	248	496
125	250	500
126	252	504
127	254	508

CLK = 16 MHz

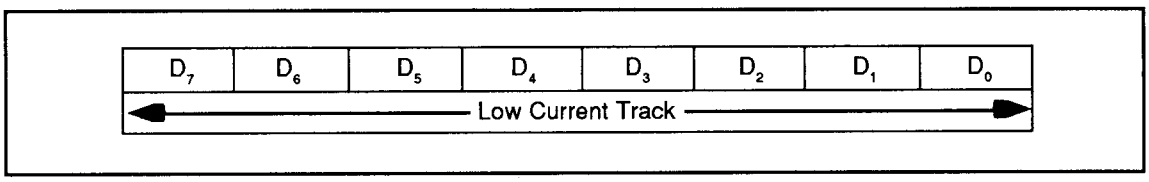


Figure 38. Low Current Track

PC1, PC0: Precompensation Delay 1, 0

PC1 and PC0 (figure 39) specify the amount of precompensation delays for the auto precompensation mode (table 15). PC0 specifies the delay for the outer tracks (smaller track numbers) and PC1 specifies the delay for the inner tracks (larger track numbers). The FDC switches between PC0 and PC1 automatically depending on the head position. The switch-over track position is specified by PCDCT. Maximum programmable values for PC1 and PC 0 are

- HEX C in 5" mode
- HEX 6 in 8" mode

Values exceeding the above limits may cause malfunction.

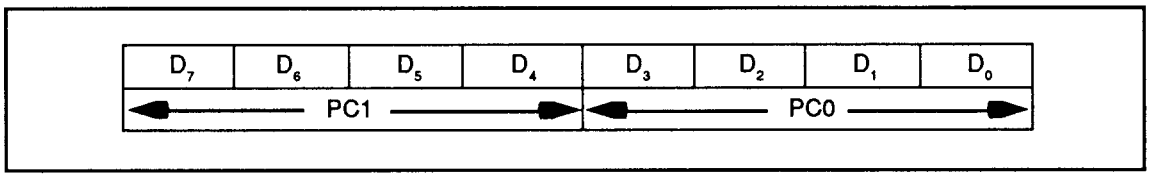


Figure 39. Precompensation Delay 1, 0

Table 15. Precompensation Delay

	Delay (ns)	
PC1, PC0	**CLK=16 MHz**	**CLK=19.2 MHz**
HEX 0	0	0
HEX 1	62.5	52.1
HEX 2	125	104.2
HEX 6	375	312.5
HEX B	687.5	572.9
HEX C	750	625

PCDCT: Precompensation Delay Change Track

PCDCT (figure 40) specifies the track where the precompensation delay amount is changed in the auto precompensation mode. For tracks with a number equal to or larger than PCDCT, the delay amount is specified by PC1, and for tracks with a smaller number, the delay is specified by PC0.
PCDCT range: 1 to 255

RESULT PARAMETERS

CA, HA, SA, and RL: Cylinder Address, Head Address, Sector Address, Record Length

CA, HA, SA, and RL are provided as command execution results and their values depend on the command type and how the command execution ended, with or without errors.

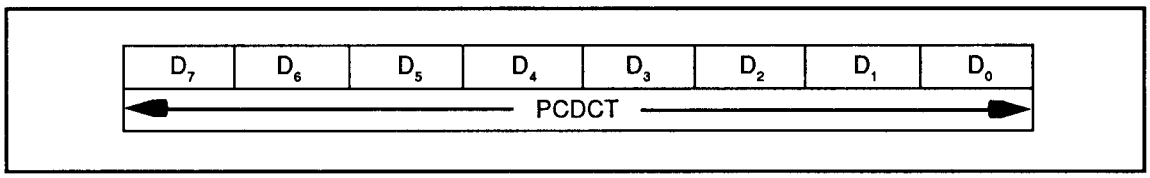


Figure 40. Precompensation Delay Change Track

SSB0: Sense Status Byte 0

INC (Interrupt Code) : INC (figure 41) indicates the cause of an interrupt request (table 16).
SED (Seek End): SED is set to 1 at the completion of SEEK and RECALIBRATE commands.
DER (Drive Error): DER is set to 1 when the fault signal is active during or at the completion of write related command execution, and when the track 0 signal cannot be detected from a drive to which 255 step pulses were applied during a RECALIBRATE command execution.
DNR (Drive Not Ready): DNR is set to 1 when a low level ready signal is detected from a drive at the start of or during the execution of drive access commands other than the CHECK DEVICE STATUS command.
HSL (Head Select): HSL indicates the head selected at the completion of command execution. In response to the CHECK INTERRUPT STATUS command, a zero is returned.
US1, US0 (Unit Select 1, 0): US1 and US0 indicate the drive number selected at the completion of a command execution or the one that caused an interrupt request.

SSB1: Sense Status Byte 1

NDE (No DMA End): NDE (figure 42) is set to 1 if the DEND signal is not received active even after the last sector data has been transferred with a read/write related command. The last sector is determined depending on the MT (multi track) bit value as follows:

Table 16. Interrupt Code

D7	D6	Code Symbol	Code Name	Meaning
0	0	NOR	Normal End	Command normally ended
0	1	ABE	Abnormal End	Command abnormally ended
1	0	IVC	Invalid Command	Issued command is invalid
1	1	CDS	Change in Drive Status	Ready signal level from a drive is inverted compared to the last time it was polled

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
INC		SED	DER	DNR	HSL	US1	US0

Figure 41. Sense Status Byte 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
NDE	0	CER	DOR	0	INF	WPM	ANF

Figure 42. Sense Status Byte 1

- MT = 0: The last sector is specified by the ESN (end sector number) byte on the track of the side specified as part of the command parameters.
- MT = 1: The last sector is specified by the ESN byte but always corresponds to the track on side 1.

CER (CRC Error): CER is set to 1 when a CRC error is detected in the ID or data field. READ ID command does not have any effect on this bit. For CRC errors in the ID field, only the CER bit is set to 1. For CRC errors in the data field, the CDF bit of SSB2 as well as the CER bit are set to 1.

DOR (Data Overrun): DOR is set to 1 if the host cannot complete data transfer requested by the FDC within a specified time to satisfy the FDC data throughput requirements. For details, see section 6.5, "Command Functions".

INF (ID Not Found): The meaning of INF depends on its context.

1. In READ DATA, READ DELETED DATA, READ LONG, WRITE DATA, WRITE DELETED DATA, WRITE LONG, and COMPARE commands: INF is set to 1 if the sector number (CA, HA, SA, RL) specified by a command parameter or updated during a multisector read/write operation cannot be found by the time three index pulses are detected.
2. In READ ID command: INF is set to 1 when an address mark in the ID field was detected but a CRC error-free ID was not found by the time three index pulses were detected.
3. In READ ERRONEOUS DATA command: INF is set to 1 if ID data in the FDC does not match the ID found.

WPM (Write Protected Medium): WPM is set to 1 when an active write protected signal is detected at the start of write related command execution.

ANF (AM not Found): ANF is set to 1 if no ID address mark is detected by the time three index pulses are detected. ANF as well as the NAM bit of SSB2 are set to 1 when no address mark (data address mark or deleted data address mark) is detected in the data field within 1 ms after the desired ID was found, or when the first data other than HEX 00 found after the desired ID and at least 4 bytes (FM mode) or 5 bytes (MFM mode) of HEX 00 were detected is not AM.

SSB2: Sense Status Byte 2

DDA (Deleted Data Address Mark): DDA (figure 43) is set to 1 when a deleted data address mark is detected. In executing the READ DELETED DATA command, however, it is set to 1 when a normal data address mark is detected.
CDF (CRC Error in Data Field): CDF is set to 1 if a CRC error is detected in the data field.
CAU (Cylinder Address Unmatch): CAU is set to 1 when the disk ID's CA byte does not match the command parameter's CA byte, except when the disk ID's CA byte is HEX FF. However, CAU is not set by the READ ERRONEOUS DATA command.
CCS (Compare Condition Satisfied): CCS is set to 1 when the equal condition is satisfied while executing a COMPARE command.
CNS (Compare Condition Not Satisfied): CNS is set to 1 when the specified compare condition is not satisfied while executing a COMPARE command.
BDC (Bad Cylinder): BDC is set to 1 when the CA byte read from the disk does not match the command parameter's CA byte and also when the read CA byte is HEX FF. However, BDC is not set by the READ ERRONEOUS DATA command.
NAM (No Data Address Mark): NAM is set to 1 if no address mark (data address mark or deleted data address mark) is detected in the data field within 1 ms after the desired ID was found, or when the first data other than HEX 00 found after the desired ID and at least 4 bytes (FM mode) or 5 bytes (MFM mode) of HEX 00 were detected is not AM.

SSB3: Sense Status Byte 3

1) FLT,WPT, RDY, TRZ, and DSD: Sense bits FLT, WPT, RDY, TRZ, and DSD indicate the status of the drive specified in the CHECK DEVICE STATUS command.
2) HSL, US1, and US0: Sense bits HSL, US1, and US0 have the same values as HSL, US1, and US0 of the command parameters.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	DDA	CDF	CAU	CCS	CNS	BDC	NAM

Figure 43. Sense Status Byte 2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
FLT	WPT	RDY	TRZ	DSD	HSL	US1	US0

FLT: Fault
WPT: Write Protected
RDY: Ready
TRZ: Track 0
DSD: Double Sided
HSL: Head Select
US1: Unit Select 1
US0: Unit Select 0

Figure 44. Sense Status Byte 3

PCN: Physical Cylinder Number

PCN (figure 45) represents the physical address of the drive head position stored in the FDC (physical number of the track where a head is currently placed). If a SEEK or RECALIBRATE command ends abnormally, the PCN value may not match the head's current physical address. When the FDC is reset, the PCN values for all four drives are set to HEX 00. Accordingly, drives with an auto-recalibrate function (a function which automatically moves the heads onto track 0 at power on) do not require the RECALIBRATE command to be issued after the power on reset. The lower two bits of SSB0 read last indicate which drive the PCN value belongs to.

ISSUING COMMANDS

Writing Command Codes

Command can be issued by writing the desired command codes into the FDC. The status register must be read before issuing a command.

The FDC is ready to accept commands when the status register bits are as shown in figure 46.

When any of the D0S to D3S bits are set to 1:

1. CHECK DEVICE STATUS command and CHECK INTERRUPT STATUS command can be issued for all four drives. However, CHECK INTERRUPT STATUS command is treated as an invalid command when the FDC has no SEEK end and no READY inversion status.
2. SEEK and RECALIBRATE commands can be issued only for drives whose corresponding D0S to D3S bits are zeros.

Commands other than CHECK related and SEEK related commands can be issued when the status register value equals HEX 80.

An ABORT command can be issued independent of the status register value.

When a command code is written, the status register is set as shown in figure 47 and the FDC begins to decode the command.

If the Data Register is read in the command waiting state, the FDC will malfunction since the FDC considers it as a command issue. So, during command waiting state, do not attempt to read the Data Register.

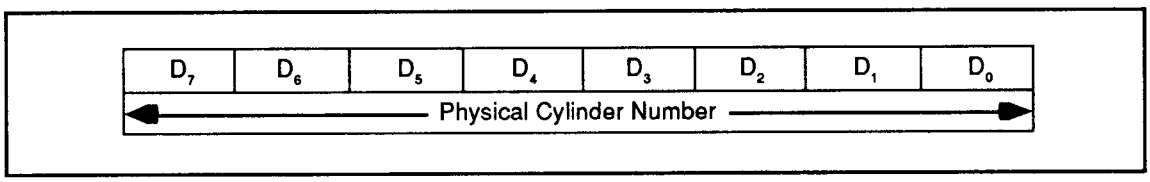


Figure 45. Physical Cylinder Number

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	0	0	×	×	×	×

Figure 46. Status Register Before Issuing a Command

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
0	0	0	1	×	×	×	×

Figure 47. Status Register After Issuring a Command

Writing Command Parameters

At the completion of command code decoding, for commands requiring command parameters, the FDC sets the status register as shown in figure 48 and wait for command parameters.

TXR bit is cleared to zero every time a command parameter byte is received.
When the FDC is ready to receive the next command parameter byte the TXR bit is again set to one and the next byte is transferred. After all the command parameter bytes have been received, no more transfer requests are made.

Transferring Data

Data transfer is performed during command execution in response to an FDC request. Data transfer requests are made by setting the $\overline{IRQ}$ signal active in Non-DMA mode or the $\overline{DREQ}$ signal active in DMA mode. Status register contents for both types of data transfer requests are shown in figure 49. Once data transfer begins, the $\overline{IRQ}$ and $\overline{DREQ}$ signals are made inactive and the TXR bit is cleared to zero.

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	0	1	×	×	×	×

Figure 48. Status Register Waiting for Command Parameters

Read request in Non-DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	1	1	0	0	0	0

Write request in Non-DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	1	1	0	0	0	0

Read request in DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	0	1	0	0	0	0

Write request in DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	0	1	0	0	0	0

Figure 49. Status Register Contents for Various Data Transfer Requests

Transferring Result Status

For commands having a result status, the FDC requests the host to accept the result parameter bytes at the completion of the command execution. Commands which have no result status are SEEK, RECALIBRATE, SPECIFY1, SPECIFY2, SLEEP, and ABORT. Commands which cause the status register to be set up as shown in figure 50 and request the host to accept the result parameters are: CHECK DEVICE STATUS, CHECK INTERRUPT STATUS, and INVALID.

The above commands do not activate the $\overline{IRQ}$ signal in order to transfer the result parameters.
After one byte of the result parameters has been transferred, TXR and DIR are cleared to zero. When the next byte of the result parameters is ready to be transferred, it is loaded into the data register. Then both the DIR and TXR bits of the status register are set to 1 requesting the host to accept the new parameter byte. After the last byte of the result parameters has been transferred, some dummy data is loaded into the data register, TXR is set to 1 and BSY is cleared to 0 to enter the command waiting state (DIR remains zero).
For all the other commands, the result status transfer is performed by setting the $\overline{IRQ}$ signal active and the status register as shown in figure 51. The $\overline{IRQ}$ signal is active only when the first byte of the result parameters is transferred, and becomes inactive after that.

The first byte of the result parameters is transferred according to the following sequence of operations.
- $\overline{IRQ}$ signal is set active
- DIR bit is set to 1
- Result parameter byte is loaded into the data register
- TXR bit is set to 1
- FDC waits for the result parameter byte to be transferred
- Host reads the result parameter byte and TXR bit is reset to 0.
- DIR bit is reset to 0.
- $\overline{IRQ}$ signal is set inactive.

The remaining bytes are transferred in the same way except that the $\overline{IRQ}$ signal is not activated again. After the last byte of the result parameters is transferred, some dummy data is loaded into the data register, TXR is set to 1 and BSY is cleared to 0 to enter the command waiting state (DIR remains zero).

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	0	1	×	×	×	×

Figure 50. Status Register Requesting Result Parameter Transfer (No $\overline{IRQ}$)

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	0	1	0	0	0	0

Figure 51. Status Register Requesting Result Parameter Transfer (with $\overline{IRQ}$)

DRIVE POLLING

This FDC performs drive polling every 1 ms (actually 1.024 ms) in 8" mode and every 2 ms (2.048 ms) in 5" mode during command waiting. During sleep and head loading, no polling is performed. Polling and seek operation (step pulse output) are performed concurrently.

US0 and US1 signals are changed (figure 52) and the Ready signals of all four drives are polled (figure 53). During this time, a step pulse is issued to the drive requiring it (figure 53). When high speed seek mode is specified using SPECIFY 2 command, 1 ms polling is performed even in 5" mode.

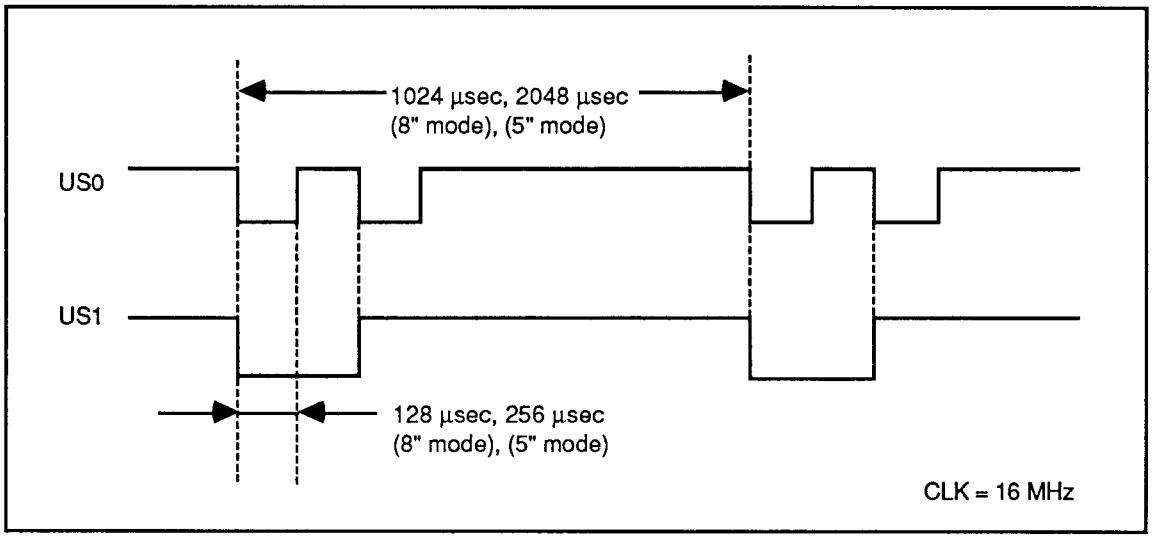


Figure 52. Drive Selection Timing during Polling

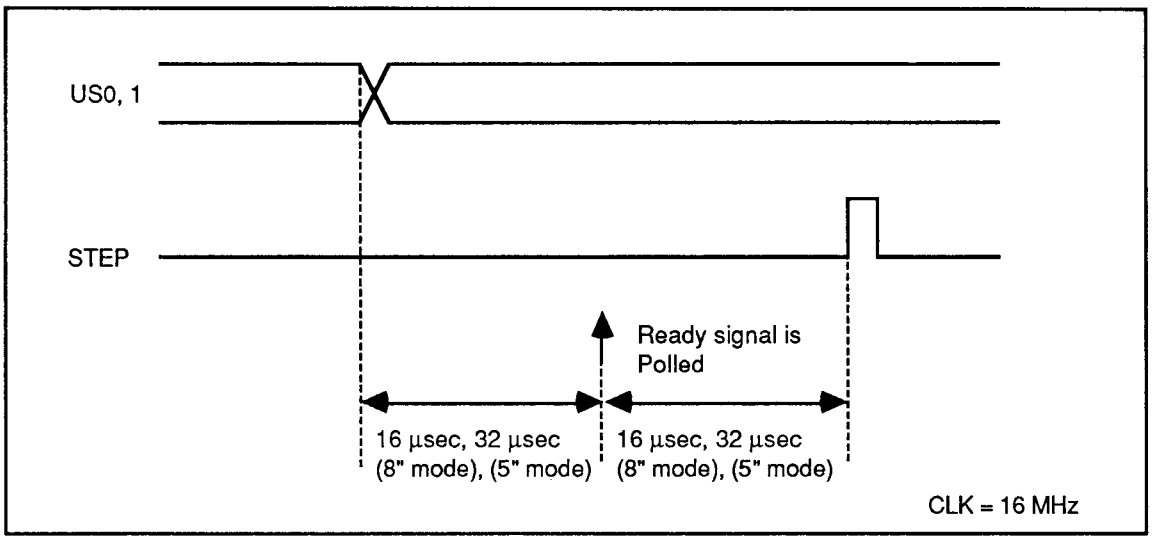


Figure 53. Ready Signal Polling and Step Pulse Output Timing

During polling , if the ready signal level is inverted compared to the last time it was polled:

- INC (interrupt code) bits of SSB0 are set to CDS (Change in Drive Status) code,
- US1 and US0 bits of SSB0 are updated to the drive number whose ready signal is inverted, and
- $\overline{IRQ}$ signal is set active to request the host to issue CHECK INTERRUPT STATUS command.

Also, when a drive completes a seek operation, $\overline{IRQ}$ is set active to make a request for CHECK INTERRUPT STATUS command.

When a CHECK INTERRUPT STATUS command request source is accepted from the FDC by the CHECK INTERRUPT STATUS command, if there is no Seek-End status information in the FDC, the next command request is not generated even if the Ready Signal Inversion status information is present. However, when the CHECK INTERRUPT STATUS command is issued, the command is not treated as the INVALID command; the Ready Signal Inversion status information can be accepted. When Ready Signal Inversion is detected while the $\overline{IRQ}$ signal is inactive, the CHECK INTERRUPT STATUS command is requested by activating the $\overline{IRQ}$ signal.

If the FDC has statuses for more than one CIS command request, it returns FDD statuses to the host each time a CIS command is issued, starting at the lowest-numbered FDD's status.

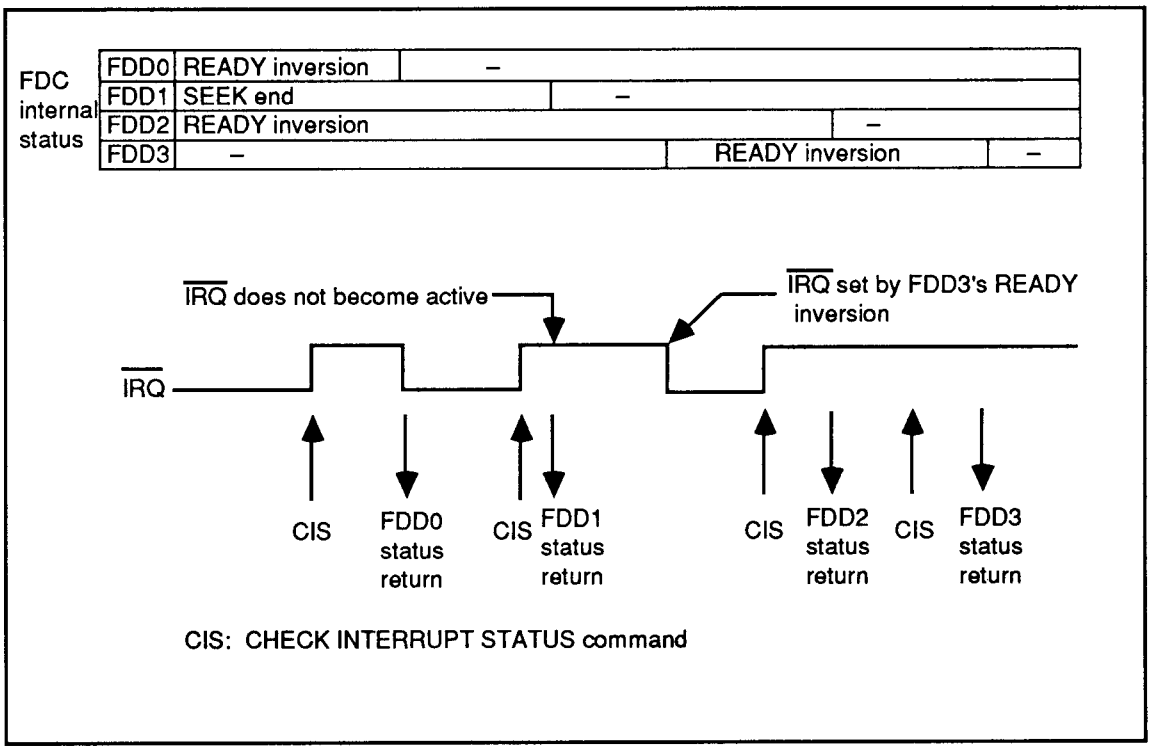


Figure 54. FDD status returning order and $\overline{IRQ}$ output

Internal Circuit Specification

VFO Circuit

- Analog PLL type VFO circuit
- Adjustment free and high accuracy with optimized PLL loop gain and stabler circuits
- No adjustment required
- Selectable data synchronization rate

FM mode: 125, 150, 250 kbps
MFM mode: 250, 300, 500 kbps

To synchronize to the data transferred at 150 kbps in FM mode or 300 kbps in MFM mode, a 19.2 MHz clock must be input to CLK pin with 8"/$\overline{5"}$ pin tied low.

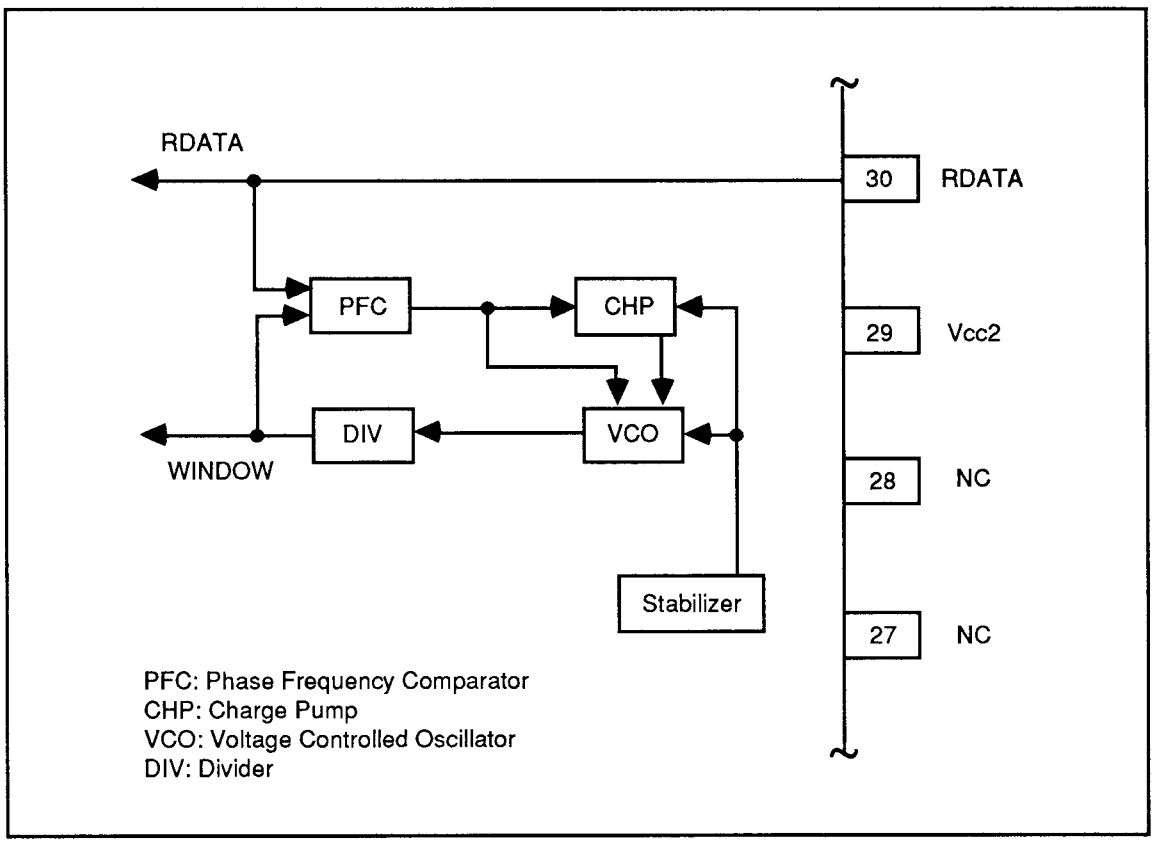


Figure 55. Internal Block Diagram

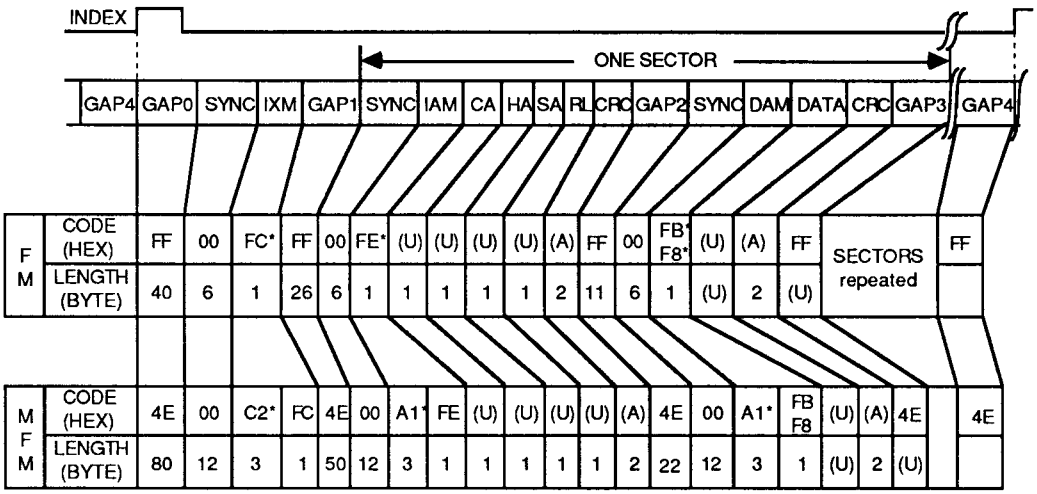
WRITE PRECOMPENSATION CIRCUIT

- Digital precompensation circuit
- Delay time programmable by software
- Delay time independently selectable for inner and outer tracks
- Outer to inner switchover track specifiable
- When auto-precompensation mode is not selected by command SPECIFY 2, the precompensation control signals (EARLY, LATE) are output. When auto-precompensation mode is selected, the control signals are not output; EARLY and LATE are fixed at low level.
- Delay time programmable by 62.5 ns increments (Note)
- Auto-precompensation and precompensation control signals are output in MFM mode only
- Range of delay time programmable (in MFM mode)
  250 kbps: 0 – 750 ns
  300 kbps: 0 – 625 ns (Note)
  500 kbps: 0 – 375 ns
  When a value beyond this range is specified, FDC may malfunction.

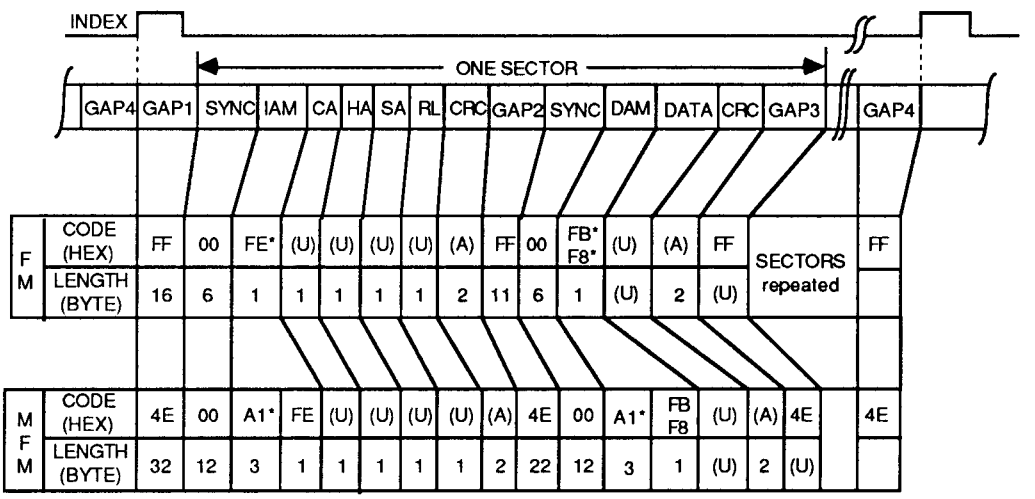
Note: CLK = 19.2 MHz delay time programmable by 52.1 ns increments at 300 kbps.

Track Format

SFORM = 1 IBM Format



SFORM = 0 ISO Format



(U) : User programmable
(A) : Automatically calculated

CA : Cylinder Address
HA : Head Address
SA : Sector Address
RL : Record Length

IXM : Index Mark
IAM : ID Address Mark
DAM : DATA (Deleted Data) Address Mark

GAP4 Length extends from the end of GAP3 in the last sector to the next Index pulse.
Codes marked asterisk (*) indicate that a code contains missing clock.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} (Note 1)	– 0.3 to + 7.0	V
Input Voltage	V_{in} (Note 1)	– 0.3 to V_{CC} + 0.3	V
Allowable Output Current	$\|I_O\|$ (Note 2)	5	mA
Total Allowable Output Current	$\|\Sigma I_O\|$ (Note 3)	80	mA
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

Notes: 1. This value is in reference to V_{SS} = 0 V

2. The allowable output current is the maximum current that may be drawn from, or flow out to, output terminal or one input/output common terminal.
3. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.
4. Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be used under recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} (Note)	4.75	5.0	5.25	V
Input Low Level Voltage	V_{IL} (Note)	0	–	0.8	V
Input High Level Voltage	V_{IH} (Note)	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

Note: This value is in reference to V_{SS} = 0 V

Electrical Characteristics

DC Characteristics

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0 to + 70 °C unless otherwise noted)

Item		Symbol	Measuring Conditions	Limits Min	Limits Max	Unit
Supply Voltage	$V_{CC}1$-$V_{CC}4$	V_{CC}		4.75	5.25	V
Input High Level Voltage	All Inputs	V_{IH}		2.2	V_{CC}	V
Input Low Level Voltage	All Inputs	V_{IL}		– 0.3	0.8	V
Input Leak Current	All Inputs except D0 – D7	I_{in}	V_{in} = 0 to V_{CC}	– 2.5	2.5	µA
Three State (Off State) Input Current	D0 – D7	I_{TSI}	V_{in} = 0.4 to V_{CC}	– 10	10	µA
Output High Level Voltage	All Outputs except $\overline{IRQ}$ when IFS = 1	V_{OH}	I_{OH} = – 400 µA	2.4	–	V
Output Low Level Voltage	All Outputs	V_{OL}	I_{OL} = 1.6 mA	–	0.5	V
Output Leak Current (Off State)	$\overline{IRQ}$ when IFS = 1	I_{LOH}	V_{OH} = V_{CC}	–	10	µA
Input Capacitance	All inputs and outputs	C_{in}	V_{in} = 0 V, T_a = 25 °C f = 1.0 MHz	–	15	pF
Current Consumption	$V_{CC}1$-$V_{CC}4$	I_{CC}	FDC unselected and Disk operation with data transfer in progress	–	40	mA
			FDC in sleep mode	–	10	mA

AC Timing Specification

No.	Item	Symbol	Min	Typ	Max	Unit
1	Clock cycle time	$t_{cyc}C$	50	62.5	80	ns
2	Clock high level width	PW_{HC}	15			ns
3	Clock low level width	PW_{LC}	15			ns
4	Clock falling time	t_{Cf}			20	ns
5	Clock rising time	t_{Cr}			20	ns
6	Read data high level width	PW_{HRDT}	40			ns
7	Read data low level width	PW_{LRDT}	40			ns
8	Write data high level width	PW_{HWDT}		4		$t_{cyc}C$[2]
9	Index signal high level width	PW_{IDX}	6[1]			$t_{cyc}C$
10	Fault reset signal high level width	PW_{FRS}	136[1]		140[1]	$t_{cyc}C$
11	$\overline{DEND}$ signal low level width	PW_{DEND}	40			ns
12	$\overline{RESET}$ signal low level width	PW_{RES}	28[1]			$t_{cyc}C$
13	Enable signal cycle time	$t_{cyc}E$	410			ns
14	Enable signal low level width	PW_{EL}	200			ns
15	Enable signal high level width	PW_{EH}	200			ns
16	Enable signal rising time	t_{Er}			20	ns
17	Enable signal falling time	t_{Ef}			20	ns
18	Address setup time	t_{AS}	0			ns
19	Address hold time	t_{AH}	0			ns
20	Data delay time	t_{DDR}			140	ns
21	Data hold time	t_{DHR}	20			ns
22	$\overline{IRQ}$ release time	t_{IRQ}			200	ns
23	Data setup time	t_{DSW}	60			ns
24	Data hold time	t_{DHW}	5			ns
25	$\overline{DREQ}$ signal release time	t_{DRQ}			200	ns
26	$\overline{RD}$ signal low level width	PW_{RDL}	200		1200[1]	ns
27	$\overline{WR}$ signal low level width	PW_{WRL}	200		1200[1]	ns
28	$\overline{DACK}$ signal low level width	t_{AA}	200			ns
29	$\overline{DACK}$ signal response time	t_{RA}	0			ns
30	$\overline{RD}$ signal response time 1	t_{RR}	0			ns
31	$\overline{WR}$ signal response time 1	t_{RW}	0			ns
32	Unit selection time	t_{US}		128[1]		µs
33	STEP signal timing	t_{UP}		32[1]		µs
34	STEP signal high level width	PW_{HSTP}		7[1]		µs
35	US0 signal switching time	t_{US0}		128[1]		µs
36	US1 signal low level width	t_{US1}		256[1]		µs
37	Polling cycle time	$t_{cyc}US$		1024[1]		µs
38	Head selection signal switching time	t_{HSL}		2[1]		ms
39	FDD selection time	t_{SFD}			3[1]	µs
40	EARLY, LATE signal high level width	PW_{ELH}		1[1]		µs

Notes: 1. These numbers are doubled for 5.25 inch mode.

2. $t_{cyc}C$ refers to a clock period of the input clock (CLK).

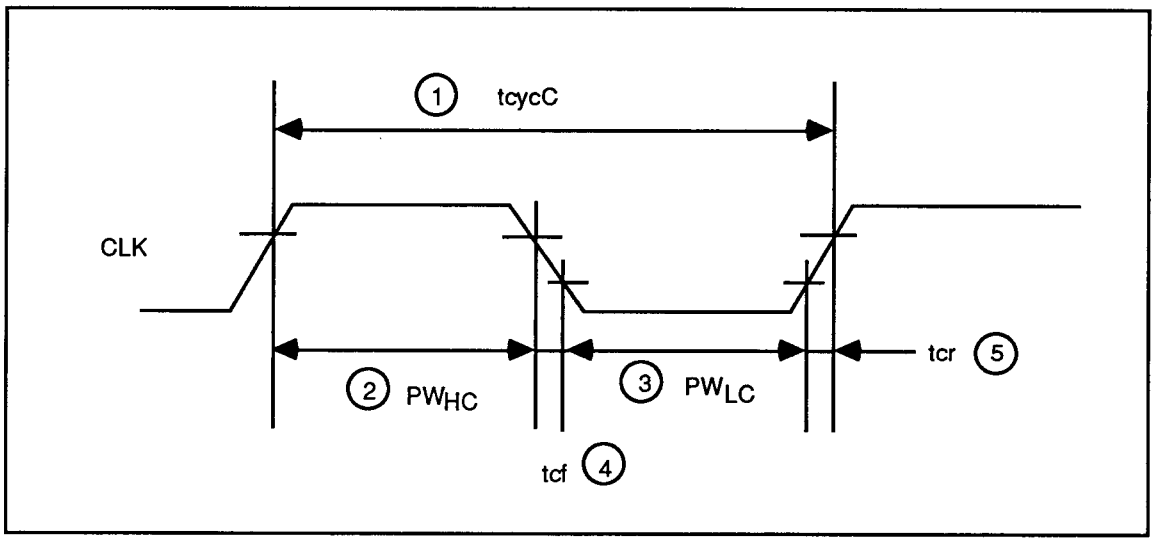


Figure 56. Clock Timing

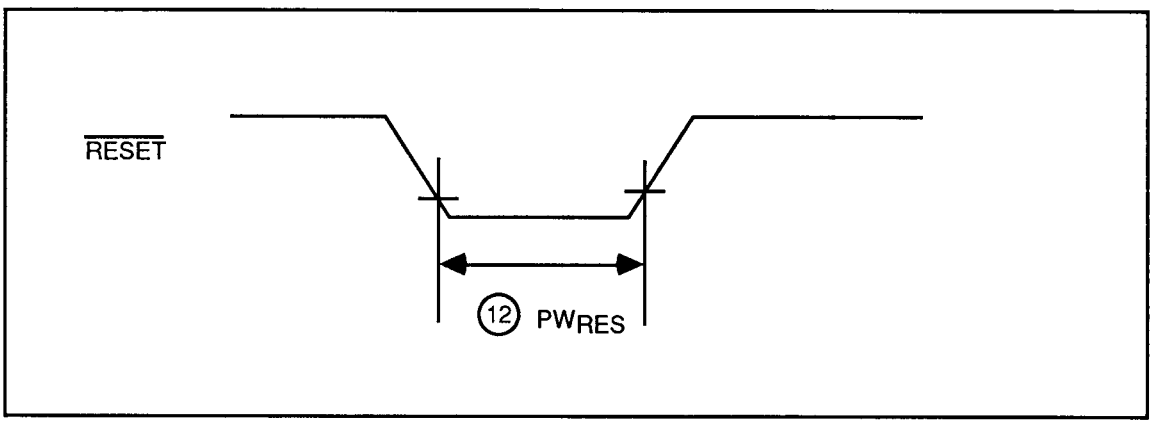


Figure 57. Reset Timing

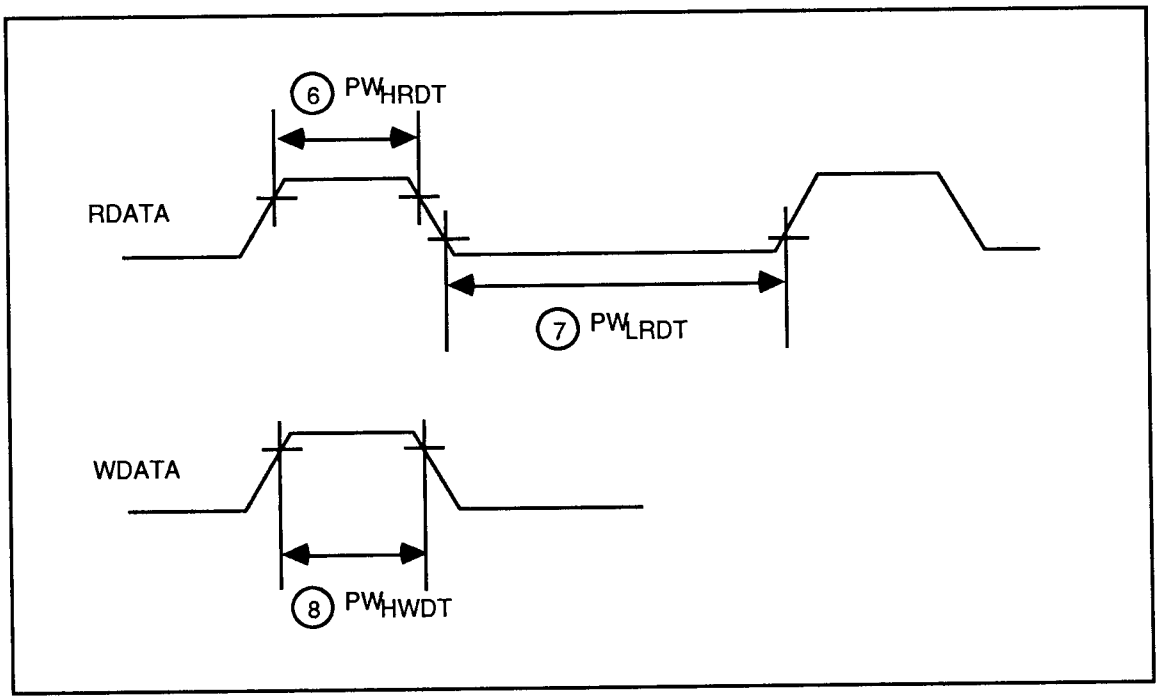


Figure 58. FDD Data Timing

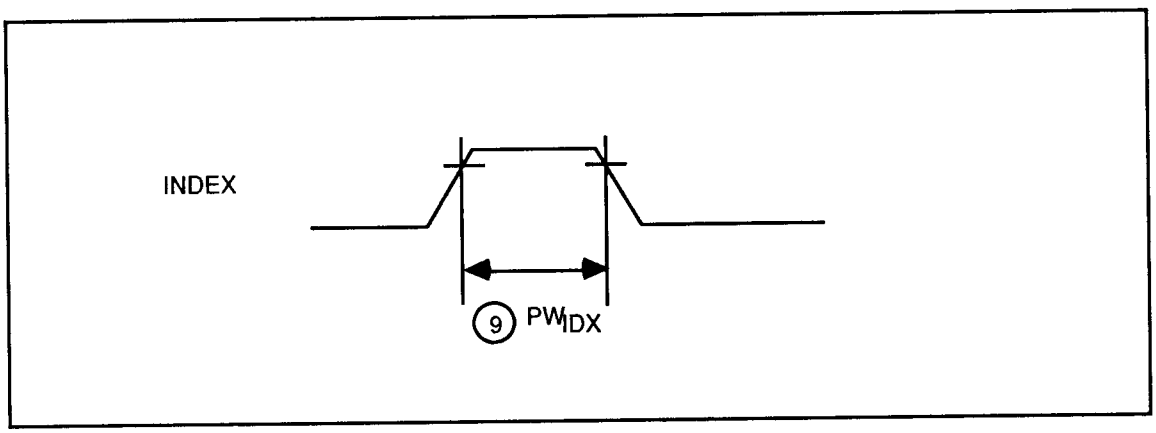


Figure 59. Index Timing

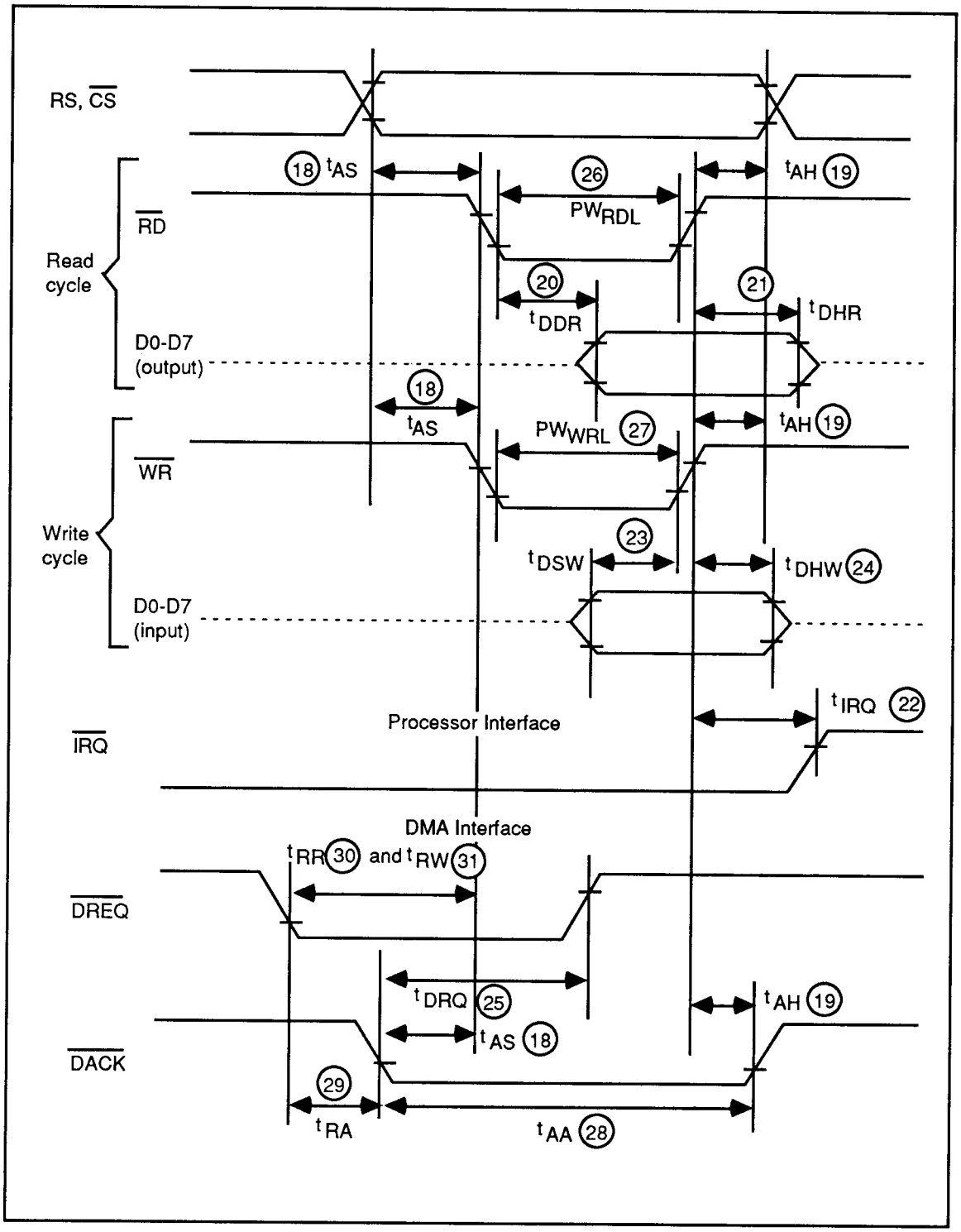


Figure 60. Data Transfer Timings for 80XX Interface

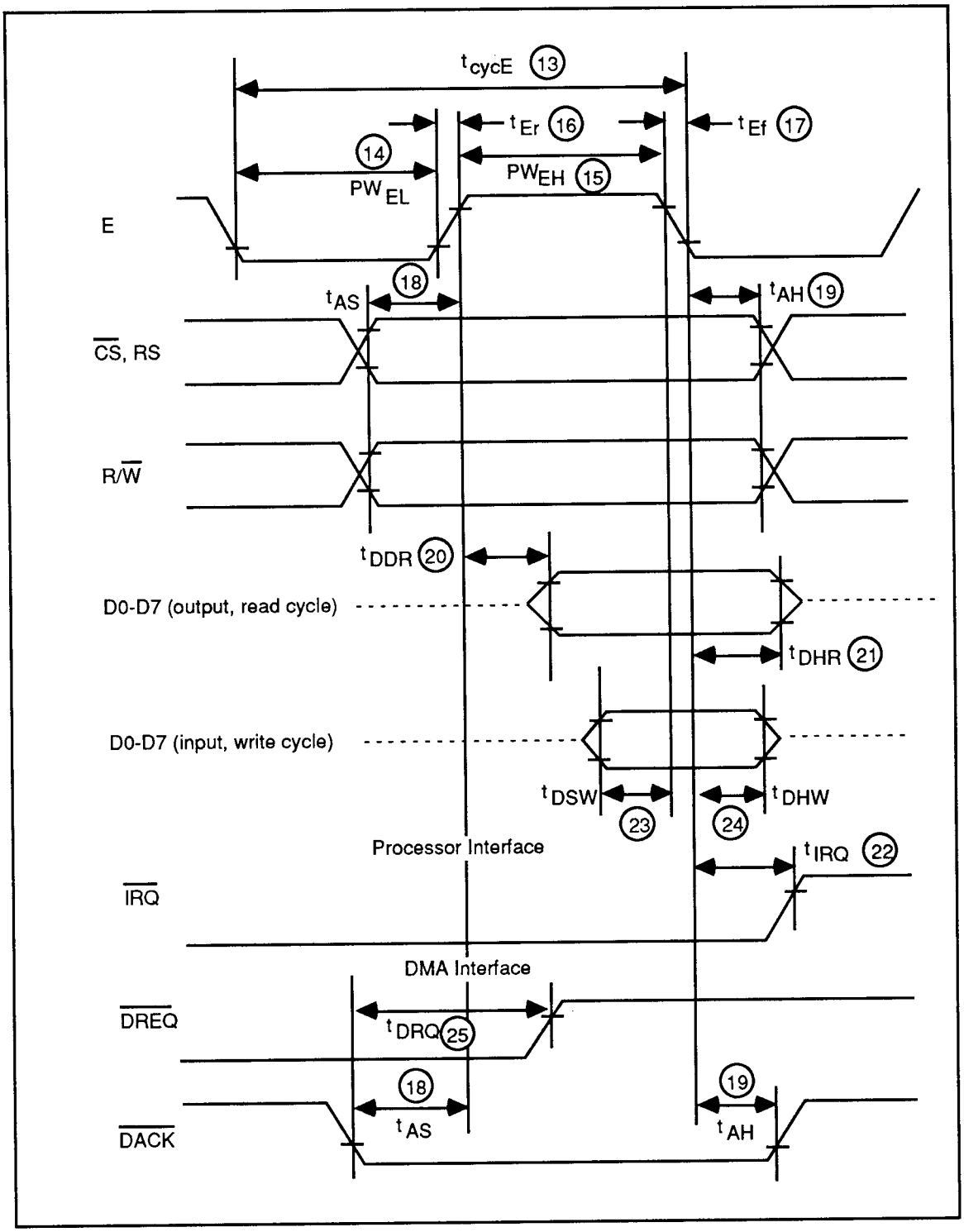


Figure 61. Data Transfer Timings for 68XX Interface

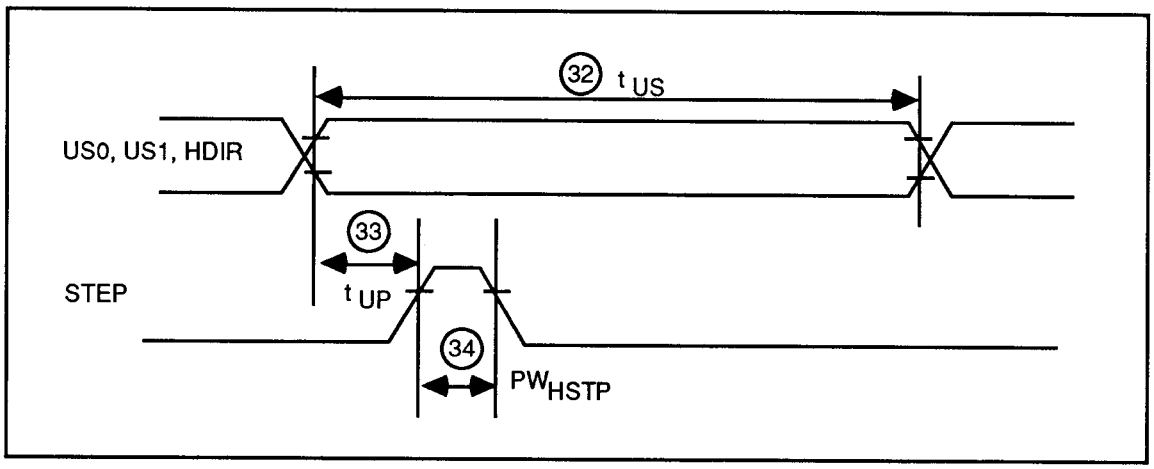


Figure 62. Seek, Recalibrate Timing

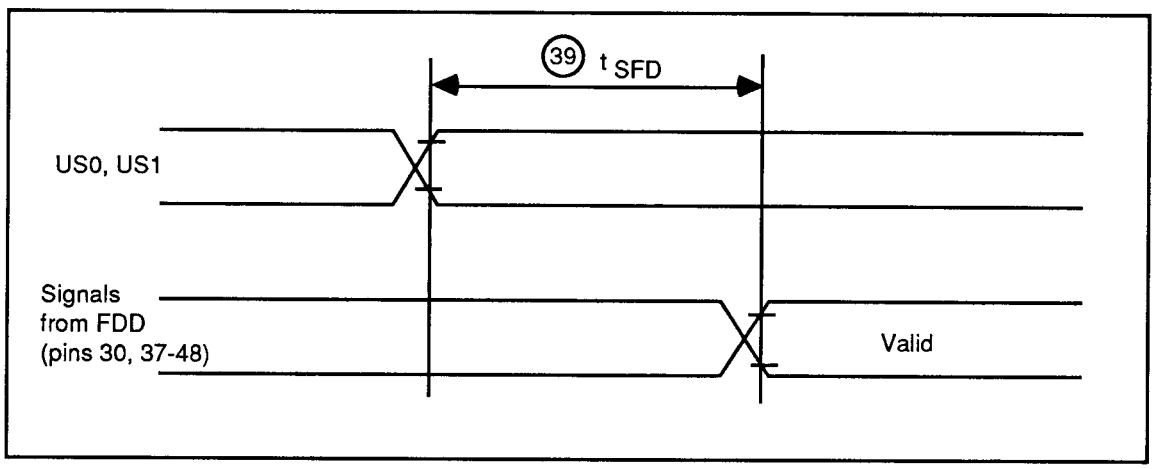


Figure 63. Drive Select Timing

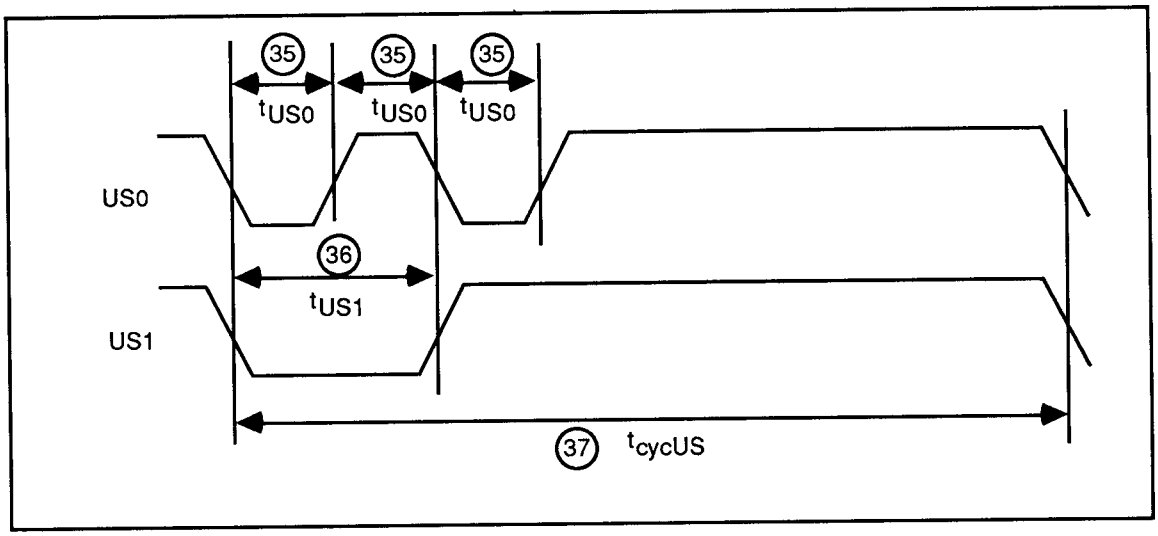


Figure 64. Automatic Polling Timing

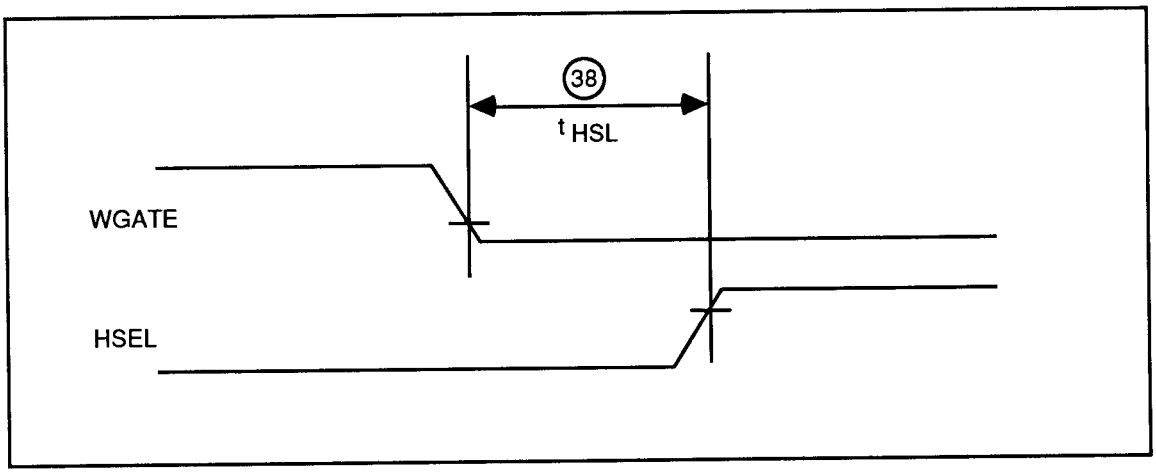


Figure 65. Multitrack Write Timing

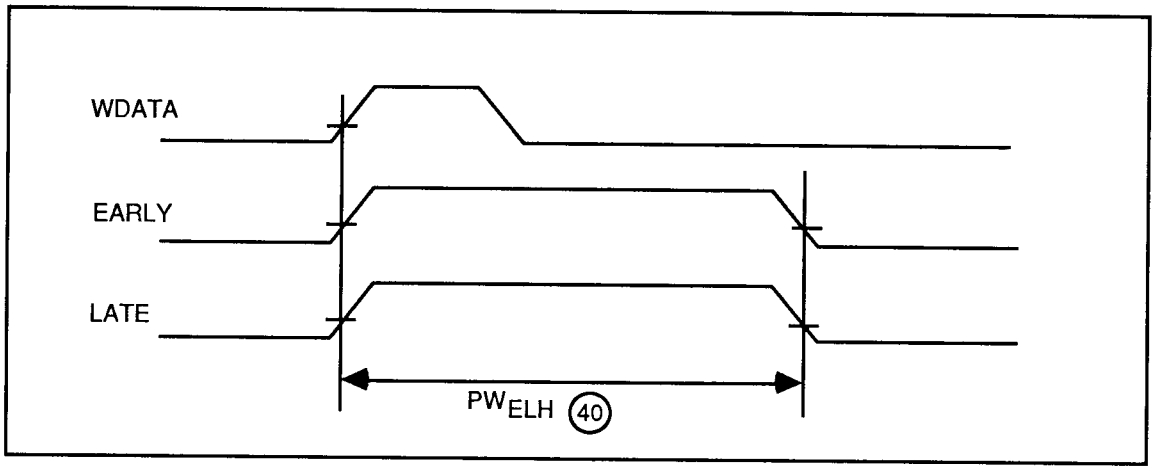


Figure 66. Precompensation Timing

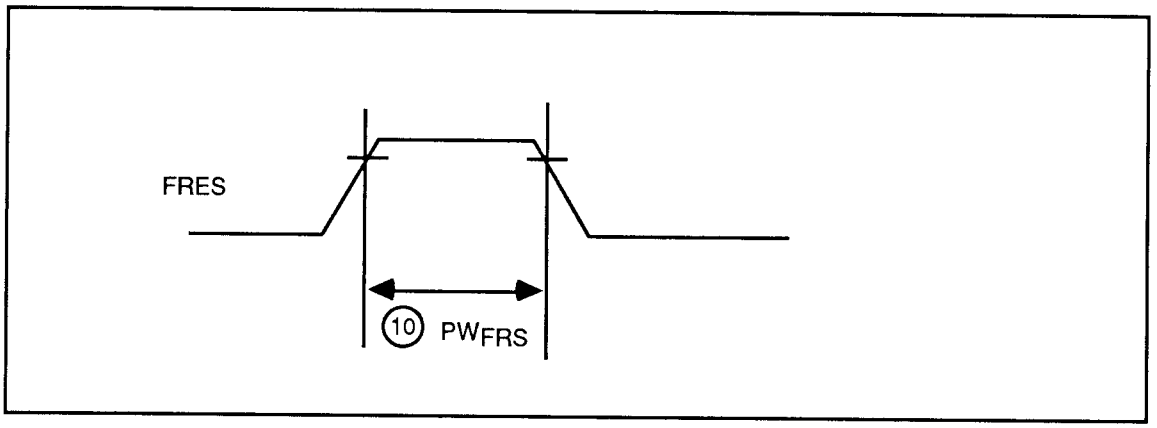


Figure 67. Fault Reset Timing

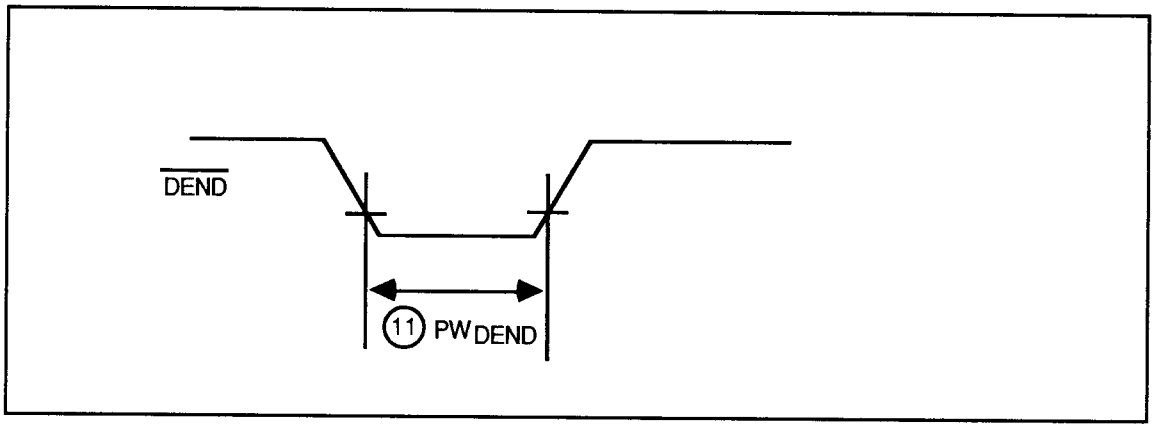
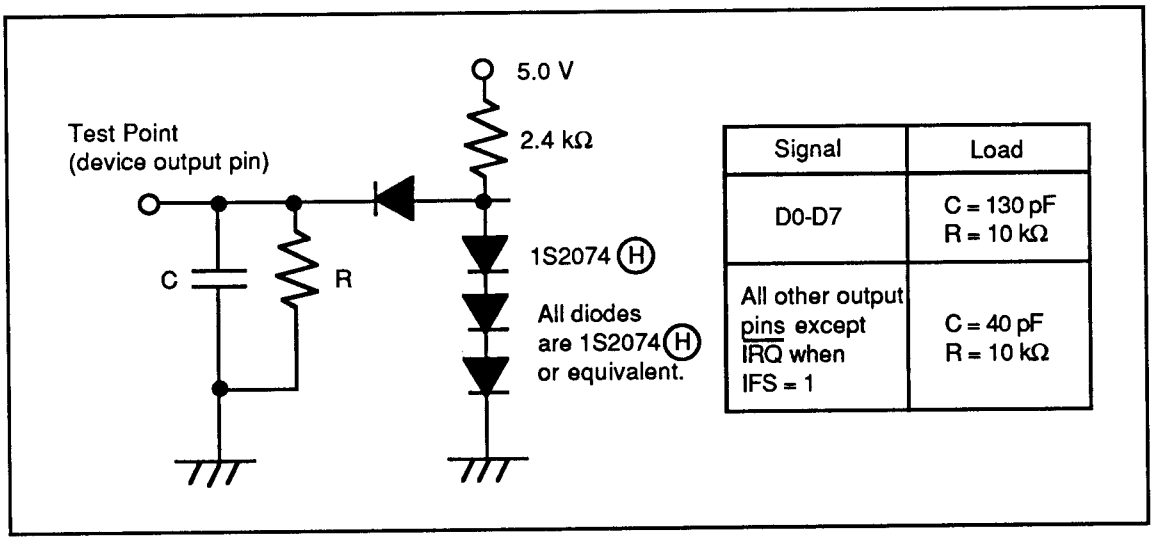


Figure 68. DMA End Timing



Signal	Load
D0-D7	C = 130 pF R = 10 kΩ
All other output pins except $\overline{IRQ}$ when IFS = 1	C = 40 pF R = 10 kΩ

Figure 69. Output Load Circuit for AC Testing

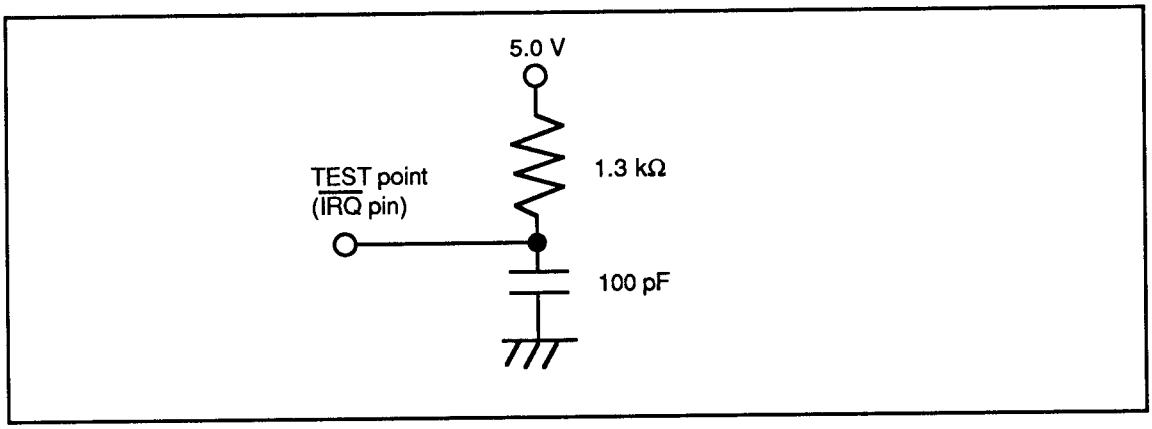


Figure 70. $\overline{IRQ}$ Load Circuit for AC Testing when IFS = 1

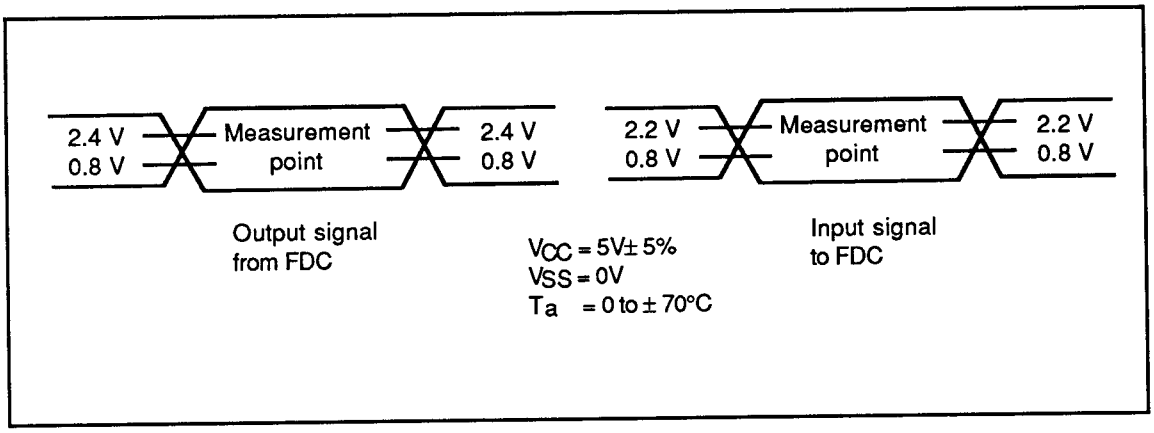


Figure 71. AC Testing Measurement Conditions

Refer to user's manual (No. ADE-602-001) for detail of this product.