ICs for Communications

ATM OAM Processor
AOP

PXB 4340 E Version 1.1

Data Sheet 04.2000

DS 1

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1 Overview

The PXB 4340 E ATM OAM Processor is a member of the Infineon ATM622 chip set. The whole chip set consists of:

- PXB 4330 E ATM Buffer Manager ABM
- PXB 4340 E ATM OAM Processor AOP
- PXB 4350 E ATM Layer Processor ALP
- PXB 4360 F Content Addressable Memory Element CAME

Main ATM Layer functionality is achieved with only two chips, ALP and ABM. The combination of these two devices provides elementary ATM functionality like header translation, policing, OAM support, multicast and traffic management (Fig.1). The functionality is upgradeable to full OAM support by the AOP (Fig.2) and to arbitrary header translation by CAME (Fig.3).

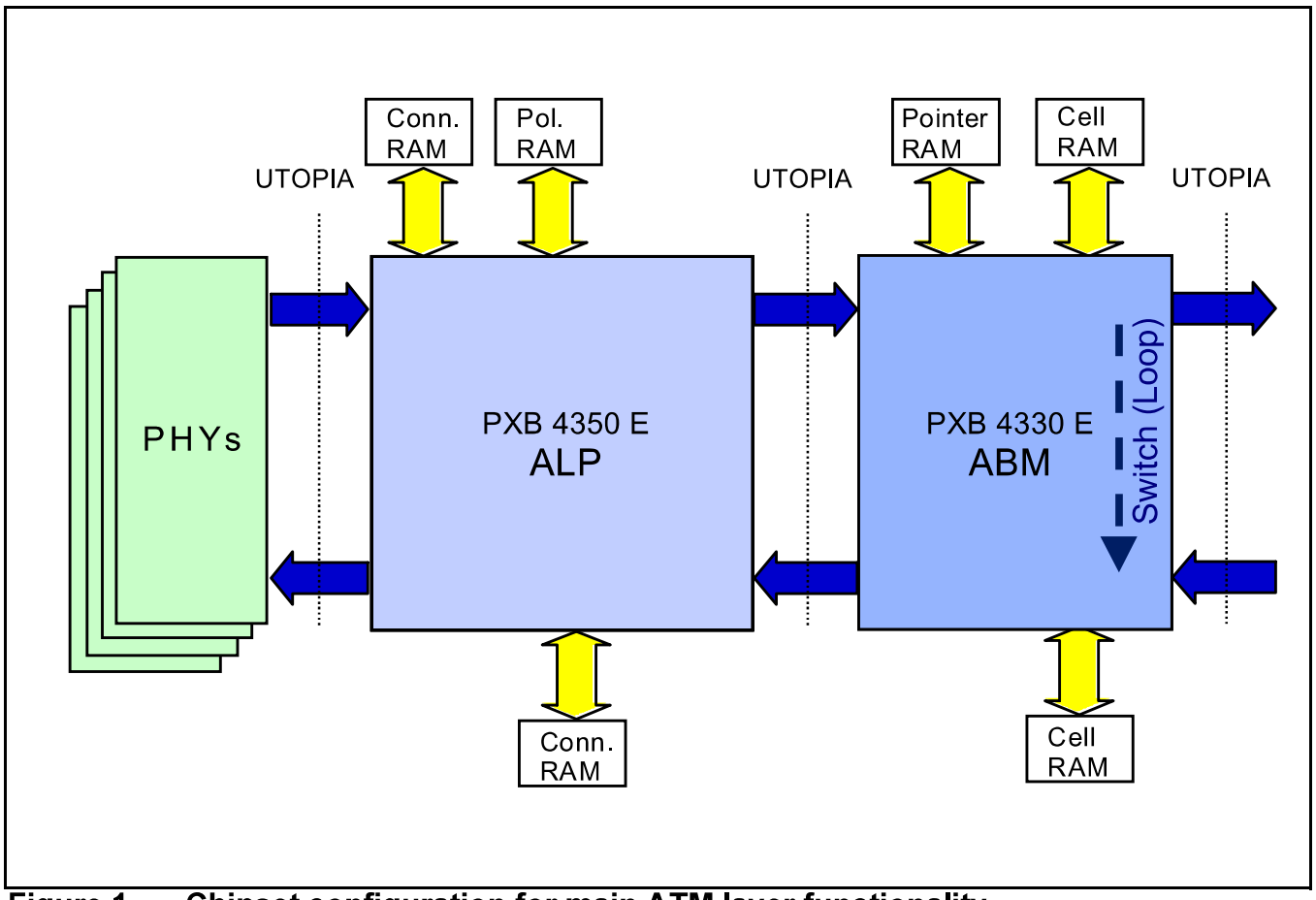


Figure 1 Chipset configuration for main ATM layer functionality

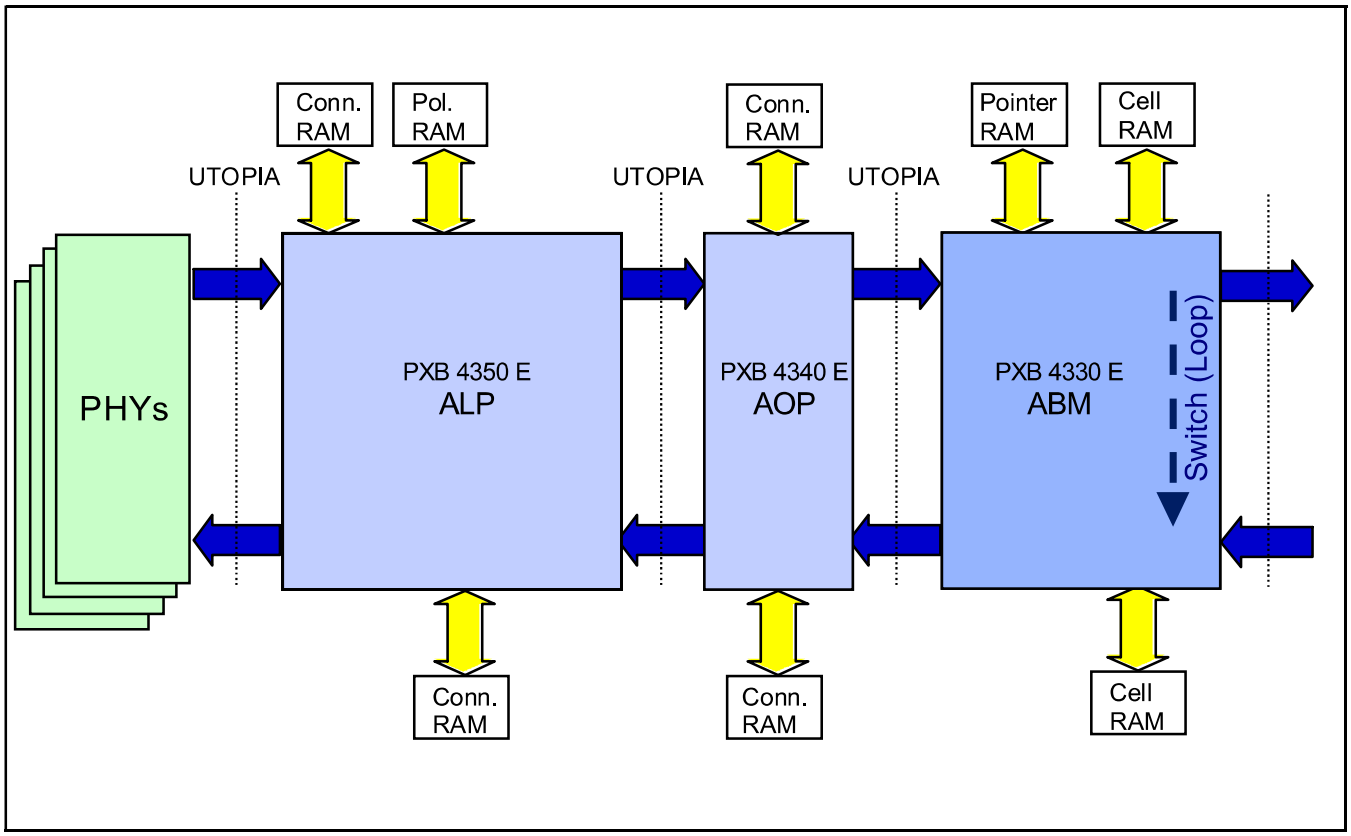


Figure 2 Chipset configuration for main ATM layer functionality plus full OAM

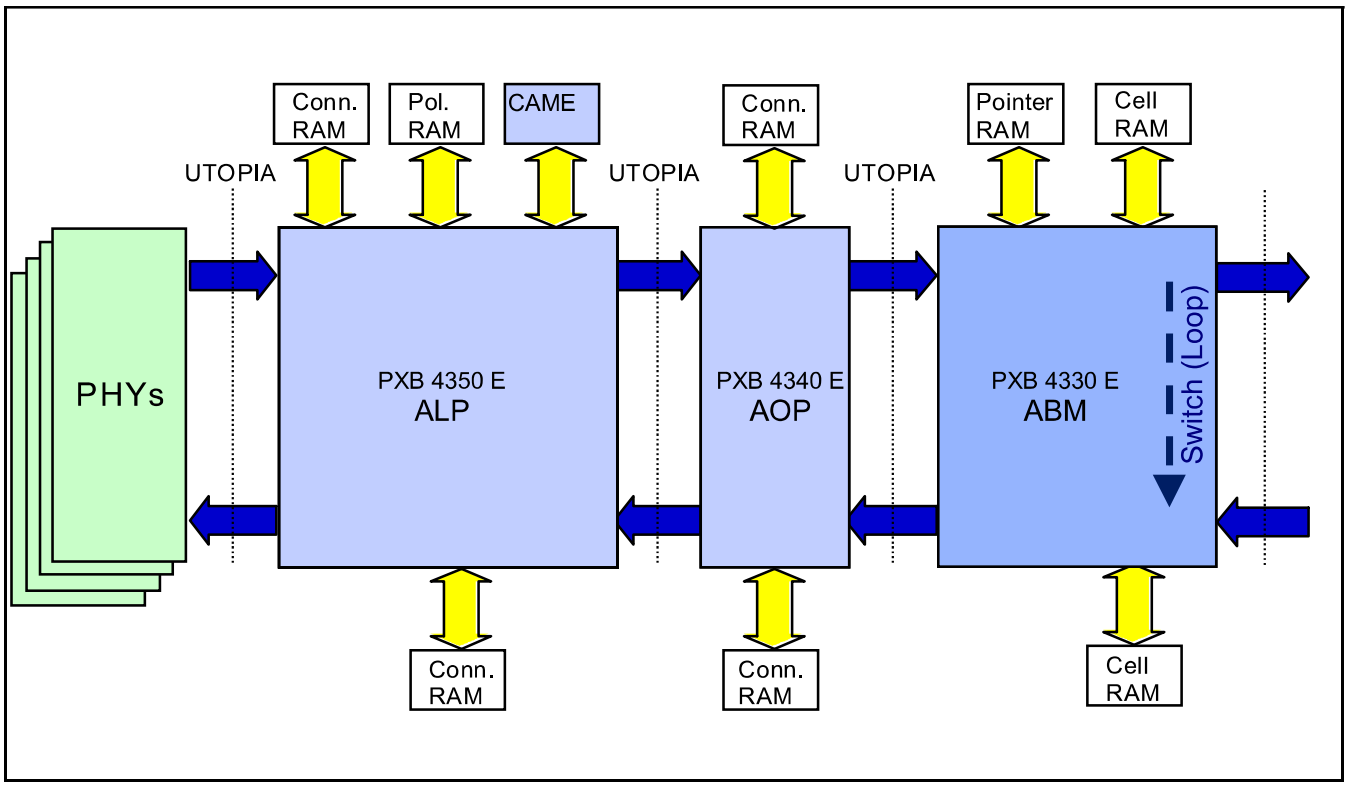


Figure 3 Chipset configuration for main ATM layer functionality plus full OAM and arbitrary header translation.

The ATM 622 Layer devices can be used as ....

...a full switch in:
ADSL Concentrators / Multiplexers (DSLAM)
Access Multiplexers
Access Concentrators
Multiservice switches

...Line card in:
Workgroup Switches
Edge Switches
Core Switches

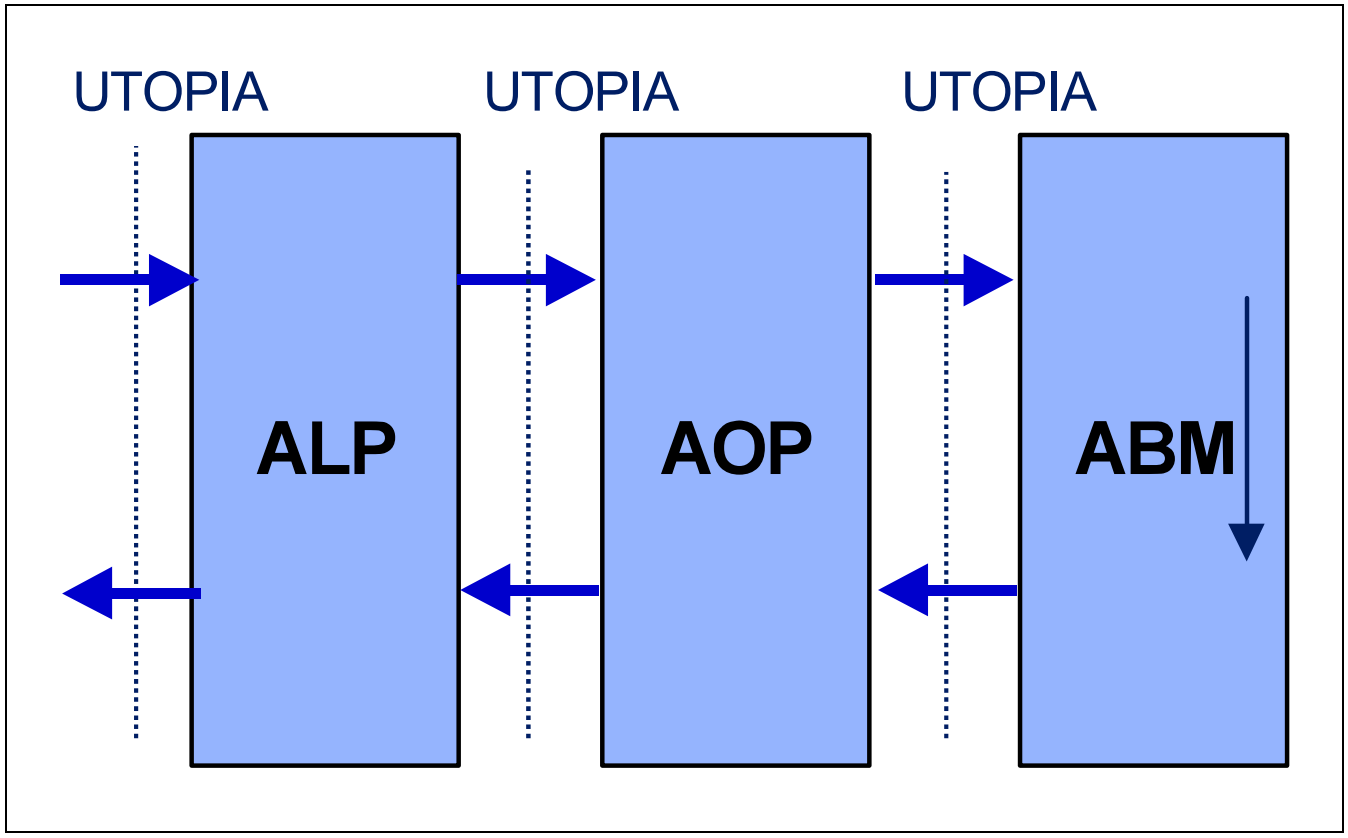


Figure 4 Miniswitch configuration

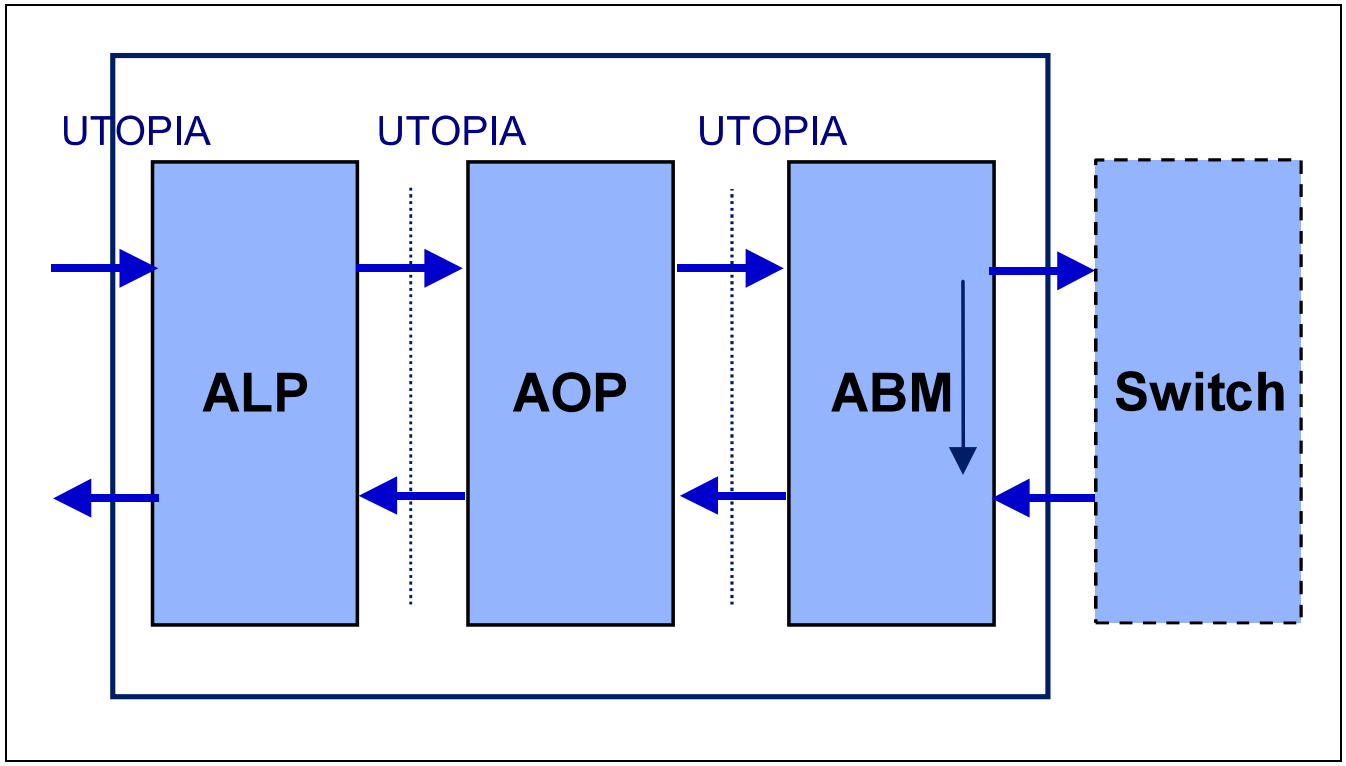
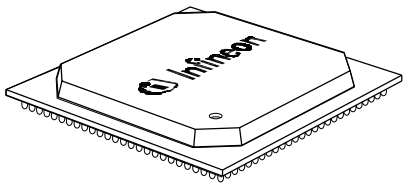


Figure 5 Line card configuration

Due to their most flexible scaling facilities, feature set and throughput the Infineon ATM622 layer chips are the ideal devices for almost any ATM system.

1.3 Features



P-BGA-352

Performance

- Performance up to STM-4/OC-12 equivalent ATM layer processing
- Flexibel throughput from1 .. 687 Mbit/s bi-directional
- Up to 16384 connections in both directions (VPC/ VCC)
- Temperature range from 0°C to 70°C
- Multiport UTOPIA Level 2 interface in up- and downstream direction according to ATM Forum, UTOPIA Level 1 and 2 specifications [**1, 2**]
- 16-bit microprocessor interface, e.g. 386EX
- Cell insert/extract function
- 32 cell FIFO buffer at UTOPIA upstream receive interface
- 96 cell shared buffer for up to 24 PHYs at UTOPIA downstream transmit interface
- Boundary scan support according to JTAG [**4**]
- Internal data stream loop at ATM and at PHY side

External RAMs

- Two external SSRAMs for connection related data, one for upstream and one for downstream direction, 2 x 4 Mbit for 16K connections
- DMA for fast data transfer between external RAM and microprocessor
- All entries parity protected

OAM Functions

- OAM Levels and Flows (F4/F5) according to ITU-T/I.610 [**6**] and Bellcore GR-1248 [**7**]
- All OAM cell types hard-wired
- Generation, discard, extraction and insertion of OAM cells
- Programmable OAM cell types for future standardization

AIS/RDI/CC Functions

- AIS/RDI/CC function for all connections permanently active
- Automatic generation of VP/VC-AIS cells at line failures

Type	Package
PXB 4340 E	P-BGA-352-2

- Automatic generation of VC-AIS cells for all VCCs of a VPC at the endpoint including automatic backward emission of VP-RDI cells
- Automatic generation of VP/VC-CC cells to detect ATM layer failures
- Optional internal CC function for switch test (proprietary)
- Programmable guard times and cell insertion intervals
- Support of CC activation/deactivation cells

Loopback

- Automatic loop of cells for all connections with LB ID inversion
- Programmable Port ID for on the fly comparison with Location ID or Source ID of LB cells
- Insertion/extraction of LB cells via microprocessor

Performance Monitoring

- 128 simultaneous PM generation/ evaluation processors shared for up- and downstream direction
- Full HW evaluation of FM cells and generation of BR cells
- Full HW support of data collection according to Bellcore GR-1248 for 128 connections
- Support of PM activation/deactivation cells
- Support of simultaneous PM flows of F4 and F5 level
- Support of adjacent PM segments in one PXB 4340 AOP
- 128 PM data collection processors shared for up- and downstream direction
- Collection of the following data:
  - Severely errored cell blocks
  - Errored cells
  - Lost high priority cells (CLP0)
  - Total lost cells (CLP0+1)
  - Transmitted high priority cells (CLP0)
  - Total transmitted cells (CLP0+1)
  - Misinserted cells
  - Impaired blocks

Microprocessor Control

- Intel 386EX microprocessor Interface
- Low external processing power required

Technology

- 0.35 µ CMOS, 3.3V
- Plastic BGA-352 package
- Extended temperature range from -40°C to +85°C
- Power dissipation 2.2 W

OAM Functions which are not supported

- Combined Monitoring and Reporting OAM cells for performance monitoring
- Time stamp in Forward Monitoring OAM cells
- Defect type and defect location fields in AIS/RDI cells
- Segment AIS/RDI
- Simultaneous generation of end-to-end and segment FM cells

1.4 Logic Symbol

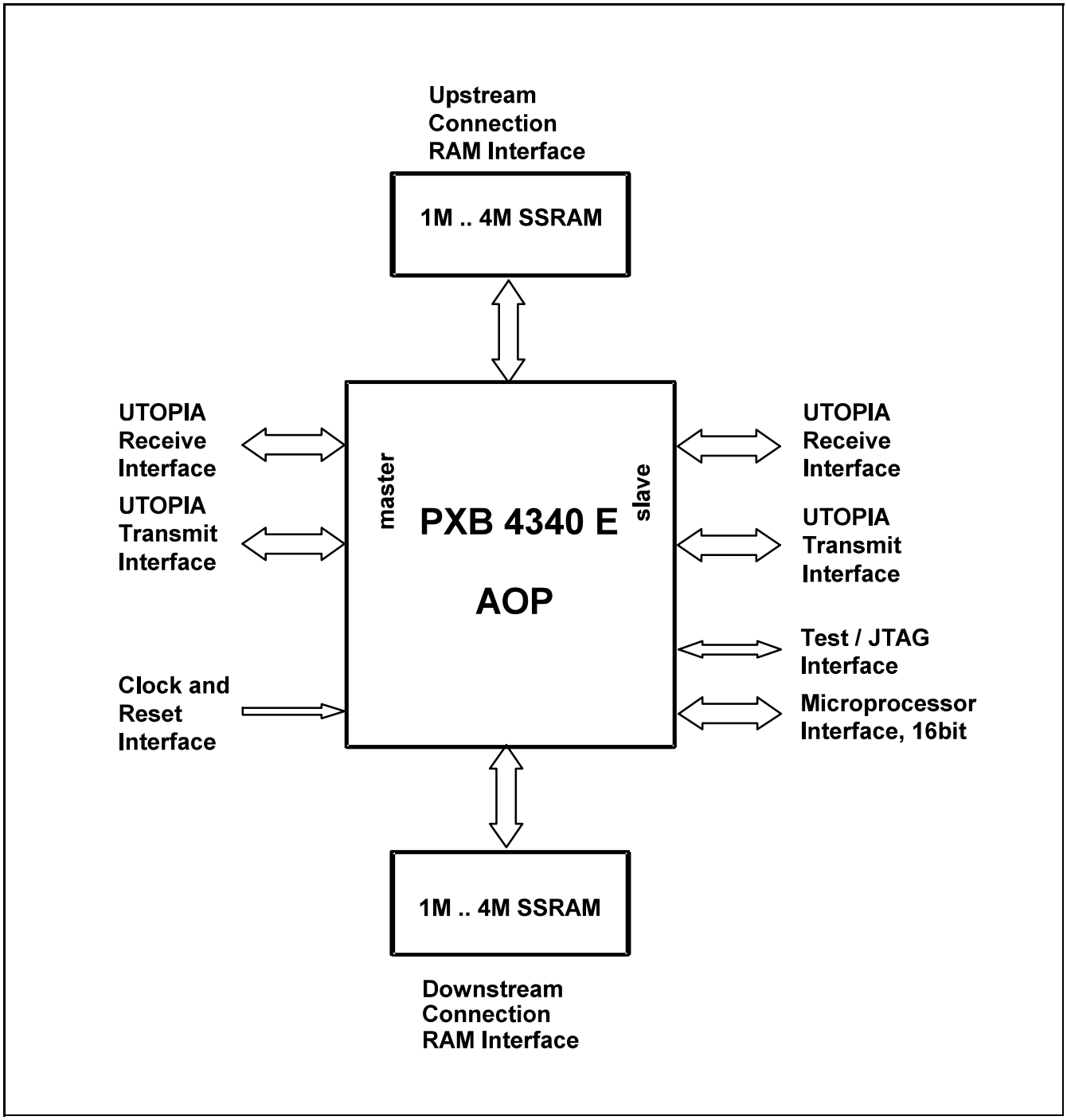


Figure 6 Logic Symbol

1.5 System Integration

The PXB 4340 AOP is located at the ports of a switch so that each ATM cell passes two PXB 4340 AOP devices, one at the ingress port and one at the egress port.

The PXB 4340 AOP assumes that all connections are set-up bi-directional with the same Local Connection Identifier LCI in both directions. In the Infineon Technologies ATM chip set environment (**see figures 1, 2 and figure 3**) the LCI is provided by the PXB 4350 ALP and contains VPI, VCI and PHY information. The PXB 4340 AOP uses pointers to define a connection as VPC or VCC (**see figure 13**); the PHY number is not evaluated. If the PXB 4340 AOP is not used together with the PXB 4350 ALP it can operate on VPI or VCI identifiers only. In these cases the OAM functionality is reduced accordingly.

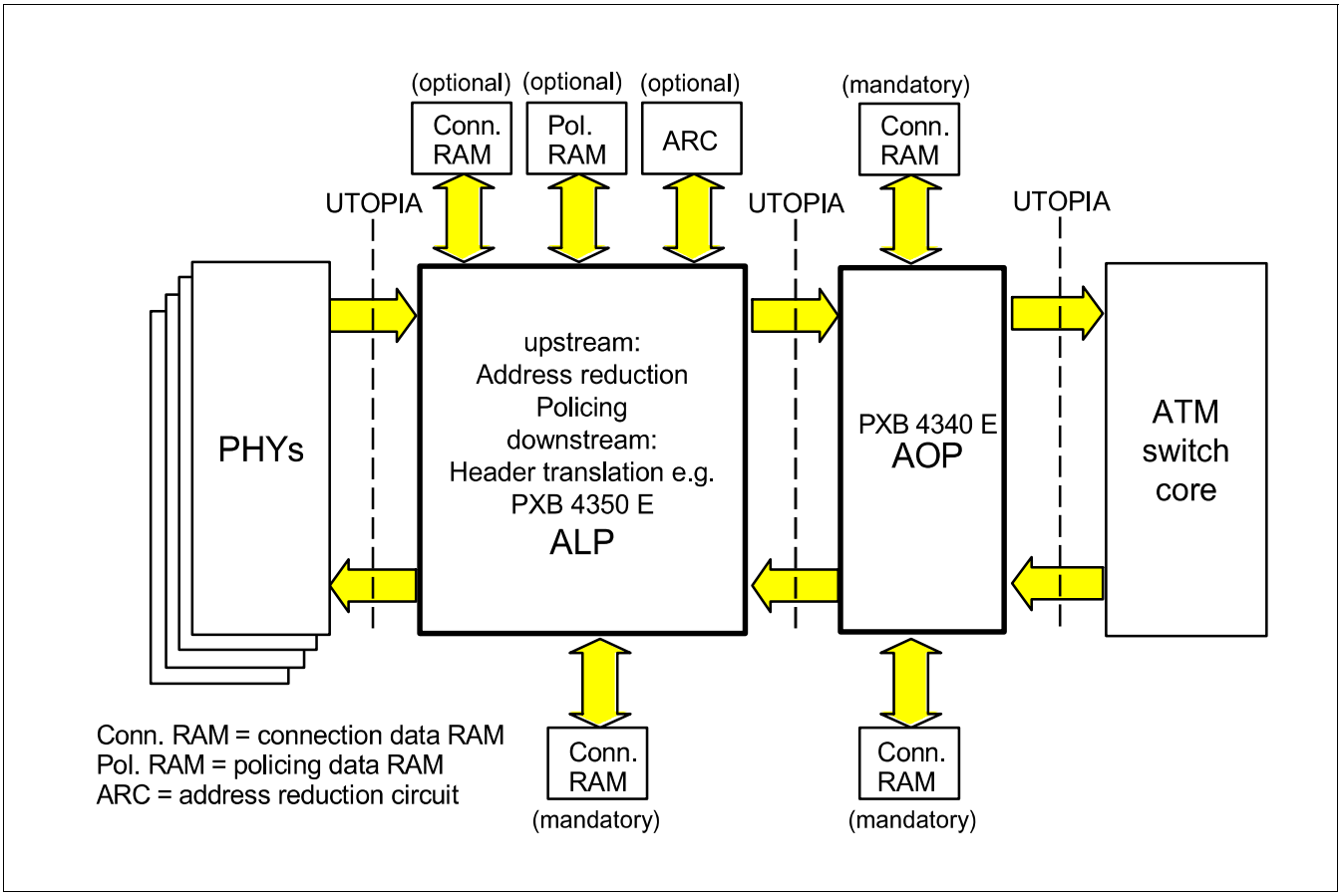


Figure 7 Location of PXB 4340 E AOP on a Switch Port

1.6 Layer Point Concept

This concept is introduced to enable the automatic execution of OAM functions by the AOP. For each connection, VPC or VCC the layer point is configured at connection setup. Then the OAM functions required for this layer point are executed automatically by the AOP. There are 3 different layer points:

- End point EP
- Segment end point SP
- Intermediate point IP

End points and segment end points can be originating or terminating and can belong to a VPC or a VCC; they are referenced as e.g. VPC originating end point VP-OEP or VCC terminating segment point VC-TSP.

As an example a (terminating) segment end point would ignore arriving AIS cells, as AIS cells have always the end-to-end identification. The same layer point would loop arriving forward segment LB cells. **Table 1** gives a coarse overview over the OAM functions executed by the AOP at each layer point. Monitoring functions can be enabled optionally. The details are described with the upstream and downstream external RAM entries.

Table 1 OAM Functionality Determined by Layer Point Configuration

	AIS Cell Insertion Forward non-inclusive Monitoring	RDI Cell Insertion Backward non-inclusive Monitoring	PM Generate Loop Evaluate (De-) Activation	LB Cell Insert Loopback	CC Cell Generate Terminate (De-) Activate	Future OAM Functions [1]
IP	Yes	No Monitor only	Evaluate only	Intra-Domain LB only	No	Yes
SP	Yes	No Monitor only	Yes Segment Cells only	Yes Segment Cells only	Yes Segment Cells only	Yes
EP	Yes (F4 to F5 error propagation)	Yes	Yes	Yes	Yes	Yes

[1] via 2 programmable OAM cell filters with discard/drop/monitor/ignore options

In the following scenarios examples for four layer point configurations are shown. In these figures a switch with its incoming and outgoing port is represented by the symbol shown in **figure 8**.

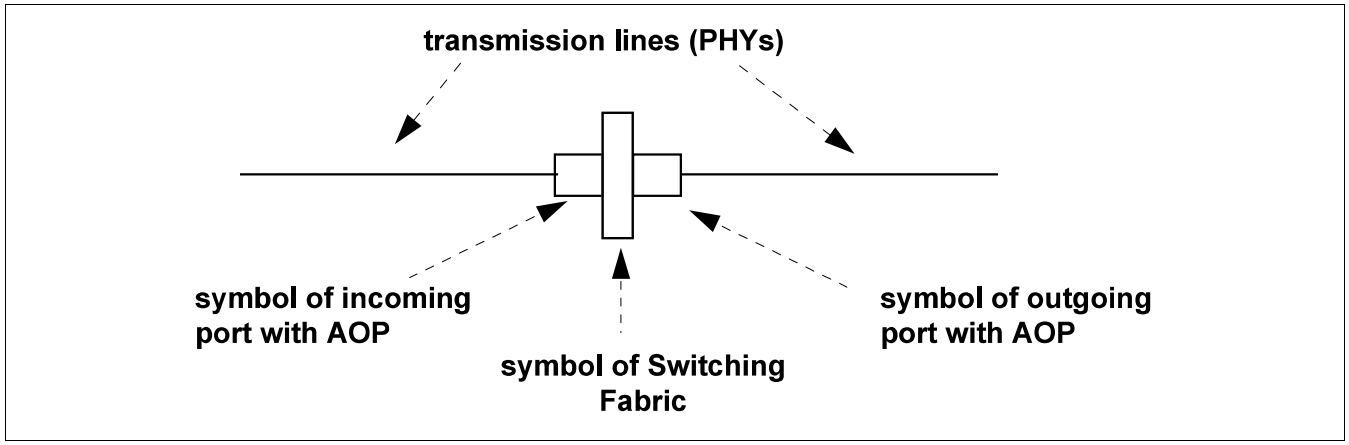


Figure 8 Symbol for Switch with AOPs

The PXB 4340 AOP can be configured according to its location in the network as shown in the following examples.

Within a pure ATM network VPCs may be originated or terminated. In addition VP segments can be originated or terminated as shown in **figure 9**.

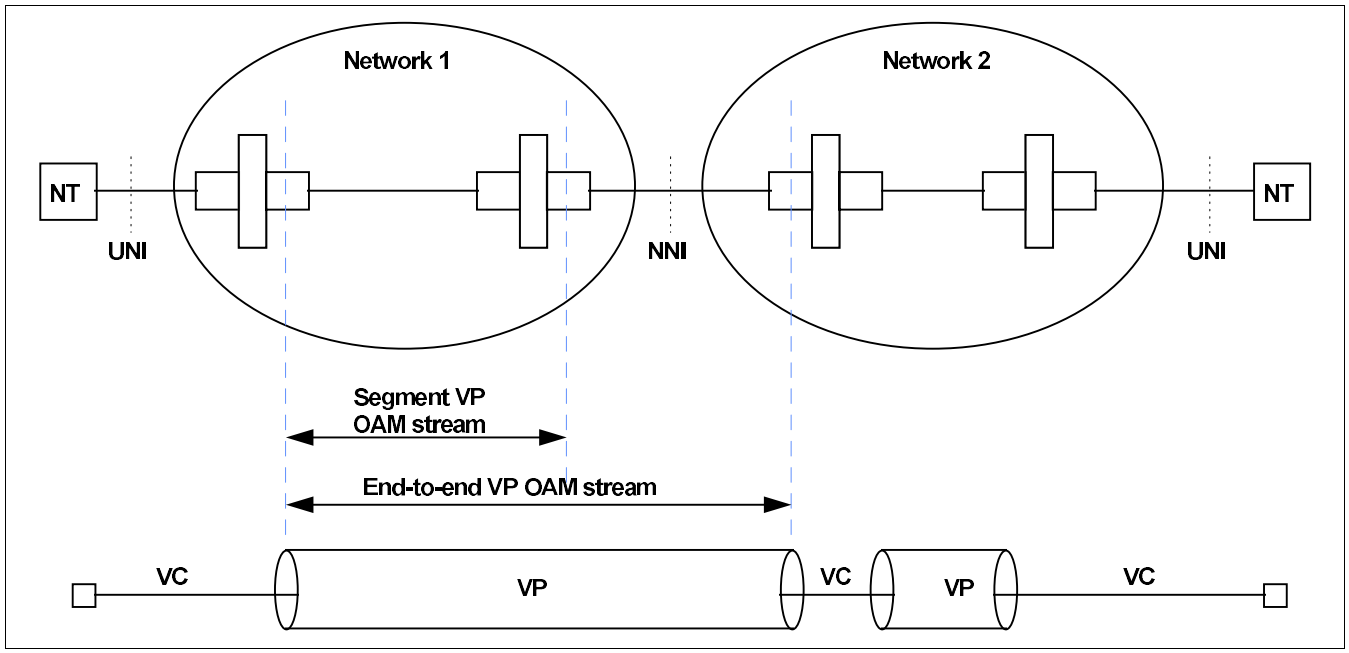


Figure 9 VP Level OAM Functions

As VPCs are always terminated at an ingress port and originated at an egress port, the functionality of the PXB 4340 AOP is restricted accordingly. For example it is not possible to terminate VP-AIS cells at the egress port of a switch. **Table 1** shows an overview over all possible layer points.

VCCs are not originated or terminated within a pure ATM network, but only VC segments (**figure 10**).

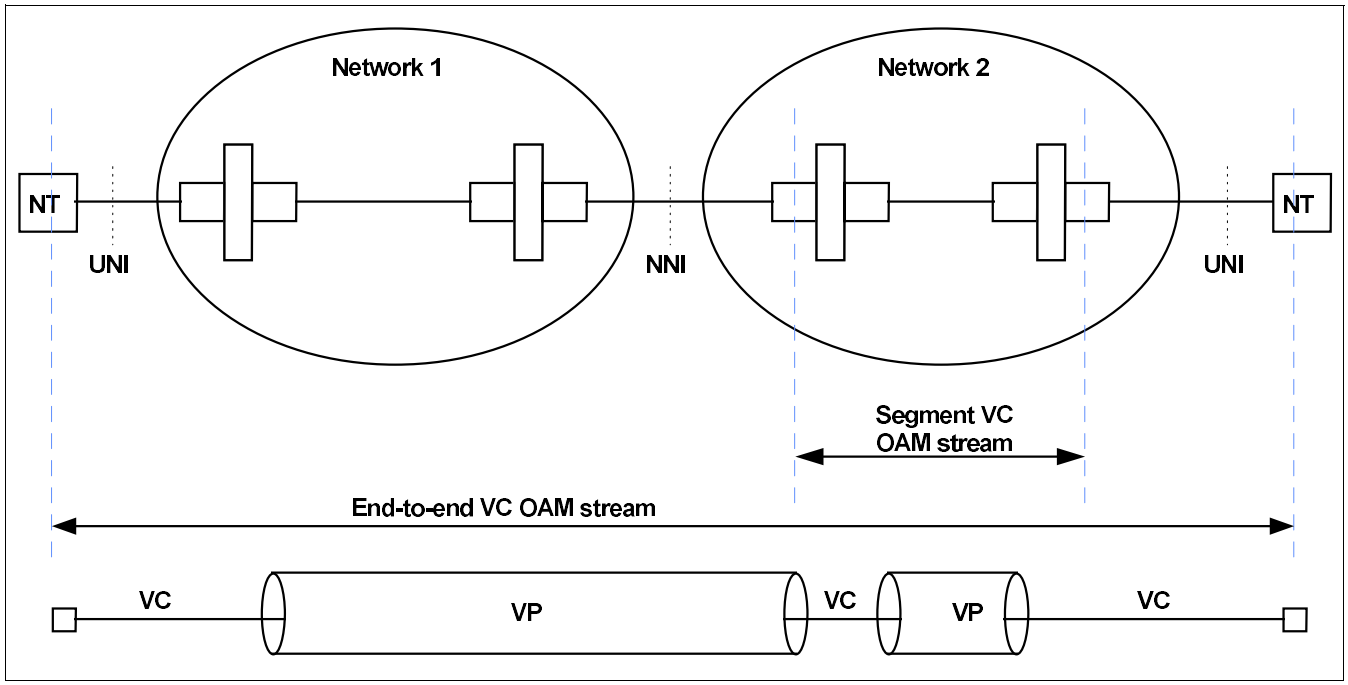


Figure 10 VC Level OAM Functions

In a heterogeneous network containing ATM and non-ATM interfaces VCC origination or termination occurs at the AAL function, as e.g. Circuit Emulation Service (CES) with AAL1 or Segmentation and Reassembly (SAR) with AAL5 as shown in **figure 11.**

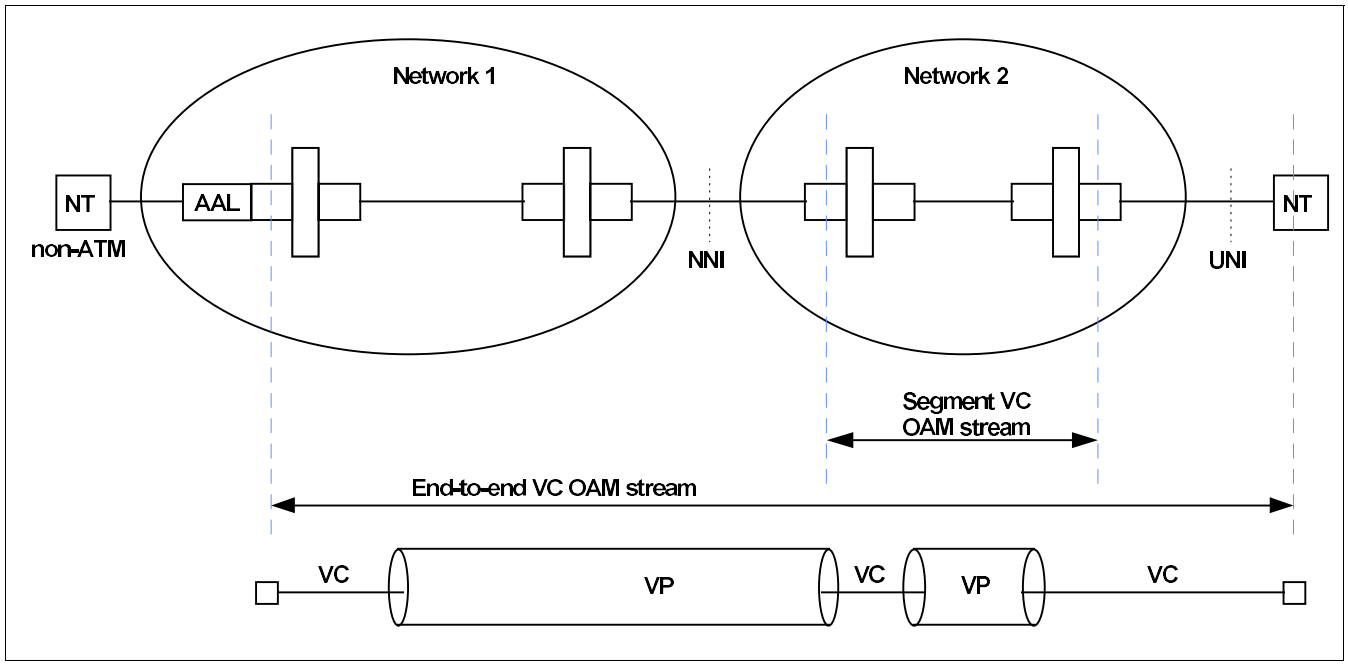


Figure 11 VC Endpoint inside the Network

The PXB 4340 AOP in downstream direction terminates the OAM cell stream just before the AAL device which terminates the ATM connections.

2 Functional Description

2.1 Overview

The PXB 4340 AOP provides full standardized OAM functionality of the ATM layer in one device, covering the functions Fault Management (AIS, RDI, CC, LB) and Performance Monitoring (FM flow, BR flow, Data Collection). It has STM-4/OC-12 equivalent throughput in upstream and downstream direction.

The AIS, RDI, CC mechanism can be applied to a range of up to 16K (=16384) connections. Performance Monitoring can be done for 128 connections simultaneously with each connection selectable from up- or downstream direction. Loopback functionality can be applied to the full range of up to 16K connections (see **section 2.7,** page 27 and **section 2.8,** page 34).

Data cells are transferred via industry standard Level 2, single-port/ multi-port UTOPIA interfaces based on cell level handshake. They can be adjusted for 8-bit or 16-bit data transfer. The ATM side UTOPIA interface is operating in slave mode, the PHY side UTOPIA interface in master mode. The PHY number of a cell is transported transparently through the chip, i.e. a cell input at an UTOPIA receive interface with the PHY number P is output at the corresponding UTOPIA transmit interface with the same PHY number P. Note that the PHY number is not the UTOPIA address, but contains address and handshake line pair information (see **section 5.1**)

Two 32 bit external SSRAM blocks are provided for OAM data storage for each connection. Their size is depending on the number of supported connections (see **section 5.2,** page 139).

Chip control is performed by a standard 16-bit asynchronous microprocessor interface (e.g. for 80386EX). The microprocessor can access the external RAMs any time during operation. This is necessary for connection set up/release, data read/modify/write and configuration adjustment. The external RAM is not memory mapped into the microprocessor address range. Accesses occur via a transfer register set using transfer commands or via DMA (see **section 5.3,** page 141). All functions are supported to a great extent in HW, so that SW effort is minimized.

2.2 Throughput

Data throughput is depending on the chip operating clock SYSCLK, which is used for the chip core and the external SSRAMs. The PXB 4340 AOP needs 32 cycles of the SYSCLK to process one ATM cell. Thus in 32 cycles 64 octets are transported through the chip for a 53 octet ATM cell, giving a penalty of 53/64. Hence the ATM cell throughput is:

ATM cell throughput[Mbit/s] = SYSCLK[MHz] x 16 x 53/64 = SYSCLK[MHz] x 13.25

For a frequency of 51.84 MHz the throughput is 686.88 Mbit/s. The 51.84 MHz are easy to generate, as this is 1/3 of 155.52 MHz, the generic SDH/SONET frequency.

The clock of the UTOPIA interfaces is independent of SYSCLK. It should be less or equal to the SYSCLK frequency. This is not a restriction, as the transfer time for a cell in the UTOPIA interface is only 27 clock cycles.

2.3 Cell Handling

Each cell entering the PXB 4340 AOP via the upstream/downstream receive UTOPIA interface is identified either as user cell or as OAM cell. The chip recognizes all standardized OAM cells and has two programmable comparators for possible new OAM cell types. Data stored on a connection basis in the external RAMs determines if a connection is enabled and which layer point is configured (see **table 27** for all possible configurations). Accordingly the respective function is performed.

- For example a VP-AIS cell would be ignored at a VP segment endpoint.
- As an other example a user cell belonging to a VPC for which end-to-end performance monitoring is enabled is counted and its checksum (BIP-16) is added to the checksum in the AOP located at the VP endpoint.

In the respective OAM processing block new status information is calculated, for example alarm indication bits, BIP-16 checksums, cell counts etc.

Whereas user cells are never modified and are always forwarded, OAM cells can be

- generated and inserted into the cell stream in up- or downstream direction
- extracted from the cell stream and discarded or dropped to the receive cell buffer of the µP
- forwarded with or without modification
- looped back with modification.

For OAM cell generation the PXB 4340 AOP uses the configuration bits of the respective connection to determine the OAM cell type. Therefore it distinguishes between F4 and F5 flow and between segment and end-to-end flow.

When detecting OAM cells the PXB 4340 AOP recognizes F4 or F5 OAM cells for end-to-end or segment. According to the configuration the required actions are performed.

2.4 Cell Buffering and OAM Cell Insertion

The PXB 4340 AOP has four cell buffers located close to the two UTOPIA interfaces in each direction (**figure 12**):

- UTOPIA upstream receive interface: 32 cells, single queue
- UTOPIA upstream transmit interface: 4 cells, single queue
- UTOPIA downstream receive interface: 4 cells, single queue
- UTOPIA downstream transmit interface: 96 cells, shared buffer with 24 queues.

The 4-cell buffers satisfy the needs of the UTOPIA slave handshake at the upstream transmit and downstream receive interface.

The 32 cells wide upstream receive buffer stores incoming user cells during the insertion of OAM cells. OAM cells can be generated or looped from the opposite direction. The PXB 4340 AOP uses forced insertion for all OAM cells. Forced insertion is disabled beyond a buffer filling level which is programmable for upstream direction via register OAMTHRU (see **section 3.7.5,** page 90 and **figure 13**, part a). The OAM cells to be inserted are lost in this case. Also see **table 1** for illustration of the cell handling at the UTPOIA upstream receive interface. When the receive buffer filling level is lower then the threshold the OAM and user cells are processed with the shown priority.

Table 1 UTOPIA priority list[1)]

upstream		downstream	
receive FIFO fill level < threshold	**receive FIFO fill level ≥ threshold**	**utopia transmit FIFO not full**	**utopia transmit FIFO full**
1 BR cell from downstream	1 utopia	1 FM cell insertion	backpressure to adjacent device
2 LB cell from downstream		2 BR cell from upstream	
3 FM cell from downstream		3 LB cell from upstream	
4 scan poll		4 scan poll	
5 scan OAM insertion		5 scan OAM insertion	
6 µP cell insertion		6 µP cell insertion	
7 µP RAM access (RMW)		7 µP RAM access (RMW)	
8 utopia		8 utopia	

1) 1 = highest priority, 8 = lowest priority

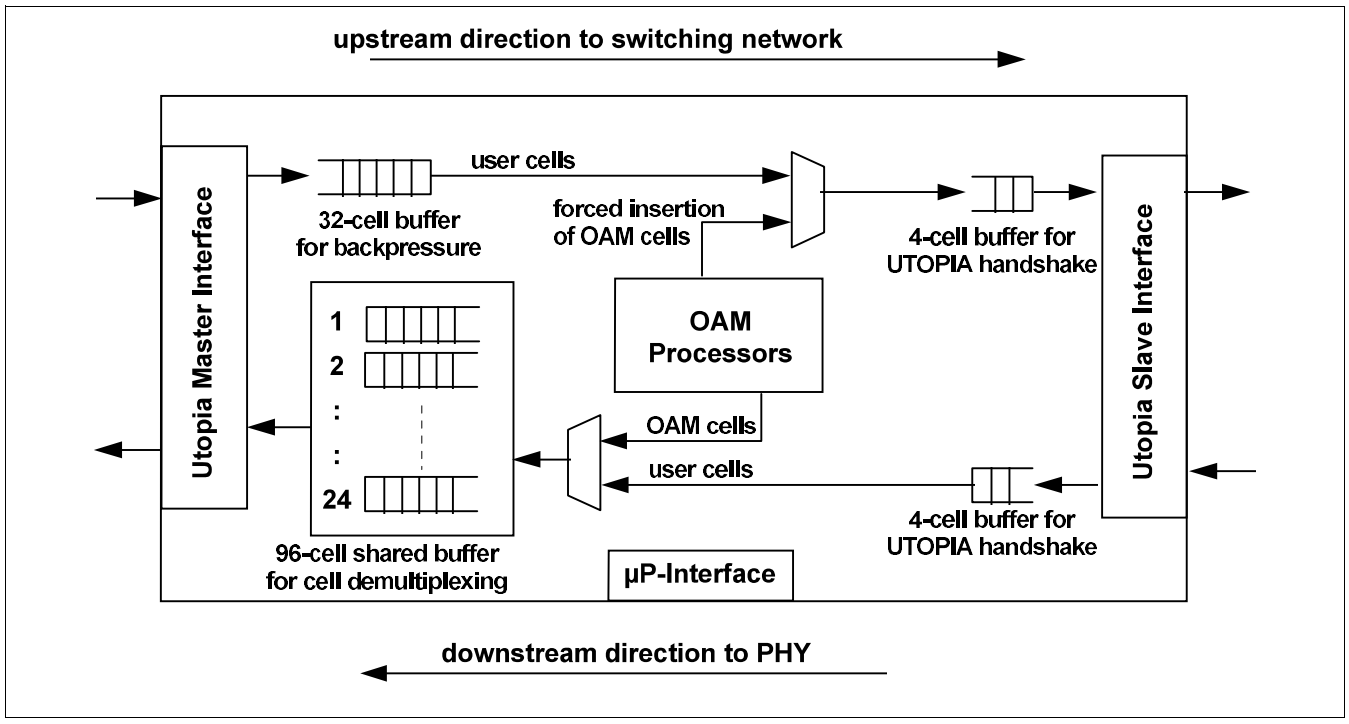


Figure 12 Cell Buffers in PXB 4340 AOP

The downstream transmit buffer also does forced OAM cell insertion by back-pressuring user cells to the downstream receive interface and possibly to the previous chip. It is realized as shared buffer of up to 24 queues, associated to the respective PHYs. The back-pressured user cells are released in bursts of up to 687 Mbit/s when no other cells with higher priority according to **table 1** are present. These bursts must be stored by the downstream transmit buffer and released to the PHYs according to their respective speed.

The downstream transmit buffer has 2 thresholds for each queue:

- the UTOPIA backpressure threshold:
  beyond this threshold the backpressure signal is given to the downstream receive interface for this PHY (see **section 3.7.7,** page 91)
- the OAM cell insertion threshold:
  beyond this threshold the insertion of OAM cells is disabled (see **section 3.7.6,** page 91). As with the upstream receive buffer in this state OAM cells to be inserted are lost.

The two thresholds are identical for all queues. The UTOPIA backpressure threshold should be programmed to a value lower than the OAM cell insertion threshold, this difference guarantees a cell storage space for OAM cells (see **figure 13**, part b).

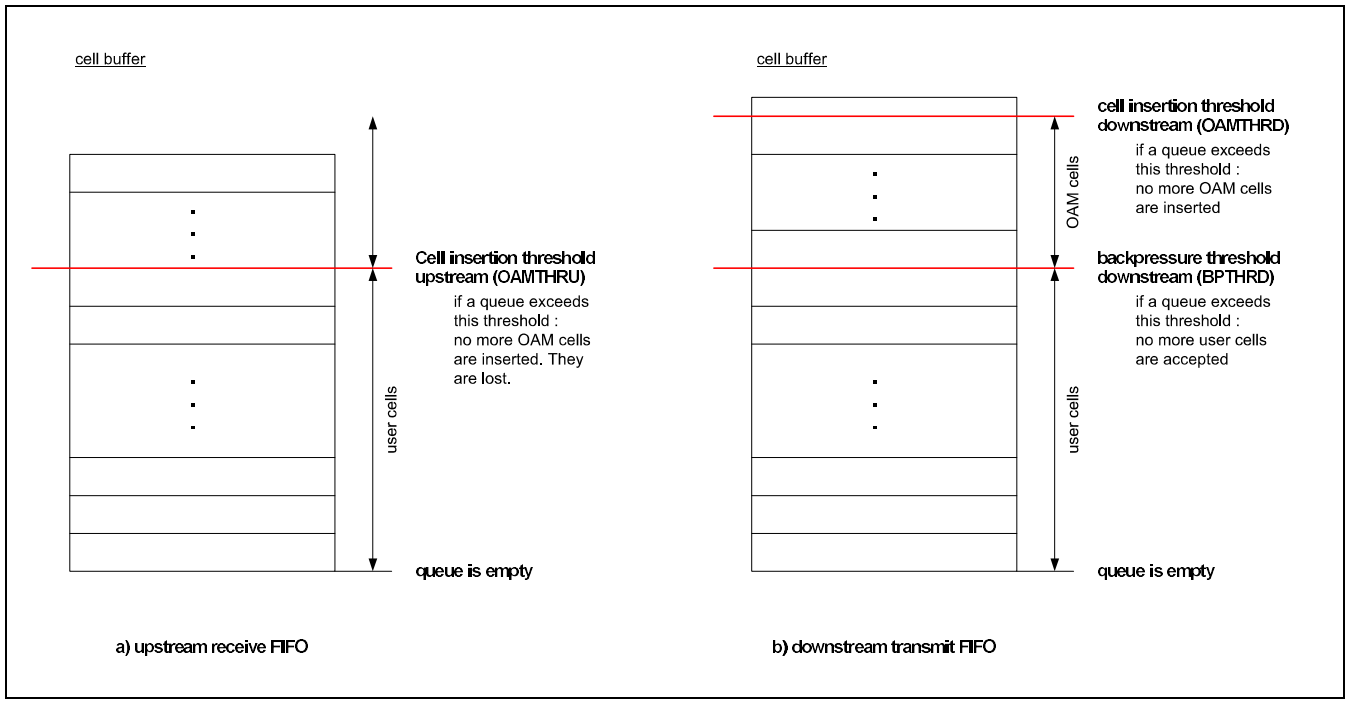


Figure 13 Thresholds in UTOPIA cell buffers

The ATM cell load should be selected by the user in a way that the probability to loosing OAM cells is almost zero (e.g. 10^{-11}). This is done by reserving bandwidth for the inserted OAM cells. OAM cell bandwidth is mainly depending on the selected PM block size (128, 256, 512, 1024). In worst case, when F4 and F5 level PM cell streams are generated, the overhead is still less than 2%.

Lost OAM cells do not lead to system malfunction. If e.g. an FM cell is lost the PM processor continues to count user cells and BIP-16 checksums. The correct values will be sent out with the next block. Thus block size would be e.g. 256 instead of 128 in case of a lost cell. The insertion of AIS/RDI/CC cells will only be halted temporarily during the (very unlikely) case of a buffer overflow. An LB cell to be looped, however, will be lost. Here only the repeat function would help.

2.5 Addressing of external RAMs

The external RAMs for the storage of connection related OAM data are symmetrical in up- and downstream direction. Also the addressing is symmetrical as the LCI values for forward and backward connection are identical. Note that according to the standards each ATM connection is set-up bi-directional, but not necessarily with the same bit rate in both directions.

Both external RAMs are divided into an F4 and an F5 OAM table. Each connection entry has 4 dwords. With the LCI of the cell first the VC-specific table is addressed. Therein an F4 pointer is contained pointing to a VP-specific entry. There are two cases, both depicted in the circle of **figure 14**.

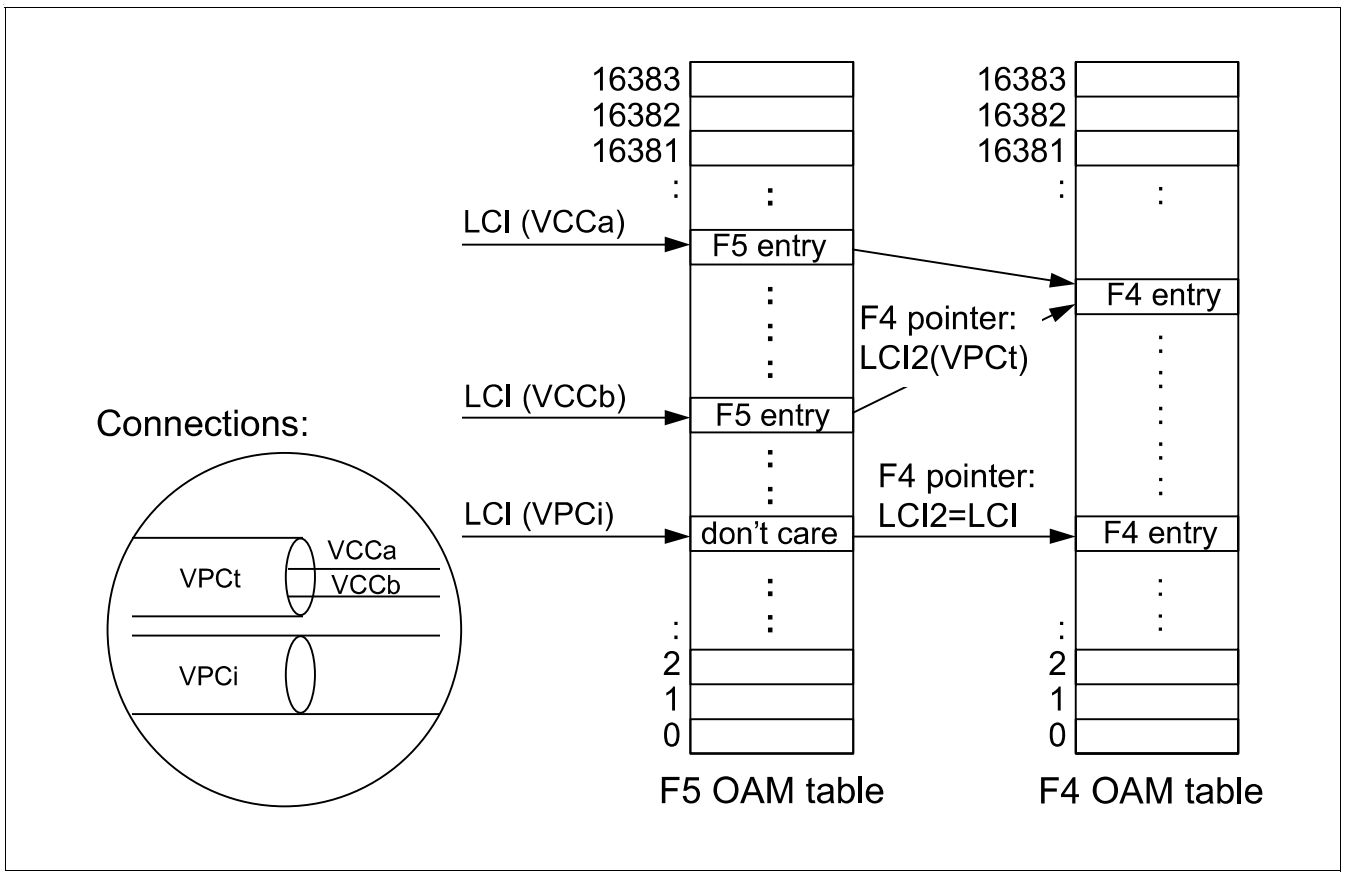


Figure 14 Pointer Structure of up- and downstream OAM Tables

1. A VPC intermediate point
   In this case the F5 entry is "don't care", except some common fields. See e.g. VPC_i in **figure 14**. The VP-specific entry contains the OAM data for the VPC.
2. A terminated VPC decomposed into VCCs
   In this case each VCC has an F5 entry with identical F4 pointers pointing all to the same F4 entry. See e.g. VCC_a and VCC_b of VPC_t in **figure 14**.

2.6 OAM Functions Overview

There are two groups of applications for OAM functions: alarms and measurements. Alarm functions inform users and network operators about network failures. These include the OAM functions

- Alarm Indication Signal (AIS)
- Remote Defect Indication (RDI)
- Continuity Check (CC).

AIS and RDI are used to convey transmission line failure information to subscriber and network operator; CC detects ATM layer failures.

As failure events are unpredictable the alarm supervising HW is always running. When a failure occurs the notification process starts automatically.

Measurements are initiated for diagnosis purposes by the network operator. Therefore these functions do not need to be active permanently for all connections. The respective OAM functions are:

- Loopback LB
- Performance Monitoring PM

LB checks the connectivity of a connection by sending a single cell which is looped back at predefined points. LB is used e.g. immediately after connection set-up or periodically to check all permanent connections of a network using end-to-end or segment LB. A network operator could also use intra-domain LB to localize a failed link. Another option for loopback are subscriber initiated loops either end-to-end to the partner or access line LB to the first node in the network.

PM is a more precise tool than LB. It checks not only the connectivity, but the real performance of a connection in terms of bit failures and cell losses. As it requires complex HW support and SW performance PM will not be activated permanently for all connections. E.g. VPCs or permanent VCCs could be monitored if a subscriber pays for this service. Also a network operator would use PM to check the quality of a connection if a subscriber complains about it.

2.7 Alarm OAM Functions (AIS/RDI/CC)

There are two types of failures detected by the alarm functions: transmission line failures and ATM layer failures. Transmission line failures are e.g. line brakes, failures of lasers or failures of reception diodes. Typical ATM layer failures are the misrouting of cells in the switching fabric or a falsified entry in a routing table. In this case all cells of a connection are forwarded to a wrong destination.

2.7.1 Transmission Line Failures (AIS/RDI)

Transmission line failures are recognized by the receiving PHY and conveyed to the PXB 4340 AOP by the on-board control processor. It is sufficient to set one single bit for the respective PHY to initiate the periodic insertion of AIS cells for all affected connections. In the external RAM entry a bit CARIEN exists for F5-AIS and a bit PARIEN for F4-AIS (for CARIEN see **section 3.9.1.2,** page 100, for upstream and **section 3.9.3.2,** page 112, for downstream; for PARIEN see **section 3.9.2.2,** page 107, for upstream and **section 3.9.4.2,** page 118, for downstream). When these bits are set to ’1’, the insertion of AIS cells is enabled. Note, that no F4 OAM/User-Flow is supported if the LCI-Mode "10" in register UTCONF1 is selected (see **section 3.7.2,** page 88). Further the bit DISF4 and DISF5 in the external RAM entries have to be set to ’0’ to enable the

F4/F5 processing (see **section 3.9.1.1,** page 98, **section 3.9.3.1,** page 110, for DISF5 in up- and downstream direction; **section 3.9.2.1,** page 105, **section 3.9.4.1,** page 116, for DISF4 in up- and downstream direction). Otherwise all F4/F5 cells are discarded at the receiving point. The PXB 4340 AOP automatically inserts VP-AIS cells for VPCs and VC-AIS cells for VCCs. **Figure 15** shows that this case occurs at the incoming port of a switch.

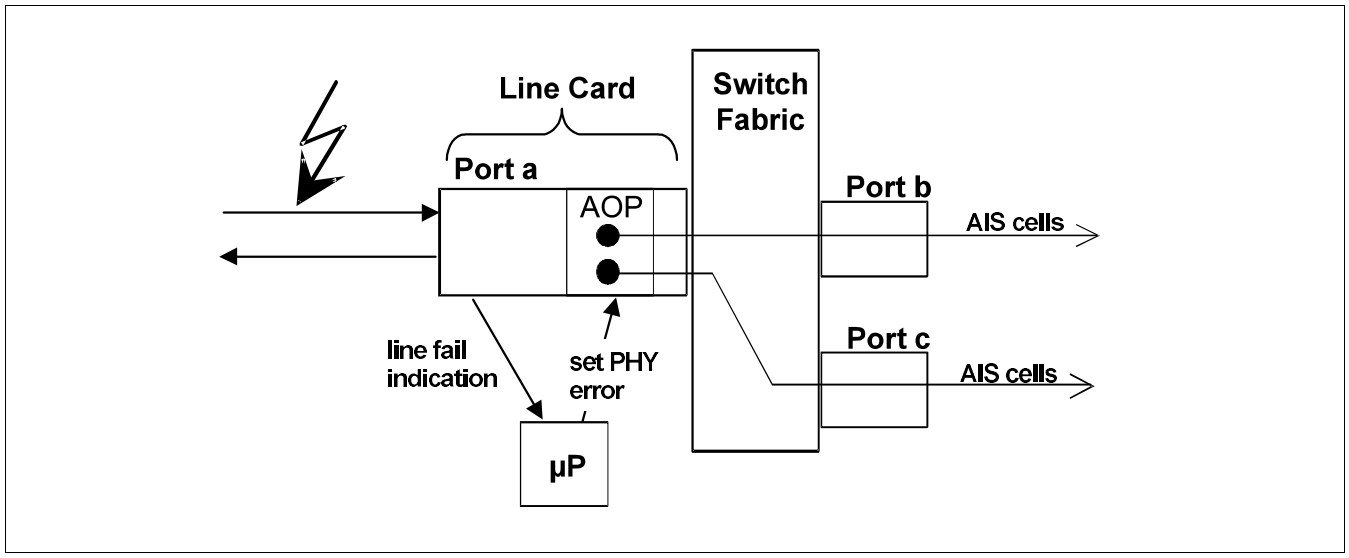


Figure 15 Example for Line Failure Notification via AIS cells

The generated VC-AIS cells travel up to the endpoint of the connection, which normally is the user terminal. Thus within a very short time delay - determined by the control processor's response time, the PXB 4340 AOP insertion delay and the cell transfer time - the user is informed about the failure.

The generated VP-AIS cells travel up to the VP terminating endpoint which normally is within the network. At the VP terminating endpoint - which is always at the incoming port of a switch - VC-AIS cells must be generated for all VCCs contained in the VPC. Again, all affected user terminals are informed.

The PXB 4340 AOP automatically performs the following actions when receiving VP-AIS cells at a VP terminating endpoint (see **figure 16**):

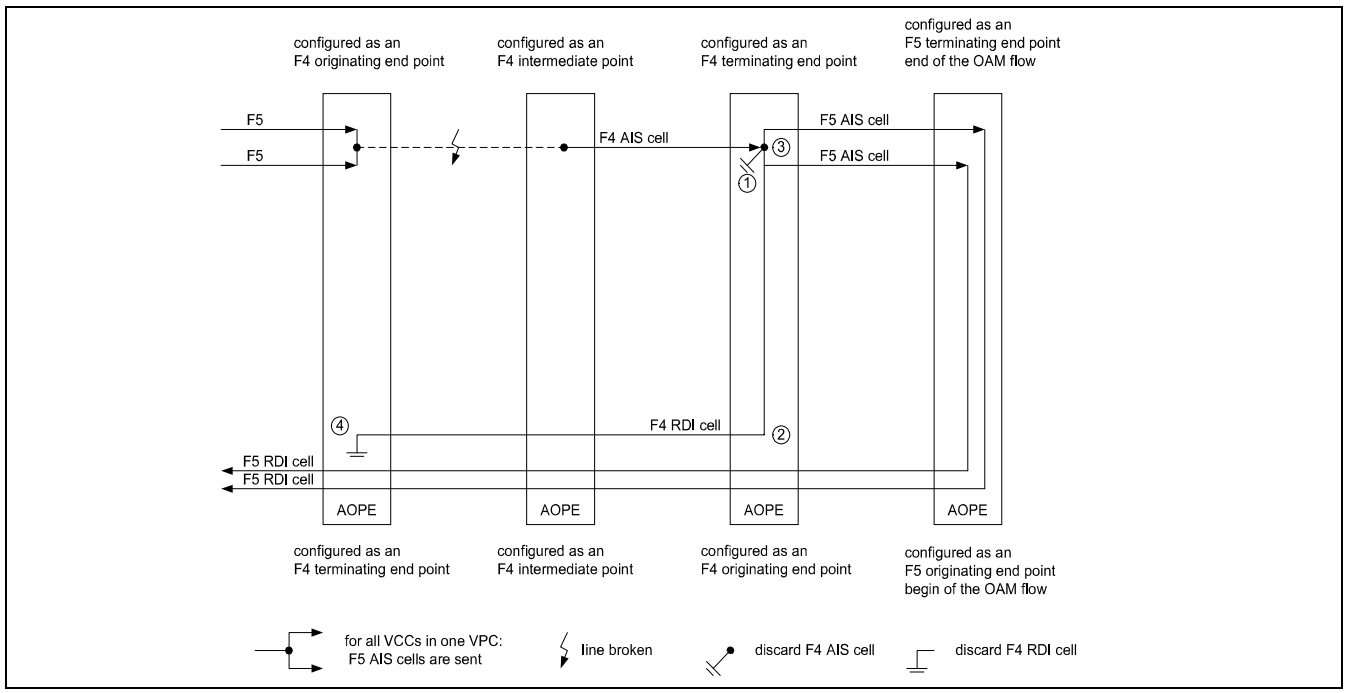


Figure 16 VP-AIS/RDI-Flow (F4-AIS/RDI-Flow)

- Discard of VP-AIS cells (see **figure 16**, marker ①)
- Execution of the (VP-)AIS state diagram shown in **figure 17** for the respective VPC.
- Insertion of VP-RDI cells in backward direction. This informs the originating endpoint of the VPC about the failure. RDI makes sense in cases where the failure of the line affects only one direction. The automatic RDI generation in backward direction assumes bi-directional connections with the same identifier (LCI) in both directions (see **figure 16**, marker ②).
- Insertion of VC-AIS cells in forward direction for each VCC of this VPC. This informs all users sharing this VPC about the failure in the network (see **figure 16**, marker ③).
- Declaration of AIS/RDI **failure** states after 3.5 seconds (standard) persistence of AIS defect state. The cell insertions continue unaffected.

At the originating endpoint of the VPC the following actions are perfomed:

- Discard of VP-RDI cells (see **figure 16**, marker ④)
- Execution of the RDI state diagram shown in **figure 18**.
- Declaration of RDI failure state after 3.5 seconds (standard) duration of RDI defect state.

The AIS state diagram executed at the sink endpoint of a connection is shown in **figure 17**. Note that in accordance for the anomaly-defect-failure mechanism only transitions to and from failure state are notified to the microprocessor. This avoids unnecessary interrupts.

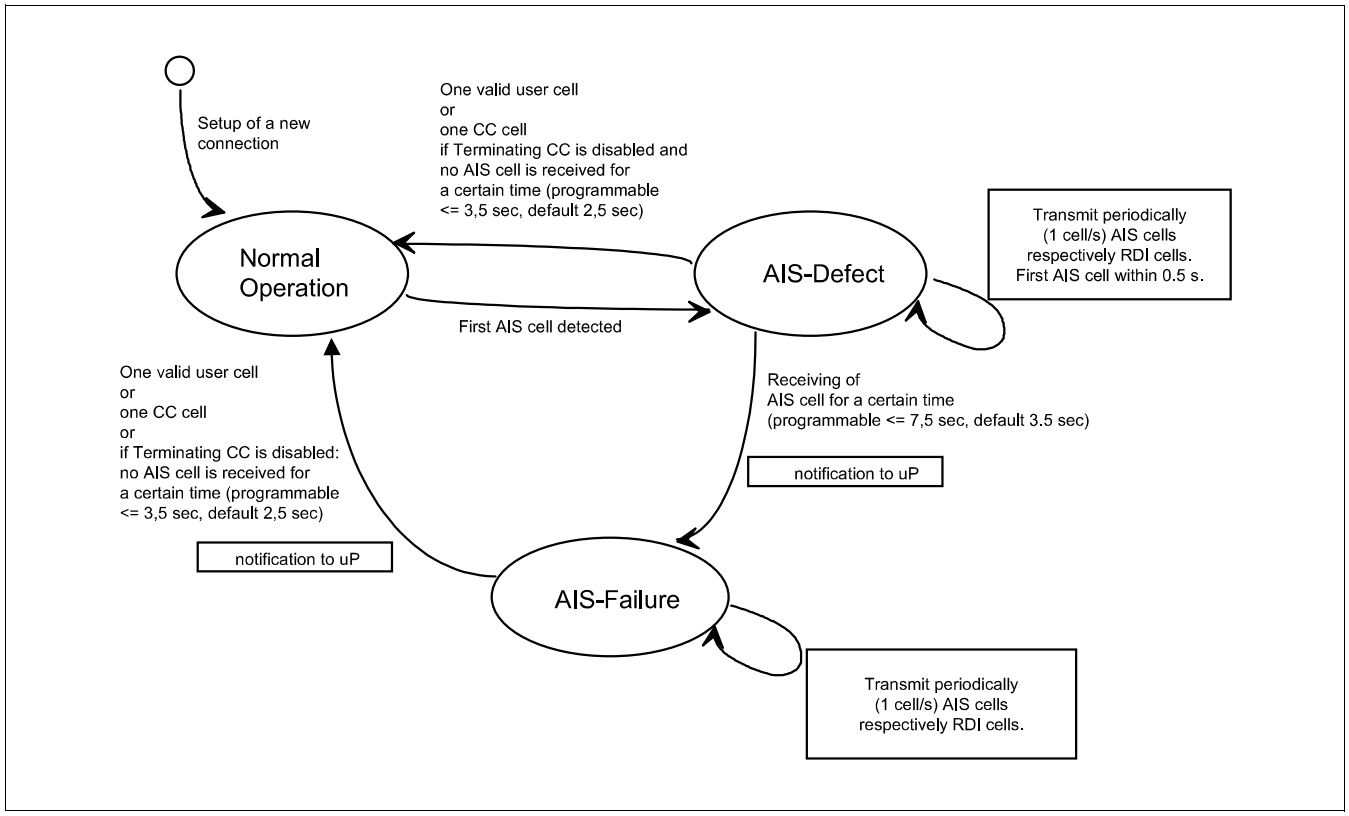


Figure 17 AIS State Diagram

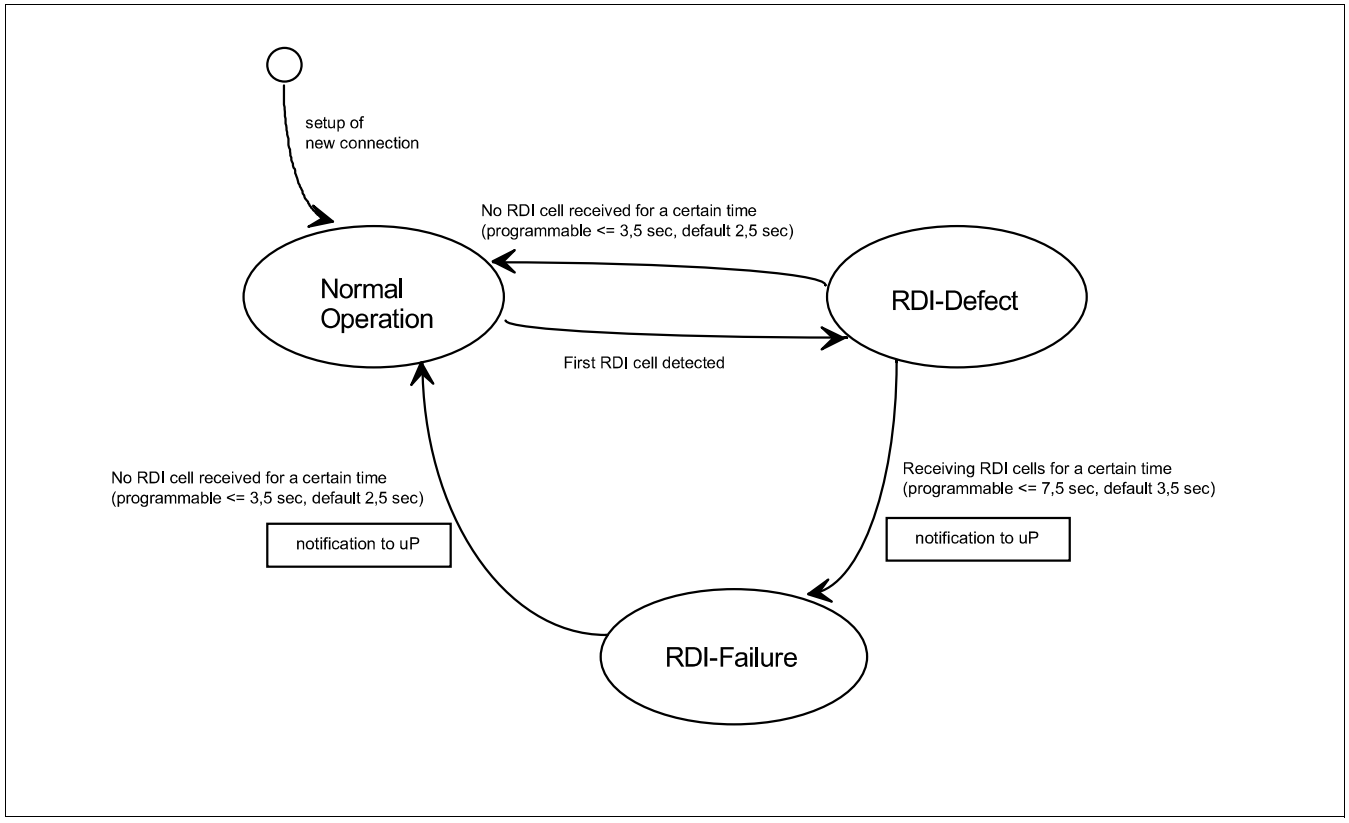


Figure 18 RDI State Diagram

The actual F5-AIS/RDI state is indicated by bits 14..19 in Dword2 of the downstream external Ram entry (**section 3.9.3.3,** page 114) and the upstream external RAM entry (**section 3.9.1.3,** page 102). For the actual F4-AIS/RDI state information use bits 22..27 in Dword4 of the downstream external RAM entry (**section 3.9.4.1,** page 116) and the upstream external RAM entry (**section 3.9.2.1,** page 105). The µP is informed by the interrupts DCSTTR for downstream F5, UCSTTR for upstream F5, DPSTTR for downstream F4 and UPSTTR for upstream F4 state transitions (**section 3.6.1,** page 83).

Both forward and backward cell insertions are initiated by the SCAN mechanism (see **section 2.15**). All delay times given are default values, recommended by **[6]**. The PXB 4340 AOP allows to program these values in multiples of the 0.5 second SCAN period given by the microprocessor. Therefore consider the register description of SCCONF1 (see **section 3.5.10,** page 79).

The 0.5 second SCAN period determines the insertion delay for OAM cells. If the SCAN mechanism has passed a connection entry just before an AIS condition became true the maximum waiting time for the next SCAN access is about 0.5 second.

2.7.2 ATM Layer Failures (CC)

The mechanism to detect failures like misrouting is the Continuity Check (CC). Its idea is to insert dummy cells in a connection if it is inactive, i.e. if the user is not sending data cells. The dummy cells are called CC OAM cells and are inserted at the originating end/segment point of a connection after a one second absence of user cells. The repetition interval is also one second. At the connection/segment endpoint the CC cells are discarded. If no user or OAM cells are received within 3.5 seconds the Loss of Continuity (LOC) defect state is declared. Like AIS state LOC causes the automatic insertion of VP-AIS or VC-AIS cells for the affected connections. If LOC is detected at a terminating endpoint RDI cells are generated in backward direction.

Figure 19 shows an example for the operation of CC: two VCCs entering a switch at ports a and b should both be forwarded to port c. Due to misrouting within the switching fabric the cells of VCC b are forwarded to an unconnected switch output, where they are lost without being notified. The CC detection function at port c, however, detects the absence of user cells after the 3.5 seconds time-out and inserts VC-AIS cells for connection b.

The time values given are values recommended in [6]. The PXB 4340 AOP allows to progam them in a wide range.

The PXB 4340 AOP supports the CC function for all 16384 connections in both up- and downstream direction. Setting one bit in the respective connection RAM is sufficient to activate the origination or the termination of a CC flow. This is bit 11 in Dword1 (up-/downstream) for originating F5 segment CC, bit 10 in Dword1 (up-/downstream) for originating F5 end-to-end CC and bit 11 in Dword4 (up-/downstream) for originating F4 segment CC (see **section 3.9,** page 98). All other actions are automatic:

At the CC origination point (see **figure** and **figure 21**):

- continuous supervision of user cell stream (see **figure** , marker ①)
- periodic insertion of CC cells in one second intervals after one second (standard) time-out (see **figure** , marker ①)

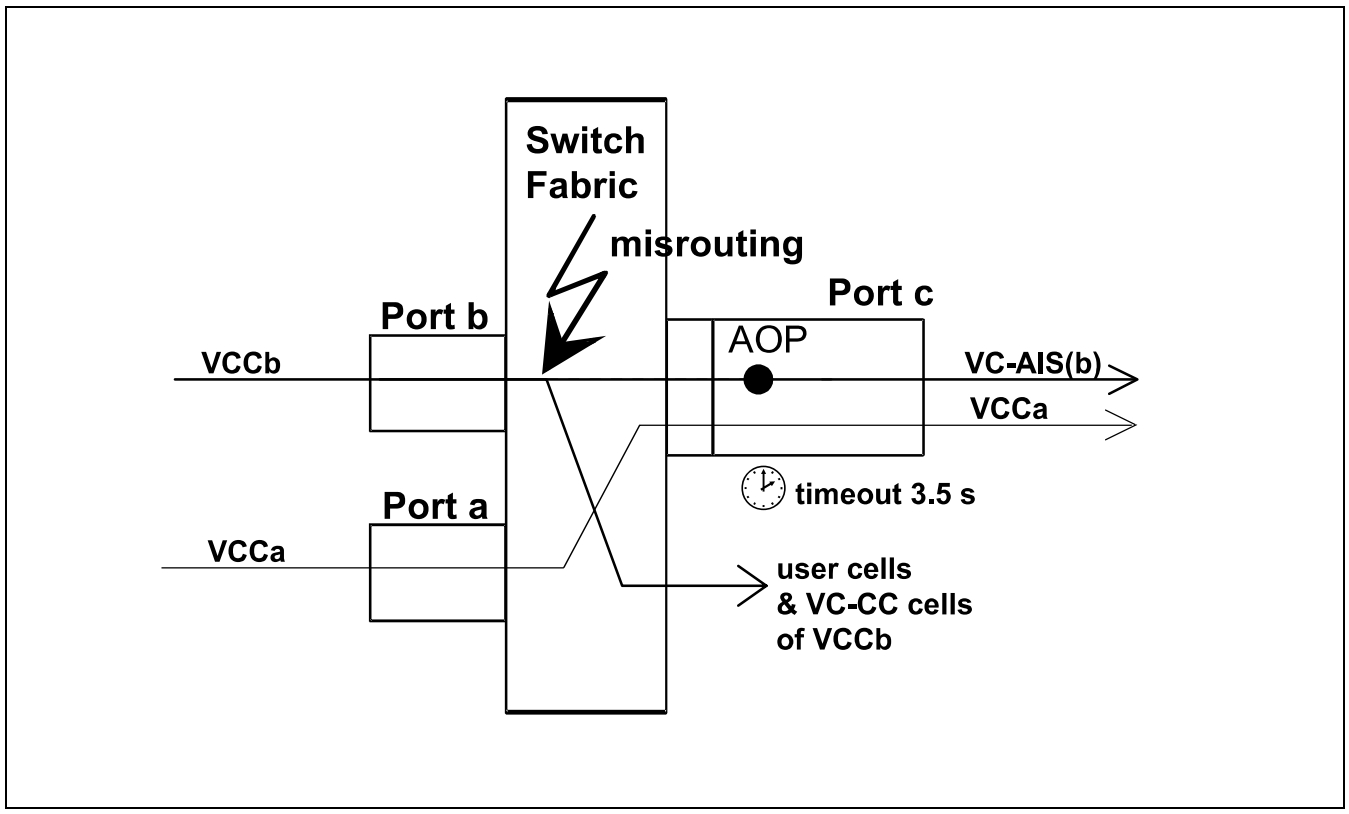


Figure 19 Example for Misrouting Failure Detection

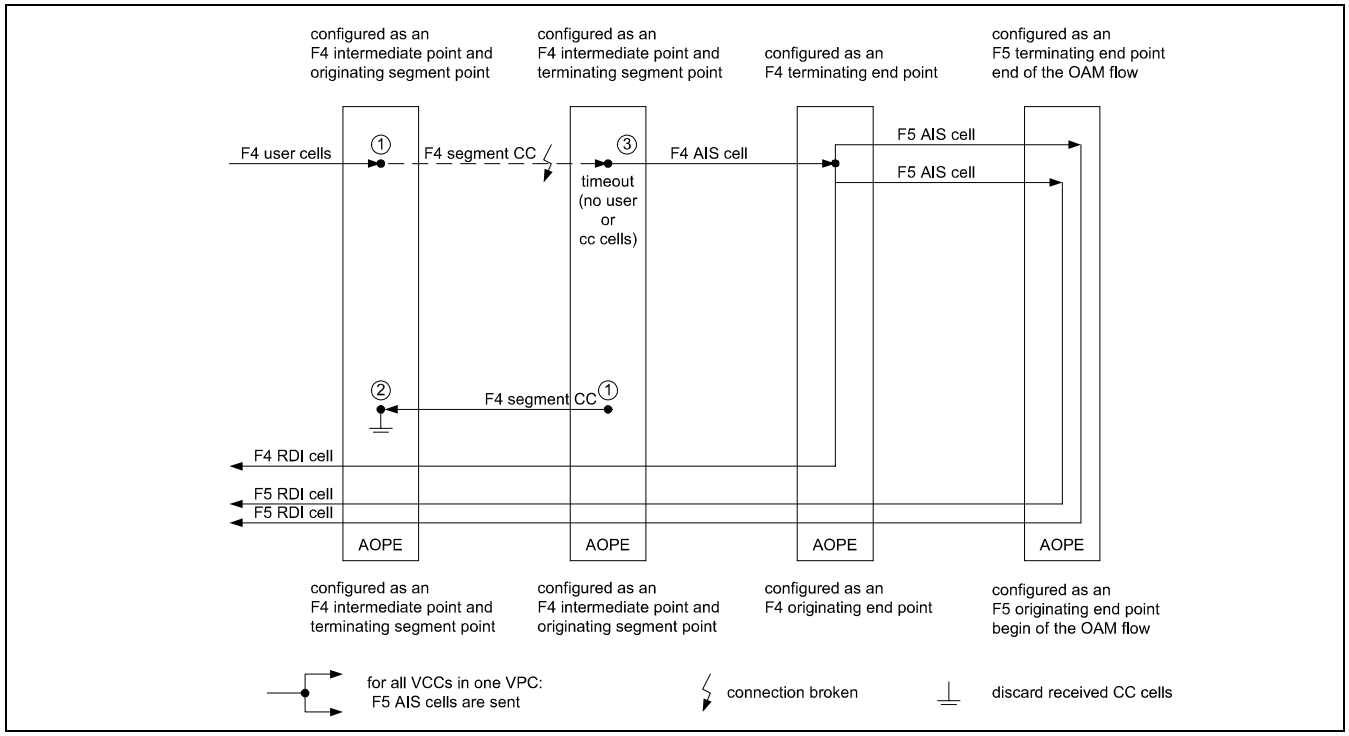


Figure 20 F4 segment CC Flow

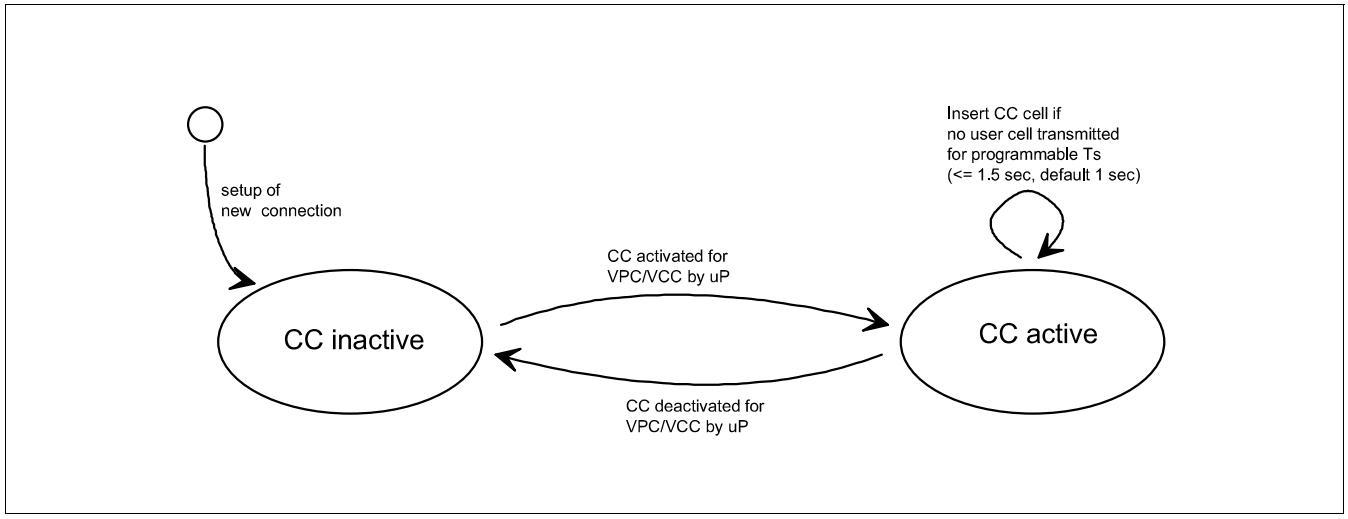


Figure 21 Continuity Check Cell Generation State Diagram

At the CC termination point (see **figure 22**):

- discard of CC cells (see **figure** , marker ②)
- declaration of LOC **defect** state and insertion of AIS cells in one second intervals after 3.5 seconds absence of user or OAM cells (see **figure** , marker ③)
- declaration of LOC **failure** state if LOC defect state persists for 2.5 seconds.

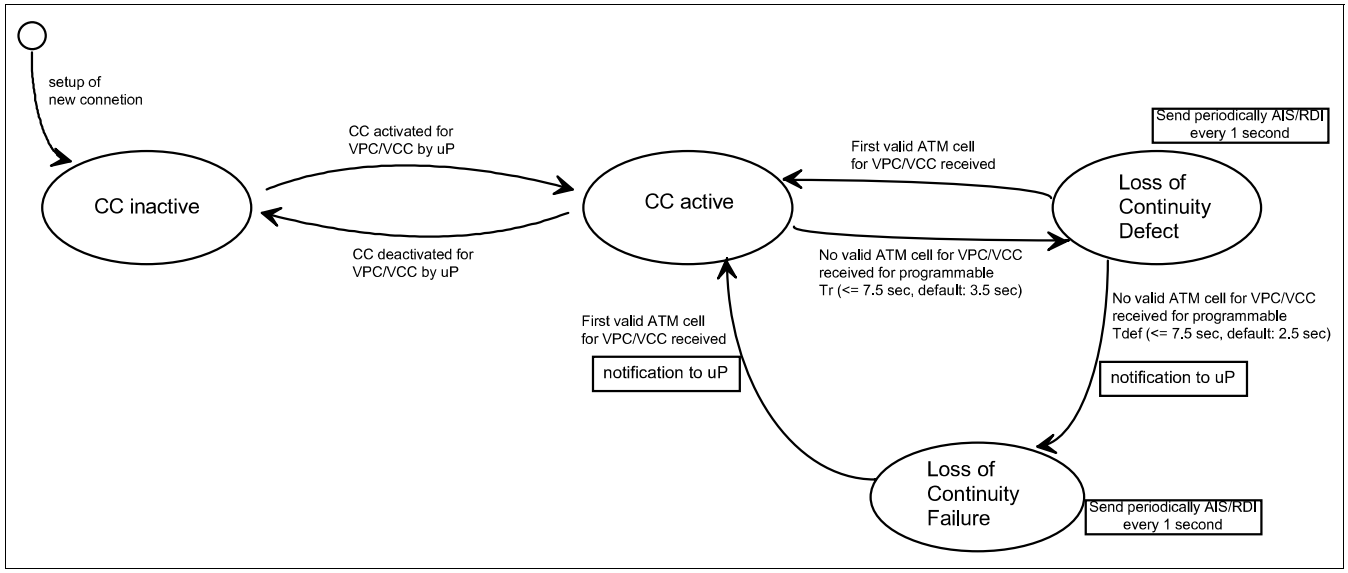


Figure 22 Continuity Check Evaluation State Diagram

The LOC failure state is notified to the control processor, while still AIS cells are automatically generated. This additional filtering according to the standards avoids frequent notifications to the microprocessor due to sporadic errors (see bits 3..0 of register ISR0, **section 3.6.1**).

All cell insertions are initiated by the SCAN mechanism (see **section 2.15**). The delay times given are default values, recommended by I.610 [**6**]. The PXB 4340 AOP allows to program these values in multiples of the SCAN frequency which in turn is given by the microprocessor. The corresponding register is named SCCONF0 (see **section 3.5.9,** page 78).

To further limit the load for the microprocessor the DMA function is provided which transfers relevant status bits for all connections to the control processor memory in the background (see **chapter 2.15**).

The insertion of AIS cells occurs as in the AIS state (**chapter 2.7.1**), i.e. with periodic insertion of VP-AIS or VC-AIS cells and VP-RDI cells in backward direction. No additional AIS cells are inserted if AIS and LOC state are declared simultaneously.

Additionally to the standardized CC an Internal Continuity Check ICC is provided as proprietary function. It uses CC cells with a specially marked header (see **section 8.2.4**) between incoming and outgoing port. If no AOPE Continuity Check is active a network element ICC can be activated in order to check the connectivity across the switching network between AOPE upstream and AOPE downstream. The functionality of ICC does not differ from the AOPE CC since a received ICC cell is treated like a CC cell, i.e. the same checkers/generators which otherwise do CC processing are used for ICC with the following consequences :

- insertion of ICC cells in the upstream direction of the AOPE (originating point) if no valid user cell has been received for a specified time interval of one second.
- supervision of arrived user cells or ICC cells at downstream direction of the AOPE (terminating point) within a specific time interval of 3.5 +/- 0.5 seconds.
- Loss of ICC cells in downstream direction of the AOPE will result in AIS/RDI generation as described in **section 2.7.1**. The AIS/RDI generation is adjustable via VPC/VCC.

ICC can be activated by software for each valid VPC/VCC.

ICC cells are distinguished from CC cells by the HK bits (HK=100) in the UTOPIA cell header (UDF1 field). For ICC segment CC cell format is used. If evaluation of the UDF1 field is not enabled, ICC is not supported.

For ICC the VP/VC segment configuration flags are not relevant. Therefore 3 ATM layer configuration cases for upstream cell generation are remaining :

- generation of VP ICC cells at VP intermediate points
- geneartion of VC ICC cells at VC originating end points
- generation of VC ICC cells at VC intermediate points

For downstream evaluation are remaining :

- evaluation of VP ICC cells at VP intermediate points
- evaluation of VC ICC cells at VC terminating end points
- evaluation of VC ICC cells at VC intermediate points

ICC cells never leave a switch while ICC is intended for connection supervision within a switch.

2.8 Network Connectivity Check (LB)

2.8.1 General

The loopback (LB) OAM function is intended for checking the connectivity of a virtual connection by sending a single LB cell along the connection. The LB cell is extracted at well defined points of the network and sent back to the source via the backward connection. Note that each ATM connection has an associated connection in backward direction with the same connection identifiers.

There are three possibilities for specifying the loopback point of an LB cell:

- End-to-end LB processing
- Segment LB processing
- End Point LB processing

The loopback function determines which loopback activities are executed dependent on ATM layer configuration of the network element (originating segment/end point, terminating segment/ end point, intermediate point) and the received F4/F5 LB cell at the AOPE (upstream, downstream). Loop of LB cells including reset of the LB indication bit in the cell is done without microprocessor interaction at the respective segment or connection end points. The VPC consistency flag (see **section 2.8.1.4,** page 39) indicates the availability of the VPC to the microprocessor at the loopback port.

The loopback processing selects the loopback actions dependent on the loopback state and the loopback location/source ID flag of the F4/F5 flow and the content of the received F4/F5 LB cell payload (LB indication, LB location ID, LB source ID) at the AOPE (upstream or downstream). The evaluation of the LB location/source ID of the LB cell payload is switchable via the LB location/source ID flag. The correlation tag of the LB cell payload is supported by SW.

If the connection is in loopback state (LB state = 1) then an LB cell can be copied or dropped from cellstream into the cell buffer of the µP.

If the LB location/source ID flag is set a compare has to be done between the LB location/source ID and the network element ID (see **section 3.9,** page 98).

At the originating segment/end point, the F4/F5-LB cell can be inserted into the cellstream in upstream or downstream direction. The insertion of the LB cell is done by SW via the transmit cell buffer of the µP (see marker ① in **figure 23**, **figure 24** and **figure 25**). If a looped F4/F5 LB cell arrived at the originating segment/end point, this cell is dropped to the cell receive buffer of the µP (see marker ④ in **figure 23**, **figure 24** and **figure 25**).

Cell insertion and extraction functions are described in **section 2.16,** page 49.

The ATM layer configuration, the loopback state of a connection and the LB location/source ID flag are VP and VC connection specific data. This data is located in external RAMs for upstream and downstream direction (see **section 3.9,** page 98).

Note that the automatic loop function assumes identical connection identifiers for both forward and backward connections.

2.8.1.1 F4/F5 End-to-End Loopback Processing

If the LB indication bit of an LB cell is equal to 1 the LB cell is forwarded to the terminating end point. At the terminating end point the LB indication flag is set to 0 and the LB cell is looped back (loopback point, see **figure 23**, marker ②).

If the LB indication is equal to 0 (LB cell already looped) and the connection is in LB state (LB state = 1) and the LB source ID of the LB cell is equal the network element ID (LB source ID match) then the LB cell is copied to the receive cell buffer of the µP and the LB cell is also forwarded to the terminating end point (see **figure 23**, marker ③).

If the LB source ID flag of this connection is disabled the same loopback actions are done.

If the connection isn't in LB state (LB state = 0) or an LB source ID mismatch occurs the LB cell is forwarded to the terminating end point (see **figure 23**, marker ⑤).

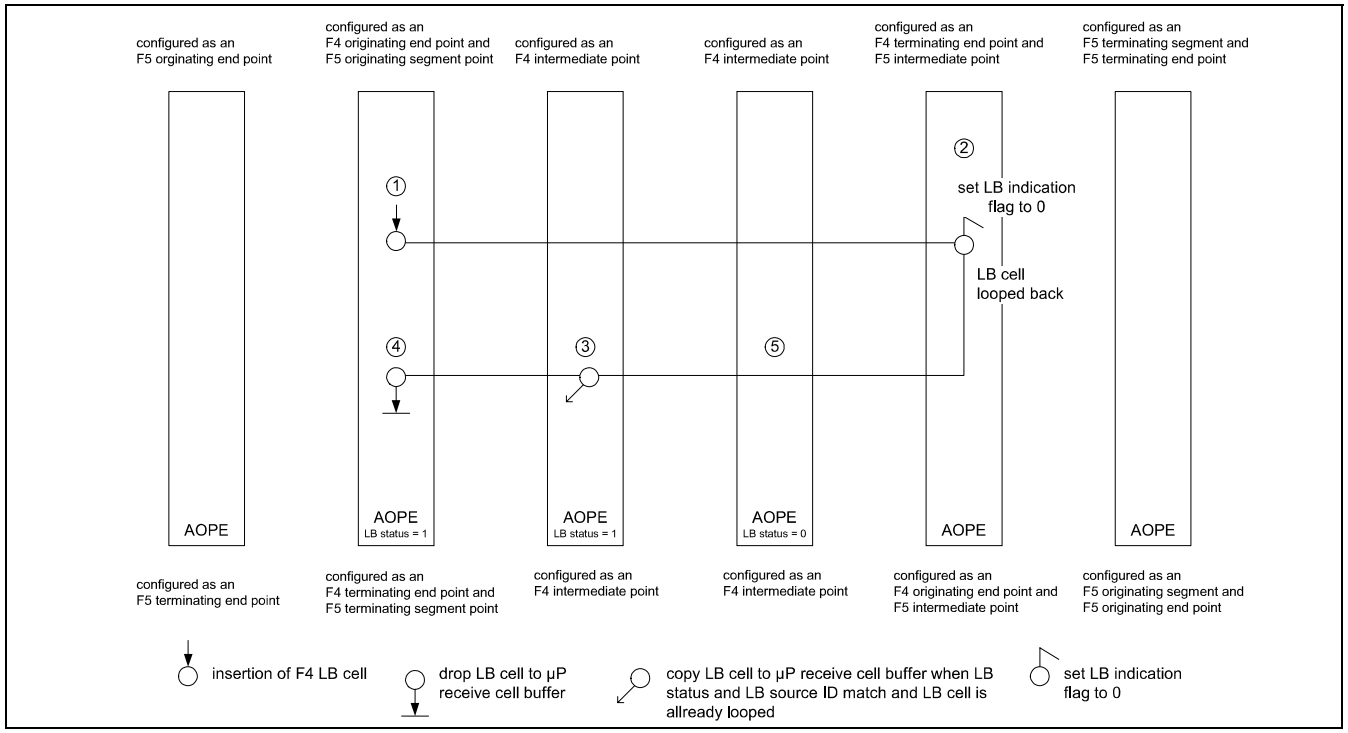


Figure 23 Example of F4 End-to-End Loopback Processing

Table 2 End-to-End Loopback Processing

LB indication	LB state	LB Location/ Source ID Flag	LB Location/ Source ID	Loopback Action
1	don't care	don't care	don't care	forward LB cell to terminating end point
0	0	don't care	don't care	forward LB cell to terminating end point
	1	disabled	don't care	• copy of LB cell to µP receive cell buffer • forward LB cell to terminating end point
		enabled	match	
		enabled	mismatch	forward LB cell to terminating end point

2.8.1.2 F4/F5 Segment Loopback Processing

If the LB indication bit of an LB cell is equal to 1 and an LB location ID of the LB cell is equal to the network element ID (LB location ID match) the loopback indication flag is set to 0 and the LB cell is looped back (loopback point, see **figure 24**, marker ②). Additionally the unchanged LB cell is forwarded to the terminating segment point. This cell is looped back at the terminating segment point (see **figure 24**, marker ③). If the LB location ID flag is disabled or an LB location ID mismatch occurs the LB cell is forwarded to the terminating segment point (see **figure 24**, marker ⑤)

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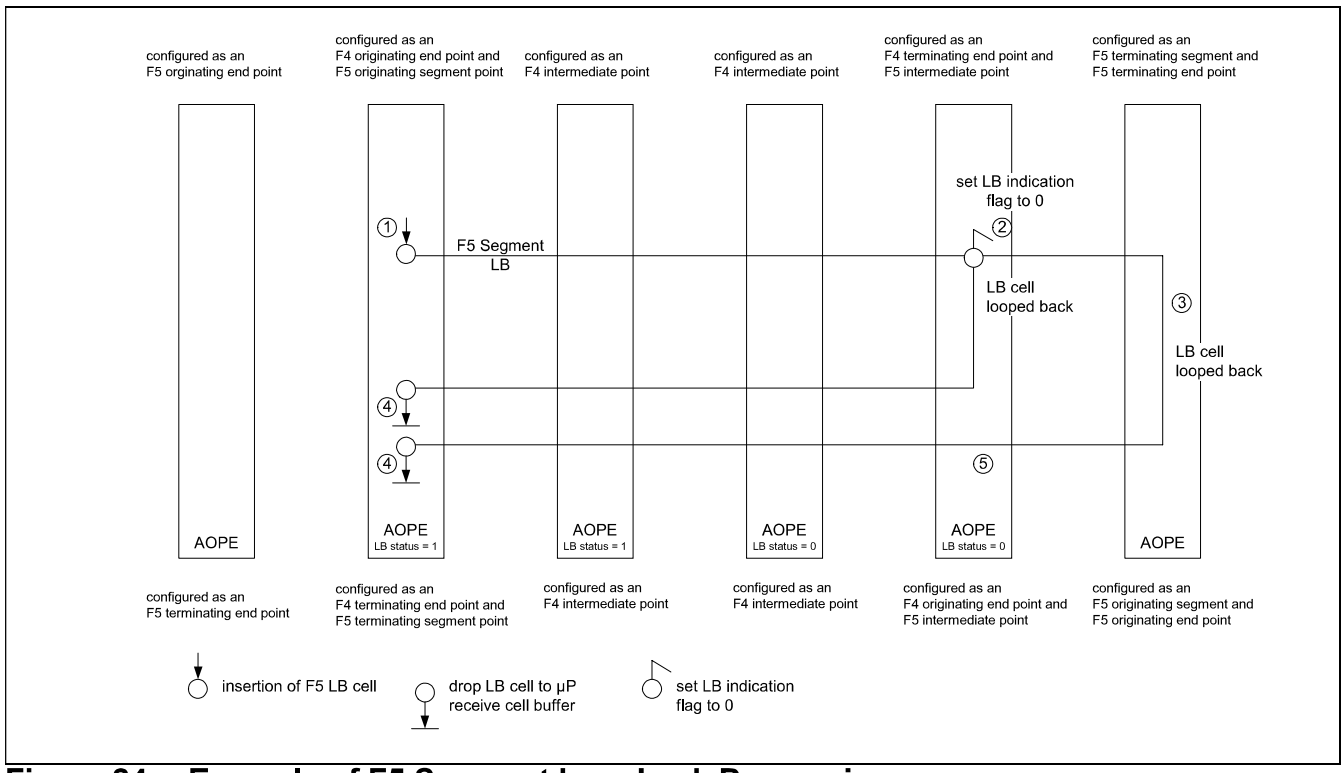


Figure 24 Example of F5 Segment Loopback Processing

If the LB indication of an LB cell is equal to 0 (LB cell already looped) and the connection is in LB state (LB state = 1) and the LB source ID of the LB cell is equal to the network element ID (LB source ID match) the LB cell is copied into the receive cell buffer of the µP and the LB cell is forwarded to the terminating segment point. If the LB source ID flag of a connection is disabled the LB cell is also copied into the receive cell buffer of the µP and the LB cell is forwarded to the terminating segment point.

Table 3 Segment Loopback Processing

LB Indication	LB State	LB Location/ Source ID Flag	LB Location/ Source ID	Loopback Action
1	don't care	enabled	match	• set LB indication to 0 • LB cell is looped back • forward of LB cell to terminating segment point
		enabled	mismatch	forward of LB cell to terminating segment point
		disabled	don't care	
0	0	don't care	don't care	forward of LB cell to terminating segment point
	1	disabled	don't care	• copy of LB cell to µP receive cell buffer • forward of LB cell to terminating segment point
		enabled	match	
		enabled	mismatch	forward of LB cell to terminating segment point

2.8.1.3 F4/F5 End Point Loopback Processing

If the LB indication of an LB cell is equal to 1 and an LB location ID of the LB cell is equal to the network element ID (LB location ID match) the LB indication flag is set to 0 and the LB cell is looped back (loopback point, see **figure 25**, marker ②). This means that the AOPE ASIC sends the LB cell to the opposite direction of AOPE (from upstream direction to downstream direction and in opposite direction). In case of an LB location ID mismatch the LB cell is discarded.

Additionally the loopback processing sets a 'consistency' flag for the µP only at the VP terminating end point (AOPE upstream) in order to support the VPCI consistency check. The 'consistency' flag is reset by SW.

If the LB indication of an LB cell is equal to 0 (LB cell already looped) and the connection is in LB state (LB state = 1) and the source ID of the LB cell is equal the network element ID (LB source ID match) the LB cell is dropped into the receive cell buffer of the µP (see **figure 25**, marker ③). If the LB source ID flag of a connection is disabled or an LB source ID mismatch occurs then the LB cell is discarded. If the connection isn't in LB state (LB state = 0) the LB cell is discarded.

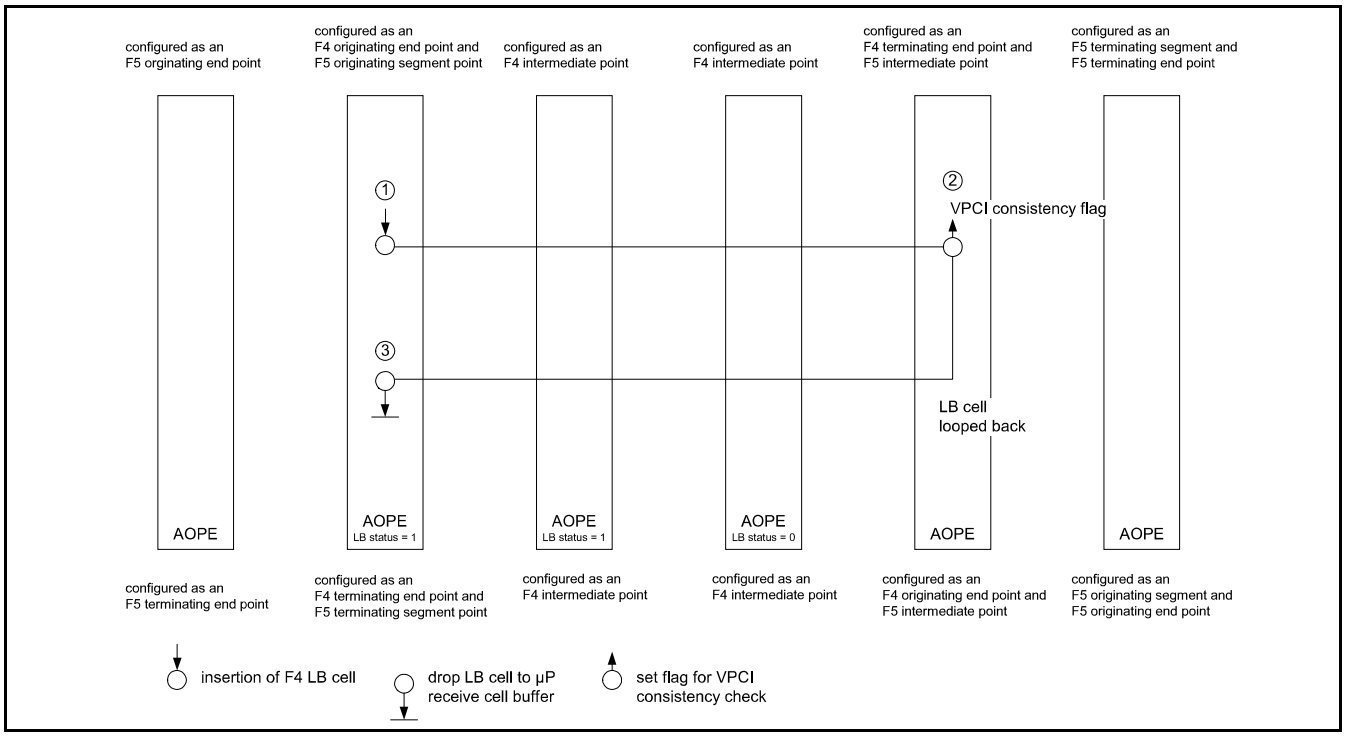


Figure 25 Example of F4 End Point Loopback Processing

Table 4 End Point Loopback Processing

LB indication	LB state	LB Location/ Source ID Flag	LB Location/ Source ID	Loopback Action
1	don't care	don't care	match	• set LB indication flag to 0 • LB cell looped back • set a flag for VPCI consistency check
			mismatch	discard LB cell
0	0	don't care	don't care	discard LB cell
	1	disable	don't care	drop of LB cell to receive cell buffer of the µP
		enabled	match	
		enable	mismatch	discard LB cell

2.8.1.4 VPCI Consistency Check

VPCI consistency check is supported by the LB function at the VPC terminating end point. The loopback function of AOPE (upstream) indicates 'VPCI consistency' by setting a flag, if an F4 end-to-end LB cell is received and successfully looped back at VPC terminating end point. This flag is reset by SW. The bit VPCCHK in Dword4 of the external RAM entry is the corresponding to this flag (see **section 3.9.2.1,** page 105, and **section 3.9.4.1,** page 116).

2.9 Connection Quality Measurement (PM)

2.9.1 General

To make measurement of connection quality possible, the AOPE provides a number of counters. The Performance Monitoring (PM) flow allows the use and evaluation of these counters. The counter values are stored in the internal PM main RAM (see **section 3.9.5,** page 121).

The AOPE can process 128 bidirectional PM flows configurable for the upstream or downstream direction on a connection basis (see **section 3.9,** page 98). PM flows can be applied to the F4/ F5 layer as a segment flow or end-to-end flow.

In the PM flow, forward error detection information (e.g. the error detection code) is communicated by the PM end points using Forward Monitoring (FM) cells. The performance monitoring results are received on the reverse direction using Backward Reporting (BR) cells.

After a block of user cells has been received, the related FM cell can be inserted directly within the next cell cycle. The blocksize is defined in **section 3.9.5.3,** page 122. The first FM cell sent from the PM originating point is used to initialize the PM terminating point. After an FM cell has been received at a PM terminating point, the corresponding BR cell is generated (if enabled) and sent back via the opposite direction, i.e. if it is received upstream it is sent downstream and if it is received downstream it is sent upstream.

The first BR cell is generated when the first FM cell for this PM flow has been received. This BR cell carries valid data to initialize the BR data collection point, but no valid data for data collection. Only the following BR cells contain valid data for data collection.

The PM function is split into three different parts:

- PM generation
- PM analysis and loop
- PM data collection.

PM generation includes

- Calculation of total user cell count for all cells and for high priority cells (CLP=0)
- Calculation of a BIP-16 checksum over user cell payload
- Generation of FM cells containing the calculated results.

The FM cells are coded as F4 or F5 automatically for VPCs and VCCs, respectively, end-end or segment as specified. FM cell sequence number and CRC-10 checksum are also generated. The blocksize can be selected between 2 and 65536. The optional time stamp of the FM cell is not generated.

Forced OAM cell insertion is used for both up- and downstream FM cell insertion. During insertion of FM cells the user cell stream is stored in the respective buffers (see **section 2.4**).

PM analysis and loop include

- Calculation of total user cell count for all cells and for high priority cells (CLP=0)
- Extraction of FM cells
- Appending of calculation results to the end of the cell
- Conversion of the cell into a BR cell
- Re-insertion of the BR cell in opposite direction.

PM analysis uses the same PM processor circuits as the generation process. In total 128 PM processor circuits are shared by up- and downstream direction.

For PM data collection 128 circuits are provided, which are independent of the PM processor circuits. Both PM and data collection processors have their respective entries in the internal PM/ data collection RAMs.

The assignment of PM and data collection processors to connections in up- or downstream direction is arbitrary. VPCs and VCCs can be assigned by programming pointers in the F4 and F5 entries, respectively (see **section 3.9.5,** page 121, and **section 3.9.6,** page 123).

2.9.2 Example

A typical PM scenario is shown in **figure 26** in case of VP end-to-end monitoring. Two nodes are involved, Node 'a' where the $VPC_{a\text{-}b}$ is created and Node 'b' where $VPC_{a\text{-}b}$ is terminated. In backward direction the associated $VPC_{b\text{-}a}$ is created in Node 'b' and terminated in Node 'a'. Creation of a VPC allways occurs at an outgoing port of a node and termination at an incoming port. Hence the Originating End Point (OEP) of $VPC_{a\text{-}b}$ is located in the downstream part of the PXB 4340 AOP in Node a, and the Terminating End Point (TEP) of $VPC_{a\text{-}b}$ is located in the upstream part of the PXB 4340 AOP in Node b. For $VPC_{b\text{-}a}$ the situation is mirrored according to **figure 26**.

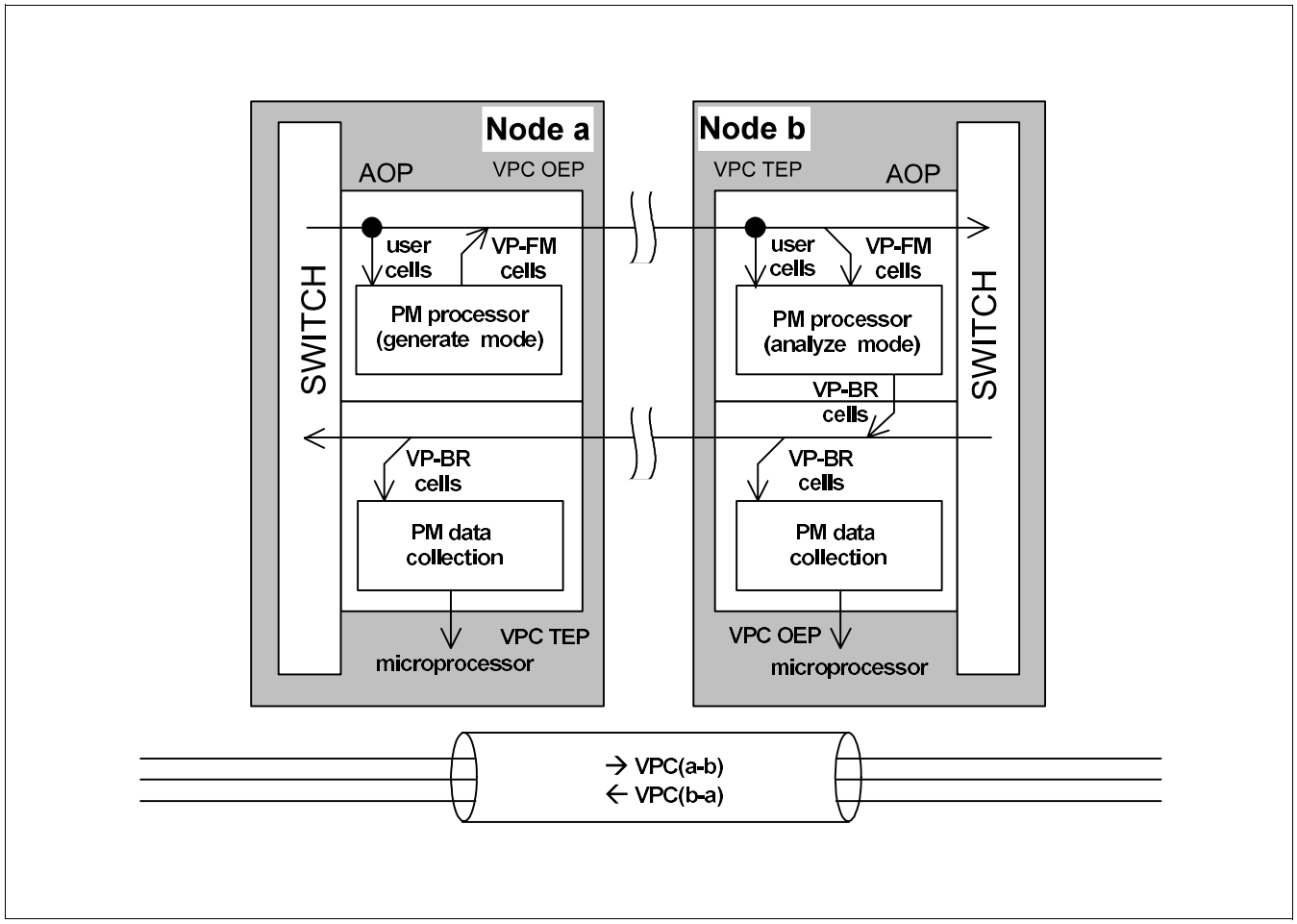


Figure 26 PM Configuration Example

Note that between Nodes 'a' and 'b' a number of intermediate nodes can be located. All PXB 4340 AOP chips on these nodes must be configured either as Originating or Terminating Segment Points (OSP, TSP) or as Intermediate Points (IP).

One of the 128 PM processors in the PXB 4340 AOP upstream part of Node a is configured in generate mode, i.e. it monitors all user cells of VPC_{a-b}, computes PM data and inserts it after blocks of user cells into the cell stream as Forward Monitoring (FM) cells.

At the terminating PXB 4340 AOP one of the 128 PM processors is configured in analyze mode, i.e. it monitors all user cells of VPC_{a-b}, computes PM data and adds it to the PM data contained in the FM cells. The FM cells are extracted from the cell stream, converted into Backward Reporting (BR) cells and re-inserted in backward direction in VPC_{b-a}. The conversion into BR cells includes the calculation of the differences between measured PM data and the PM data contained in the FM cells. The differences are written into the BR cells.

Back at the originating Node a, the BR cells are discarded after evaluation.

Note that the re-insertion of BR cells in backward direction assumes the same identifier (LCI) of the backward direction connection.

2.9.3 PM Data Collection

The data collection procedure is independent of the FM/BR cell mechanism. It uses one of the 128 data collection processors contained in the PXB 4340 AOP. Each of them can evaluate the BR data flow from upstream or downstream direction. Data collection can be done at any node along the way of the BR cells. In the example of **figure 26** Nodes a or b could be selected for data collection. It can be done concerning the data of an incoming BR cell or after a BLER0+1 calculation concerning the data of an incoming FM cell. The TUCdiff/TUCdiff0 calculation has to be done before the Data Collection can be started. In the Data Collection processing it is first proved whether TUCdiff/TUCdiff0 is zero. If it is zero, the BLER0+1 is checked. If TUCdiff/ TUCdiff0 is not zero, it is not reasonable to prove the BLER0+1. According to the defined thresholds certain counters have to be updated. **Table 5** is a summery of counters, which are updated for Data Collection (see **section 3.9.6,** page 123).

Table 5 Updated counters for Data Collection

Acronyms	term
IMPB	impaired blocks
SECB	severely errored cell blocks
SECBERR	severely errored cell block errored counter
ERRC	errored cells
LOSTC	lost cells
MISC	misinserted cells
TLOST0	total lost cells
SECBMIS	severely errored cell blocks of misinserted cells
LOSTC0	lost cells of the CLP=0 flow
TLOSTC0	total lost cells of the CLP=0 flow
TRANSUC0	transmitted user cells of CLP=0 flow
TRANSUC	transmitted user cells of CLP-0+1 flow

The Counters SECB, SECBERR, SECBMIS and TLOSTC0 are updated if a related threshold value is reached.

The threshold values are set in several µP registers (see **section 3.4,** page 71). TUCdiff is the difference between the transmitted cells of the PM originating point and the received cells of the PM terminating point. TUCdiff is calculated for the CLP-0+1 flow and TUCdiff0 for the CLP=0 flow.

The BLER-0+1 counts the BIP16 errors of a block of user cells if no user cells are lost or misinserted, i.e. TUCdiff = 0.

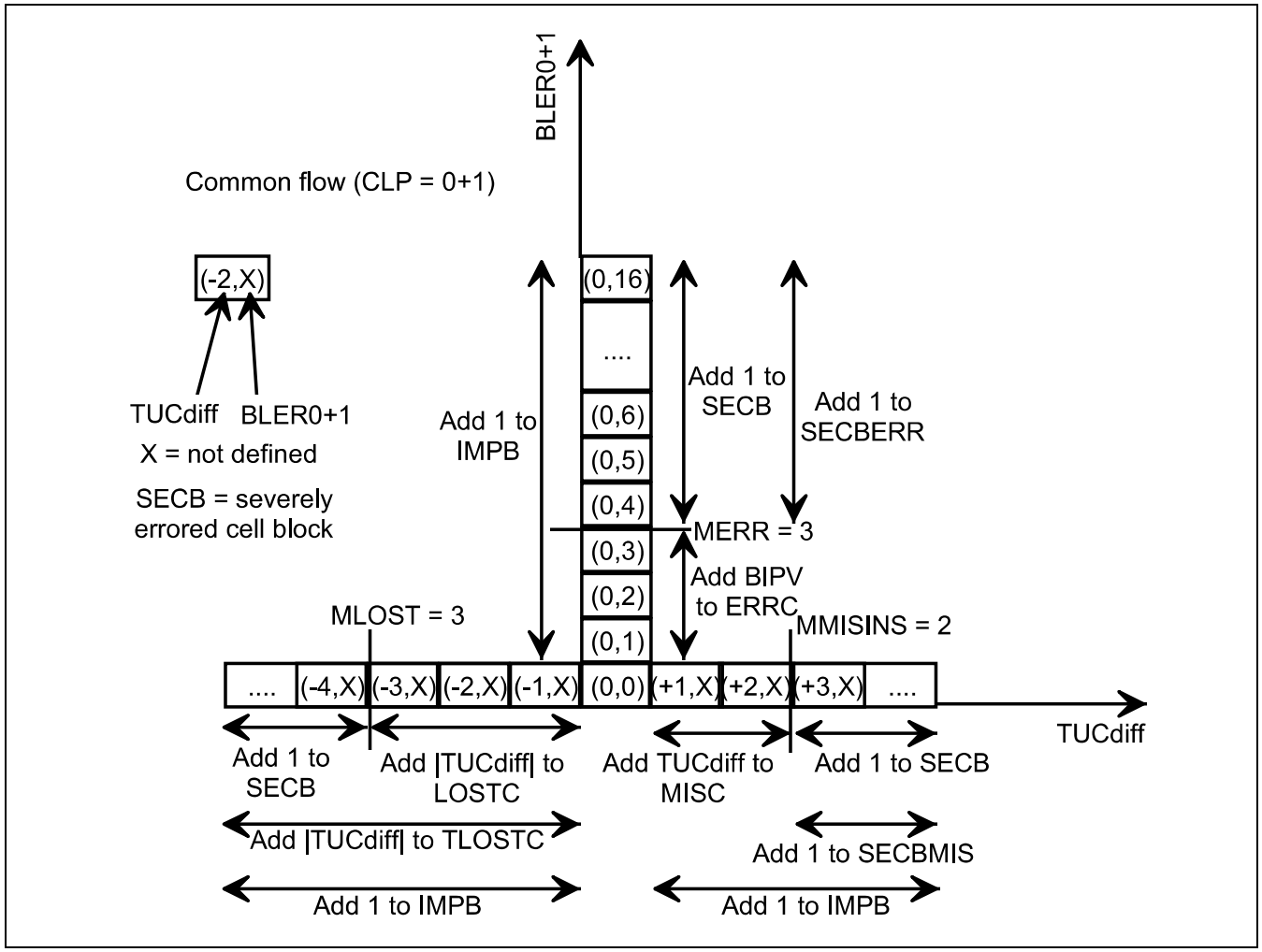


Figure 27 PM Data Collection

Note: The thresholds MLOST (0+1 and 0), MMISINS and MERR can be programmed for up- and downstream direction separately. They apply for all connections.

2.9.4 Simultaneous PM flows

The PXB 4340 AOP contains 128 PM processors which may be used to generate an FM flow or to terminate an FM flow. Terminating an FM flow means analyzing and looping of the FM cells as BR cells. During one cell cycle **four** PM processors can be executed arbitrary for F4 and F5 level.

It may happen that a user cell belongs to a VCC for which F5 segment PM is done. E.g. in the example of **figure 27** node b could be a VCC Originating Segment Point (OSP) in addition to the VPC TEP. In this case the arrival of a VCC user cell triggers two PM processors in the upstream part of the PXB 4340 AOP.

In case of F4 and F5 segments e.g. the downstream part of a PXB 4340 AOP could be configured as VPC OSP and VCC OSP (**refer to table 30**). In this case a user cell not only triggers two PM processors simultaneously, but might also complete two PM blocks. Then two FM cells have to be generated simultaneously. In this case the PXB 4340 AOP first inserts the VP-FM cell and then the VC-FM cell.

2.9.5 Adjacent PM Segments

The arbitrary assignment of PM processors to connections also allows e.g. to terminate a Segment PM flow and generate a new Segment PM flow for the same connection within one PXB 4340 AOP as shown in **figure 28**.

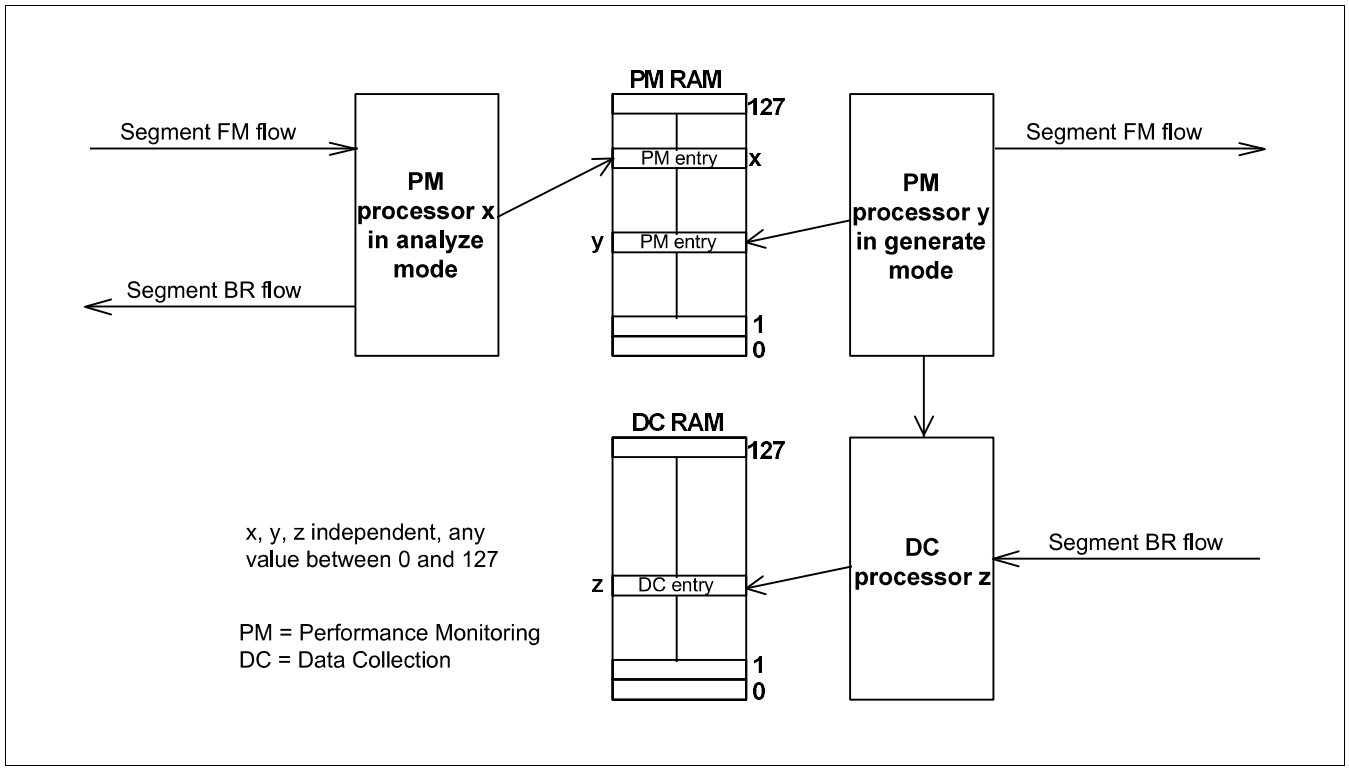


Figure 28 Example for adjacent PM Segments

2.10 Activation and Deactivation Cells

These cell types are generated by the microprocessor and transmitted via the cell insertion function (**section 2.16**) of the PXB 4340 AOP.

The detection and extraction of activation/deactivation cells is done automatically at the respective segment or end-to-end points if the PXB 4340 AOP is configured correctly and the function is enabled (which is possible per connection). Extracted cells are stored in the receive buffer (**section 2.16**).

2.11 Interactions between OAM Functions

The PXB 4340 AOP does failure propagation automatically, e.g. a received VP-AIS cell automatically leads to the generation of VC-AIS and VP-RDI cells at the VP endpoint. Also the generation of AIS/RDI as a consequence of LOC state is done automatically. Failure propagation from degraded performance, detected with the PM function, to AIS/RDI insertion, however is not done automatically, but must be initiated by the microprocessor.

To enforce VP-level AIS/RDI insertion command bits are available per connection. If enabled the PXB 4340 AOP automatically inserts VC-AIS cells for all VCCs of a VPC.

Connection specific AIS state is left when user or CC cells are detected. Only end-to-end cells may react in this way with AIS because "shorter" CC flows such as segment CC or ICC may cause a mixture of AIS and SCC/ICC cells which would corrupt AIS recognition in the cases a)

and b) outlined in figure X. Consequently the AIS analyser implementation totally ignores SCC/ ICC cells. Neither the occurrence of SCC/ICC cells causes return to AIS normal state nor the setup for activation of the CC checker disables return to AIS normal state by a timeout criterion.

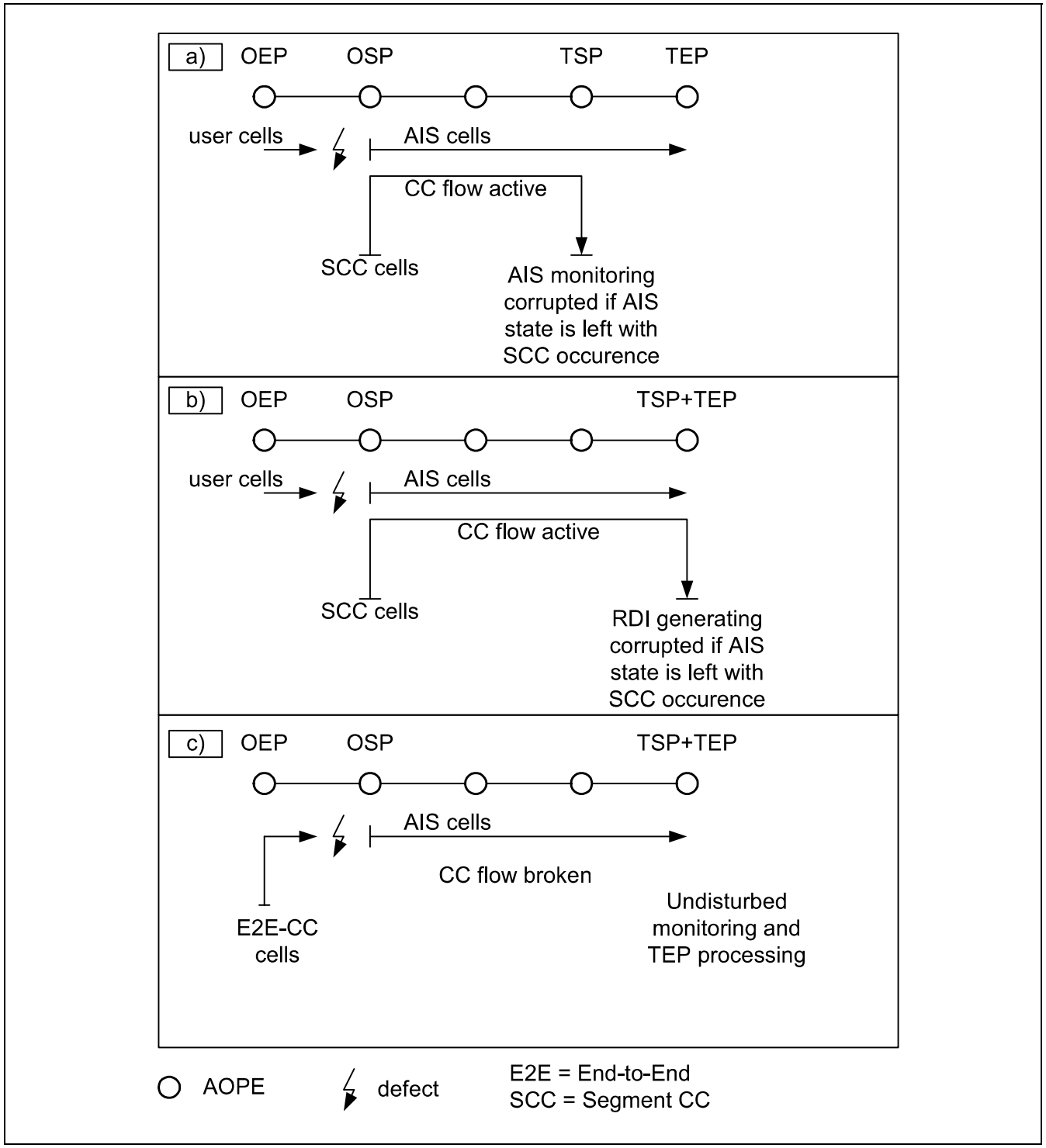


Figure 29 Effect of CC cells on AIS recognition

2.12 Cell Filters

The PXB 4340 AOP provides two types of cell filters:

- filters for special OAM cells
- filters for general purpose ATM cells

For both filter types two filters are provided.

2.12.1 Special OAM Cell Filters

For these filters only the first payload byte of the desired OAM cell (OAM type and function type field) has to be programmed. The other criteria of OAM cells, VCI or PT coding are hard-wired in the chip. All OAM cells, F4 and F5, segment and end-to-end are detected. The filters are working for up- and downstream direction. For each filter the action upon the detection of an OAM cell of the programmed type can be programmed:

- ignore cell (default)
- discard cell
- extract to receive buffer
- copy to receive buffer and forward.

Applications for this filter function are e.g. proprietary OAM functions using the standardized System OAM cell coding or the treatment of future OAM cell types.

2.12.2 General purpose Cell Filters

These filters consist of 3 programmable words for the comparison of all 5 cell header bytes plus the first payload byte. The UTOPIA cell format described in **section 5.1** is compared. Each bit can be individually masked with the mask pattern defined in 3 programmable mask registers. A masked bit matches always when the pattern is compared to the ATM cells. Cells from both up- and downstream direction are compared. Upon match the following actions can be selected:

- ignore cell (default); e.g. forward cell
- discard cell
- extract to receive buffer
- copy to receive buffer and forward.

See **section 2.16** for the receive buffer description.

In addition to the these actions the match signals of both comparators and for up- and downstream direction are output at four pins as a short pulse. The pulses can be further processed by external logic. This feature could be used for measurements.

Other applications for the general purpose cell filters are e.g. communication channels within a switch or the filtering of RM cells.

2.13 Microprocessor Control

A 16-bit microprocessor interface for embedded controllers like e.g. the 386EX is provided for configuration and operation of the PXB 4340 AOP. 8 address lines allow to address 172 registers (non-contiguous addresses). Interrupts are provided for the notification of unexpected events. DMA support is provided for fast data transfer to and from the external RAMs.

2.14 Access to internal and external RAMs

The microprocessor can not access these RAMs directly, but uses a transfer register set. It consists of three blocks:

- read register block
- write register block
- mask register block.

In addition an address register specifying the entry to be accessed and a command register to specify the RAM and to start the transfer are defined. The PXB 4340 AOP uses one single access type, the read-modify-write transfer, where the old data is transferred from the specified RAM entry to the Read Transfer Registers and the contents of the Write Transfer Registers are written to the RAM entry for those bits which are unmasked.

In addition to the read-modify-write access executed upon microprocessor command for a single entry, there are two other access types to the external RAM (figure 30):

- the access initiated by the passing ATM cell
- the SCAN access for OAM and/or DMA.

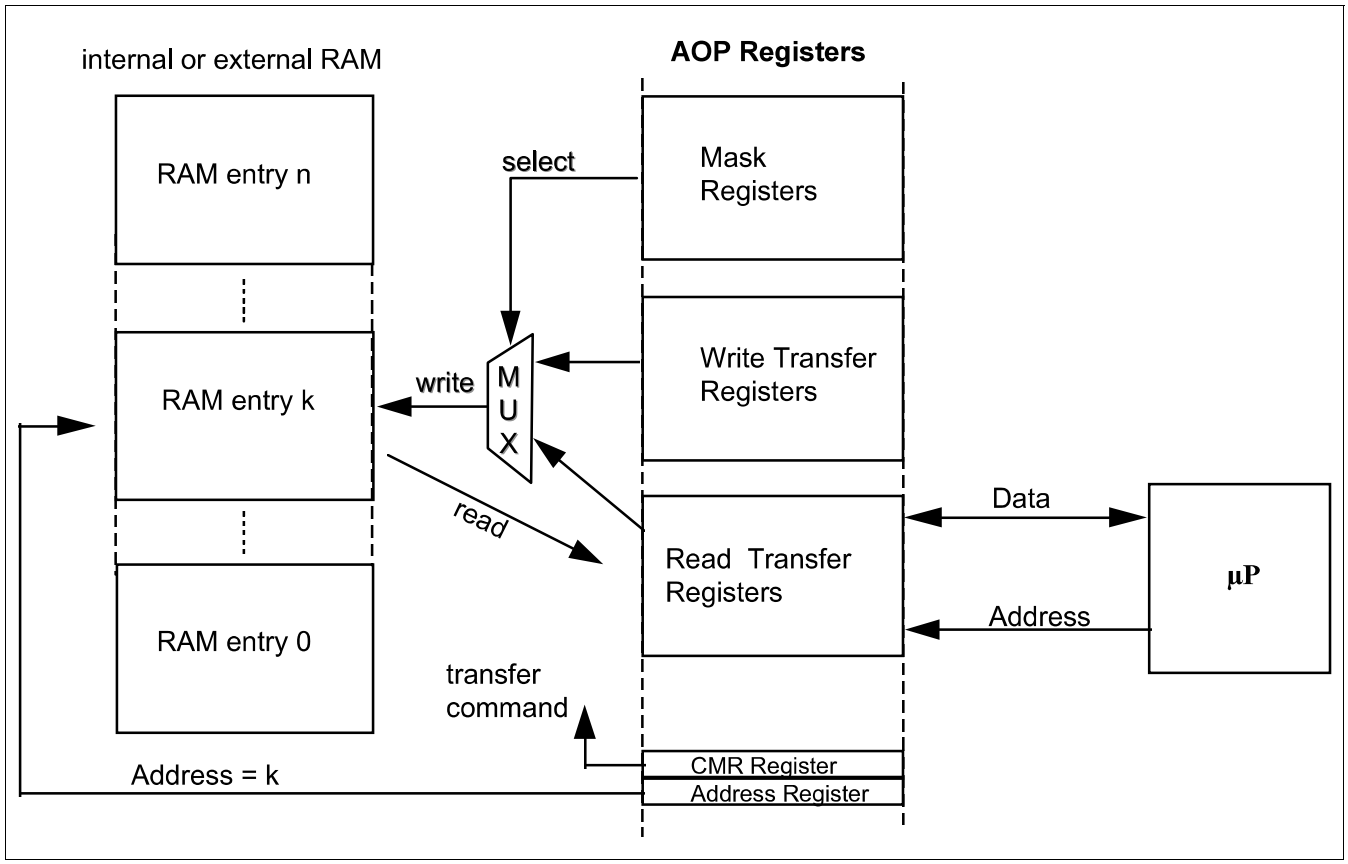


Figure 30 Access to internal or external RAMs

2.15 SCAN Mechanism with OAM and/or DMA Function

This mechanism has to be triggered by the microprocessor. It is recommended to trigger it in a 0.5 s time frame, as all time-out values are determined based on this time interval. During a SCAN all entries within the specified range of the external RAMs are accessed sequentially using the read-modify-write access described in **section 2.14**. The SCAN must be programmed in a way that it covers all used RAM entries in a little less than 0.5 s. To initialize the SCAN mechanism use register SCCONF2 (see **section 3.5.11,** page 79). The SCAN is processed for all connections inside the range selected by register SCCONF4 (see **section 3.5.13,** page 80) and register SCCONF5 (see **section 3.5.14,** page 81). To initiate the SCAN bit STARTSC in register SCCONF3 has to be set (see **section 3.5.12,** page 80). The following equation can be used to calculate the scan cycle period (SCP) :

$$SCP = \frac{(scanperiod - tolerance) \times \frac{f_{Core}}{cycles\ per\ cell}}{LCI_{max} - LCI_{min} + 1}$$

with : scanperiod + tolerance < 500 ms !

Example : The AOP needs 32 cycles per cell. At a core frequency of 51.84 MHz the AOP can process 1.62 M cells per second. If SCAN has to process e.g. 8192 connections within 350 ms (scanperiod + tolerance) the SCP is calculated as :

$$SCP = \frac{350ms \times 1.62\ M \cdot \frac{cells}{s}}{8192} = 69.21\ cells$$

Here SCP is equal to the time the AOP needs to process 69.21 cells. The values of the register entry SCP is of type integer. So the SCP is rounded to 69. If the result of the SCP calculation is 40 or less SCAN operation is no more guaranteed at full traffic load because SCAN operation requires a number of empty cycles.

With each SCAN trigger two functions can be enabled independently for up- and downstream direction: OAM function and DMA transfers. OAM functions include all the necessary actions for AIS/RDI/CC processing, i.e. update of counters, check for time-out values and execution of state transitions, OAM cell insertions and interrupts. The DMA function allows to transfer data to and from the external RAM during the SCAN. The DMA function has two modes, the normal DMA function and the compressed DMA.

In the normal DMA mode a specified dword of each external RAM entry is transferred to a range of the microprocessor main memory. Each bit of the specified dword can be overwritten by a specified value for all entries. So the normal DMA can be used to initialize the whole external RAM to common values or also to verify entries of all connections.

In compressed DMA mode one dword with pre-defined bits collected from several dwords of the external RAM is transferred to a microprocessor memory range. The pre-defined bits are status bits and status transition bits. The status transition bits must be reset with each SCAN, which can be achieved with appropriate settings of write and mask registers. The compressed DMA is typically used in-service together with the OAM function (see **section 4.1.6**).

For the DMA data transfers a 32 word FIFO is provided on-chip for DMA read (figure 31). It is emptied by the microprocessor via consecutive reads of the DMA register. The DMA request pin of the PXB 4340 AOP is asserted when the FIFO is occupied and deasserted when it is empty. The DMA transfer itself must be executed by an external DMA controller.

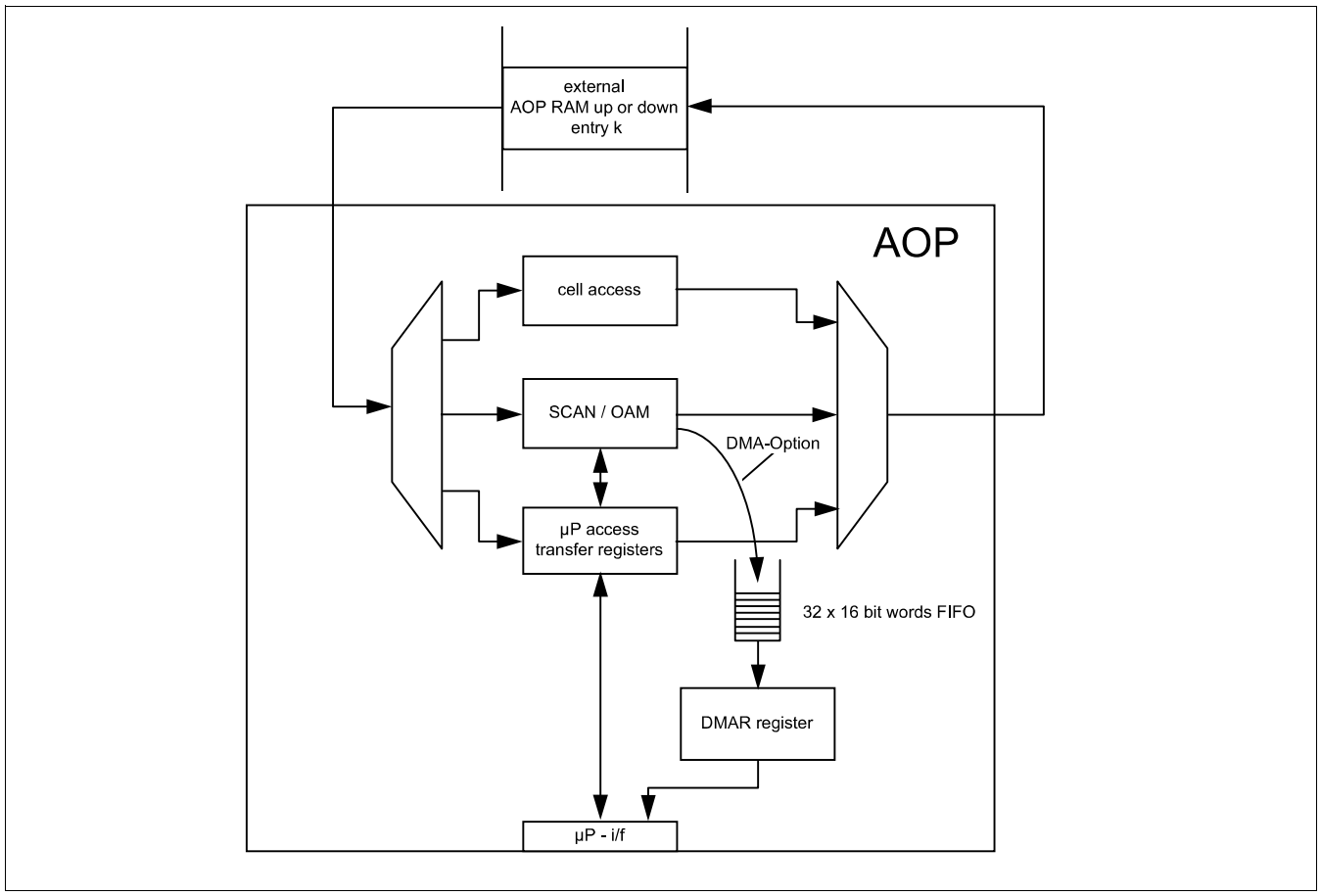


Figure 31 Scan Mechanism with OAM and/or DMA Function

2.16 Receive and Transmit Buffer

The PXB 4340 AOP provides a 12-cell receive buffer and a 1-cell transmit buffer. They are used for insertion and extraction of LB cells, activation and deactivation cells and special cells defined with the cell filters (see **section 2.12**).

The buffers are realized differently. The transmit buffer consists of 27 words, directly addressable by the microprocessor for read and write. When the cell is assembled it can be inserted by setting a command bit. The command bit is reset after complete insertion of the cell into the data stream. The insertion direction, up- or downstream can be selected and also if the CRC-10 should be computed automatically by the chip or not.

The receive buffer is realized as FIFO with word-wise access via a single register. A cell is read with 27 consecutive read accesses to this register. Reception of a cell is signalled to the microprocessor via an interrupt bit. The interrupt bit is reset by the chip automatically after the last read access if no more cell is in the buffer. The receive buffer collects cells from up- and downstream direction, they are distinguished with a bit in the UDF2 octet. Cell format for both receive and transmit buffer is the 16-bit UTOPIA format as described in **section 5.1**.

3 Register Description

Table 2 AOP Register Overview

adr (hex)	register	description	ASIC core	µP	reset value	see page
Read-Mask-Write Registers						
00	WDR0L	Write Data Register 0 (15.. 0)	r	rw	0000_H	59
01	WDR0H	Write Data Register 0 (31..16)	r	rw	0000_H	59
02	WDR1L	Write Data Register 1 (15.. 0)	r	rw	0000_H	59
03	WDR1H	Write Data Register 1 (31..16)	r	rw	0000_H	59
04	WDR2L	Write Data Register 2 (15.. 0)	r	rw	0000_H	59
05	WDR2H	Write Data Register 2 (31..16)	r	rw	0000_H	59
06	WDR3L	Write Data Register 3 (15.. 0)	r	rw	0000_H	59
07	WDR3H	Write Data Register 3 (31..16)	r	rw	0000_H	59
08	WDR4L	Write Data Register 4 (15.. 0)	r	rw	0000_H	59
09	WDR4H	Write Data Register 4 (31..16)	r	rw	0000_H	59
0A	WDR5L	Write Data Register 5 (15.. 0)	r	rw	0000_H	59
0B	WDR5H	Write Data Register 5 (31..16)	r	rw	0000_H	59
0C	WDR6L	Write Data Register 6 (15.. 0)	r	rw	0000_H	59
0D	WDR6H	Write Data Register 6 (31..16)	r	rw	0000_H	59
0E	WDR7L	Write Data Register 7 (15.. 0)	r	rw	0000_H	59
0F	WDR7H	Write Data Register 7 (31..16)	r	rw	0000_H	59
10	WDR8L	Write Data Register 8 (15.. 0)	r	rw	0000_H	59
11	WDR8H	Write Data Register 8 (31..16)	r	rw	0000_H	59
12	WDR9L	Write Data Register 9 (15.. 0)	r	rw	0000_H	59
13	WDR9H	Write Data Register 9 (31..16)	r	rw	0000_H	59
14	WDR10L	Write Data Register 10 (15.. 0)	r	rw	0000_H	59
15	WDR10H	Write Data Register 10 (31..16)	r	rw	0000_H	59
16	WDR11L	Write Data Register 11 (15.. 0)	r	rw	0000_H	59
17	WDR11H	Write Data Register 11 (31..16)	r	rw	0000_H	59
18	WDR12L	Write Data Register 12 (15.. 0)	r	rw	0000_H	59
19	WDR12H	Write Data Register 12 (31..16)	r	rw	0000_H	59
1A	WDR13L	Write Data Register 13 (15..0)	r	rw	0000_H	59

Table 2 AOP Register Overview

adr (hex)	register	description	ASIC core	µP	reset value	see page
1B	WDR13H	Write Data Register 13 (31..16)	r	rw	0000_H	59
1C	RDR0L	Read Data Register 0 (15.. 0)	rw	r	0000_H	60
1D	RDR0H	Read Data Register 0 (31..16)	rw	r	0000_H	60
1E	RDR1L	Read Data Register 1 (15.. 0)	rw	r	0000_H	60
1F	RDR1H	Read Data Register 1 (31..16)	rw	r	0000_H	60
20	RDR2L	Read Data Register 2 (15.. 0)	rw	r	0000_H	60
21	RDR2H	Read Data Register 2 (31..16)	rw	r	0000_H	60
22	RDR3L	Read Data Register 3 (15.. 0)	rw	r	0000_H	60
23	RDR3H	Read Data Register 3 (31..16)	rw	r	0000_H	60
24	RDR4L	Read Data Register 4 (15.. 0)	rw	r	0000_H	60
25	RDR4H	Read Data Register 4 (31..16)	rw	r	0000_H	60
26	RDR5L	Read Data Register 5 (15.. 0)	rw	r	0000_H	60
27	RDR5H	Read Data Register 5 (31..16)	rw	r	0000_H	60
28	RDR6L	Read Data Register 6 (15.. 0)	rw	r	0000_H	60
29	RDR6H	Read Data Register 6 (31..16)	rw	r	0000_H	60
2A	RDR7L	Read Data Register 7 (15.. 0)	rw	r	0000_H	60
2B	RDR7H	Read Data Register 7 (31..16)	rw	r	0000_H	60
2C	RDR8L	Read Data Register 8 (15.. 0)	rw	r	0000_H	60
2D	RDR8H	Read Data Register 8 (31..16)	rw	r	0000_H	60
2E	RDR9L	Read Data Register 9 (15.. 0)	rw	r	0000_H	60
2F	RDR9H	Read Data Register 9 (31..16)	rw	r	0000_H	60
30	RDR10L	Read Data Register 10 (15.. 0)	rw	r	0000_H	60
31	RDR10H	Read Data Register 10 (31..16)	rw	r	0000_H	60
32	RDR11L	Read Data Register 11 (15.. 0)	rw	r	0000_H	60
33	RDR11H	Read Data Register 11 (31..16)	rw	r	0000_H	60
34	RDR12L	Read Data Register 12 (15.. 0)	rw	r	0000_H	60
35	RDR12H	Read Data Register 12 (31..16)	rw	r	0000_H	60
36	RDR13L	Read Data Register 13 (15.. 0)	rw	r	0000_H	60
37	RDR13H	Read Data Register 13 (31..16)	rw	r	0000_H	60
38	MDR0L	Mask Data Register 0 (15.. 0)	r	rw	0000_H	60

Table 2 AOP Register Overview

adr (hex)	register	description	ASIC core	µP	reset value	see page
39	MDR0H	Mask Data Register 0 (31..16)	r	rw	0000_H	60
3A	MDR1L	Mask Data Register 1 (15.. 0)	r	rw	0000_H	60
3B	MDR1H	Mask Data Register 1 (31..16)	r	rw	0000_H	60
3C	MDR2L	Mask Data Register 2 (15.. 0)	r	rw	0000_H	60
3D	MDR2H	Mask Data Register 2 (31..16)	r	rw	0000_H	60
3E	MDR3L	Mask Data Register 3 (15.. 0)	r	rw	0000_H	60
3F	MDR3H	Mask Data Register 3 (31..16)	r	rw	0000_H	60
40	MDR4L	Mask Data Register 4 (15.. 0)	r	rw	0000_H	60
41	MDR4H	Mask Data Register 4 (31..16)	r	rw	0000_H	60
42	MDR5L	Mask Data Register 5 (15.. 0)	r	rw	0000_H	60
43	MDR5H	Mask Data Register 5 (31..16)	r	rw	0000_H	60
44	MDR6L	Mask Data Register 6 (15.. 0)	r	rw	0000_H	60
45	MDR6H	Mask Data Register 6 (31..16)	r	rw	0000_H	60
46	WMASK	Mask for word 7-13	r	rw	0000_H	61
47	RMWC	RMW Control Register	rw	rw	0000_H	62
48	RMWADR	LCI/PM pointer for RMW	r	rw	0000_H	63
Celltype Recognition Registers						
60	LSIDR0	LB location/source identifier	r	rw	0000_H	64
61	LSIDR1	LB location/source identifier	r	rw	0000_H	64
62	LSIDR2	LB location/source identifier	r	rw	0000_H	64
63	LSIDR3	LB location/source identifier	r	rw	0000_H	64
64	LSIDR4	LB location/source identifier	r	rw	0000_H	64
65	LSIDR5	LB location/source identifier	r	rw	0000_H	64
66	LSIDR6	LB location/source identifier	r	rw	0000_H	64
67	LSIDR7	LB location/source identifier	r	rw	0000_H	64
68	CTR0	Special OAM cell filter 0	r	rw	0000_H	64
69	CTR1	Special OAM cell filter 1	r	rw	0000_H	64
6A	CTR10	Cell filter1	r	rw	0000_H	65
6B	CTR11	Cell filter1	r	rw	0000_H	65
6C	CTR12	Cell filter1	r	rw	0000_H	65

Table 2 AOP Register Overview

adr (hex)	register	description	ASIC core	µP	reset value	see page
6D	CTR20	Cell filter2	r	rw	0000_H	65
6E	CTR21	Cell filter2	r	rw	0000_H	65
6F	CTR22	Cell filter2	r	rw	0000_H	65
70	MR10	Mask for cell filter 1	r	rw	0000_H	65
71	MR11	Mask for cell filter 1	r	rw	0000_H	65
72	MR12	Mask for cell filter 1	r	rw	0000_H	65
73	MR20	Mask for cell filter 2	r	rw	0000_H	65
74	MR21	Mask for cell filter 2	r	rw	0000_H	65
75	MR22	Mask for cell filter 2	r	rw	0000_H	65
Transmit-Receive-Registers						
80	TXR0	Transmit Cell Register 0 (Header)	r	rw	0000_H	67
81	TXR1	Transmit Cell Register 1 (Header)	r	rw	0000_H	67
82	TXR2	Transmit Cell Register 2 (Header)	r	rw	0000_H	67
83	TXR3	Transmit Cell Register 3 (Payload)	r	rw	0000_H	68
⋮	⋮	⋮	⋮	⋮	⋮	⋮
9A	TXR26	Transmit Cell Register 26 (Payload)	r	rw	0000_H	68
9C	TMCR	Tx Command Register	rw	rw	0000_H	69
9D	RXRCEL	Receive Cell Buffer	w	r	0000_H	70
Performance Monitoring Registers						
A0	UMLOST	Upstream Max. Lost cells	r	rw	0000_H	71
A1	UMMISINS	Upstream Max. Misinserted cells	r	rw	0000_H	71
A2	UMLOST0	Upstream Max. Lost CLP0 cells	r	rw	0000_H	71
A3	UMERR	Upstream Max. Errors	r	rw	0000_H	71
A4	DMLOST	Downstream Max. Lost cells	r	rw	0000_H	72
A5	DMMISINS	Downstream Max. Misinserted cells	r	rw	0000_H	72
A6	DMLOST0	Downstream Max. Lost CLP0 cells	r	rw	0000_H	72
A7	DMERR	Downstream Max. Errors	r	rw	0000_H	72

Table 2 AOP Register Overview

adr (hex)	register	description	ASIC core	µP	reset value	see page
Scan Registers						
B0	DWDRL	DMA Write-Register (15..0)	r	rw	0000_H	74
B1	DWDRH	DMA Write-Register (31..16)	r	rw	0000_H	74
B2	DMRL	DMA Mask-Register (15.. 0)	r	rw	0000_H	75
B3	DMRH	DMA Mask-Register (31..16)	r	rw	0000_H	75
B4	PHYERRL	Port 15..0 upstream only	r	rw	0000_H	76
B5	PHYERRH	Port 23..16 upstream only	r	rw	0000_H	76
B6	DMAR	DMA-Register of DMA-FIFO	rw	r	0000_H	77
B7	DCONF	DMA configuration register	r	rw	0000_H	77
B8	SCCONF0	OAM timeout values	r	rw	0275_H	78
B9	SCCONF1	OAM timeout values	r	rw	0057_H	79
BA	SCCONF2	SCAN cycle period/tolerance	r	rw	$002D_H$	79
BB	SCCONF3	SCAN command register	r	rw	0000_H	80
BC	SCCONF4	SCAN start LCI	r	rw	0000_H	80
BD	SCCONF5	SCAN end LCI	r	rw	0000_H	81
BE	SCSTAT0	SCAN status register 0	rw	r	0000_H	81
BF	SCSTAT1	SCAN status register 1	rw	r	8000_H	82

Table 2 AOP Register Overview

adr (hex)	register	description	ASIC core	µP	reset value	see page
Interrupt Registers						
D0	ISR0	Interrupt Status Register 0	rw	rw	0000_H	83
D1	ISR1	Interrupt Status Register 1	rw	rw	0000_H	84
D2	IMR0	Interrupt Mask Register 0	r	rw	0000_H	85
D3	IMR1	Interrupt Mask Register 1	r	rw	0000_H	85
D4	CIFL	Cell Insertion Fault Port bit map (downstream)	rw	r	0000_H	85
D5	CIFH		rw	r	0000_H	85
Utopia Configuration Registers						
E0	UTCONF0	Config. UTOPIA ATM side	r	rw	0000_H	87
E1	UTCONF1	Config. UTOPIA PHY side	r	rw	0000_H	88
E2	UPRTENL	UTOPIA port 23..0 enable upstream	r	rw	0000_H	89
E3	UPRTENH		r	rw	0000_H	89
E4	DPRTENL	UTOPIA port 23..0 enable downstream	r	rw	0000_H	89
E5	DPRTENH		r	rw	0000_H	90
E6	OAMTHRU	Threshold for forced OAM cell insertion upstream	r	rw	$001E_H$	90
E7	OAMTHRD	Threshold for cell insertion downstream	r	rw	0060_H	91
E8	BPTHRD	Queue backpressure level downstream	r	rw	0060_H	91

Table 2 AOP Register Overview

adr (hex)	register	description	ASIC core	µP	reset value	see page
Miscellaneous Registers						
F0	MISC	SW reset, 1Mbit/2Mbit RAM	rw, r	rw	0000_H	92
F1	TESTR1	Test register 1	r	rw	0000_H	92
F2	TESTR2	Test register 2	r	rw	0000_H	93
F3	VERL	Version register (15.. 0)	-	r	$A06D_H$	94
F4	VERH	Version register (31..16)	-	r	$523B_H$	94
F5	BISTML	BIST Mode Low register	r	rw	0000_H	95
F6	BISTMH	BIST Mode High register	r	rw	0000_H	95
F7	BISTDON	BIST Done	rw	r	0000_H	96
F8	BISTERR	BIST Error	rw	r	0000_H	97

3.1 Transfer Registers

These registers are provided for data transfer to and from the external connection RAMs or the internal RAMs.Two internal RAMs are provided, one for PM data processing and one for the collection of analysed PM results. Both PM RAMs are shared for up- and downstream direction. The entries in each RAM have different sizes as shown in **Table 3**.

Table 3 Internal and external RAMs

RAM type	Location	Number of entries	Dwords per entry
Upstream connection RAM	External	4 - 16k*	8
Downstream connection RAM	External	4 - 16k*	8
PM processing data	On-chip	128	3
PM data collection	On-chip	128	14

* Depending on external RAM size

There is only one single RAM access type, the read-modify-write transfer shown in **figure 32**.

It consists of two steps: in the first step all data from the specified RAM entry is transferred into the read register set RDR. In the second step the data is written back again. It can be either the original data or new data specified in the write register set WDR. The decision if original or new data is written to the RAM entry is done via the mask register set MDR and the mask register WMASK. For the lower 7 Dwords of an entry the source of each single bit can be individually selected by the corresponding bit of the respective MDR register (bit-by-bit basis), for the upper 7 Dwords one single bit of WMASK selects the source for a whole Dword.

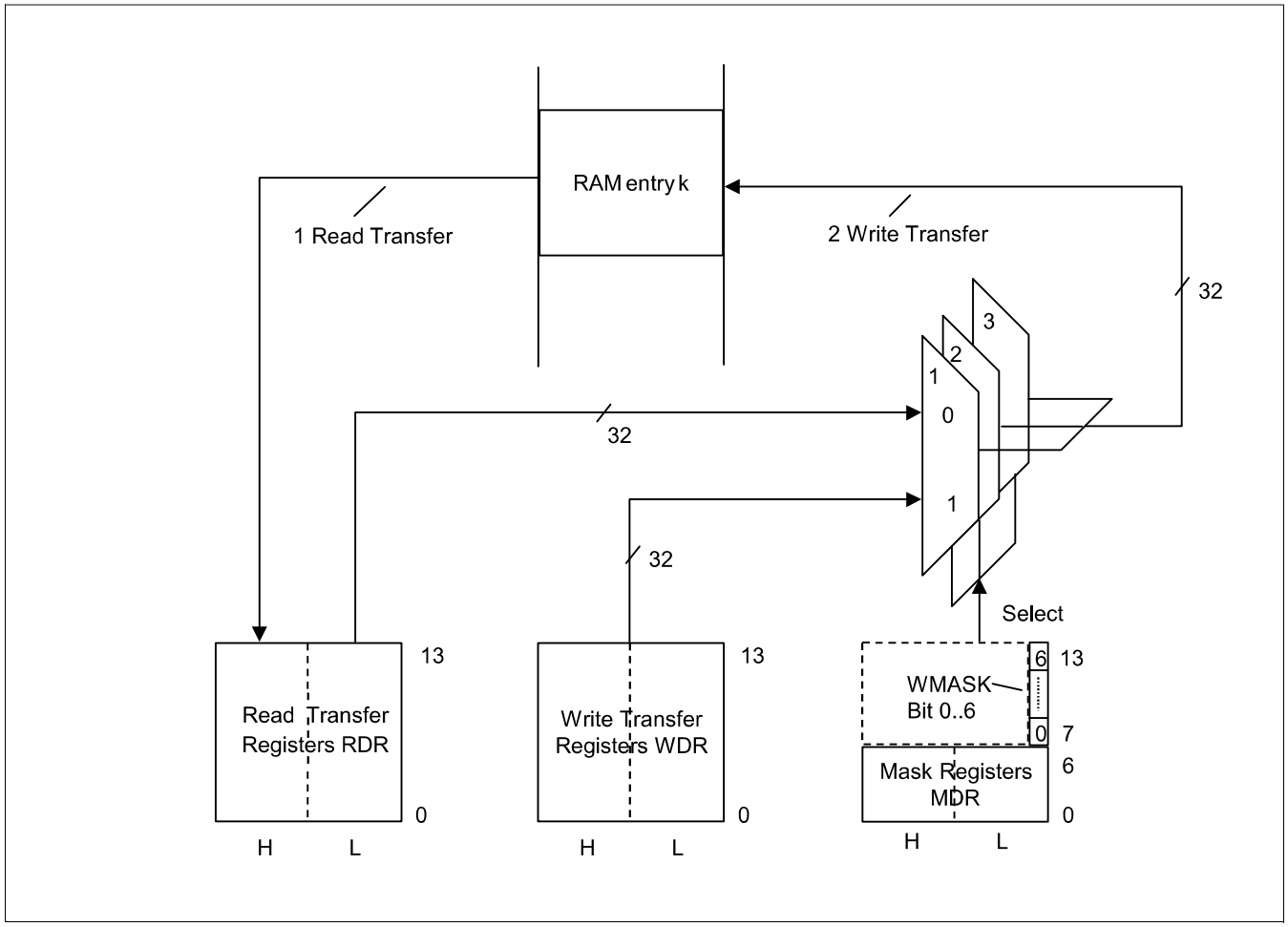


Figure 32 Read-modify-write Transfer

The address of the selected entry is given in register RMWADR. Register bits for specifying the target RAM and initiating the transfer are contained in the read-modify-write control register RMWC. This register also contains command bits for setting or clearing all mask register bits.

Read and write register sets RDR and WDR contain 14 Dwords in 28 registers. For simplification the mask register set is slightly different: MDR0..6 have a one-to-one bit mapping with RDR0..6 and WDR0..6. For RDR7..13 and WDR7..13 one single mask bit for each Dword is provided in the WMASK register, bits 0..6.

When accessing RAM entries with less than 14 Dwords (see **Table 3**) only the lower registers of RDR, WDR and MDR are involved, e.g. for accesses to the 8-Dword size entries of the external connection tables RDR0..7, WDR0..7, MDR0..6 and bit 0 of WMASK are involved.

For accesses to the different RAMs the RDR and WDR register bits have different meaning. This is described for each target RAM in the mapping tables (see **section 3.9**).

3.1.1 Write Transfer Registers (WDR0L..WDR13H)

Read/write Address 00_H..$1B_H$
Value after reset 0000_H

The write transfer registers are shown below with their mapping to the 32-bit Dwords 0..13.

Dword	31 23	15 7 0
13	Register WDR13H / Address $1B_H$	Register WDR13L / Address $1A_H$
12	Register WDR12H / Address 19_H	Register WDR12L / Address 18_H
11	Register WDR11H / Address 17_H	Register WDR11L / Address 16_H
10	Register WDR10H / Address 15_H	Register WDR10L / Address 14_H
9	Register WDR9H / Address 13_H	Register WDR9L / Address 12_H
8	Register WDR8H / Address 11_H	Register WDR8L / Address 10_H
7	Register WDR7H / Address $0F_H$	Register WDR7L / Address $0E_H$
6	Register WDR6H / Address $0D_H$	Register WDR6L / Address $0C_H$
5	Register WDR5H / Address $0B_H$	Register WDR5L / Address $0A_H$
4	Register WDR4H / Address 09_H	Register WDR4L / Address 08_H
3	Register WDR3H / Address 07_H	Register WDR3L / Address 06_H
2	Register WDR2H / Address 05_H	Register WDR2L / Address 04_H
1	Register WDR1H / Address03_H	Register WDR1L / Address 02_H
0	Register WDR0H / Address 01_H	Register WDR0L / Address 00_H

When accessing the external RAM bit 31 of each Dword controls the parity bit of the entry. If bit 31=0 the correct parity bit is generated. If bit 31=1 the parity bit is inverted.

3.1.2 Read Transfer Registers (RDR0L..RDR13H)

Read Address $1C_H..37_H$
Value after reset 0000_H

The read transfer registers are shown below with their mapping to the 32-bit Dwords 0..13.

Dword	31 23	15 7 0
13	Register RDR13H / Address 37_H	Register RDR13L / Address 36_H
12	Register RDR12H / Address 35_H	Register RDR12L / Address 34_H
11	Register RDR11H / Address 33_H	Register RDR11L / Address 32_H
10	Register RDR10H / Address 31_H	Register RDR10L / Address 30_H
9	Register RDR9H / Address $2F_H$	Register RDR9L / Address $2E_H$
8	Register RDR8H / Address $2D_H$	Register RDR8L / Address $2C_H$
7	Register RDR7H / Address $2B_H$	Register RDR7L / Address $2A_H$
6	Register RDR6H / Address 29_H	Register RDR6L / Address 28_H
5	Register RDR5H / Address 27_H	Register RDR5L / Address 26_H
4	Register RDR4H / Address 25_H	Register RDR4L / Address 24_H
3	Register RDR3H / Address 23_H	Register RDR3L / Address 22_H
2	Register RDR2H / Address 21_H	Register RDR2L / Address 20_H
1	Register RDR1H / Address $1F_H$	Register RDR1L / Address $1E_H$
0	Register RDR0H / Address $1D_H$	Register RDR0L / Address $1C_H$

When reading the external RAM bit 31 contains the result of the parity check. Bit 31=0 indicates that the external parity bit stored in bit 31 was correct, bit 31=1 indicates a wrong parity bit.

3.1.3 Mask Data Registers (MDR0L..MDR6H)

Read/write Address $38_H..45_H$
Value after reset 0000_H

These registers have a bit-to-bit correspondence to the 7 lower read and write transfer registers RDR0..RDR6 and WDR0..WDR6. If a bit in MDR0L..MDR6H is cleared, the corresponding bit of the RAM entry remains unchanged, if set the RAM entry bit is overwritten by the value contained in the corresponding write register bit.

The upper 7 transfer registers are masked globally with one bit each. These bits are contained in the WMASK register.

The mask data registers are shown below with their mapping to the 32-bit Dwords 0..6.

Dword	31 … 23	15 … 7 … 0
6	Register MDR6H / Address 45_H	Register MDR6L / Address 44_H
5	Register MDR5H / Address 43_H	Register MDR5L / Address 42_H
4	Register MDR4H / Address 41_H	Register MDR4L / Address 40_H
3	Register MDR3H / Address $3F_H$	Register MDR3L / Address $3E_H$
2	Register MDR2H / Address $3D_H$	Register MDR2L / Address $3C_H$
1	Register MDR1H / Address $3B_H$	Register MDR1L / Address $3A_H$
0	Register MDR0H / Address 39_H	Register MDR0L / Address 38_H

3.1.4 Write Mask Register (WMASK)

Read/write Address 46_H
Value after reset 0000_H

15 … 8							
Unused							
7							**0**
Unused	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 6	Mask for Dword 13.
Bit 5	Mask for Dword 12.
Bit 4	Mask for Dword 11.
Bit 3	Mask for Dword 10.
Bit 2	Mask for Dword 9.
Bit 1	Mask for Dword 8.
Bit 0	Mask for Dword 7.

3.1.5 Read-Modify-Write Control Register (RMWC)

Read/write Address 47_H
Value after reset 0000_H

15					8
Unused					

7					0
Unused	RAMSEL(1:0)	START	UP/$\overline{DN}$	WRA	RDA

RAMSEL(1:0)	Select RAM for RMW access	
	00	PM data processing RAM
	01	External RAM (up- or downstream selected with bit 2).
	1x	PM data collection RAM
START	Command bit. Set =1 to start the RMW-access specified with bits 2, 4 and 5. Bit 3 is reset after execution of the command. RDR registers should not be read before, otherwise it will result in unexpected values.	
UP/$\overline{DN}$	Selection of external RAM for RMW-Access:	
	0	Downstream-RAM.
	1	Upstream-RAM.
WRA	Write all. Setting this bit together with the START bit sets all mask register bits to one **before** the RMW access. This results in a write access of the whole entry. All Dwords of the specified entry are overwritten. The mask bits remain cleared after the access. WRA is reset to zero after execution of the RMW access.	
RDA	Read all. Setting this bit together with the START bit sets all mask register bits to zero **before** the RMW access. This results in a read only access. No data in the specified entry is modified. The mask bits remain set after the access. RDA is reset to zero after execution of the RMW access.	

Note: The select bits RAMSEL(1:0), UP/$\overline{DN}$ *and RDA or WRA can be set together with the START bit in the same write access.*

Note: RDA and WRA must not be set simultaneously.

Note: Register RMWC is write protected as long as START is set.

3.1.6 Read-Modify-Write Address Register (RMWADR)

Read/write Address 48_H
Value after reset 0000_H

15	8
Unused	ADR(13:8)
7	**0**
ADR(7:0)	

ADR(13:0)	Specifies the base address for the RMW access. In 4x1M mode the bits 13..12 selects the RAM, the bits 11..0 defines the address. In 2x2M mode the bit 13 selects the RAM and the bits 12..0 defines the address. Should not be outside the physical range of the respective RAM (see **Table 3**).

Note: Register RMWADR is write protected as long as the START bit of RMWC is set.

3.2 Registers for Celltype Recognition

3.2.1 Location / Source Identifier Registers (LSIDR0..7)

Read/write Address $60_H..67_H$
Value after reset 0000_H

Addr	Name	15 8	7 0
60	LSIDR0	Port ID byte #15	Port ID byte #14
61	LSIDR1	Port ID byte #13	Port ID byte #12
62	LSIDR2	Port ID byte #11	Port ID byte #10
63	LSIDR3	Port ID byte #9	Port ID byte #8
64	LSIDR4	Port ID byte #7	Port ID byte #6
65	LSIDR5	Port ID byte #5	Port ID byte #4
66	LSIDR6	Port ID byte #3	Port ID byte #2
67	LSIDR7	Port ID byte #1	Port ID byte #0

The 16-octet Port ID defines a unique identifier for the switch port. It is used for intra-domain LB cells. Depending on layer point configuration and settings the Port ID is compared with Location or Source ID of the LB cell.

3.2.2 Special OAM Cell Filter (CTR0, CTR1)

Read/write Address $68_H..69_H$
Value after reset 0000_H

Both CTR0 and CTR1 have the same mapping:

15 8	
Unused	ACTION(1:0)
7	**0**
OAMTYP(3:0)	FUNCTYP(3:0)

Using these registers two OAM cell types can be defined. OAM cells in the cell stream which match a programmed pattern are treated according to the four options defined in the corresponding ACTION(1:0) bits. The action is executed for all matching cells in up- and downstream direction. This function is provided to support new or proprietary OAM cell types. These could be dropped to the microprocessor and handled by SW.

Recognized as OAM cells are: all cells with either PTI=100 or 101 or VCI=3 or 4 and which have the correct CRC-10. OAM cells with incorrect CRC-10 are discarded anyway with notification in interrupt status register ISR0 and additionally an indication in the external connection RAM entry for the respective connection (LCI).

ACTION(1:0)	Action in case of cell filter match	
	00	Ignore cell. Use this selection to disable the function.
	01	Discard cell.
	10	Drop cell; the cell is extracted from the cell stream and stored in the receive buffer.
	11	Monitor cell; the cell is copied into the receive buffer.
OAMTYP(3:0)	Defines the OAM Type bits of the OAM cell to be filtered.	
FUNCTYP(3:0)	Defines the Function Type bits of the OAM cell to be filtered.	

3.2.3 Cell Filter 1 and 2 Registers (CTRxy, MRxy)

Read/write Address $6A_H..75_H$
Value after reset 0000_H

Using these 12 registers two free programmable cell types can be filtered. The complete UTOPIA cell header (including 5 bits of the UDF1 octet but without the UDF2 octet) and the first payload octet are compared. Each bit within these six octets can be individually masked by setting the corresponding mask bit to one. Masked bits match anyway, unmasked bits must match with the corresponding bit in the passing cells.

The programmed patterns are compared to all cells in up- and downstream direction. If all unmasked bits match one of the four actions defined in the action bits (8 and 9 of words CTRx2) is executed for the cell.

This function can be used to treat selected cells by SW, e.g. by extracting them from the cell stream and processing them by SW. This could be OAM cells or any other type of cells, e.g. RM cells or internal message cells.

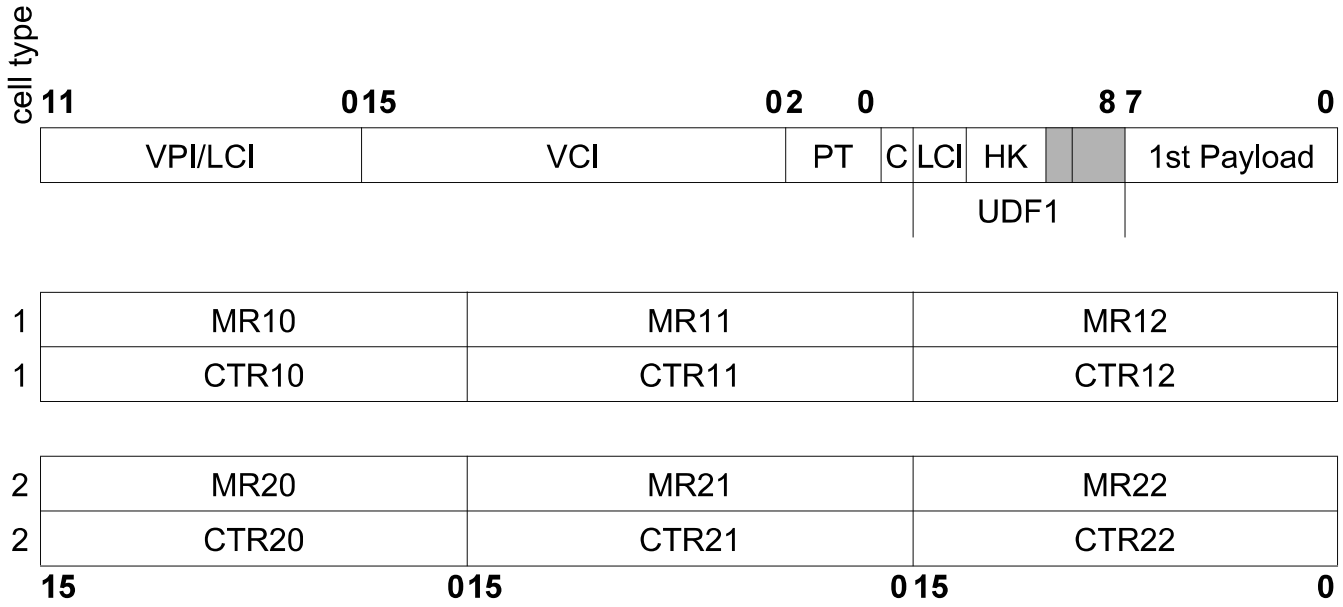
In addition four pins are provided to indicate the match of filter 1 or 2 in up- and downstream direction. These detector pins are activated upon match if not disabled via ACTION(1:0)=00.

Table 4 Cell Filter Detector Outputs

Match of Cell Filter	Direction	Activated Pin
1	upstream	FPCT1U
1	downstream	FPCT1D
2	upstream	FPCT2U
2	downstream	FPCT2D

The match signals of the indication pins FPCTxy can be used e.g. to determine the CDV of a certain connection with external evaluation circuitry.

Programming of the two cell filters is identical:



Only the 5 MSBs of the UDF1 octet are compared. The 3 LSBs are treated like masked and match always. In case of the proprietary cell format UDF1(7:3) contains the two MSBs of the LCI and the housekeeping bits. See **Figures 35** and **36** for cell formats.

CTRxy, MRxy	Meaning of the indices x, y:	
	x	Selects filter 1 or filter 2.
	y	Selects one of the three registers for each filter.
Bit 10 of CTRx2	Unused	
Bit 9,8 of CTRx2	Define the action to be done in case of match:	
	00	Ignore cell. Use this selection to disable the function.
	01	Discard cell.
	10	Drop cell; the cell is extracted from the cell stream and stored in the receive buffer.
	11	Monitor cell; the cell is copied into the receive buffer.

3.3 Transmit / Receive Registers

These registers are used to insert ATM cells into the cell stream and to extract or copy cells from the cell stream. For the insertion one set of 27 registers (TXR0...TXR26) is provided capable of storing a complete ATM cell in UTOPIA cell format. When assembled the ATM cell is inserted into either up- or downstream data stream via the command register TMCR. For cell extraction/ copy an internal 12-cell receive buffer is provided. A non-empty receive buffer is signalled via bit 9 of interrupt status register ISR0. Cells are read from the internal receive buffer by repeated reading of the RXRCEL register.

3.3.1 Transmit Cell Header Registers (TXR0..2)

Read/write Address 80_H...82_H
Value after reset 0000_H (for all)

Addr.	Name	15 8	7 0	
80	TXR0	Header octet 1	Header octet 2	
81	TXR1	Header octet 3	Header octet 4	
82	TXR2	UDF1(7:0)	UDF2(7:5)	PN(4:0)

Header octets 1..4 as well as UDF1 and UDF2 octets are mapped transparently to the cell. The only field which is interpreted by the AOP is PN(4:0); it selects the (internal) PHY port number the cell is destined to. For the determination of the UTOPIA port number and header formats see **section 5.1**. In case of 8-bit UTOPIA PN(4:0) is evaluated but not transferred to the data stream.

3.3.2 Transmit Cell Payload Registers (TXR3..TXR26)

Read/write Address 83_H...$9A_H$
Value after reset 0000_H (for all)

Addr.	Name	15 8	7 0
83	TXR3	Payload octet 1	Payload octet 2
84	TXR4	Payload octet 3	Payload octet 4
85	TXR5	Payload octet 5	Payload octet 6
86	TXR6	Payload octet 7	Payload octet 8
87	TXR7	Payload octet 9	Payload octet 10
88	TXR8	Payload octet 11	Payload octet 12
89	TXR9	Payload octet 13	Payload octet 14
8A	TXR10	Payload octet 15	Payload octet 16
8B	TXR11	Payload octet 17	Payload octet 18
8C	TXR12	Payload octet 19	Payload octet 20
8D	TXR13	Payload octet 21	Payload octet 22
8E	TXR14	Payload octet 23	Payload octet 24
8F	TXR15	Payload octet 25	Payload octet 26
90	TXR16	Payload octet 27	Payload octet 28
91	TXR17	Payload octet 29	Payload octet 30
92	TXR18	Payload octet 31	Payload octet 32
93	TXR19	Payload octet 33	Payload octet 34
94	TXR20	Payload octet 35	Payload octet 36
95	TXR21	Payload octet 37	Payload octet 38
96	TXR22	Payload octet 39	Payload octet 40
97	TXR23	Payload octet 41	Payload octet 42
98	TXR24	Payload octet 43	Payload octet 44
99	TXR25	Payload octet 45	Payload octet 46
9A	TXR26	Payload octet 47	Payload octet 48

Note: Address $9B_H$ is unused.

All octets are mapped transparently into the transmitted cell. In case the automatic CRC-10 generation is enabled the two LSBs of octet 47 and octet 48 will be overwritten. The 6 MSBs of octet 47 are mapped transparently into the cell. Hence to be conform to the standardized OAM cell format these bits must be programmed to zero before inserting an OAM cell.

3.3.3 Transmission Command Register (TMCR)

Read/write Address $9C_H$
Value after reset 0000_H

15							8
Unused							
7							**0**
Unused					ENCRC	TXUP	TXDN

ENCRC	Enable automatic CRC-10 generation of inserted cell	
	0	No automatic CRC10. Must be provided by µP.
	1	CRC10 automatically generated by AOP. It is inserted into payload octets 47 and 48 (see **section 8.2**).
TXUP	Writing this bit to 1 initiates insertion of the cell specified in registers 80...9A into upstream data path. Insertion is done with the next available free cell cycle. After completed insertion TXUP is reset.	
TXDN	Writing this bit to 1 initiates insertion of the cell specified in registers 80_H...$9A_H$ into the downstream data path. Insertion is done with the next available free cell cycle. After completed insertion TXDN is reset.	

Note: It is not possible to set both TXUP and TXDN simultaneously; TXUP will be set.

Note: The cell transmit registers TXR0...13 and the transmit command register TMCR itself are write protected as long as one of the insertion command bits TXUP or TXDN is set. This avoids erroneous modification of the cell during the transmission phase.

3.3.4 Receive Cell Buffer Read Register (RXRCEL)

Read Address $9D_H$
Value after reset 0000_H

15							8
RXRCEL(15:8)							
7							**0**
RXRCEL(7:0)							

RXRCEL(15:0) Receive Cell Buffer access. A cell extracted or copied from the data stream is transferred from the internal receive buffer to the microprocessor by 27 read accesses of RXRCEL. The accesses need not be consecutive; it is allowed to access other registers in between.

Received cell(s) are indicated with bit 9 of ISR0 set. After read-out of the last cell ISR0(9) is reset by the AOP.

Cell format of the extracted cell is:

Read Access	**15** 8	**7** 0
1st access	Header octet 1	Header octet 2
2nd access	Header octet 3	Header octet 4
3rd access	UDF1(7:0)	7 | 6 | UDF2(5:0)
4th access	Payload octet 1	Payload octet 2
: :	: :	: :
27th access	Payload octet 47	Payload octet 48

The cell format is identical to the insertion cell format except the UDF2 octet:

Bit 7 UDF2(7) of the extracted cell (don't care in case of 8-bit UTOPIA)

Bit 6 Source of the received cell (overwrites UDF2(6) of extracted/copied cell) :

0 Cell from downstream direction

1 Cell from upstream direction

UDF2(5:0) 6 LSBs of the UDF2 octet of the extracted cell (don't care in case of 8-bit UTOPIA).

3.4 Performance Monitoring Configuration Registers

These registers define the thresholds in the PM data collection algorithm described in **figure** 26. The referenced counters are located in the PM Data Collection RAM (see **section** 3.9.6).

3.4.1 Upstream Maximum Lost cells (UMLOST)

Read/write Address $A0_H$
Value after reset 0000_H

Recommended value 0003_H.

UMLOST(15:0) holds the global MLOST threshold (CLP0+1 cells) for the PM data collection in upstream direction. A PM block with more than MLOST lost cells is considered severely errored by the data collection algorithm. Accordingly the SECB counter is incremented. If less or equal MLOST cells are missing the lost cell counters are incremented.

3.4.2 Upstream Maximum Misinserted cells (UMMISINS)

Read/write Address $A1_H$
Value after reset 0000_H

Recommended value 0002_H.

UMISINS(15:0) holds the global MMISINS threshold for the PM data collection in upstream direction. A PM block with more than MMISINS misinserted cells is considered severely errored by the data collection algorithm. Accordingly the SECB counter is incremented. If less or equal MMISINS cells are misinserted the misinserted cell counters are incremented.

3.4.3 Upstream Maximum Lost CLP0 cells (UMLOST0)

Read/write Address $A2_H$
Value after reset 0000_H

Recommended value 0003_H.

UMLOST0(15:0) holds the global MLOST0 threshold (CLP0 cells only) for the PM data collection in upstream direction. A PM block with more than MLOST0 lost cells is considered severely errored by the data collection algorithm. Accordingly the SECB counter is incremented. If less or equal MLOST0 cells are missing the lost cell counters are incremented.

3.4.4 Upstream Maximum Errors (UMERR)

Read/write Address $A3_H$
Value after reset 0000_H

Recommended value 0003_H.

UMERR(15:0) holds the global MERR threshold for the PM data collection in upstream direction. A BR cell carrying a block error result BLER value greater than MERR denotes a severely errored block. Accordingly the SECB counter is incremented. If BLER is less or equal MERR the BLER value is added to the error counter ERRC.

3.4.5 Downstream Maximum Lost cells (DMLOST)

Read/write Address $A4_H$
Value after reset 0000_H

Recommended value 0003_H.

DMLOST(15:0) holds the global MLOST threshold (CLP0+1 cells) for the PM data collection in downstream direction. A PM block with more than MLOST lost cells is considered severely errored by the data collection algorithm. Accordingly the SECB counter is incremented. If less or equal MLOST cells are missing the lost cell counters are incremented.

3.4.6 Downstream Maximum Misinserted cells (DMMISINS)

Read/write Address $A5_H$
Value after reset 0000_H

Recommended value 0002_H.

DMMISINS(15:0) holds the global MMISINS threshold for the PM data collection in downstream direction. A PM block with more than MMISINS misinserted cells is considered severely errored by the data collection algorithm. Accordingly the SECB counter is incremented. If less or equal MMISINS cells are misinserted the misinserted cell counters are incremented.

3.4.7 Downstream Maximum Lost CLP0 cells (DMLOST0)

Read/write Address $A6_H$
Value after reset 0000_H

Recommended value 0003_H.

DMLOST0(15:0) holds the global MLOST0 threshold (CLP0 cells only) for the PM data collection in downstream direction. A PM block with more than MLOST0 lost cells is considered severely errored by the data collection algorithm. Accordingly the SECB counter is incremented. If less or equal MLOST0 cells are missing the lost cell counters are incremented.

3.4.8 Downstream Maximum Errors (DMERR)

Read/write Address $A7_H$
Value after reset 0000_H

Recommended value 0003_H.

DMERR(15:0) holds the global MERR threshold for the PM data collection in downstream direction. A BR cell carrying a block error result BLER value greater than MERR denotes a severely errored block. Accordingly the SECB counter is incremented. If BLER is less or equal MERR the BLER value is added to the error counter ERRC.

3.5 Scan Registers

The SCAN performs the OAM functions AIS, RDI and CC for all connections. It must be triggered by the microprocessor in 500 ms intervals. The SCAN procedure goes through all requested entries of the external connection memory, reads the data and writes back updated information. E.g. the SCAN checks if user cells has been received, increments counters and accordingly performs transitions in the AIS/RDI/CC state diagrams. Also AIS/RDI/CC cell insertion is done by the scan. The SCAN starts with the lower LCI bound programmed by the user and ends at the higher LCI bound. If for a connection a cell is to be inserted the SCAN halts the user cell stream for one cell cycle. The user cells are buffered intermediately (see **figure** 12).

A SCAN cycle of one LCI lasts 32 clock cycles like a cell access. It uses idle times, i.e. it is initiated if no complete cell is available in the input UTOPIA buffer. Hence a certain number of idle cell cycles is needed by the SCAN to do its work. The idle cell cycles can be calculated from the difference between the sum of PHY payload rates and the maximum cell processing rate of the PXB 4340 AOP. **Table 5** shows some example values for SCAN period times as a function of PHY payload rates. It can be seen that 673 Mbit/s is the highest possible aggregate PHY payload rate if 16 K connections are used.

Table 5 SCAN periods for a core clock of 51.84 MHz

Sum of PHY payload rates	Cell cycles used for user cells	Cell cycles available for SCAN	Minimum SCAN period for 16384 connections
600 Mbit/s	1.415 Mcells/s	204 906 cycles/s	80 ms
625 Mbit/s	1.474 Mcells/s	145 943 cycles/s	112 ms
650 Mbit/s	1.533 Mcells/s	86 981 cycles/s	188 ms
673 Mbit/s	1.587 Mcells/s	32 768 cycles/s	500 ms
687 Mbit/s	1.620 Mcells/s	0	not possible

The SCAN periods in **Table 5** are minimum values, as additional idle cycles occur if the PHYs user cell rate is below 100%. A typical link load value is <100%. The spare bandwidth is used for OAM cell insertion and microprocessor accesses to the external RAMs.

While the SCAN mechanism processes the entries of all connections the DMA function can be activated. The read value of one specified Dword of each entry can be transferred to the microprocessor via a 32-entry DMA buffer. The occupied DMA buffer is signalled to the microprocessor via the MPDREQ pin. Also selected bits of the specified DMA entry can be overwritten during the DMA process, e.g. to clear state transition flags.

With the Compressed DMA option a special Dword with a collection of state transition and status flags is transferred to the DMA buffer during the scan. This option allows to check the status of all connections rapidly.

Note: The SCAN registers are write protected during the SCAN mechanism is running (SCSTAT0.SCAN_ACT0 = '1').

3.5.1 DMA Write Register 15..0 (DWDRL)

Read/write Address $B0_H$
Value after reset 0000_H

15	8
DWDRL(15:8)	
7	**0**
DWDRL(7:0)	

DWDRL(15:0)	DMA Write Register(15:0), specifies the lower 16-bit of the Dword to be written into the external connection RAM via DMA. The bit positions to be overwritten in the connection RAM Dword are specified with the associated mask register DMRL, the Dword of the RAM entry is selected by DCONF.INDEX.

3.5.2 DMA Write Register 31..16 (DWDRH)

Read/write Address $B1_H$
Value after reset 0000_H

15		8
SP	DWDRH(14:8)	
7		**0**
DWDRH(7:0)		

SP	Select Parity: if SP=0 the correct parity is generated when the dword is transferred to the external RAM; if SP=1 a false parity bit is generated.
DWDRH(14:0)	DMA Write Register(31:16), specifies the upper 16-bit of the Dword to be written into the external connection RAM via DMA. The bit positions to be overwritten in the connection RAM Dword are specified with the associated mask register DMRL, the Dword of the RAM entry is selected by DCONF.INDEX.

3.5.3 DMA Mask Register 15..0 (DMRL)

Read/write Address $B2_H$
Value after reset 0000_H

15	8
DMRL(15:8)	
7	**0**
DMRL(7:0)	

DMRL(15:0)	DMA Mask Register(15:0):	
	0	Bit is unchanged.
	1	Bit is replaced by corresponding DWDR-Bit, used for RMW operation on external RAM word selected by DCONF.INDEX.

3.5.4 DMA Mask Register High 31..16 (DMRH)

Read/write Address $B3_H$
Value after reset 0000_H

15	8
DMRH(15:8)	
7	**0**
DMRH(7:0)	

DMRH(15:0)	DMA Mask Register(31:16):	
	0	Bit is unchanged.
	1	Bit is replaced by corresponding DWDR-Bit, used for RMW operation on external RAM word selected by DCONF.INDEX.

3.5.5 PHY Error Indication 15..0 (PHYERRL)

Read/write Address $B4_H$
Value after reset 0000_H

15	8
PHYERRL(15:8)	
7	**0**
PHYERRL(7:0)	

PHYERRL(15:0) These bits have a one-to-one correspondence with the PHYs that are connected to the switch port. In case of an interruption of the physical transmission (e.g. laser failure) the microprocessor sets the respective PHYERR bit. The SCAN mechanism uses this indication together with the PHY number stored in each connection entry of the upstream external RAM (see **section 3.9.1.1**) to generate AIS cells.

PHYERR bits are used in upstream direction only.

3.5.6 PHY Error Indication 23..16 (PHYERRH)

Read/write Address $B5_H$
Value after reset 0000_H

15	8
Unused	
7	**0**
PHYERRL(23:16)	

PHYERRH(23:16) These bits have a one-to-one correspondence with the PHYs that are connected to the switch port. In case of an interruption of the physical transmission (e.g. laser failure) the microprocessor sets the respective PHYERR bit. The SCAN mechanism uses this indication together with the PHY number stored in each connection entry of the upstream external RAM (see **section 3.9.1.1**) to generate AIS cells.

PHYERR bits are used in upstream direction only.

3.5.7 DMA Read Register (DMAR)

Read Address $B6_H$
Value after reset 0000_H

15							8
DMAR(15:8)							
7							**0**
DMAR(7:0)							

DMAR(15:0)	DMA Read Register of DMA-FIFO (32 words deep). The external DMA controller has to be programmed to read this address.

Note: Output sequence of DMA data:
32 bit from the external RAM are always output as 2 consecutive 16 bit words.
Bits 31..16 are always located in the first word, 15..0 in the second word.
Hereby bit 31 always indicates the source:
0 = from downstream RAM
1 = from Upstream RAM.

3.5.8 DMA Configuration Register (DCONF)

Read/write Address $B7_H$
Value after reset 0000_H

15							8
Unused							
7							**0**
Unused				DMAEN	MODE	INDEX(2:0)	

DMAEN	Enable $\overline{\text{MPDREQ}}$ output signal:
	0 $\overline{\text{MPDREQ}}$ is always tristate and $\overline{\text{MPDACK}}$ is not evaluated.
	1 $\overline{\text{MPDREQ}}$ gets low impedance if DMA is requested, otherwise tristate. $\overline{\text{MPDREQ}}$ is $\overline{\text{MPDACK}}$ controlled.
MODE	Selects standard DMA or compressed DMA
	0 Standard DMA: 32 bit RMW operation on Dword of LCI entry selected with INDEX(2:0) using DWDR and DMR.
	1 Compressed DMA: 32 bit RMW operation on all interrupt relevant flags in LCI entry, no influence of DWDR, for bit mapping see **section** 4.1.6.1.
INDEX(2:0)	Selects which word (0..7) in the LCI table is object of the RMW operation of standard DMA. INDEX is don't care in compressed mode (MODE=1).

3.5.9 Time Constant Register 0 (SCCONF0)

Read/write Address $B8_H$
Value after reset 0275_H

15							8
Unused							MAXTS(1:0)
7							**0**
MAXTR(3:0)				CCDEFMAX(3:0)			

MAXTS(1:0)	Time for generation of CC cells if no user cell has arrived in the CC generation. Counted in multiples of SCAN cycles (typ. 500 ms).
MAXTR(3:0)	Time for transition from normal operation to LOC defect state in the CC evaluation. Counted in multiples of SCAN cycles (typ. 500 ms).
CCDEFMAX(3:0)	Time for transition from LOC defect to LOC failure state in the CC evaluation. Counted in multiples of SCAN cycles (typ. 500 ms).

3.5.10 Time Constant Register 1 (SCCONF1)

Read/write Address $B9_H$
Value after reset 0057_H

15							8
F4F5 PROP	Unused						
7							**0**
Unused	IDLEMAX(2:0)			ARDEFMAX(3:0)			

F4F5PROP — Control forced AIS/RDI cell generation (ARINS bit in external RAM) behaviour at F4TEP:

- 0 — Generate 'F4RDI only' if ARINS is set.
- 1 — Generate 'F4RDI and F5AIS for all included VCCs if ARINS is set.

IDLEMAX(2:0) — Time for transition from AIS defect/failure to normal operation or from RDI defect/failure to normal operation. Counted in multiples of SCAN cycles.

ARDEFMAX(3:0) — Time for transition from AIS defect to AIS failure state or RDI defect to RDI failure state. Counted in multiples of SCAN cycles.

Note: The typical value for the SCAN cycle period is 500ms.

3.5.11 Time Constant Register 2 (SCCONF2)

Read/write Address BA_H
Value after reset $002D_H$

15							8
SCPTOL(5:0)						SCP(9:8)	
7							**0**
SCP(7:0)							

SCPTOL(5:0) — Scan cycle tolerance: (maximum time - minimum time) for complete processing of 1 LCI counted in cell cycles).

Note: SCP must be > 0 for SCPTOL usage !

SCP(9:0) — Scan cycle period: minimum time for processing of 1 LCI counted in cell cycles; necessary for equal distribution of OAM cells over 1 scan cycle, avoids OAM bursts generated by SCAN).

- 0 — Disables SCAN.

3.5.12 SCAN Command Register (SCCONF3)

Read/write Address BB_H
Value after reset 0000_H

15			8
Unused	DMA UP	OAM UP	Unused
7			**0**
Unused	DMA DN	OAM DN	START SC

DMAUP	Select SCAN with DMA transfer upstream.
OAMUP	Select SCAN with OAM processing upstream.
DMADN	Select SCAN with DMA transfer downstream.
OAMDN	Select SCAN with OAM processing downstream.
STARTSC	Start Scan up- and downstream with the selected processing. This bit is set by the microprocessor every 500 ms. As soon as the SCAN mechanism is started, this bit is reset to 0. The select bits can be defined with the same write access.

The select bits are modified only by the microprocessor. The SCAN start bit is set by the microprocessor and reset by the AOP immediately after the start of the SCAN. To determine the termination of the scan refer to the SCAN Status Register below.

3.5.13 Lower Boundary of LCI Range (SCCONF4)

Read/write Address BC_H
Value after reset 0000_H

15	8
Unused	LCIMIN(13:8)
7	**0**
LCIMIN(7:0)	

LCIMIN(13:0)	Lower boundary of LCI range processed by SCAN (up- and downstream).

3.5.14 Upper Boundary of LCI Range (SCCONF5)

Read/write Address BD_H
Value after reset 0000_H

15							8
Unused							LCIMAX(13:8)
7							**0**
LCIMAX(7:0)							

LCIMAX(13:0)	Upper boundary of LCI range processed by SCAN (up- and downstream).

3.5.15 SCAN Status Register (SCSTAT0)

Read only Address BE_H
Value after reset 0000_H

15					8
Unused	CGENP	DMAD	OAMD	UTOG	Unused
7					**0**
Unused	CGENP	DMAD	OAMD	DTOG	SCAN ACT[1]

CGENP	Upstream cell generation pending, internal state for debugging.
DMAD	Upstream DMA done, internal state for debugging.
OAMD	Upstream OAM done, internal state for debugging.
UTOG	Upstream toggle flag, used for VP processing once in a SCAN cycle.
CGENP	Downstream Cell generation pending, internal state for debugging.
DMAD	Downstream DMA done, internal state for debugging.
OAMD	Downstream OAM done, internal state for debugging.
DTOG	Downstream toggle flag, used for VP processing once in a SCAN cycle.
SCANACT[1]	SCAN mechanism was started and has not yet finished.

Note: The 'scan finished' condition is: SCANACT = '0' and SCCON3.STARTSC = '0'.

3.5.16 Currently Processed LCI (SCSTAT1)

Read only Address BF_H
Value after reset 8000_H

15		8
DE	DF	LCIS(13:8)
7		**0**
LCIS(7:0)		

DE	DMA buffer empty = 0 words in FIFO.
DF	DMA buffer full ≥ 32 words in FIFO.
LCIS(13:0)	Currently processed LCI up- and downstream. Internal state for debugging.

Note: In applications SCAN has to be started by the µP every 500ms, the times given here are based on this timing. In the HW the settings above represent 'Number of SCAN cycles'. For test SCAN may be started in arbitrary time periods.

3.6 Interrupt and Interrupt Mask Registers

Interrupt bits signal unpredictable events to the controlling microprocessor, e.g. errors. Each interrupt bit signals a different event. Events which are associated to a certain connection, as e.g. the misinserted OAM cell interrupt are stored additionally also in the external connection RAM under the respective LCI entry. If one of these interrupt indications is set the corresponding error might have occured for at least one or more connections. Thus the microprocessor has to check all entries of the connection RAM dedicated to the respective direction for the indicated error.

To clear interrupt bits the microprocessor must write a '1' to the respective bit. Writing a '0' has no effect. This behaviour simplifies interrupt management by separate interrupt routines. After a HW interrupt more than one interrupt bit might be set. Then each interrupt routine can clear the respective bit separately after having checked or corrected the interrupt cause.

3.6.1 Interrupt Status Register 0 (ISR0)

Read/write Address $D0_H$
Value after reset 0000_H

Bit 15	UUPED	UTOPIA parity error detected upstream.
Bit 14	DUPED	UTOPIA parity error detected downstream.
Bit 13	UUSOCE	UTOPIA start of cell or cell length error detected upstream.
Bit 12	DUSOCE	UTOPIA start of cell or cell length error detected downstream.
Bit 11	UEDCER	CRC-10 error detected in OAM cell in upstream direction. This error indication is also stored in Dword2, bit 13 in the upstream connection RAM entry of the respective LCI (see **section** 3.9.1.3).
Bit 10	DEDCER	CRC-10 error detected in OAM cell in downstream direction. This error indication is also stored in Dword2, bit 13 in the downstream connection RAM entry of the respective LCI (see **section** 3.9.3.3).
Bit 9	RXCEL	Indicates a non-empty receive buffer. It is cleared automatically after 27 read accesses of the RXRCEL register, i.e. after read-out of a complete cell. If further cells are in the receive buffer this bit is set again immediately.
Bit 8	RXOV	Indicates an overflow of the receive buffer; is set if at least one cell has been discarded due to a full receive cell buffer.
Bit 7	OCIF	Bit OCIF is set if • an OAM cell generated by the SCAN could not be inserted in downstream direction; • BR or FM cells could not be inserted in downstream direction; • "central control" loopback of LB cells could not be performed because insertion in downstream direction was not possible; • FM cells transformed to BR cells could not be inserted in downstream direction; This bit is the OR function result of all bits of CIFL and CIFH registers. *Note: Writing a '1' to bit OCIF will also reset registers CIFL and CIFH.*
Bit 6		Is set if an OAM cell generated by the SCAN could not be inserted in upstream direction. This occurs if during the insertion window defined in register SCCONF2 the upstream internal 32-cell buffer filling was constantly beyond the insertion threshold defined in register OAMTHRU.
Bit 5	DUTBO	UTOPIA Transmit-Buffer Overflow downstream.

Bit 4	DBERR	DMA Buffer Overflow or Underflow.
(Bit 3..0)	These bits indicate important transitions of AIS, RDI or CC state diagrams (see **Figures** 17, 18 and 22) for any connection with the respective functionality enabled. These are collection interrupts of the respective connection specific flags in the external RAM:	
Bit 3	DCSTTR	Downstream VC-related state transition occurred, i.e. one of the bits 14..19 of Dword2 in downstream external RAM entry set (see **section** 3.9.3.3).
Bit 2	UCSTTR	Upstream VC-related state transition occurred, i.e. one of the bits 14..19 of Dword2 in upstream external RAM set (see **section** 3.9.1.3).
Bit 1	DPSTTR	Downstream VP-related state transition occurred, i.e. one of the bits 22..27 of Dword4 in downstream external RAM set (see **section** 3.9.4.1).
Bit 0	UPSTTR	Upstream VP-related state transition occurred, i.e. one of the bits 22..27 of Dword4 in upstream external RAM set (see **section** 3.9.2.1).

3.6.2 Interrupt Status Register 1 (ISR1)

Read/write Address $D1_H$
Value after reset 0000_H

Bit 15:9	Unused	
Bit 8	SCTOUT	Time-out for Scan processing within SCP.
Bit 7	Upstream Loopback cell discarded.	
Bit 6	Downstream Loopback cell discarded.	
Bit 5	Cell received for an invalid connection (VCON=0) upstream. VCON is bit19 in Dword0 of upstream RAM (see **section** 3.9.1.1).	
Bit 4	Cell received for an invalid connection (VCON=0) downstream. VCON is bit19 in Dword0 of downstream RAM (see **section** 3.9.3.1).	
Bit 3	RAM-Parity error occurred upstream.	
Bit 2	RAM-Parity error occurred downstream.	
Bit 1	UOAMIS	Mis-inserted OAM cell detected upstream. This indication is also stored per connection in bit 12 of Dword2 in the upstream external RAM.
Bit 0	DOAMIS	Mis-inserted OAM cell detected downstream. This indication is also stored per connection in bit 12 of Dword2 in the downstream external RAM.

3.6.3 Interrupt Mask Register 0 (IMR0)

Read/write Address $D2_H$
Value after reset 0000_H

15							8
IMR0(15:8)							
7							**0**
IMR0(7:0)							

IMR0(15:0) Interrupt mask register for ISR0:

- 0 Setting of corresponding bit in ISR0 does not activate the interrupt pin $\overline{\text{MPINT}}$.
- 1 Setting of corresponding bit in ISR0 activates $\overline{\text{MPINT}}$.

3.6.4 Interrupt Mask Register 1 (IMR1)

Read/write Address $D3_H$
Value after reset 0000_H

15							8
Unused							IMR1(8)
7							**0**
IMR1(7:0)							

IMR1(8:0) Interrupt mask register for ISR1:

- 0 Setting of corresponding bit in ISR1 does not activate the interrupt pin $\overline{\text{MPINT}}$.
- 1 Setting of corresponding bit in ISR1 activates $\overline{\text{MPINT}}$.

3.6.5 Cell Insertion Fault Register low and high (CIFL and CIFH)

Low:

Read Address $D4_H$
Value after reset 0000_H

15							8
CIF(15:8)							
7							**0**
CIF(7:0)							

High:

Read Address $D5_H$
Value after reset 0000_H

15	8
Unused	
7	**0**
CIF(23:16)	

CIF(23:0) For the respective Port 15..0 in downstream direction an OAM cell could not be inserted. This occurs during the SCAN process if between consecutive LCIs there is no opportunity to insert the required OAM cell. OAM cells are not inserted if the filling level of the respective qeue exceeds the threshold specified in the OAMTHRD register.

The indication may also be generated for any of the following reasons:

- BR or FM cells could not be inserted in downstream direction;
- "central control" loopback of LB cells could not be performed because insertion in downstream direction was not possible;
- FM cells transformed to BR cells could not be inserted in downstream direction;

Bit OCIF in register ISR0 is the OR function result of all bits of CIFL and CIFH registers.

Note: Writing a '1' to bit OCIF in register ISR0 will also reset registers CIFL and CIFH.

3.7 UTOPIA Interface Registers

3.7.1 UTOPIA Configuration Register 0 (UTCONF0)

Read/write Address $E0_H$
Value after reset 0000_H
This register configures the ATM side UTOPIA interfaces.

15				8
Unused				
7				**0**
Unused	UTA16	UTAPAR	Unused	UTACONF(1:0)

Bit (15:5)	Unused	
UTA16	Select 8- or 16-bit UTOPIA Data bus	
	0	8 bit data bus at ATM side.
	1	16 bit data bus at ATM side.
UTAPAR	Enables/disables parity check	
	0	Don’t check parity of ATM receive data.
	1	Check parity of ATM receive data.
Bit (2)	Unused	
UTACONF(1:0)	Configuration of mode at ATM side :	
	00	4 x 6 port
	01	3 x 8 port
	10	2 x 12 port
	11	UTOPIA Level 1 (4 x 1 port)

3.7.2 UTOPIA Configuration Register 1 (UTCONF1)

Read/write Address $E1_H$
Value after reset 0000_H
This register configures the PHY side UTOPIA interfaces and the defines the LCI location.

15				8
Unused				LCIMOD(1:0)
7				**0**
Unused	UTP16	Unused	UTPPAR	UTPCONF(1:0)

Bit(15:10)	Unused	
LCIMOD(1:0)	Position of LCI up/downstream:	
	00	LCI(13:12) = UDF(7:6), LCI(11:0) = VPI(11:0)
	01	LCI(13:12) = 00, LCI(11:0) = VPI In this mode no ICC possible.
	10	LCI(13:0) = VCI(13:0) F4-OAM/User-Flow not supported.
	11	Is not allowed, will be handled as ’10’.
Bit(7:5)	Unused	
UTP16	Select 8- or 16-bit UTOPIA Data bus	
	0	8 bit data bus at PHY side.
	1	16 bit data bus at PHY side.
Bit(3)	Unused	
UTPPAR	Enables/disables parity check	
	0	Don’t check parity of PHY receive data.
	1	Check parity of PHY receive data.
UTPCONF(1:0)	Configuration of mode at PHY side :	
	00	4 x 6 port
	01	3 x 8 port
	10	2 x 12 port
	11	UTOPIA Level 1 (4 x 1 port)

3.7.3 Upstream Port Enable low and high (UPRTENL and UPRTENH)

Low:

Read/write Address $E2_H$
Value after reset 0000_H

15	8
UPORTEN(15:8)	
7	**0**
UPORTEN(7:0)	

High:

Read/write Address $E3_H$
Value after reset 0000_H

15	8
Unused	
7	**0**
UPRTEN(23:16)	

Bit(15:8)	Unused	
UPRTEN(23:16)		
	0	Disables UTOPIA port upstream.
	1	Enables UTOPIA port upstream.

3.7.4 Downstream Port Enable low and high (DPRTENL and DPRTENH)

Low:

Read/write Address $E4_H$
Value after reset 0000_H

15	8
DPRTEN(15:8)	
7	**0**
DPRTEN(7:0)	

High:

Read/write Address $E5_H$
Value after reset 0000_H

15	8
Unused	
7	**0**
DPRTEN(23:16)	

Bit(15:0)	Unused	in High word only
DPRTEN(23:0)		
	0	Disables UTOPIA port downstream.
	1	Enables UTOPIA port downstream.

3.7.5 OAM Cell Insertion Threshold Upstream (OAMTHRU)

Read/write Address $E6_H$
Value after reset $001E_H$

15	8
Unused	
7	**0**
Unused	OAMTHRU(5:0)

OAMTHRU(5:0)	Threshold for forced OAM cell insertion in upstream direction. If the upstream 32-cell buffer is filled beyond this level OAM cells are inserted with lower priority than user cells. Recommended value 30 ($1E_H$).	
	0	OAM cell insertion upstream only possible if no cell from UTOPIA is received.
	1..31	Cell insertion has higher priority until filling level of upstream 32-cell buffer reaches this threshold.
	>31	OAM cells are always inserted with higher priority (in case of 32-cell buffer overflow backpressure to PHY).

3.7.6 OAM Cell Insertion Threshold Downstream (OAMTHRD)

Read/write Address $E7_H$
Value after reset 0060_H

15	8
Unused	

7	0
Unused	OAMTHRD(6:0)

OAMTHRD(6:0) Threshold for forced OAM cell insertion in downstream direction. If a queue of the downstream shared buffer is filled beyond this level OAM cells destined to the respective PHY are not inserted.

- 0 — No cell insertion downstream possible.
- 1...95 — Cell insertion is possible until queue filling level reaches threshold.
- >95 — Cell insertion downstream only limited by buffer overflow condition.

3.7.7 Backpressure Threshold Downstream (BPTHRD)

Read/write Address $E8_H$
Value after reset 0060_H

15	8
Unused	

7	0
Unused	BPTHRD(6:0)

BPTHRD(6:0) Queue backpressure level in downstream direction. If a queue exceeds this threshold the downstream receive UTOPIA interface does not accept any more cell:

- 0 — Always backpressure to downstream receive UTOPIA interface for all ports.
- 1...95 — Backpressure to the respective PHY of the downstream receive UTOPIA interface if queue filling level reaches threshold.
- >95 — Queue specific backpressure disabled, backpressure controlled by shared buffer overflow only.

(Recommended value is 65.)

3.8 Miscellaneous Registers

3.8.1 RAM Type Select Register (MISC)

Read/write Address $F0_H$
Value after reset 0000_H

15			8
Unused			
7			**0**
Unused	RAMSEL(1:0)		SWRES

RAMSEL(1:0)	Selects the type of RAM used for upstream and downstream external connection RAM.	
	00	1 Mbit external RAM.
	01	2 Mbit external RAM.
SWRES	SW-reset. If set to one the internal reset cycle is executed.	

3.8.2 Test Register 1 (TESTR1)

Read/write Address $F1_H$
Value after reset 0000_H

15				8
Unused				
7				**0**
Unused	TINT	LOOPUD	LOOPDU	

Unused(15:3)

TINT Test of Interrupt.

0	Normal operation, test of interrupts is disabled.
1	Interrupt generation test mode: Normal interrupt generation is disabled; interrupt test procedure is controlled by consecutive write accesses to register RXRCEL (offset address: $9D_H$):
1. write:	will set bit ISR0(0)
2. write:	will set bit ISR0(1)
...	...
10. write:	will **NOT** set bit ISR0(9) *Note: This interrupt status bit is an exception and cannot be tested by this procedure.*
11. write:	will set bit ISR0(10)
...	...
16. write:	will set bit ISR0(15)
17. write:	will set bit ISR1(0)
...	...
32. write:	will set bit ISR1(15)

Bit TINT has to be set to ’0’ to re-enter normal operation.

LOOPUD

1	Enable testloop up-to-downstream.

LOOPDU

1	Enable testloop down-to-upstream.

3.8.3 Test Register 2 (TESTR2)

Read/write Address $F2_H$
Value after reset 0000_H

Reserved for device test only. Don’t write.

3.8.4 Version Register low and high (VERL and VERH)

Low:

Read Address $F3_H$
Value after reset $A06D_H$

High

Read Address $F4_H$
Value after reset $523B_H$

15								8							0	15								8							0
0	1	0	1	0	0	1	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	0	1	1	0	1	1	0	1
VERH																VERL															

Note: These are the 32 ID-bits of the boundary scan sequence.

3.8.5 BIST Mode Register Low (BISTML)

Read/write Address $F5_H$
Value after reset 0000_H

15			8
RXR	NCP	UTTXD3	UTTXD2
7			**0**
UTTXD1	UTRXD	UTTXU	UTRXU

Bit coding(1:0)	Selects the BIST function.	
	00	BIST inactive, normal operation mode.
	01	Test of BIST circuit.
	10	Start BIST.
	11	Diagnose mode (not used).
RXR	Select BIST function for Receive Buffer	
NCP	Select BIST function for Cell Processing RAM	
UTTXD1..3	Select BIST function for UTOPIA Downstream Transmit (shared) Buffer 1..3	
UTRXD	Select BIST function for UTOPIA Downstream Receive Buffer	
UTTXU	Select BIST function for UTOPIA Upstream Transmit Buffer	
UTRXU	Select BIST function for UTOPIA Upstream Receive Buffer	

3.8.6 BIST Mode Register High (BISTMH)

Read/write Address $F6_H$
Value after reset 0000_H

15			8
PMDC6	PMDC5	PMDC4	PMDC3
7			**0**
PMDC2	PMDC1	PMDC0	PMAIN

Bit coding(1:0)	Selects the BIST function.	
	00	BIST inactive, normal operation mode.
	01	Test of BIST circuit.
	10	Start BIST.
	11	Diagnosis mode (not used).
PMDC6..0	Select BIST function for PM data collection RAM part 6..0	
PMAIN	Select BIST function for PM main RAM	

3.8.7 BIST Done Register (BISTDN)

Read Address $F7_H$
Value after reset 0000_H

The 16 bits of this register have a one-to-one correspondence with internal RAM blocks. These bits are set by the AOP if the respective BIST is completed. All bits are reset by any write to the BISTERR register. After completion of a BIST the AOP must be reset.

Bit 15..9	BIST of PMDC6..0 RAM block is completed
Bit 8	BIST of PMAIN RAM is completed
Bit 7	BIST of RXR Buffer is completed
Bit 6	BIST of NCP RAM is completed
Bit 5..3	BIST of UTOPIA Downstream RAM block 3..1 is completed
Bit 2	BIST of UTOPIA Downstream Receive Buffer is completed
Bit 1	BIST of UTOPIA Upstream Transmit Buffer is completed
Bit 0	BIST of UTOPIA Receive Upstream Buffer is completed

3.8.8 BIST Error Register (BISTERR)

Read Address $F8_H$
Value after reset 0000_H

The 16 bits of this register have a one-to-one correspondence with internal RAM blocks. These bits are set if during BIST execution an error occured in the respective RAM block.

Bit 15..9	BIST of PMDC6..0 RAM block is faulty
Bit 8	BIST of PMAIN RAM is faulty
Bit 7	BIST of RXR Buffer is faulty
Bit 6	BIST of NCP RAM is faulty
Bit 5..3	BIST of UTOPIA Downstream RAM block 3..1 is faulty
Bit 2	BIST of UTOPIA Downstream Receive Buffer is faulty
Bit 1	BIST of UTOPIA Upstream Transmit Buffer is faulty
Bit 0	BIST of UTOPIA Receive Upstream Buffer is faulty

3.9 External and Internal RAM

3.9.1 Upstream External RAM F5 Entry: Dwords 0..3

Dword	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	31	30	29	28	CEDCID(6:0)								CSDCID(6:0)								CPMTID(6:0)								CPMOID(6:0)			
2	31				CTSDCID(6:0)								19	18	17	16	15	14	13	12	11..7					6	5	4	3..0			
1	31	30..15																14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	31	30	29	28	27	26	25	24	23	22	21	20	19	LCI2(13:0)															PN(4:0)			

3.9.1.1 Upstream F5 OAM Entry: Dword0

Bit 31 PAR
Dword parity protection. In normal operation write to 0. Should always read as 0.

Bit 30 CPMTEN
Enable a Terminating F5 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier CPMTID in Dword3.

Bit 29 CPMOEN
Enable an Originating F5 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier CPMOID in Dword3.

Bit 28 CLBS
F5 Loopback State according to I.610. Should be set before inserting a LB cell, cleared after reception of the looped cell.

Bit 27 CSRCIDEN
Loopback of F5 LB cells using LB source ID

1 Enabled. Normally this bit is =0 as the location ID is used to detect intra-domain LB cells.

Bit 26 CLOCIDEN
Loopback of F5 LB cells using LB location ID

1 Enabled. Normally this bit is =1 as according to the standard the location ID is used to detect intra-domain LB cells

Bit 25 ACDEAC
Treatment of Activation/Deactivation cells at their destination points:

0 Discard (if Activation/ Deactivation function is not used)

1 Extract to receive buffer (if Activation/ Deactivation is supported)

Bit 24	DISF5	
	0	Enable F5 processing, default.
	1	Disable F5 processing. All F5 OAM cells are discarded.
Bit 23	CTSP	
	0	No F5 Terminating Segment Point.
	1	F5 Terminating Segment Point. Do not adjust at F5 OEP.
Bit 22	COSP	
	0	No F5 Originating Segment Point.
	1	F5 Originating Segment Point.
Bit 21	Unused It is recommended to initialize with ’0’.	
Bit 20	CIP	
	0	F5 Originating End Point (OEP).
	1	F5 Intermediate Point.
Bit 19	VCON	
	0	Connection not activated, cells for this LCI are discarded.
	1	Connection activated.
LCI2(13:0)18..5	Pointer to the VP connection data of the actual VCC. F4 pointer in **figure 14**. Meaning of bits 18..5 depends on bit field ’lcimod’ in register UTCONF1.	
PN(4:0)4..0	PHY Number associated with this LCI. Used for PHY specific AIS generation (see µP register PHYERR).	

3.9.1.2 Upstream F5 OAM Entry: Dword1

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.	
Bit 30..15	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 14	CICCEN	
	1	Enable Internal Continuity Check, originating ICC in upstream direction. Set to 0 if ICC is not used.
Bit 13	CSCCTEN	
	1	Terminate a F5 Segment Continuity Check. Should only be enabled at a F5 TSP (CTSP=1).
Bit 12	Reserved, set to 0.	
Bit 11	CSCCOEN	
	1	Originate a F5 Segment Continuity Check Flow. Should only be enabled at a F5 OSP (COSP=1).
Bit 10	CECCOEN	
	1	Originate a F5 End-to-End Continuity Check Flow. Should only be enabled at a F5 OEP (CIP=0).
Bit 9	CRDIMEN	
	0	F5 RDI monitoring disabled.
	1	F5 RDI monitoring enabled. State transition to RDI failure state and out of RDI failure state is reported by use of the µP interrupt UCSTTR.
Bit 8	CAISMEN	
	0	F5 AIS monitoring disabled.
	1	F5 AIS monitoring enabled. State transition to AIS failure state and out of AIS failure state is reported by use of the µP interrupt UCSTTR.
Bit 7	CCCMEN	
	0	F5 CC monitoring disabled.
	1	F5 CC monitoring enabled. State transition to LOC failure state and out of LOC failure state is reported by use of the µP interrupt UCSTTR.

Bit 6	CARIEN	
	0	F5 AIS Cell insertion disabled.
	1	F5 AIS Cell insertion enabled. Independent on the reason for cell generation (forced insertion by ARINS, physical error by µP register PHYERR, detected LOC or AIS state) AIS/RDI cell generation is always controlled by this flag. Used e.g. to suppress RDI at endpoints of multicast connections.
Bit 5	CLOCFAI F5 LOC failure state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 4	CLOCDEF F5 LOC defect state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 3	CRDIFAI F5 RDI failure state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 2	CRDIDEF F5 RDI defect state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 1	CAISFAI F5 AIS failure state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 0	CAISDEF F5 AIS defect state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.	

3.9.1.3 Upstream F5 OAM Entry: Dword2

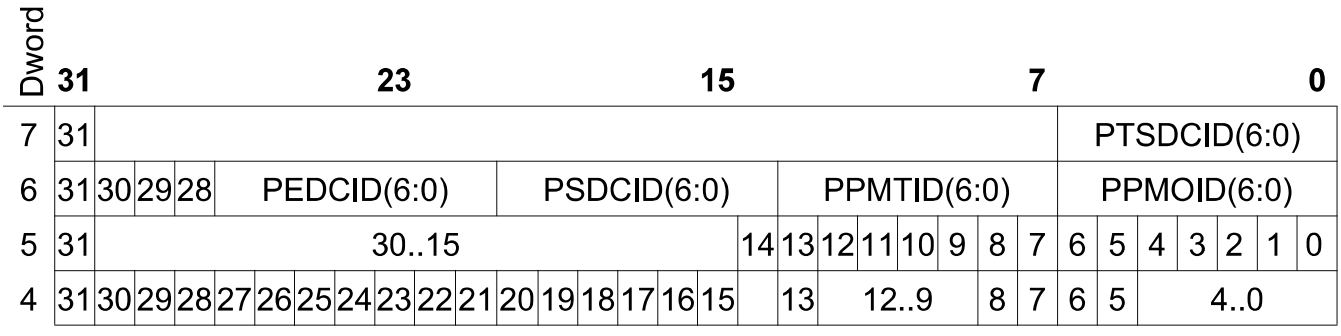
Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.	
30..27	Unused It is recommended to initialize with ’0’.	
CTSDCID(6:0)	Identifier for Data Collection on terminated / intermediate Segment F5 BR cells. Related enable CTSDCEN in Dword3.	
Bit 19	CLOCF2N	
	1	Indication for a state transition from F5 LOC failure state to F5 LOC normal state. Set by AOP, must be cleared by the µP. Reported with interrupt UCSTTR if enabled with CCCMEN=1 (Dword1).
Bit 18	CLOCD2F	
	1	Indication for a state transition from F5 LOC defect state to F5 LOC failure state. Set by AOP, must be cleared by the µP. Reported with interrupt UCSTTR if enabled with CCCMEN=1 (Dword1).
Bit 17	CRDIF2N	
	1	Indication for a state transition from F5 RDI failure state to F5 RDI normal state. Set by AOP, must be cleared by the µP. Reported with interrupt UCSTTR if enabled with CRDIMEN=1 (Dword1).
Bit 16	CRDID2F	
	1	Indication for a state transition from F5 RDI defect state to F5 RDI failure state. Set by AOP, must be cleared by the µP. Reported with interrupt UCSTTR if enabled with CRDIMEN=1 (Dword1).
Bit 15	CAISF2N	
	1	Indication for a state transition from F5 AIS failure state to F5 AIS normal state. Set by AOP, must be cleared by the µP. Reported with interrupt UCSTTR if enabled with CAISMEN=1 (Dword1).
Bit 14	CAISD2F	
	1	Indication for a state transition from F5 AIS defect state to F5 AIS failure state. Set by AOP, must be cleared by the µP. Reported with interrupt UCSTTR if enabled with CAISMEN=1 (Dword1).

Bit 13	EDCERR	
	1	Wrong EDC (CRC10) in an OAM cell detected on this connection. Reported with interrupt UEDCER.
Bit 12	OAMMIS	
	1	Mis-inserted OAM cell discarded on this connection. Reported with interrupt UOAMIS.
Bit 11..7	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 6	CCCINS	
	0	Default; normal CC cell insertion
	1	Force insertion of F5 CC Cells for all activated CC flows; period determined by MAXTS in register SCCONF1.
Bit 5	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 4	CARINS:	
	1	Force insertion of F5 AIS Cells upstream. Cells are generated with every 2nd SCAN. Used e.g. for AIS insertion due to VCC performance degrade (determined by PM function).
Bit 3..0	Initialize to 0 at connection setup. Do not change by µP in normal operation.	

3.9.1.4 Upstream F5 OAM Entry: Dword3

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.
Bit 30	CEDCEN Enable Data Collection on F5 End-to-End BR cells. Related identifier CEDCID.
Bit 29	CSDCEN Enable Data Collection on F5 Segment BR cells directly generated from F5 segment FM cells. Related identifier CSDCID.
Bit 28	CTSDCEN Enable Data Collection on terminated / intermediate F5 Segment BR cells, related identifier CTSPMDCID is in Dword2.
CEDCID(6:0)	Identifier for Data Collection on F5 End-to-End BR cells. Related enable CEDCEN.
CSDCID(6:0)	Identifier for Data Collection on F5 Segment BR cells directly generated from F5 segment FM cells. Related enable CSDCEN.
CPMTID(6:0)	Identifier for a terminating F5 Segment or End-to-End FM flow. Related enable CPMTEN in Dword0.
CPMOID(6:0)	Identifier for an originating F5 Segment or End-to-End FM flow. Related enable CPMOEN in Dword0.

3.9.2 Upstream External RAM F4 Entry: Dwords 4..7



3.9.2.1 Upstream F4 OAM entry: Dword4

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.	
Bit 30	PPMTEN Enable a terminating F4 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier PPMTID in Dword6.	
Bit 29	PPMOEN Enable an originating F4 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier PPMOID in Dword6.	
Bit 28	Initialize to 0 at a connection setup. Do not change by µP in normal operation.	
Bit 27	PLOCF2N	
	1	Indication for a state transition from LOC failure state to LOC normal state. Set by AOP, must be cleared by the µP. Reported with interrupt UPSTTR if enabled with PCCMEN=1 in Dword5.
Bit 26	PLOCD2F	
	1	Indication for a state transition from LOC defect to LOC failure state. Set by AOP, must be cleared by the µP. Reported with interrupt UPSTTR if enabled with PCCMEN=1 in Dword5.
Bit 25	PRDIF2N	
	1	Indication for a state transition from AIS failure to AIS normal state. Set by AOP, must be cleared by the µP. Reported with interrupt UPSTTR if enabled with PRDIMEN=1 in Dword5.
Bit 24	PRDID2F	
	1	Indication for a state transition from AIS defect to AIS failure state. Set by AOP, must be cleared by the µP. Reported with interrupt UPSTTR if enabled with PRDIMEN=1 in Dword5.
Bit 23	PAISF2N	
	1	Indication for a state transition from AIS failure to AIS normal state. Set by AOP, must be cleared by the µP. Reported with interrupt UPSTTR if enabled with PAISMEN=1 in Dword5.

Bit 22	PAISD2F	
	1	Indication for a state transition from AIS defect to AIS failure state. Set by AOP, must be cleared by the µP. Reported with interrupt UPSTTR if enabled with PAISMEN=1 in Dword5.
Bit 21	PLBS F4 Loopback State according to I.610. Should be set before inserting a LB cell, cleared after reception of the looped cell.	
Bit 20	VPCCHK VPCI consistency check. If set indicates that a LB cell has been looped.	
Bit 19	PSRCIDEN Loopback of F4 LB Cells using LB source ID	
	1	Enabled. Normally this bit is =0 as the location ID is used to detect intra-domain LB cells.
Bit 18	PLOCIDEN Loopback of F4 LB Cells using LB location ID	
	1	Enabled. Normally this bit is =1 as according to the standard the location ID is used to detect intra-domain LB cells.
Bit 17	DISF4	
	0	Enable F4 processing, default.
	1	Disable F4 processing. All F4 OAM cells are discarded. Option selected e.g. at AAL interworking point.
Bit 16	PTSP	
	0	No F4 Terminating Segment Point.
	1	F4 Terminating Segment Point.
Bit 15	POSP	
	0	No F4 Originating Segment Point.
	1	F4 Originating Segment Point. Do not adjust at F4 TEP.
Bit 13	PIP	
	0	F4 Terminating End Point (TEP).
	1	F4 intermediate Point.
Bit 12..9	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 8	PCCINS	
	1	Force insertion of F4 CC Cells for all activated CC flows; period determined by MAXTS in register SCCONF1.

Bit 7	Initialize to 0 at connection setup. Do not change by µP in normal operation.
Bit 6	PARINS
	1 Force insertion of F4 AIS Cells upstream. Used e.g. for AIS insertion due to VPC performance degrade (determined by PM function).
Bit 5	Initialize to 1 at connection setup. Do not change by µP in normal operation.
Bit 4..0	Initialize to 0 at connection setup. Do not change by µP in normal operation.

3.9.2.2 Upstream F4 OAM Entry: Dword5

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.
Bit 30..15	Initialize to 0 at connection setup. Do not change by µP in normal operation.
Bit 14	PICCEN
	1 Enable Internal Continuity check, in upstream direction originating ICC is enabled.
Bit 13	PSCCTEN
	1 Terminate a F4 Segment Continuity Check. Should only be enabled at a F4 TSP (PTSP=0).
Bit 12	PECCTEN
	1 Terminate a F4 End-to-End Continuity Check. Should only be enabled at a F4 TEP (PIP=0).
Bit 11	PSCCOEN
	1 Originate a F4 Segment Continuity Check. Should only be enabled at a F4 OSP (POSP=1).
Bit 10	Reserved, set to 0.
Bit 9	PRDIMEN
	0 F4 RDI monitoring disabled.
	1 F4 RDI monitoring enabled. State transition to RDI failure state and out of RDI failure state is reported by use of the interrupt UPSTTR.

Bit 8	PAISMEN	
	0	F4 AIS monitoring disabled.
	1	F4 AIS monitoring enabled. State transition to AIS-failure state and out of AIS-failure state is reported by use of the µP interrupt UPSTTR.
Bit 7	PCCMEN	
	0	F4 CC monitoring disabled.
	1	F4 CC monitoring enabled. State transition to LOC failure state and out of LOC failure state is reported by use of the µP interrupt UPSTTR.
Bit 6	PARIEN	
	0	F4 AIS/RDI Cell insertion disabled.
	1	F4 AIS/RDI Cell insertion enabled. Independent of the reason for cell generation (forced insertion by ARINS, physical error by µP register PHYERR, detected LOC or AIS state) AIS/RDI cell generation is always enabled with this flag. Used e.g. to suppress RDI at endpoints of multicast connections.
Bit 5	PLOCFAI	
	1	F4 LOC failure state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.
Bit 4	PLOCDEF	
	1	F4 LOC defect state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.
Bit 3	PRDIFAI	
	1	F4 RDI failure state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.
Bit 2	PRDIDEF	
	1	F4 RDI defect state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.
Bit 1	PAISFAI	
	1	F4 AIS failure state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.
Bit 0	PAISDEF	
	1	F4 AIS defect state indication. Initialize to 0 at connection setup. Do not change by µP in normal operation.

3.9.2.3 Upstream F4 OAM Entry : Dword6

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.
Bit 30	PEDCEN Enable Data Collection on F4 End-to-End BR cells. Related identifier PEDCID.
Bit 29	PSDCEN Enable Data Collection on F4 Segment BR cells directly generated from F4 Segment FM cells. Related identifier PSDCID.
Bit 28	PTSDCEN Enable Data Collection on terminated / intermediate F4 Segment BR cells, related identifier PTSDCID in Dword7.
PEDCID(6:0)	Identifier for Data Collection on F4 End-to-End BR cells. Related enable PEDCEN.
PSDCID(6:0)	Identifier for Data Collection on F4 Segment BR cells directly generated from F4 Segment FM cells. Related enable PSDCEN.
PPMTID(6:0)	Identifier for a terminating F4 Segment or End-to-End FM flow. Related enable PPMTEN in Dword4.
PPMOID(6:0)	Identifier for an originating F4 Segment or End-to-End FM flow. Related enable PPMOEN in Dword4.

3.9.2.4 Upstream F4 OAM Entry: Dword7

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.
Bit 30..7	Unused It is recommended to initialize with ’0’.
PTSDCID(6:0)	Identifier for Data Collection on terminated / intermediate F4 Segment BR cells. Related enable PTSDCEN in Dword6.

3.9.3 Downstream External RAM F5 Entry: Dwords 0..3

Dword	31															15								7								0
3	31	30	29	28	CEDCID(6:0)							CSDCID(6:0)							CPMTID(6:0)							CPMOID(6:0)						
2	31	CTSDCID(6:0)							19	18	17	16	15	14	13	12	11..7					6	5	4	3..0							
1	31	30..15																			14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	31	30	29	28	27	26	25	24	23	22		20	19	LCI2(13:0)															PN(4:0)					

3.9.3.1 Downstream F5 OAM Entry: Dword0

Bit 31 PAR
Dword parity protection. In normal operation write to 0. Should always read as 0.

Bit 30 CPMTEN
Enable a Terminating F5 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier CPMTID in Dword3.

Bit 29 CPMOEN
Enable an Originating F5 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier CPMOID in Dword3.

Bit 28 CLBS
F5 Loopback State according to I.610. Should be set before inserting a LB cell, cleared after reception of the looped cell.

Bit 27 CSRCIDEN
Loopback of LB cells using LB source ID

1 Enabled. Normally this bit is =0 as the location ID is used to detect intra-domain LB cells.

Bit 26 CLOCIDEN
Loopback of LB cells using LB location ID

1 Enabled. Normally this bit is =1 as according to the standard the location ID is used to detect intra-domain LB cells.

Bit 25 ACDEAC
Treatment of Activation/Deactivation cells at their destination points:

0 Discard (if Activation / Deactivation function is not used)

1 Extract to receive buffer (if Activation / Deactivation is supported)

Bit 24	DISF5	
	0	Enable F5 processing, default.
	1	Disable F5 processing. All F5 OAM cells are discarded.
Bit 23	CTSP	
	0	No F5 Terminating Segment Point.
	1	F5 Terminating Segment Point.
Bit 22	COS	
	0	No F5 Originating Segment Point.
	1	F5 Originating Segment Point. Do not adjust at F5 TEP.
Bit 20	CIP	
	0	F5 Terminating End Point (TEP).
	1	F5 Intermediate Point.
Bit 19	VCON	
	0	Connection not activated, cells for this LCI are discarded.
	1	Connection activated.
LCI2(13:0)	Pointer to the VP connection data of the actual VCC. F4 pointer in **figure 14**). Meaning of bits 18..5 depends on bit field 'lcimod' in register UTCONF1.	
PN(4:0)	PHY Number associated with this LCI. Used for PHY specific RDI cell generation.	

3.9.3.2 Downstream F5 OAM Entry: Dword1

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.	
Bit 30..15	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 14	CICCEN	
	1	Enable Internal Continuity Check, terminating ICC in downstream direction. Set to 0 if ICC is not used.
Bit 13	CSCCTEN	
	1	Terminate a F5 Segment Continuity Check. Should only be enabled at a F5 TSP (CTSP=1).
Bit 12	CECCTEN	
	1	Terminate a F5 End-to-End Continuity Check Flow. Should only be enabled at a F5 TEP (CIP=0).
Bit 11	CSCCOEN	
	1	Originate a F5 Segment Continuity Check Flow. Should only be enabled at a F5 OSP (COSP=1).
Bit 10	Reserved, set to 0.	
Bit 9	CRDIMEN	
	0	F5 RDI monitoring disabled.
	1	F5 RDI monitoring enabled. State transition to ASI failure state and out of ASI failure state is reported by use of the µP interrupt DCSTTR.
Bit 8	CAISMEN	
	0	F5 AIS monitoring disabled.
	1	F5 AIS monitoring enabled. State transition to AIS failure state and out of AIS failure state is reported by use of the µP interrupt DCSTTR.

Bit 7	CCCMEN	
	0	F5 CC monitoring disabled.
	1	F5 CC monitoring enabled. State transition to LOC failure state and out of LOC failure state is reported by use of the µP interrupt DCSTTR.
Bit 6	CARIEN	
	0	F5 AIS or RDI Cell insertion disabled.
	1	F5 AIS or RDI Cell insertion enabled. Independent of the reason for cell generation (forced insertion by ARINS, detected LOC or AIS state) AIS/RDI cell generation is always controlled by this flag. Necessary e.g. to suppress RDI at endpoints of multicast or unidirectional connections.
Bit 5	CLOCFAI F5 LOC failure state. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 4	CLOCDEF F5 LOC defect state. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 3	CRDIFAI F5 RDI failure state. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 2	CRDIDEF F5 RDI defect state. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 1	CAISFAI F5 AIS failure state. Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 0	CAISDEF F5 AIS defect state. Initialize to 0 at connection setup. Do not change by µP in normal operation.	

3.9.3.3 Downstream F5 OAM Entry: Dword2

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.	
CTSDCID(6:0)	Identifier for Data Collection on terminated / intermediate F5 Segment BR cells. Related enable is CTSDCEN in Dword3.	
Bit 19	CLOCF2N	
	1	Indication for a state transition from F5 LOC failure state to F5 LOC normal state. Set by AOP, reset by the µP. Reported with interrupt DCSTTR if enabled with CAISMEN=1 (Dword1).
Bit 18	CLOCD2F	
	1	Indication for a state transition from F5 LOC defect state to F5 LOC failure state. Set by AOP, reset by the µP. Reported with interrupt DCSTTR if enabled with CCCMEN=1 (Dword1).
Bit 17	CRDIF2N	
	1	Indication for a state transition from F5 RDI failure state to F5 RDI normal state. Set by AOP, reset by the µP. Reported with interrupt DCSTTR if enabled with CRDIMEN (Dword1).
Bit 16	CRDID2F	
	1	Indication for a state transition from F5 RDI defect state to F5 RDI failure state. Set by AOP, reset by the µP. Reported with interrupt DCSTTR if enabled with CRDIMEN=1. (Dword1.
Bit 15	CAISF2N	
	1	Indication for a state transition from F5 AIS failure state to F5 AIS normal state. Set by AOP, reset by the µP.Reported with interrupt DCSTTR if enabled with CAISMEN=1 (Dword1).
Bit 14	CAISD2F	
	1	Indication for a state transition from F5 AIS defect state to F5 AIS failure state. Set by AOP, reset by the µP. Reported with interrupt DCSTR if enabled with CAISMEN=1 (Dword1).
Bit 13	EDCERR	
	1	Wrong EDC (CRC10) in an OAM cell detected. Reported with interrupt DEDCER.

Bit 12	OAMMIS	
	1	Miss inserted OAM cell discarded. Reported with interrupt DOAMIS.
Bit 11..7	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 6	CCCINS	
	0	Default, normal CC cell insertion.
	1	Force insertion of F5 CC Cells for all activated CC flows; period determined by MAXTS in register SCCONF1.
Bit 5	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 4	CARINS	
	1	Force insertion of F5 AIS Cells downstream (CIP=1).
Bit 3..0	Initialize to 0 at connection setup. Do not change by µP in normal operation.	

3.9.3.4 Downstream F5 OAM Entry: Dword3

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.
Bit 30	CEDCEN Enable Data Collection on F5 End-to-End BR cells. Related identifier CEDCID.
Bit 29	CSDCEN Enable Data Collection on F5 Segment BR cells directly generated from F5 segment FM cells. Related identifier CSDCID.
Bit 28	CTSDCEN Enable Data Collection on terminated / intermediate F5 Segment BR cells, related identifier CTSDCID in Dword2.
CEDCID(6:0)	Identifier for Data Collection on F5 Segment BR cells. Related enable CEDCEN.
CSDCID(6:0)	Identifier for Data Collection on F5 Segment BR cells directly generated from F5 segment FM cells. Related enable CSDCEN.
CPMTID(6:0)	Identifier for a terminating F5 Segment or End-to-End FM flow. Related enable CPMTEN in Dword0.
CPMOID(6:0)	Identifier for an originating F5 Segment or End-to-End FM flow. Related enable CPMOEN in Dword0.

3.9.4 Downstream External RAM F4 Entry: Dwords 4..7

Dword	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	31																									PTSDCID(6:0)						
6	31	30	29	28	PEDCID(6:0)							PSDCID(6:0)								PPMTID(6:0)						PPMOID(6:0)						
5	31	30..15																14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15		13	12..9				8	7	6	5	4..0				

3.9.4.1 Downstream F4 OAM Entry: Dword4

Bit 31 PAR
Dword parity protection. In normal operation write to 0. Should always read as 0.

Bit 30 PPMTEN
Enable a terminating F4 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier PPMTID in Dword6.

Bit 29 PPMOEN
Enable an originating F4 Segment or End-to-End FM flow. Flow type selected with PMFT in PM RAM entry. Related identifier PPMOID in Dword6.

Bit 28 Initialize to 0 at a connection setup. Do not change by µP in normal operation.

Bit 27 PLOCF2N

1 Indication for a state transition from LOC failure state to LOC normal state. Set by AOP, reset by the µP. Reported with interrupt DPSTTR if enabled with PCCMEN=1 (Dword5).

Bit 26 PLOCD2F

1 Indication for a state transition from LOC defect state to LOC failure state. Set by AOP, reset by the µP. Reported with interrupt DPSTTR if enabled with PCCMEN=1 (Dword5).

Bit 25 PRDIF2N

1 Indication for a state transition from AIS failure state to AIS normal state. Set by AOP, reset by the µP. Reported with interrupt DPSTTR if enabled with PRDIMEN=1 (Dword5).

Bit 24	PRDID2F	
	1	Indication for a state transition from AIS defect state to AIS failure state. Set by AOP, reset by the µP. Reported with interrupt DPSTTR if enabled with PRDIMEN=1 (Dword5).
Bit 23	PAISF2N	
	1	Indication for a state transition from AIS failure state to AIS normal state. Set by AOP, reset by the µP. Reported with interrupt DPSTTR if enabled with PAISMEN=1 (Dword5).
Bit 22	PAISD2F	
	1	Indication for a state transition from AIS defect state to AIS failure state. Set by AOP, reset by the µP. Reported with interrupt DPSTTR if enabled with PAISMEN=1 (Dword5).
Bit 21	PLBS F4 Loopback State according to I.610. Should be set before inserting a LB cell, cleared after reception of the looped cell.	
Bit 20	Reserved, set to 0.	
Bit 19	PSRCIDEN Loopback of LB Cells using LB source ID:	
	1	Enabled. Normally this bit is =0 as the location ID is used to detect intra-domain LB cells.
Bit 18	PLOCIDEN Loopback of LB Cells using LB location ID	
	1	Enabled. Normally this bit is =1 as according to the standard the location ID is used to detect intra-domain LB cells.
Bit 17	DISF4	
	0	Enable F4 processing, default.
	1	Disable F4 processing. All F4 OAM cells are discarded. Option selected e.g. at AAL interworking point.
Bit 16	PTSP	
	0	No F4 Terminating Segment Point.
	1	F4 Terminating Segment Point. Do not adjust at F4 OEP.
Bit 15	POSP	
	0	No F4 Originating Segment Point.
	1	F4 Originating Segment Point.

Bit 13	PIP	
	0	F4 Originating End Point (OEP).
	1	F4 intermediate Point.
Bit 12..9	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 8	PCCINS	
	1	Insertion of F4 CC Cells for all activated CC flows; period determined by MAXTS in register SCCONF1.
Bit 7	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 6	PARINS	
	1	Force insertion of F4 AIS Cell downstream.
Bit 5	Initialize to 1 at connection setup. Do not change by µP in normal operation.	
Bit 4..0	Initialize to 0 at connection setup. Do not change by µP in normal operation.	

3.9.4.2 Downstream F4 OAM Entry: Dword5

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.	
Bit 30..15	Initialize to 0 at connection setup. Do not change by µP in normal operation.	
Bit 14	PICCEN	
	1	Enable Internal Continuity Check, terminating ICC in downstream direction. Set to 0 if ICC is not used.
Bit 13	PSCCTEN	
	1	Terminate a F4 Segment Continuity Check. Should only be enabled at a F4 TSP (PTSP=1).
Bit 12	Reserved, set to 0.	
Bit 11	PSCCOEN	
	1	Originate a F4 Segment Continuity Check. Should only be enabled at a F4 OSP (POSP=1).
Bit 10	PECCOEN	
	1	Originate a F4 End-to-End Continuity Check. Should only be enabled at a F4 OEP (PIP=0).

Bit 9	PRDIMEN	
	0	F4 RDI monitoring disabled.
	1	F4 RDI monitoring enabled. State transition to RDI failure state and out of RDI failure state is reported by use of the µP interrupt DPSTTR.
Bit 8	PAISMEN	
	0	F4 AIS monitoring disabled.
	1	F4 AIS monitoring enabled. State transition to AIS failure state and out of AIS failure state is reported by use of the µP interrupt DPSTTR.
Bit 7	PCCMEN	
	0	F4 CC monitoring disabled.
	1	F4 CC monitoring enabled. State transition to LOC failure state and out of LOC failure state is reported by use of the µP interrupt DPSTTR.
Bit 6	PARIEN	
	0	F4 AIS/RDI Cell insertion disabled.
	1	F4 AIS/RDI Cell insertion enabled. Independent of the reason for cell generation (forced insertion by ARINS, detected LOC or AIS state) AIS cell generation is always controlled by this flag.
Bit 5	PLOCFAI	
	1	F4 LOC failure state indication. Initialize to 0. Do not change by µP in normal operation.
Bit 4	PLOCDEF:	
	1	F4 LOC defect state indication. Initialize to 0. Do not change by µP in normal operation.
Bit 3	PRDIFAI:	
	1	F4 RDI failure state indication. Initialize to 0. Do not change by µP in normal operation.
Bit 2	PRDIDEF:	
	1	F4 RDI defect state indication. Initialize to 0. Do not change by µP in normal operation.
Bit 1	PAISFAI:	
	1	F4 AIS failure state indication. Initialize to 0. Do not change by µP in normal operation.

Bit 0	PAISDEF:	
	1	F4 AIS defect state indication. Initialize to 0. Do not change by µP in normal operation.

3.9.4.3 Downstream F4 OAM Entry: Dword6

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.
Bit 30	PEDCEN Enable Data Collection on F4 End-to-End BR cells. Related identifier PEDCID.
Bit 29	PSDCEN Enable Data Collection on F4 Segment BR cells directly generated from F4 Segment FM cells. Related identifier PSDCID.
Bit 28	PTSDCEN Enable Data Collection on terminated / intermediate F4 Segment BR cells, related identifier PTSDCID in Dword7.
PEDCID(6:0)	Identifier for Data Collection on F4 End-to-End BR cells. Related enable PEDCEN.
PSDCID(6:0)	Identifier for Data Collection on F4 Segment BR cells directly generated from F4 Segment FM cells. Related enable PSDCEN.
PPMTID(6:0)	Identifier for a terminating F4 Segment or End-to-End FM flow. Related enable PPMTEN in Dword4.
PPMOID(6:0)	Identifier for an originating F4 Segment or End-to-End FM flow. Related enable PPMOEN in Dword4.

3.9.4.4 Downstream F4 OAM Entry: Dword7

Bit 31	PAR Dword parity protection. In normal operation write to 0. Should always read as 0.
PTSDCID(6:0)	Identifier for Data Collection on terminated/intermediate F4 Segment BR cells, related to PTSDCEN in Dword6.

3.9.5 Internal PM Main RAM Entry: Dwords 0..2

Dword	31	23	15			7	0
2	FMDIFF(15:0)		BL(3:0)	FT		8	Unused
1	BIP16(15:0)		MCSNUP(7:0)				MCSN(7:0)
0	TUC(15:0)		TUC0(15:0)				

3.9.5.1 Internal PM Main RAM Entry: Dword 0

Bit 31:16 TUC(15:0)

Total user cell count high and low priority cells (CLP0+1). Used at originating and terminating point. Initialized to all 0 at PM set-up.

Bit 15:0 TUC0(15:0)

Total user cell count high priority cells only (CLP=0). Used at originating and terminating point. Initialized to all 0 at PM set-up.

3.9.5.2 Internal PM Main RAM Entry: Dword 1

Bit 31:16 BIP16(15:0)

Bit interleaved parity accumulated over block of user cells. Used at originating and terminating point. Initialized to all 0 at PM set-up.

Bit 15:8 MCSNUP(7:0)

Monitoring cell sequence number updated by the last FM cell. Used at terminating point only. Initialized to all 0 at PM set-up.

Bit 7:0 MCSN(7:0)

Monitoring cell sequence number running counter. Used at originating and terminating point. Initialized to all 0 at PM set-up.

3.9.5.3 Internal PM Main RAM Entry: Dword 2

Bit 31:16	FMDIFF(15:0)	
	Local TUC minus TUC from incoming FM cell at FM terminating point. FMDIFF is not used at FM originating point. Initialized to all 0 at PM set-up.	
Bit 15:12	Block length encoding.	
	Programmed by the microprocessor, read by the AOP.	
	BL(3:0)	Block Length
	0000	2
	0001	4
	0010	8
	0011	16
	0100	32
	0101	64
	0110	128
	0111	256
	1000	512
	1001	1024
	1010	2048
	1011	4096
	1100	8192
	1101	16384
	1110	32768
	1111	65536
Bit(11:10)	FT(1:0)	Flow Type
	00	F4 Segment
	01	F4 End-to-end
	10	F5 Segment
	11	F5 End-to-end

Bit 9	Unused	
Bit 8	BRIDIS	
	0	Backward Reporting cell insertion enabled
	1	Backward Reporting cell insertion disabled
Bit(7:0)	Unused	

3.9.6 Internal PM Data Collection RAM Entry: Dwords 0..13

Dword	31 23 15 7 0
13	SECBMIS(31:0)
12	SECBERR(31:0)
11	TLOSTC0(31:0)
10	TLOSTC(31:0)
9	IMPB(31:0)
8	MISC(31:0)
7	TRANSUC0(31:0)
6	TRANSUC(31:0)
5	LOSTC0(31:0)
4	LOSTC(31:0)
3	ERRC(31:0)
2	31 SECB(30:0)
1	TUCOLD(15:0) TUC0OLD(15:0)
0	TRCCOLD(15:0) TRCC0OLD(15:0)

3.9.6.1 Internal PM Data Collection RAM Entry: Dword 0

TRCCOLD(15:0)	Offset values : used for TUCDiff calculation.
TRCC0OLD(15:0)	Offset values : used for TUCDiff0 calculation.

3.9.6.2 Internal PM Data Collection RAM Entry: Dword 1

TUCOLD(15:0)	Offset values : used for TUCDiff/TRANSUC calculation.
TUC0OLD(15:0)	Offset values : used for TUCDiff0/TRANSUC0 calculation.

3.9.6.3 Internal PM Data Collection RAM Entry: Dword 2

Bit 31	FBR Set after the 1. BR cell, no Data Collection is done for 1. BR cell.
SECB(30:0)	Total severely errored cell blocks.

3.9.6.4 Internal PM Data Collection RAM Entry: Dword 3

ERRC(31:0)	Total errored cells.

3.9.6.5 Internal PM Data Collection RAM Entry: Dword 4

LOSTC(31:0)	Total lost cells (CLP = 0+1).

3.9.6.6 Internal PM Data Collection RAM Entry: Dword 5

LOSTC0(31:0)	Total lost cells (CLP = 0).

3.9.6.7 Internal PM Data Collection RAM Entry: Dword 6

TRANSUC(31:0)	Total transmitted user cells (CLP = 0+1).

3.9.6.8 Internal PM Data Collection RAM Entry: Dword 7

TRANSUC0(31:0)	Total transmitted user cells (CLP = 0).

3.9.6.9 Internal PM Data Collection RAM Entry: Dword 8

MISC(31:0)	Total misinserted cells.

3.9.6.10 Internal PM Data Collection RAM Entry: Dword 9

IMPB(31:0)	Total impaired blocks.

3.9.6.11 Internal PM Data Collection RAM Entry: Dword 10

TLOSTC(31:0)	Total lost cells (CLP = 0+1).

3.9.6.12 Internal PM Data Collection RAM Entry: Dword 11

TLOSTC0(31:0)	Total lost cells (CLP = 0).

3.9.6.13 Internal PM Data Collection RAM Entry: Dword 12

SECBERR(31:0)	Total severely errored cell blocks due to bit errors.

3.9.6.14 Internal PM Data Collection RAM Entry: Dword 13

SECBMIS(31:0)	Total severely errored cell blocks due to misinserted cells.

4 Operation

4.1 Overview

This section describes the actions to be done by the microprocessor. For this purpose the following network scenario is assumed (see also **Figures 9, 10 and 11** for reference):

- The OAM functions AIS/RDI/CC are always enabled for all connections (although the AOP also supports enabling on a per-connection basis). Activating the CC function by default avoids use of CC activation/deactivation cells.
- For all time-out values the recommended values of the standard [**6**] are used.
- Performance monitoring is always initiated by the generating port (**see Figure 26**) using PM activation cells. The respective endpoint loops a cell with 'activation request confirmed' back if a PM processor is available. If all 128 PM processors are in use the 'activation request denied' cell is sent back. The deactivation cell is always confirmed.
- PM data collection is always done on the port where the FM cells are generated, i.e. the BR cells are evaluated and discarded there (the AOP supports PM data collection on any point along the backward PM cell path).
- Segment borders are fixed to transmission lines (although the AOP supports the per-connection definition of segment points).
- At originating segment points AIS/RDI monitoring for VPCs is enabled, i.e. at the entrance of the network of an operator it is detected if a VPC is received fault-free or not. So the network operator knows at any time the availability of his VPCs. Monitoring is not activated for VCCs, as these are set-up only temporary.

All these assumptions facilitate OAM management by reducing the number of parameters to be handled.

4.1.1 Guidelines for microprocessor actions

4.1.1.1 Write-Modify-Read-Access

For a normal read-modify-write access to a RAM, the following actions have to be done by the microprocessor :

1. Write the data to the write transfer registers WDR0L..WDR13H (see **section 3.1.1,** page 59).
2. Set the mask bits in the mask data registers MDR0L..MDR6H and WMASK (see **section 3.1.3,** page 60 and **section 3.1.4,** page 61). Note that RAM words 0..6 are bitwise masked with the MDR registers, RAM words 7..13 are masked completely by setting the corresponding bit in register WMASK).
3. Write the LCI to the address register RMWADR (see **section 3.1.6,** page 63).
4. Set the following bits in the read-modify-write control register RMWC (see **section 3.1.5,** page 62) : bits 5..4 (e.g. to '01' for external RAM), bit 2 equal to '1' for upstream or equal to '0' for downstream and bit 3 epual to '1', i.e. start of RMW.
5. The RMW is done when bit 3 of RMWC is set to '0' by the AOP.
6. Read the read transfer registers RDR0L..RDR13H (see **section 3.1.2,** page 60).

RMW access on PM or DC RAM is the same as for the external RAM, besides that RMWADR should have a value between 0 and 127 and for PMMAIN only registers WDR0L..WDR2H, RDR0L..RDR2H, MDR0L..MDR2H are used. The entries 0..3 will be written to address LCI defined by register RMWADR, the entries 4..7 to address LCI2 defined in entry 0. Note, that read

data from a former RMW cycle is lost during write-only-access (bit 0 of register RMWC equal to ’1’). During read or modify the external RAM parity-check will be done. While RMW is active, the registers RMWC and RMWADR are writeprotected.

4.1.1.2 Cell insertion by the microprocessor

When the microprocessor should insert cells, e.g. PM or CC, follow this guideline :

1. Write the cell data into the transmit cell payload registers TXR0..26 (see **section 3.3.1,** page 67 and **section 3.3.2,** page 68).
2. If the cell is to be inserted in downstream direction set bit 0 of the transmission command register TMCR (see **section 3.3.3,** page 69). Otherwise set bit 1 (for upstream direction). If both bits are set to ’1’, the AOP reacts in the same way as if only bit 1 is set.
3. After the insertion of the microprocessor cell into the datastream, the choosen bit in register TMCR will be reset by the AOP.

4.1.1.3 Reading of arrived cells by the microprocessor

If a cell arrives at the AOP, the microprocessor must perform the following operations :

1. The AOP signals the availability of arrived cells by setting bit 9 of the interrupt register ISR0 (see **section 3.6.1,** page 83).
2. The microprocessor has to read the receive cell register RXRCEL for 27 times.
3. Bit 6 of the UDF2 octed will indicate the source of the arrived cell (’0’ = downstream).
4. After the 27th read access the AOP will reset bit 9 of ISR0.

The cell will be read in the same order as the transmit cell, i.e. address 80 to 9C.

4.1.1.4 SCAN usage

Here is an example for the usage of the SCAN.

1. Setup the connections in the external RAM using RMW.
2. For general adjustement of the SCAN procedure, the microprocessor has to write the first LCI to be processed into register SCCONF4 (see **section 3.5.13,** page 80) and the last LCI to be processed into register SCCONF5 (see **section 3.5.14,** page 81). Write the values for SCP and SCPTOL into register SCCONF2 (see **section 3.5.11,** page 79 and **section 2.15,** page 48). Further some adjustments for DMA are needed when use of DMA is intended. Set bit 3 of the DMA configuration register DCONF (see **section 3.5.8,** page 77) to the respective value for normal or compressed mode. Additionally write the index value to the same register (bit 2..0). Write DMA data to registers DWDRL and DWDRH (see **section 3.5.1,** page 74 and **section 3.5.2,** page 74) and the RMW mask to registers DMRL and DMRH (see **section 3.5.3,** page 75 and **section 3.5.4,** page 75). At last adjustments for the OAM are needed when use of OAM is intended. Herefore setup the counter limits for state transitions in the registers SCCONF0 and SCCONF1 (see **section 3.5.9,** page 78 and **section 3.5.10,** page 79).
3. The SCAN mechanism is started by the following actions. Write respective settings to the SCAN command register SCCONF3 (see **section 3.5.12,** page 80). The SCAN is started by setting bit 0. This bit is reset as soon as the SCAN mechanism is started internally.
4. The SCAN is finished when the start bit is reset and bit 0 of the SCAN status register is equal to ’0’ (see **section 3.5.15,** page 81).

The registers in the SCAN block are write protected during the SCAN operation.

4.1.2 Initialization and Test

These are the actions to be performed after reset to prepare the AOP for operation.

- Check reset values of all registers
- Set HW configuration (RAM type, UTOPIA configuration)
- Initialize internal and external RAMs
  For this purpose the DMA feature of the chip could be used.
- Test parity detectors
- Check data path (via adjacent ATM devices)

4.1.3 Configuration

The following parameters must be known by the microprocessor for the operation of the AOP:

- Number of PHYs
- Edge-of-the-network or intra-network point for each PHY
- Switch Port ID for intra-network Loopback
- Number of supported connections
- Thresholds for PM data collection values
- Use of internal CC function or not.

4.1.4 Setup/ Cleardown of Connections

For a connection setup the following parameters are required:

- Local connection identifier LCI
- VPC or VCC
- If VCC the LCI2 value of the associated VP-entry (VP-pointer)
- VCC endpoint indication (at AAL function)
- PHY number

All further programming is done using the edge-of-the-network or intra-network configuration of the PHY (for the abbreviations see **Section 8.4**):

- In case of a VCC the upstream part of the AOP is configured as VP-TEP and the downstream part as VP-OEP. If in addition the PHY is configured as edge of a network the upstream part is configured as VC-OSP and the downstream part as VC-TSP.
- In case of a VPC without a segment border both up- and downstream parts are configured as intermediate point (VP-IP). If the PHY is configured as edge of the network the upstream part is configured as VP-OSP and the downstream part as VP-TSP.

Note: If a PHY is at the edge of a network its transmission line is connected to the network of another operator. Hence all segment streams are terminated before the ATM cells leave the node (non-overlapping mode).

- At OEPs the CC flow generation is enabled (VPC or VCC, segment or end-to-end).

4.1.5 Enable/ Disable of PM

This command is issued by the microprocessor either on request from the system controller or in the course of a activation/deactivation cell received for this connection. The following parameters are needed:

- LCI of the connection or LCI2 of the VP-pointer
- Block size 128, 256, 512 or 1024
- Mode select:
  1) generate and collect data or
  2) analyze and loop.

4.1.6 Normal Operation

4.1.6.1 Scan Process Trigger

In fault free state the main task of the microprocessor is to trigger the scan function in 500 ms intervals. This is done by setting one single bit in a register. An internal logic checks all requested entries (from LCI min. to LCI max) of both up- and downstream external RAMs. According to the actual state of the connection (AIS state, PHY failure, CC state etc.) and the programmed time-out values the respective state transitions are performed automatically by the AOP. In addition an interrupt bit is set if a state transition to or from failure state occurred. As long as no state transition occurs nothing else has to be done by the microprocessor than to trigger the scan in 500 ms intervals.

In case of an interrupt the microprocessor must determine the connection which triggered the (common) interrupt. For this purpose the compressed DMA function is enabled together with the next scan, which transfers the status dword of all connections from both up- and downstream external RAM to the microprocessor memory. The status dword contains:

- VP/VC AIS/RDI/LOC defect/failure state
- transition events between these states and fault-free state
- error indication bits
- direction bit.

The compressed DMA can be programmed to clear the transition event bits after read within the same scan/DMA process (**see Figure 31**).

The microprocessor is informed by the AOP about transitions to failure states and back to fault-free states via interrupt. According to the standards transitions to defect states are not reported.

Scan and DMA completion is indicated by flags. With one 32-bit dword transferred per connection and per direction, in total up to 32 K dwords are transferred to the microprocessor memory. The dwords are stored in the designated RAM area with ascending LCI values from lower to upper LCI limit. Upstream and downstream dword of a LCI are adjacent, but their order is undetermined. The direction bit must be evaluated for each dword.

Bit Mapping for "Compressed" DMA Mode

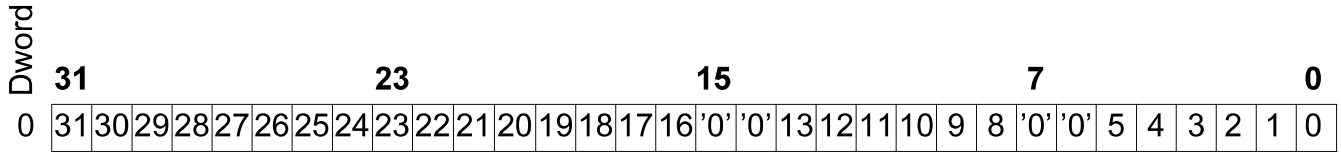


Table 6 Bit Mapping for "Compressed" DMA Mode

Bit#	Name	F4/F5	Dword[1)]	Bit#[1)]	Indication[2)]
31	'1' : Up '0' : Down	-	-	-	Indicates upstream or downstream external RAM.
30	Parity Error	-	-	-	If =1 at least one dword of the LCI entry a parity error was detected.
29	PLOCF2N	F4	4	27	Indication for a state transition from LOC Failure state to LOC Normal state.
28	PLOCD2F	F4	4	26	Indication for a state transition from LOC Defect to LOC Failure state.
27	PRDIF2N	F4	4	25	Indication for a state transition from AIS Failure to AIS Normal state.
26	PRDID2F	F4	4	24	Indication for a state transition from AIS Defect to AIS Failure state.
25	PAISF2N	F4	4	23	Indication for a state transition from AIS Failure to AIS Normal state.
24	PAISD2F	F4	4	22	Indication for a state transition from AIS Defect to AIS Failure state.
23	EDCERR	F4	2	13	Wrong EDC (CRC10) in an OAM cell detected.
22	OAMMIS	F4	2	12	Misinserted OAM cell discarded.
21	PLOCFAI	F4	5	5	F4 LOC failure state indication.
20	PLOCDEF	F4	5	4	F4 LOC defect state indication.
19	PRDIFAI	F4	5	3	F4 RDI failure state indication.
18	PRDIDEF	F4	5	2	F4 RDI defect state indication.
17	PAISFAI	F4	5	1	F4 AIS failure state indication.
16	PAISDEF	F4	5	0	F4 AIS defect state indication.
15	'0' always	-	-	-	
14	'0' always	-	-	-	
13	CLOCF2N	F5	2	19	Indication for a state transition from F5 LOC failure state to F5 LOC normal state.
12	CLOCD2F	F5	2	18	Indication for a state transition from F5 LOC defect state to F5 LOC failure state.

Table 6 Bit Mapping for "Compressed" DMA Mode

Bit#	Name	F4/F5	Dword[1)]	Bit#[1)]	Indication[2)]
11	CRDIF2N	F5	2	17	Indication for a state transition from F5 RDI failure state to F5 RDI normal state.
10	CRDID2F	F5	2	16	Indication for a state transition from F5 RDI defect state to F5 RDI failure state.
9	CAISF2N	F5	2	15	Indication for a state transition from F5 AIS failure state to F5 AIS normal state.
8	CAISD2F	F5	2	14	Indication for a state transition from F5 AIS defect state to F5 AIS failure state.
7	’0’ always	-	-	-	
6	’0’ always	-	-	-	
5	CLOCFAI	F5	1	5	F5 LOC failure state.
4	CLOCDEF	F5	1	4	F5 LOC defect state.
3	CRDIFAI	F5	1	3	F5 RDI failure state.
2	CRDIDEF	F5	1	2	F5 RDI defect state.
1	CAISFAI	F5	1	1	F5 AIS failure state.
0	CAISDEF	F5	1	0	F5 AIS defect state.

[1)] Refer to the external RAM (identical for up- and downstream RAM).

[2)] For detailed explanation see section 3.9.1, page 98, section 3.9.2, page 104, section 3.9.3, page 110 and section 3.9.4, page 116.

4.1.6.2 PM Threshold Check

Also in normal operation the local controller checks all data collection entries, compares the values with the given thresholds and if these are exceeded

- Activates AIS/RDI insertion and
- Informs network management

Optionally records of the e.g. last 15 minutes could be collected on-board for the last 24 hours.

4.1.7 Events

Events are unpredictable for the peripheral controller. These may be interrupts from the HW or command messages received from the system controller .

4.1.7.1 Transmission Line Failure

Such failures are e.g. line breaks or transmitter/receiver failure. They are detected by the PHY device and usually signalled to the local controller by interrupt. If the failure is confirmed the local controller

- sets the corresponding PHY error bit in a AOP register

to signal the failure to the ATM layer. All ensuing actions as generation of VP-AIS or VC-AIS cells in forward direction as well as the insertion of VP-RDI or VC-RDI cells in backward direction are done automatically by the scan mechanism.

4.1.7.2 LB Cell Transmission/ Reception

The transmission of a LB cell is usually initiated by the system controller. The parameters

- LCI
- segment or end-to-end or intra-domain LB
- the Location identifier in case of intra-domain LB

must be given by the system controller. Note that in case of a segment or end-to-end LB the location and source ID are set to all ones. The microprocessor assembles the LB cell and transmits it via the AOP. A timer is started for time-out supervision.

Prior to transmission the LB State bit is set for this connection. This bit causes the returning LB cell to be copied to the receive buffer. If it is not set the backward LB cell is discarded without notice. By comparing the correlation tag the peripheral controller makes sure that the cell was the one sent out before.

Note: The correlation tag is not generated by the AOP. It is recommended to generate a random number by the peripheral controller.

4.1.7.3 PM Activation/ Deactivation Cell Transmission

The request to do performance monitoring over a given VPC or VCC connection or segment is initiated by the system controller and sent to the originating point microprocessor. The parameters

- LCI or LCI2 (for F4 PM)
- Block size (128, 256, 512, 1024)

must be given. Similar to the LB procedure the microprocessor generates an appropriate activation cell for either segment or end-to-end, depending on the given configuration. After reception of the confirmation cell (**Section 2.10**) the FM generation processor is assigned as well as a data collection processor in the opposite direction. There are two restrictions to be checked:

- there are at most 128 processors for FM generation or analysis and 128 processors for data collection
- not more than 2 processors can be invoked for one user cell, one for F4 and one for F5 (**Section 2.9**).

4.1.7.4 PM Activation/ Deactivation Cell Reception

An activation/ deactivation cell may be received at any time at the receive buffer of the AOP. In such a case the peripheral controller looks for a free PM processor and assigns it to the connection. The PM processor is initialized in analyzing mode. Then a confirmation cell is sent back to the originating port. The PM endpoint is now ready for reception of the first FM cell.

4.2 Examples

4.2.1 PM Configuration

In this example a VPC containing a VCC is terminated. A number of PM measurements are performed:

- end-to-end PM at F4 (VPC) level bi-directional
- segment PM termination and creation of a new segment at F5 (VCC) level uni-directional

In total 4 PM processors and 2 data collection processors are involved. Their associated RAM entries are shown in **Figure 33**. The two connections involved, VPCa and VCCb are represented by 2 entries in each up- and downstream RAM, a F4 and a F5 entry with the F5 entry pointing to the F4 entry. Each entry has 4 pointer + enable pairs to define:

- the origination point of a PM flow
- the endpoint of a PM flow
- a data collection point for a end-to-end flow
- a data collection point for a segment flow.

For origination and termination points the selection between end-to-end and segment flows is done in the PM main RAM by setting the flow type (FT) bits. At termination points the generation of BR cells can be enabled by setting BRDIS=0. A further parameter to specify is the block length BL. In the example of **Figure 33** two different block sizes are used, 1024 (coding 1001) at the F4 level and 256 (coding 0111) at the F5 level.

The data collection function evaluates the contents of BR cells. It can be enabled at any point along the path of the BR cells, including the analyzing point where the BR cells are generated. In the present example the evaluation occurs at the end point of the BR cells.

The scenario shown in **Figure 33** can only occur at an ingress port of a switch, where VPCs are terminated. Hence the origination of a end-to-end F4 flow should not be programmed in upstream direction. Conversely in downstream direction a F4 end-to-end flow must not be enabled.

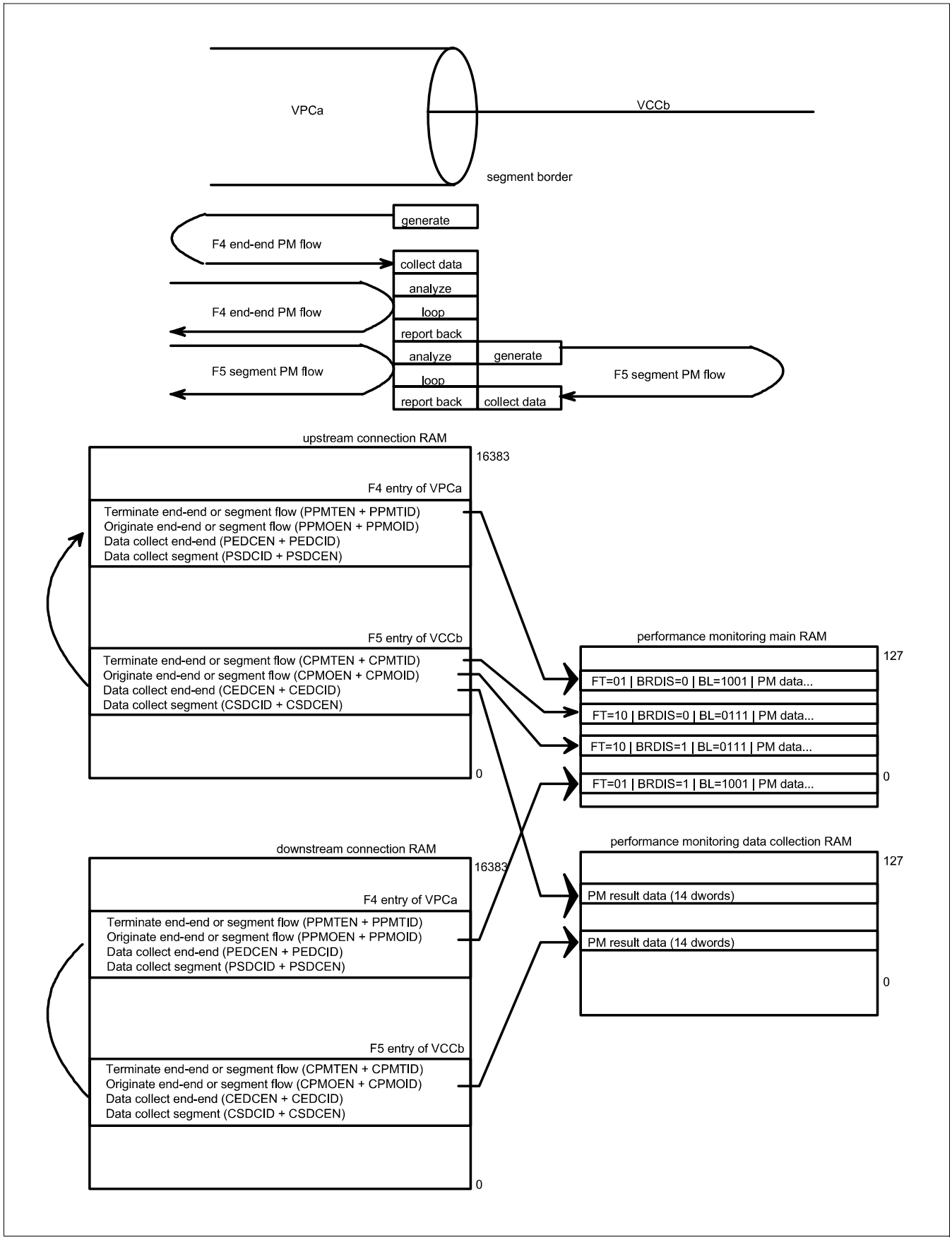


Figure 33 Performance Monitoring Example

5 Interfaces

5.1 UTOPIA Interfaces

The AOP has one UTOPIA receive interface and one UTOPIA transmit interface with master capability at the PHY side and one receive and transmit interface with slave capability at the ATM side (**figure 34**). The interfaces are compliant to the UTOPIA Level 1 and 2 specification [**1, 2**], i.e.:

- bus width is selectable either 8 or 16 bit
- single-PHY or multi-PHY configurations
- PHY number enhancement option, see specification UTOPIA Level 2 Appendix 1.

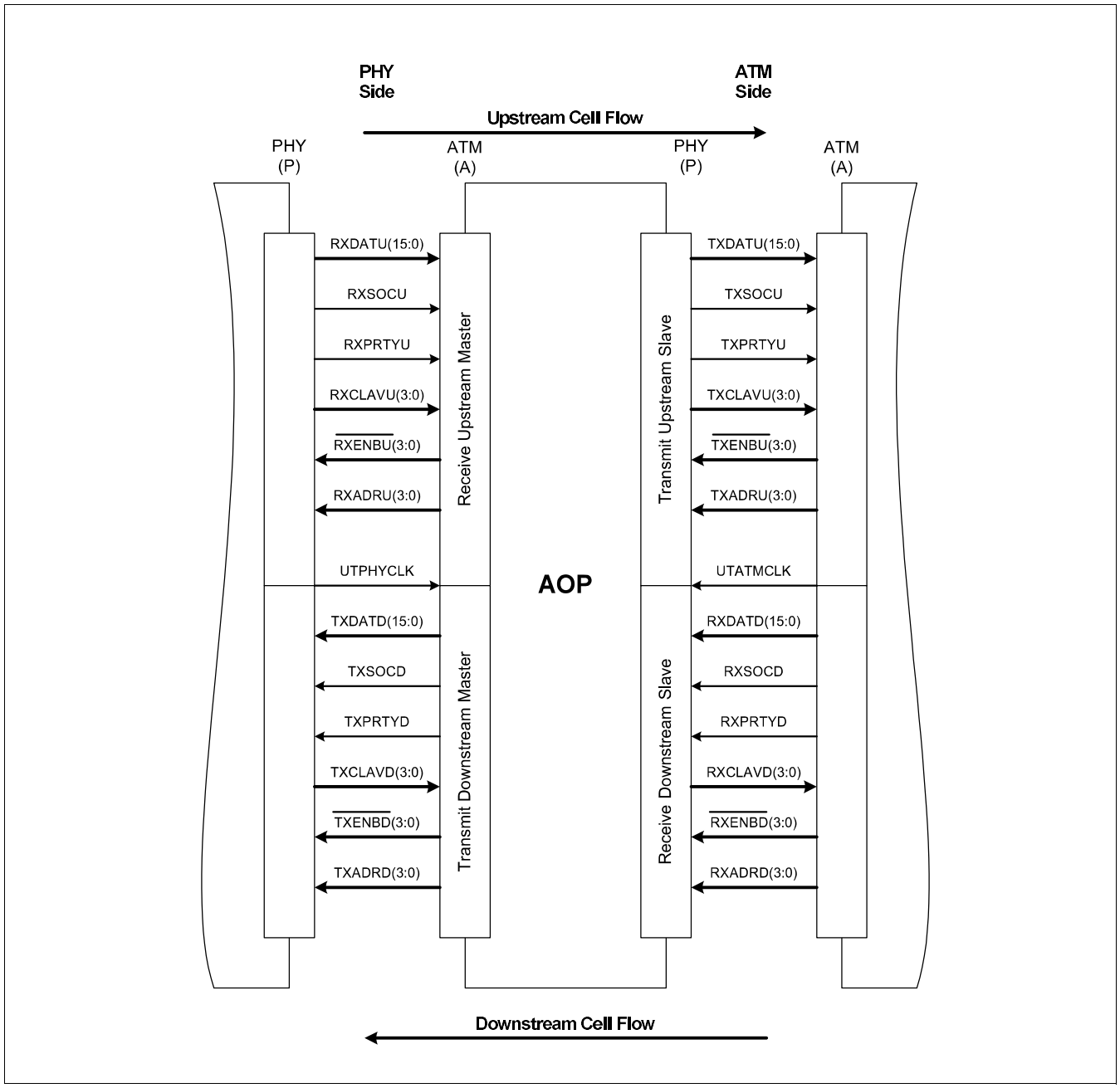


Figure 34 UTOPIA Interfaces

Receive and transmit side of ATM and PHY side UTOPIA interface operate each from one clock which may be completely independent from the main chip clock SYSCLK. The UTOPIA clock frequency must be less than or equal to the main chip clock SYSCLK.

The UTOPIA interface has an 8-bit and a 16-bit option. The 16-bit option has the 54 octet cell format shown in **figure 35** for the standardized format and in **figure 36** for the proprietary format. The 8-bit format has 53 octet without the UDF2 octet. ATM side and PHY side UTOPIA interface can be configured independently in 8-bit or 16-bit mode.

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VPI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	UDF1								UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Figure 35 Standardized UTOPIA cell format (16-bit)
all fields according to standards, unused octets shaded

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LCI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	LCI(13:12)		HK(2:0)			PN(2:0)			UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Figure 36 Proprietary UTOPIA cell format (16-bit)

with PN(2:0) = port number for PXB 4220 IWE8 (don't care for AOP)
HK(2:0) = housekeeping bits (only for Internal Continuity Check ICC)
LCI(13:0) = Logical Connection Identifier
all other fields according to standards, unused octets shaded.

5.1.1 UTOPIA Multi-PHY support

To support multi-PHY configurations with and without use of the UTOPIA PHY address the Infineon Technologies ATM switching chip set supports the Direct Status Polling option of the UTOPIA Level 2 standard [**2**]. It allows the simultaneous polling of up to 4 groups of PHYs by using 4 CLAVx/ENx signal pairs (x=0..3).

During the transfer of a cell the master UTOPIA interface polls 12 PHY addresses. The 27 clock cycles time for the transfer of a cell in 16-bit UTOPIA format allows to poll 12 PHY addresses and to select one of them for the next cell transfer. Receive and transmit UTOPIA interfaces always poll separately. To allow the support of more than 12 PHYs 4 pairs of CLAVx/ENx lines are provided in all Infineon Technologies ATM switching chips with UTOPIA interfaces.

However, although 48 PHYs could be polled by this configuration only up to 24 PHY are supported.

Note: the number of line interfaces (PHYs) to be supported by an ATM layer chip is basically depending on the number of its queues. The term 'PHY device', however, denotes 'PHY chips', which may contain more than one PHY. For electrical load considerations the number of PHY devices is important, as the standard requires that for a 25 MHz clock a minimum 8 PHY devices must be driven, for 50 MHz a minimum 4 PHY devices.

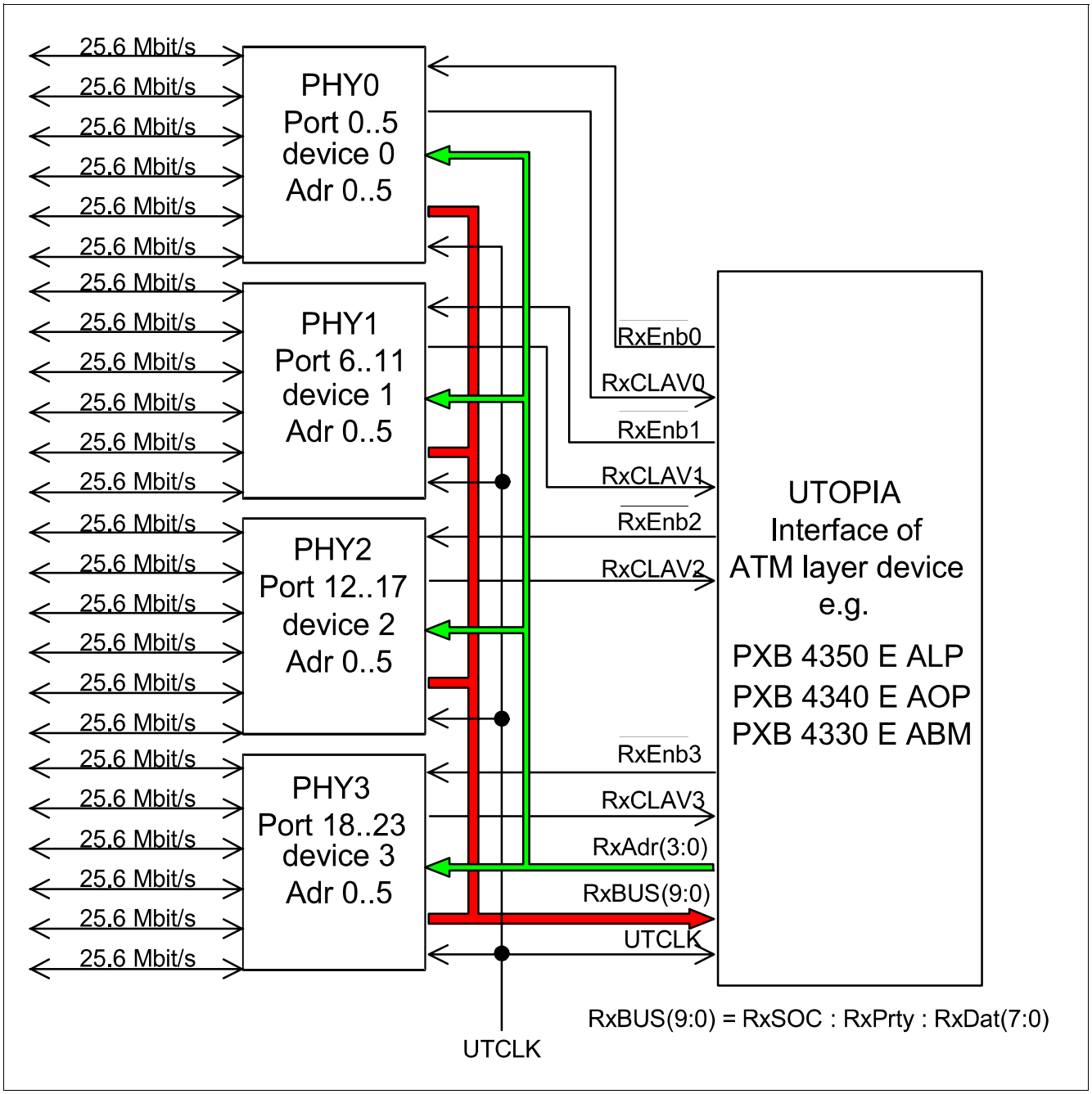


Figure 37 Upstream receive UTOPIA example for 4 x 6 PHYs

There are four different operating modes for the UTOPIA interface. Three of them are multi-PHY modes which use the address bus. One additional mode is provided, for connecting Level 1 PHY chips without address inputs. All modes are summarized in **Table 7**.

Table 7 UTOPIA polling modes.
The numbers indicate the offset which is added to the PHY number.

	Mode 2 x 12	Mode 3 x 8	Mode 4 x 6	Level 1 Mode
$\overline{EN0}$ / CLAV0	0	0	0	0
$\overline{EN1}$ / CLAV1	12	8	6	0
$\overline{EN2}$ / CLAV2	do not connect	16	12	0
$\overline{EN3}$ / CLAV3	do not connect	do not connect	18	0

The poll cycle is identical in all modes, i.e. the address lines output all addresses from 0 to 11 during one cell cycle. In one polling cycle all PHYs are polled. If the address is greater than the number of PHYs at the device, the associated CLAVx is set to 0. The real PHY number depends on the selected mode. The polling sequence of the next polling cycle depends on the current transmitting PHY, e.g. if PHY5 is the current transmitter the next polling sequence is as follows: PHY6,PHY7,...,PHY11,PHY1,PHY2,...,PHY5. In this case, PHY6 has the highest priority and PHY5 the lowest. PHY5 is polled at byte 48 of the payload only when no other PHY is selected.

The selection of the next device also depends on the current device. If the current transmitter is from device 2, the next polling cycle starts with the device 3 (highest priority), then device 4, device 1 and device 2 (lowest priority).

- In Level 1 mode the PHY numbers are identical to the CLAV/$\overline{EN}$ group: 0, 1, 2, 3.
- It is the users responsibility to program the PHY numbers in a way that ambiguous PHY numbers inside the ATM layer device are avoided.
- The mode selection can be done independently for the PHY side and the ATM side UTOPIA interface (see **section 3.7.1,** page 87 and **section 3.7.2,** page 88).
- If less than or equal to 12 PHYs are to be polled, mode 2 x 12 should only be used with the CLAV0/$\overline{EN0}$ pair connected. This minimizes the number of interconnection lines between the chips.

Examples:

1. One PHY device, e.g. a 622 Mbit/s PHY: 16-bit bus width, address lines unconnected, RxCLAV0/$\overline{RxEN0}$ and TxCLAV0/$\overline{TxEN0}$ signal pairs connected, all other CLAVx/$\overline{ENx}$ pairs unconnected (Level 1 Mode).
2. 4 PHY devices 155.52 Mbit/s PHYs: 16-bit bus width, address lines unconnected, all 4 CLAVx/$\overline{ENx}$ pairs connected, one to each PHY device.
3. 4 PHY devices of 6-fold 25.6 Mbit/s PHYs: 16-bit bus width, address and all 4 CLAVx/$\overline{ENx}$ pairs connected, one to each PHY device (Mode 4x6, see **figure 37**). The 4 CLAVx/$\overline{ENx}$ lines are connected one-to-one to 4 PHY devices, each containing 6 PHYs of 25.6 Mbit/s. In this example the maximum number of 24 PHYs is connected. The AOP gets 4 CLAVx signals with each polled address. All PHY devices have the addresses 0..5 assigned to their PHYs. Addresses greater than 5 always return CLAVx=0 when polled. In order to distinguish the PHYs the UTOPIA interface of the AOP adds offset numbers, e.g. 6, 12 and 18 in mode 4x6, to the PHY numbers from PHY device 1, 2 and 3, respectively. Then within the ATM layer device the PHY numbers range from 0..23 without ambiguity.
4. 4 PXB 4220 IWE8s: 8-bit bus width, address bus unconnected, all 4 CLAVx/$\overline{ENx}$ pairs connected, one to each IWE8 (this mode requires the PXB 4350 E ALP).

5.2 RAM Interfaces

The AOP uses external, synchronous, static RAM (SSRAM) for the storage of connection related OAM data. Two identical SSRAM interfaces are provided, one for each direction. The SSRAM chips are operated with the system clock of up to 52 MHz.

All memory entries are protected with a parity bit at the MSB location.

The size of the SSRAM is depending on the number of supported connections: 8 dwords of 32-bit are required per connection. Using SSRAM devices of 1 Mbit or 2 Mbit size, i.e. 32 K x 32 bit and 64 K x 32 bit, respectively, the possible memory configurations are:

- 2 x 2 Mbit or 4 x 1 Mbit SSRAM for 16384 connections
- 1 x 2 Mbit or 2 x 1 Mbit SSRAM for 8192 connections
- 1 x 1 Mbit SSRAM for 4096 connections

These are the values for one direction. Both up- and downstream external memory should always be configured symmetrical. The selection 1 Mbit or 2 Mbit SSRAM chips is done via register bits. **Figure 31** shows an example of maximum RAM size with two 2 Mbit devices, **figure 39** shows an example of maximum RAM size with four 1 Mbit devices.

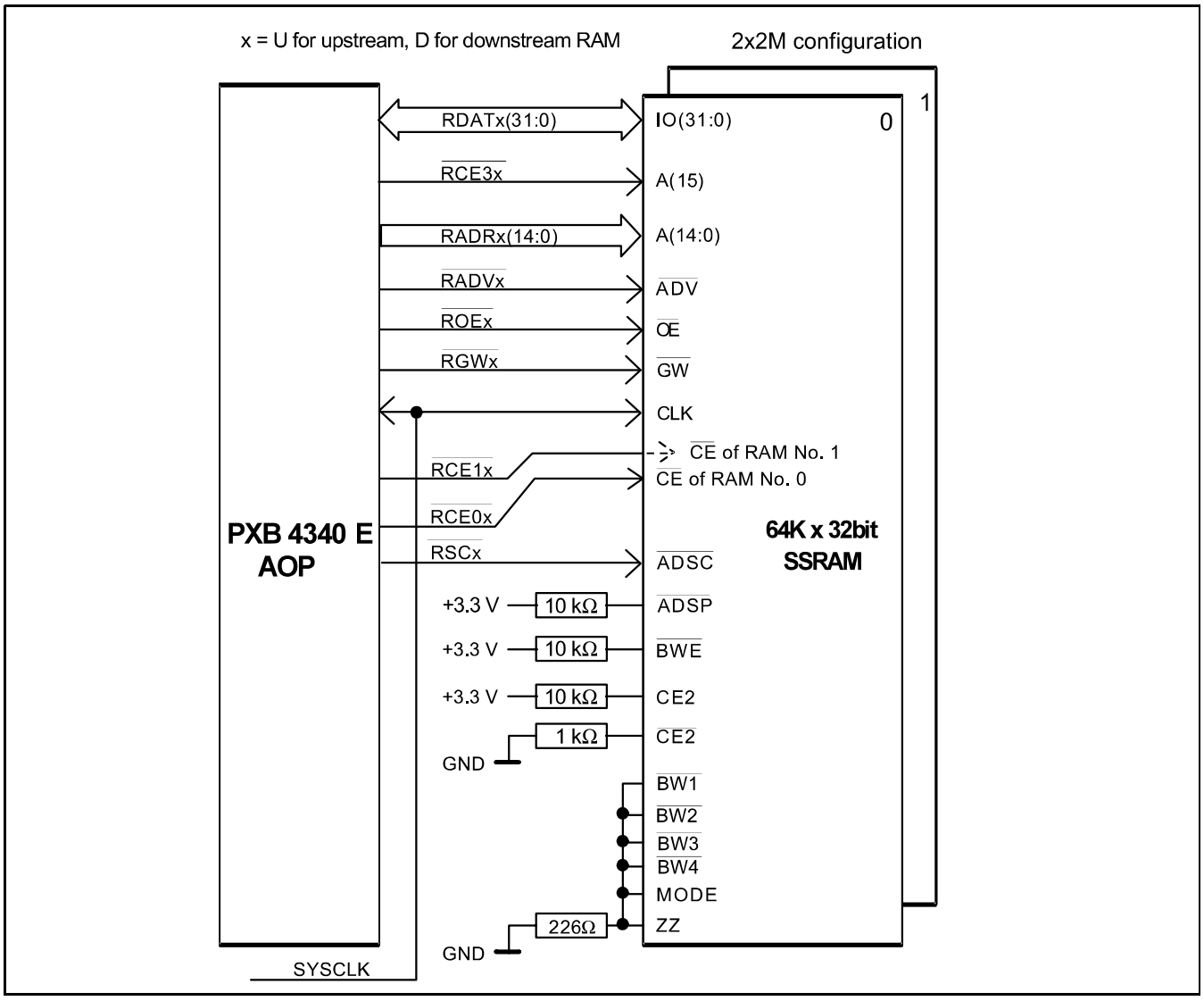


Figure 38 Upstream or downstream RAM interface using 2 Mbits RAMs

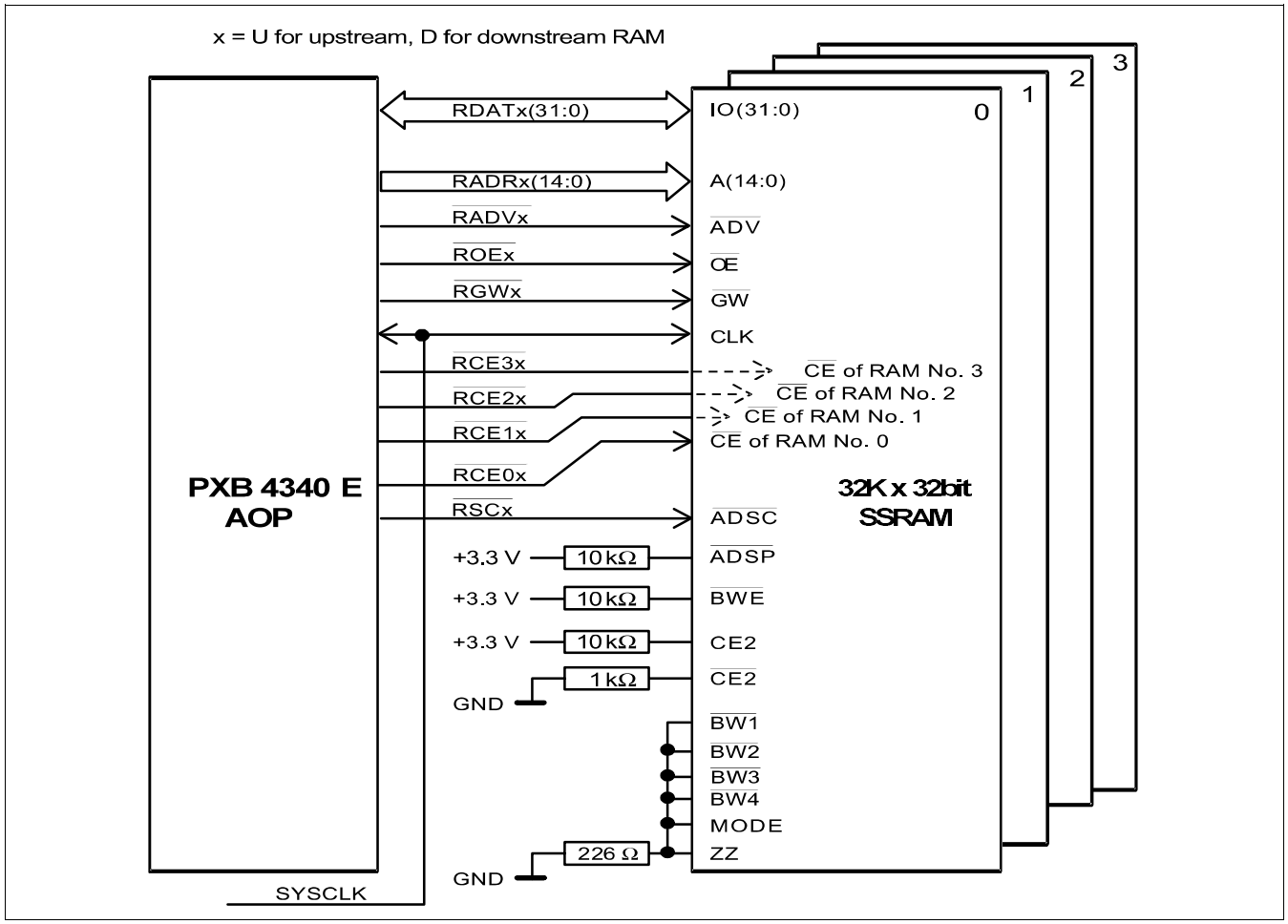
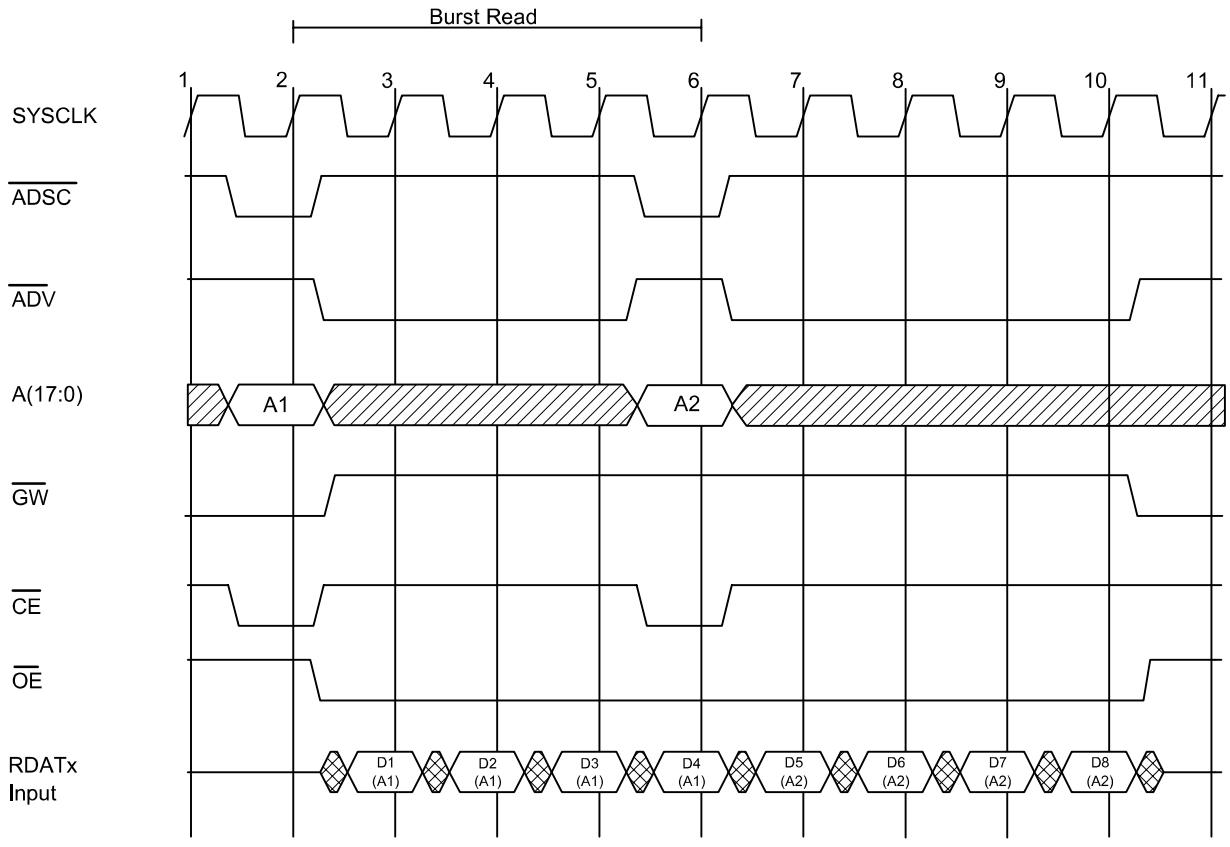


Figure 39 Upstream or downstream RAM Interface using 1 Mbit RAMs

Note that RCEx2 is unused and RCEx3 is used as additional address pin adr(15) when using 2 Mbit RAMs.The AOP uses 4-bursts to access the external RAMs. **Figure 40** shows an example for the read access. During each cell cycle two 4-burst read and two 4-burst write accesses are made at both up- and downstream RAM. If no cell is to be processed at one of the interfaces a scan/DMA access or microprocessor access is executed.



D1..D8 Dwords 1..8 from external RAM
A1 Address from RMW Address Register
A2 Address LCI2 from external RAM entry

Figure 40 Example of Execution Timing for Read Cycles (Burst Mode)

5.3 Microprocessor Interface

The AOP has a 16-bit microprocessor interface for control and operation. It is identical for all devices of the Infineon Technologies ATM switching chip set . A possible microprocessor could be the 386EX embedded controller as shown in **figure 41**.

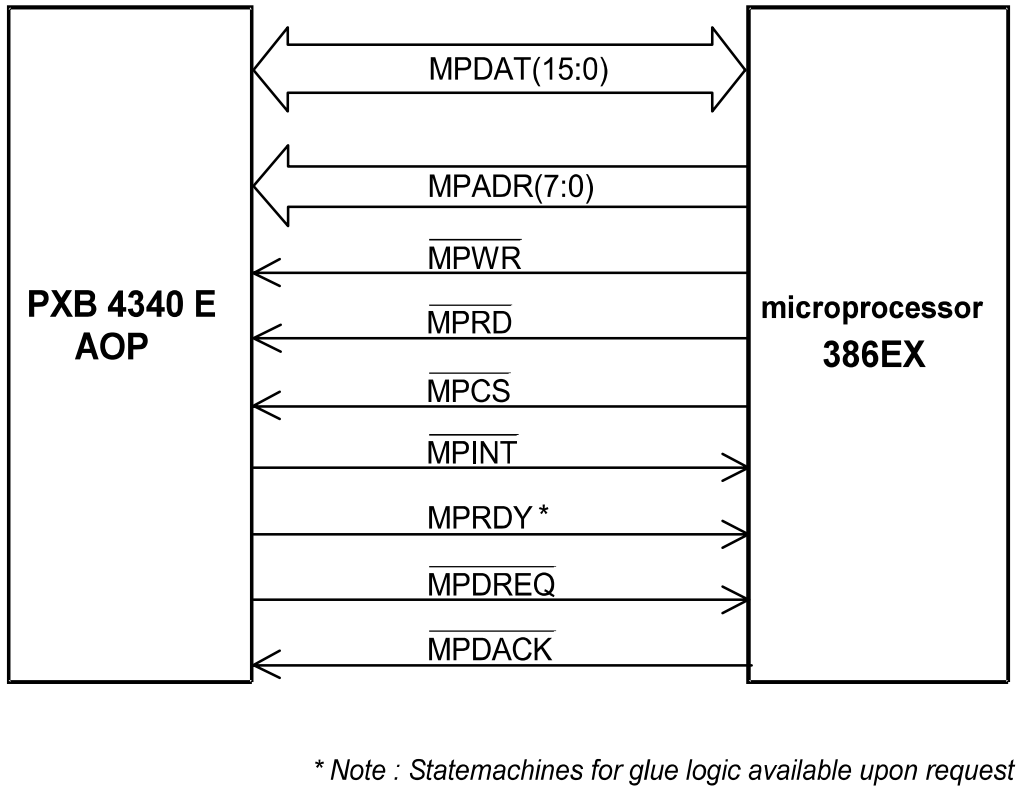


Figure 41 Microprocessor Interface

The interface is operating completely asynchronous to the system clock SysClk.

5.4 JTAG/Boundary Scan Interface

This interface contains the boundary scan of all signal pins according to the standard [**4**]. It consists of the pins shown in **figure 42**.

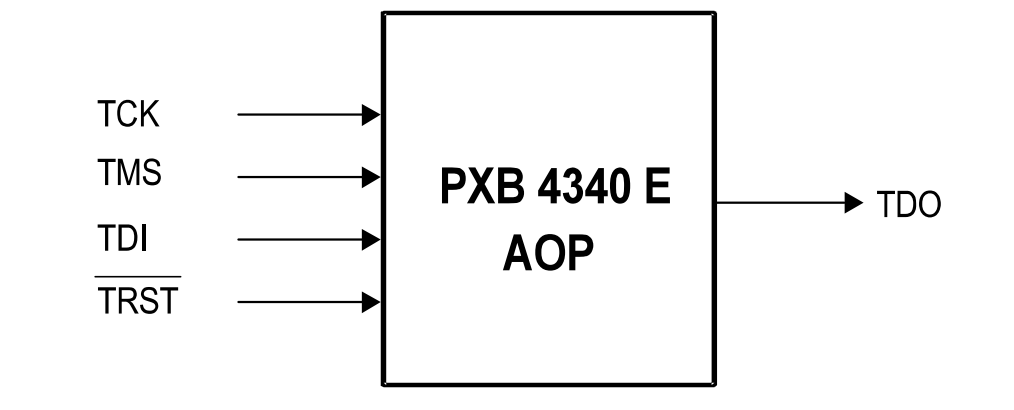


Figure 42 JTAG Interface

5.5 Test Interface

There are several additional test pins provided for board test. Please let them unconnected or connected to ground as described in section 5.6, part "Additional Testpins".

5.6 Pin Definitions and Functions

The following explanations applies for all Pins of a field in the table respectively:

- Pins with a [1] attached are connected with an internal pull up resistor.
- Pins with a [2] attached are connected with an internal pull down resistor.
- Pins with a [3] attached are 5V compatible.

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Clock and reset (4 pins)			
AC26	$\overline{\text{RESET}}$	I	Chip reset
B12	SYSCLK	I	Main chip clock
A13	UTPHYCLK	I	UTOPIA clock at PHY side (master).
AE14	UTATMCLK	I	UTOPIA clock at ATM side (slave).
Utopia-Interface (receive upstream master) (30 pins)			
B20, A20, C20, B19, D18, A19, C19, B18, A18, B17, C18, A17, D17, B16, C17, A16 [2]	RXDATU (15:0)	I	Receive data bus from PHY side.
C23, A23, B22, D22	RXADRU (3:0)	O	Address outputs to PHY side.
A21 [2]	RXPRTYU	I	Odd parity of RXDATU(15:0) from PHY side.
A25, B24, A24, B23	$\overline{\text{RXENBU}}$ (3:0)	O	Enable signal to PHY side.
A22, B21, D20, C21 [2]	RXCLAVU (3:0)	I	Cell available signal from PHY side.
C22 [2]	RXSOCU	I	Start of cell signal from PHY side.

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Utopia-Interface (transmit downstream master) (30 pins)			
D12, B10, C11, A10, D10, B9, C10, A9, B8, A8, C9, B7, D8, A7, C8, B6	TXDATD (15:0)	O	Transmit data bus to PHY side.
D13, A12, B11, C12	TXADRD (3:0)	O	Address to PHY side.
A11	TXPRTYD	O	Odd parity to PHY side.
A15, C16, B14, D15	$\overline{\text{TXENBD}}$ (3:0)	O	Enable signal to PHY side.
D7, A6, C7, B5 [2]	TXCLAVD (3:0)	I	Cell available signal from PHY side.
B15	TXSOCD	O	Start of cell signal to PHY side.
Utopia-Interface (receive downstream slave) (30 pins)			
AF9, AE9, AD8, AF8, AC9, AE8, AD7, AF7, AE7, AF6, AD6, AC7, AE6, AF5, AD5, AC5 [2]	RXDATD (15:0)	I	Receive data bus from ATM side.
AD11, AF12, AE12, AF11 [2]	RXADRD (3:0)	I	Address from ATM side.
AE5 [2]	RXPRTYD	I	Odd parity of RXDATD(15:0) from ATM side.
AD12, AF13, AC12, AE13 [1]	$\overline{\text{RXENBD}}$ (3:0)	I	Enable signals from ATM side.
AE11, AC10, AF10, AD9	RXCLAVD (3:0)	O	Cell available signal to ATM side.
AD10 [2]	RXSOCD	I	Start of cell signal from ATM side.

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Utopia-Interface (transmit upstream slave) (30 pins)			
AD18, AF19, AE19, AF18, AD17, AE18, AC17, AF17, AD16, AE17, AC15, AF16, AD15, AE16, AF15, AD14	TXDATU (15:0)	O	Transmit data bus to ATM side.
AE23, AD21, AF22, AE21 [2]	TXADRU (3:0)	I	Address from ATM side.
AE15	TXPRTYU	O	Odd parity of RXDATU(15:0) to ATM side.
AD23, AE24, AD22, AF23 [1]	$\overline{\text{TXENBU}}$ (3:0)	I	Enable signal from ATM side.
AD19, AF20, AC19, AE20	TXCLAVU (3:0)	O	Cell available signal to ATM side.
AD13	TXSOCU	O	Start of cell signal to ATM side.
Microprocessor Interface (31 pins)			
E2, E4, E3, E1, F2, G4, F3, F1, G2, G1, G3, H2, J4, H1, H3, J2	MPDAT (15:0)	I/O	Microprocessor data bus
C4, B3, C5, A4, D5, B4, C6, A5	MPADR (7:0)	I	Address from microprocessor
B1	$\overline{\text{MPWR}}$	I	Write enable from microprocessor.
C2	$\overline{\text{MPRD}}$	I	Read enable from microprocessor.
A3	$\overline{\text{MPCS}}$	I	Chip select from microprocessor.
D1 [3]	$\overline{\text{MPINT}}$	O	Interrupt request to microprocessor.
D3	$\overline{\text{MPDREQ}}$	O	DMA request to microprocessor.
D2	MPRDY	O	Ready output to microprocessor for read and write accesses.
C1	$\overline{\text{MPDACK}}$	I	µP DMA acknowledgment

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Connection Data SSRAM Upstream (55 pins)			
L25, M24, L26, M23, K25, L24, K26, K23, J25, K24, J26, H25, H26, J24, G25, H23, G26, H24, F25, G23, F26, G24, E25, E26, F24, D25, E23, D26, E24, C25, D24, C26 [2]	RDATU (31:0)	I/O	Databus of Upstream Connection RAM
R25, T26, U24, T25, M26, N24, M25, T24, R26, V25, V26, U25, V24, U26, U23	RADRU (14:0)	O	Addressbus of Upstream Connection RAM
P24	$\overline{\text{RADVU}}$	O	Address Advance Input
N23	$\overline{\text{ROEU}}$	O	Output Enable
N25	$\overline{\text{RGWU}}$	O	Global Write
P25	$\overline{\text{RCE0U}}$	O	Chip Enable RAM 0
R23	$\overline{\text{RCE1U}}$	O	Chip Enable RAM 1
P26	$\overline{\text{RCE2U}}$	O	Chip Enable RAM 2, not used in 2x2M mode
R24	$\overline{\text{RCE3U}}$	O	Chip Enable RAM 3 or Adr(15) in 2x2M mode
N26	$\overline{\text{RSCU}}$	O	Status Controller RAM

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Connection Data SSRAM Downstream (55 pins)			
T3, U1, U4, V2, U3, V1, W2, W1, V3, Y2, W4, Y1, W3, AA2, Y4, AA1, Y3, AB2, AB1, AC2, AB4, AC1, AB3, AD2, AC3, AD1, AF2, AE3, AF3, AE4, AD4, AF4 [2]	RDATD (31:0)	I/O	Databus of Downstream Connection RAM
N2, L3, M1, L1, K3, U2, R4, N1, M4, J1, K2, J3, K1, K4, L2	RADRD (14:0)	O	Address bus of Downstream Connection RAM
T1	$\overline{\text{RADVD}}$	O	Address Advance Input
T2	$\overline{\text{ROED}}$	O	Output Enable
R1	$\overline{\text{RGWD}}$	O	Global Write
P1	$\overline{\text{RCE0D}}$	O	Chip Enable RAM 0
N3	$\overline{\text{RCE1D}}$	O	Chip Enable RAM 1
R2	$\overline{\text{RCE2D}}$	O	Chip Enable RAM 2, not used in 2x2M mode
P3	$\overline{\text{RCE3D}}$	O	Chip Enable RAM 3 or Adr(15) in 2x2M mode
R3	$\overline{\text{RSCD}}$	O	Status Controller RAM

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Detector Interface (4 pins)			
W25	FPCT2D	O	Cell Filter 2 detector output downstream. In case of match a high pulse of 30 SYSCLK cycles is output. Minimum low period between 2 pulses is 2 SYSCLK cycles.
V23	FPCT1D	O	Cell Filter 1 detector output downstream. In case of match a high pulse of 30 SYSCLK cycles is output. Minimum low period between 2 pulses is 2 SYSCLK cycles.
W26	FPCT2U	O	Cell Filter 2 detector output upstream. In case of match a high pulse of 30 SYSCLK cycles is output. Minimum low period between 2 pulses is 2 SYSCLK cycles.
W24	FPCT1U	O	Cell Filter 1 detector output upstream. In case of match a high pulse of 30 SYSCLK cycles is output. Minimum low period between 2 pulses is 2 SYSCLK cycles.
Test/JTAG Boundary Scan (5 pins)			
AF24 [1]	TDI	I	Test data input; this pin has an internal pull-up resistor and need not to be connected for normal operation.
AC14 [1]	TCK	I	Test clock; this pin has an internal pull-up resistor and need not to be connected for normal operation.
AD25 [1]	TMS	I	Test mode select this pin has an internal pull-up resistor and need not to be connected for normal operation.
AD26 [1]	$\overline{\text{TRST}}$	I	TAP Controller Reset this pin has an internal pull-down resistor and need not to be connected for normal operation. If connected it must be driven to V_{SS} for normal operation.
AE26	TDO	O	Test data output; need not to be connected for normal operation.

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Additional Testpins (13 pins)			
AC25 [1]	$\overline{\text{OUTTRI}}$	I	For test only, do not connect
AC24 [1]	$\overline{\text{UTTRI}}$	I	For test only, do not connect
Y23 [2]	STEST	I	For test only, do not connect
AB25	AOPIIDD	I	Has to be connected to ground.
AA24	NDTRO	O	For test only, do not connect
AB23, AB24, AB26, AA25	TSTBUSI	I	Testbus in For test only, don't connect.
AA26, Y25, Y26, Y24	TSTBUSO	O	Testbus out For test only, don't connect.
Supply (48 pins)			
D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AA23, AC6, AC11, AC16, AC21			VDD, Chip 3.3 V supply
A1, A2, A26, B2, B25, B26, C3, C24, D4, D9, D14, D19, D23, H4, J23, N4, P23, V4, W23, AC4, AC8, AC13, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26			VSS, Chip ground
Unconnected Pins (17 pins)			
A14, B13, C13, C14, C15, M2, M3, P2, P4, AA3, AC20, AC22, AD20, AE10, AE22, AF14, AF21			not connected pins

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under biasPXB	T_A	-40 to 85	°C
Storage temperature	T_{stg}	-40 to 125	°C
IC supply voltage with respect to ground	V_{DD}	-0.3 to 3.6	V
Voltage on any pin with respect to ground	V_S	-0.4 to V_{DD} + 0.4	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2500	V

[1)] According to MIL-Std 883D, method 3015.7 and ESD Association Standard EOS/ESD-5.1-1993. The RF Pins 20, 21, 26, 29, 32, 33, 34 and 35 are not protected against voltage stress > 300 V (versus V_S or GND). The high frequency performance prohibits the use of adequate protective structures.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Operating Range

Table 9 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature under bias	T_A	-40	85	°C	
Junction temperature	T_J		125	°C	
Supply voltage	V_{DD}	3.15	3.45	V	
Ground	V_{SS}	0	0	V	
Power dissipation	P		1.9	W	

Note: In the operating range, the functions given in the circuit description are fulfilled.

Note: The nominal supply voltage (V_{DD}) should not exceed 3.45V to keep the device within the specified current and power dissipation ranges.

6.3 DC Characteristics

Table 10 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max		
General Interface Levels (does not apply to Boundary Scan Interface):						
Input low voltage	V_{IL}	–0.4		0.8	V	
Input high voltage	V_{IH}	2.0 2.1 for pin $\overline{TRST}$		V_{DD} + 0.3	V	LVTTL (3.3V)
Output low voltage	V_{OL}		0.2	0.4	V	I_{OL} = 4 mA (I_{OL} = 6 mA for TXCLAV/ RXCLAV signals)
Output high voltage(s)	V_{OH}	2.4		V_{DD}	V	I_{OH} = – 4 mA (I_{OH} = –6 mA for TXCLAV/ RXCLAV signals)
Average power supply current	I_{CC} (AV)		395	550	mA	V_{DD} = 3.45 V, SYSCLK = 52MHz; UTPHYCLK = 52MHz; UTATMCLK = 52MHz;
Average power up supply current (N SYSCLK cycles after reset)	I_{CCPU} (AV)			550	mA	V_{DD} = 3.45 V, SYSCLK = 52MHz; UTPHYCLK = 52MHz; UTATMCLK = 52MHz;
Average power dissipation	P (AV)		1.3	1.9	W	V_{DD} = 3.45 V, SYSCLK = 52MHz; UTPHYCLK = 52MHz; UTATMCLK = 52MHz;

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max		
Input current	I_{IIN}	-1		1	mA	$V_{IN} = V_{DD}$ or V_{SS}
		50		150	mA	$V_{IN} = V_{DD}$ for Inputs with internal Pull-Down resistor
		-50		-200	mA	$V_{IN} = V_{SS}$ for Inputs with internal Pull-Up resistor
Output leakage current	I_{OZ}	-1		1	mA	V_{DD} = 3.3 V, GND = 0 V, $V_{IN} = V_{DD}$ orV_{SS}, V_{OUT} in TriState

6.4 AC Characteristics

T_A = -40 to 85 ×C, V_{CC} = 3.15 V .. 3.45 V, V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical 1
and to V_{IL} = 0.4 V for a logical 0

All outputs are measured at V_H = 2.0 V for a logical 1
and at V_L = 0.8 V for a logical 0

The AC testing input/output waveforms are shown below.

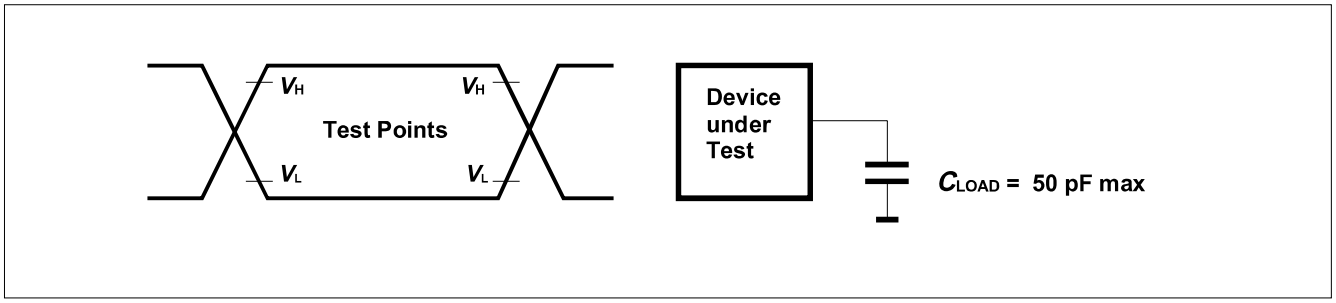


Figure 43 Input/Output Waveform for AC Measurements

Table 11 Clock Frequencies

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Core clock	SYSCLK	25	52	MHz
UTOPIA clock at PHY-side	UTPHYCLK	$f_{SYSCLK/2}$	f_{SYSCLK}	MHz
UTOPIA clock at ATM-side	UTATMCLK	$f_{SYSCLK/2}$	f_{SYSCLK}	MHz
µP clock[1)]		25	f_{SYSCLK}	MHz

[1)] Supplied only to external microprocessor;

6.4.1 Microprocessor Interface Timing

6.4.1.1 Microprocessor Write Cycle Timing

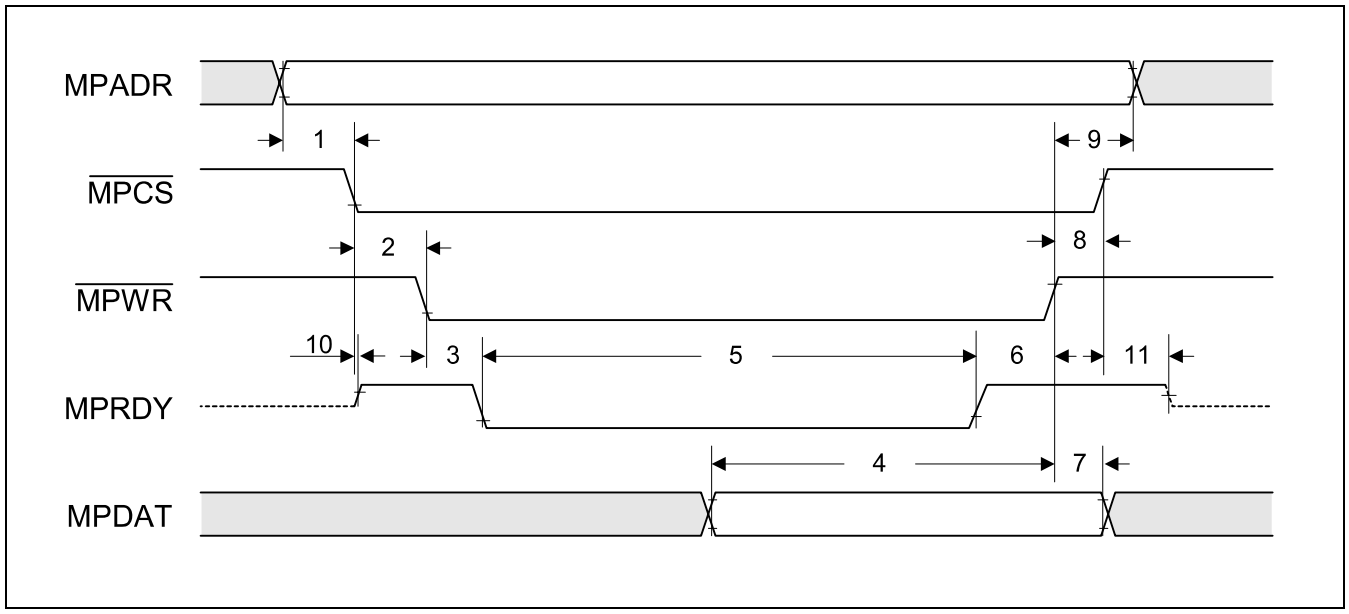


Figure 44 Microprocessor Interface Write Cycle Timing

Table 12 Microprocessor Interface Write Cycle Timing

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	MPADR setup time before MPCS low	0			ns
2	$\overline{\text{MPCS}}$ setup time before $\overline{\text{MPWR}}$ low	0			ns
3	MPRDY low delay after $\overline{\text{MPWR}}$ low	1		15	ns
4	MPDAT setup time before $\overline{\text{MPWR}}$ high	5			ns
5	Pulse width MPRDY low	3 SYSCLK cycles		4 SYSCLK cycles	
6	MPRDY high to $\overline{\text{MPWR}}$ high	5			ns
7	MPDAT hold time after $\overline{\text{MPWR}}$ high	5			ns
8	$\overline{\text{MPCS}}$ hold time after $\overline{\text{MPWR}}$ high	5			ns
9	MPADR hold time after $\overline{\text{MPWR}}$ high	5			ns
10	$\overline{\text{MPCS}}$ low to MPRDY low impedance	1		10	ns
11	$\overline{\text{MPCS}}$ high to MPRDY high impedance			15	ns

6.4.1.2 Microprocessor Read Cycle Timing

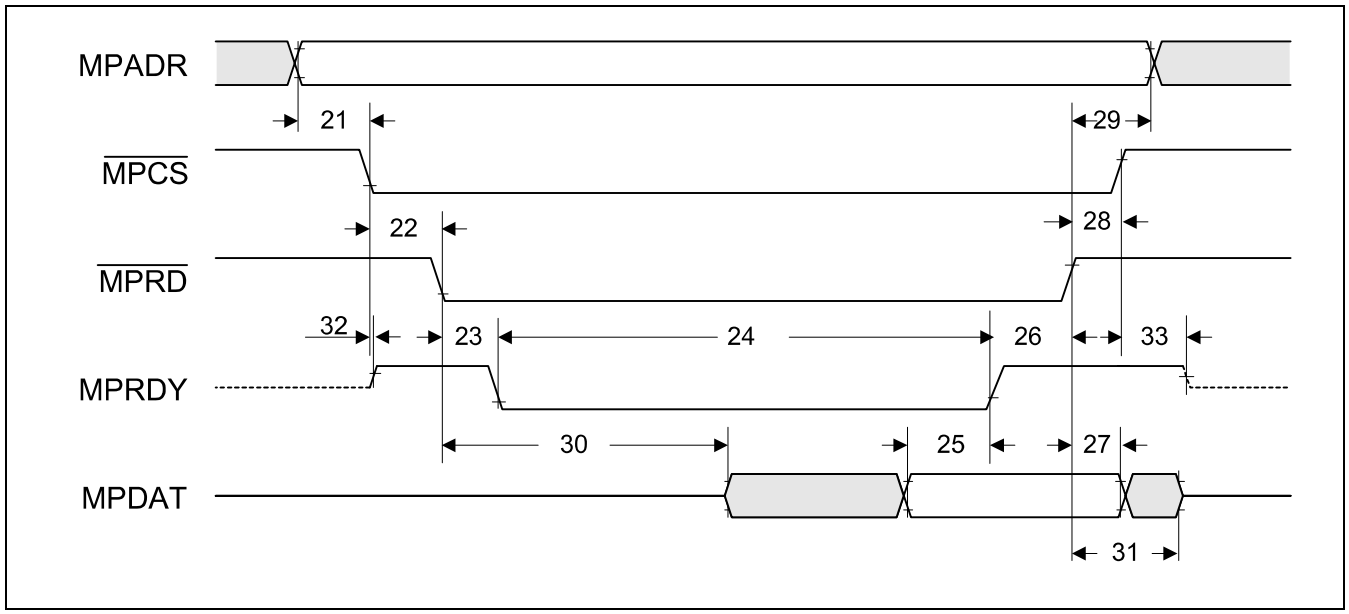


Figure 45 Microprocessor Interface Read Cycle Timing

Table 13 Microprocessor Interface Read Cycle Timing

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
21	MPADR setup time before $\overline{\text{MPCS}}$ low	0			ns
22	$\overline{\text{MPCS}}$ setup time before $\overline{\text{MPRD}}$ low	0			ns
23	MPRDY low delay after $\overline{\text{MPRD}}$ low	1		15	ns
24	Pulse width MPRDY low	4 SYSCLK cycles		5 SYSCLK cycles	
24	Pulse width MPRDY low (MPADR = $9D_H$)	6 SYSCLK cycles		7 SYSCLK cycles	
24	Pulse width MPRDY low (MPADR = $B6_H$)	7 SYSCLK cycles		8 SYSCLK cycles	
25	MPDAT valid before MPRDY high	5			ns
26	MPRDY high to $\overline{\text{MPRD}}$ high	5			ns
27	MPDAT hold time after $\overline{\text{MPRD}}$ high	2			ns
28	$\overline{\text{MPCS}}$ hold time after $\overline{\text{MPRD}}$ high	5			ns
29	MPADR hold time after $\overline{\text{MPRD}}$ high	5			ns
30	$\overline{\text{MPRD}}$ low to MPDAT low impedance	1		15	ns
31	$\overline{\text{MPRD}}$ high to MPDAT high impedance	2		15	ns

Table 13 Microprocessor Interface Read Cycle Timing

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
32	$\overline{\text{MPCS}}$ low to MPRDY low impedance	1		10	ns
33	$\overline{\text{MPCS}}$ high to MPRDY high impedance			15	ns

6.4.1.3 DMA Request Timing

For DMA operation the $\overline{\text{MPDREQ}}$ signal is necessary. It indicates that at least one more word is available within the AOP DMA buffer. When the microprocessor reads the last word in the buffer (DMAR register) it must be ensured that the $\overline{\text{MPDREQ}}$ signal is updated early enough to prohibit another read to the DMAR register.

With asynchronous sampling of the microprocessor $\overline{\text{MPDREQ}}$ input, $\overline{\text{MPDREQ}}$ has to be updated at least 1 CLKOUT cycle before the MPRDY gets active (386EX User manual, "12.2.5 Ending DMA Transfers", page 12-11). In AOP $\overline{\text{MPDREQ}}$ update is done 5 SYSCLK cycles (= 96ns at 51.84 Mhz) before MPRDY. With 25 Mhz microprocessor clock (CLK2) the CLKOUT period (twice the CLK2 period) of 80 ns is satisfied. Less than 25 Mhz microprocessor clock frequency may cause problems.

If $\overline{\text{MPDREQ}}$ gets inactive the AOP waits for $\overline{\text{MPDACK}}$ = 'high', afterwards additional 20 SYSCLK cycles (about 400ns) are spent until $\overline{\text{MPDREQ}}$ will become active again. This minimum gap was introduced to ensure co-operation with the 80386EX internal DMA controller.

For distinction of 2 successive read cycles the read signal must be '1' for at least 1 SYSCLK cycle, the chip select signal may remain active.

This 'command inactive time' is necessary for all adjacent microprocessor read and write accesses.

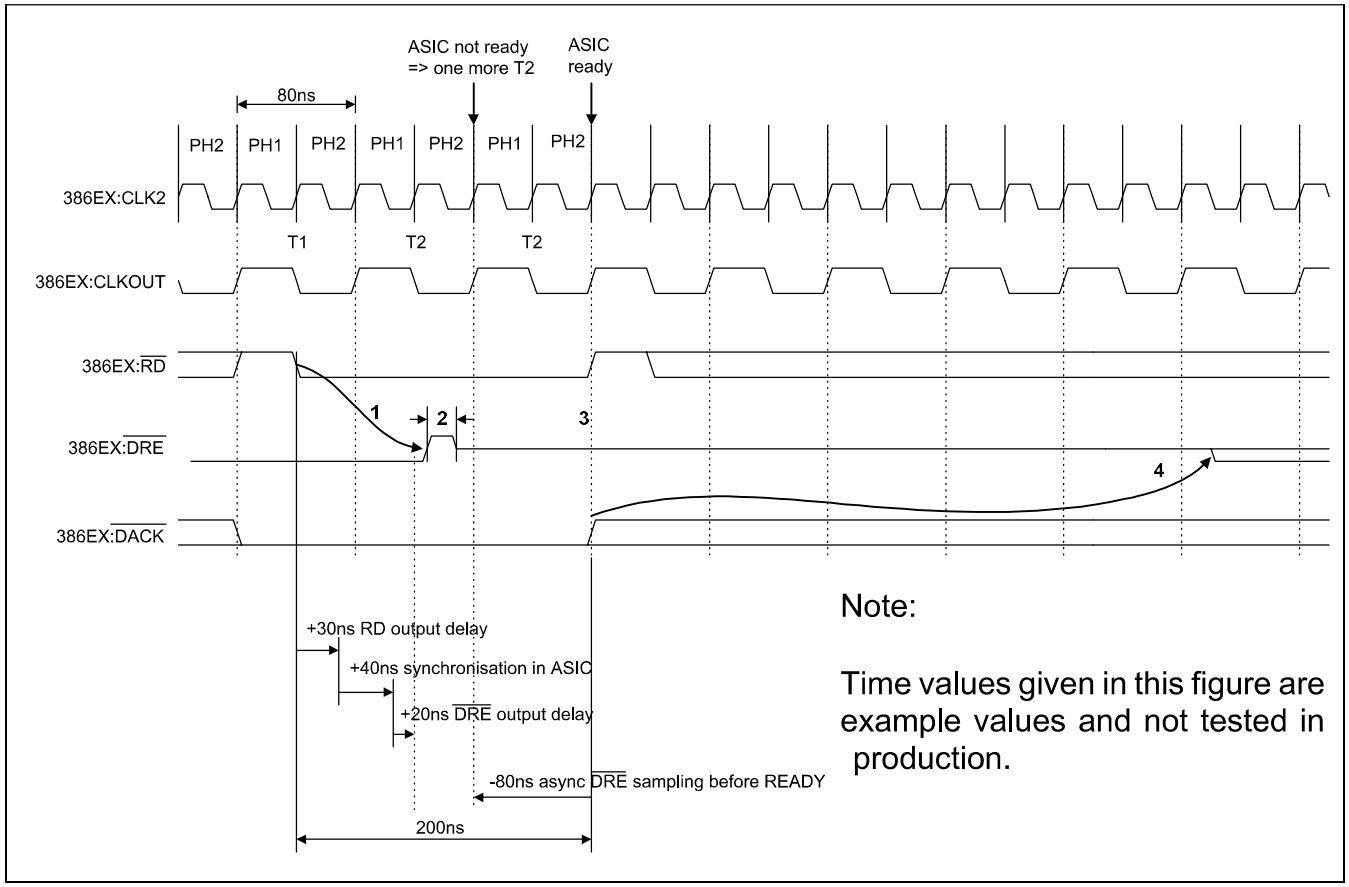


Figure 46 Microprocessor DMA Interface

Table 14 Microprocessor DMA interface

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
40	Rising edge of MPDREQ after MPRD low	1		3	SYSCLK cycles
41	MPDREQ driven high before high impedance	1		1	SYSCLK cycles
42	Interval between MPDREQ active phases (in case of successive accesses)	20			SYSCLK cycles
43	Interval between MPDACK inactive and subsequent MPDREQ active	20			SYSCLK cycles
44	MPDREQ inactive before MPRDY active (in case the DMA FIFO gets empty during the current read access)	5		5	SYSCLK cycles

6.4.2 UTOPIA Interface

The AC characteristics of the UTOPIA Interface fulfill the standard of [1] and [2]. Setup and hold times of the 50 MHz UTOPIA Specification are valid.

According to the UTOPIA Specification, the AC characteristics are based on the timing specification for the receiver side of a signal. The setup and the hold times are defined with regards to a positive clock edge, see **Figure 47**.

Taking into account the actual clock frequency (up to the maximum frequency), the corresponding (min. and max.) transmit side "clock to output" propagation delay specifications can be derived. The timing references (tT5 to tT12) are according to the data found in **Table 15** to **Table 18**.

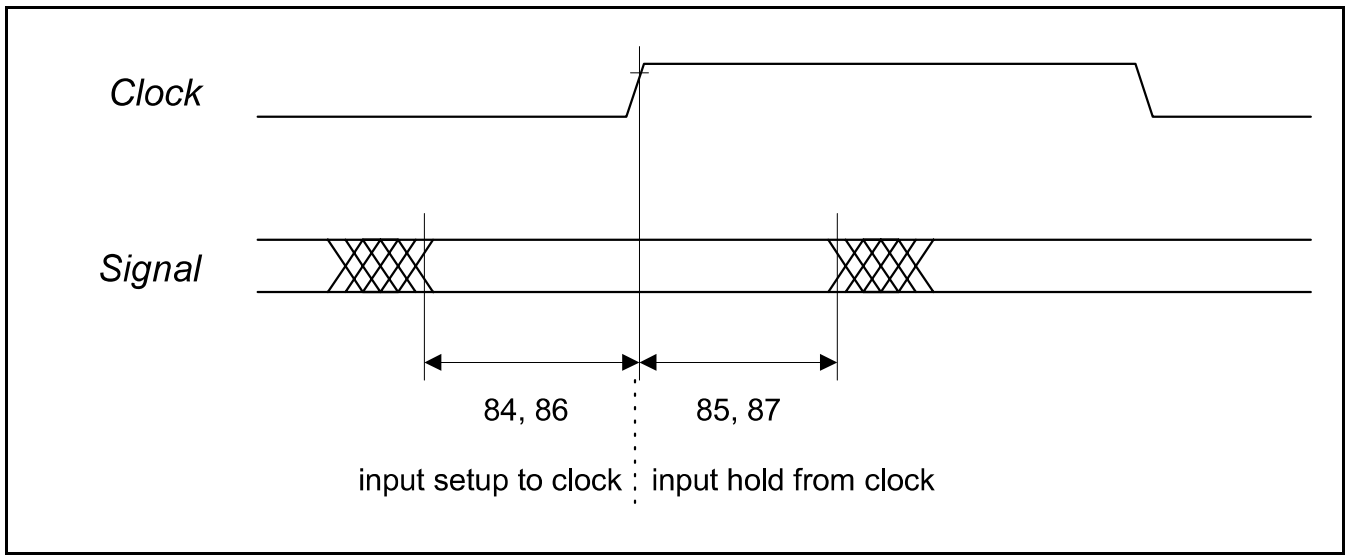


Figure 47 Setup and Hold Time Definition (Single- and Multi-PHY)

Figure 48 shows the tristate timing for the multi-PHY application (multiple PHY devices, multiple output signals are multiplexed together).

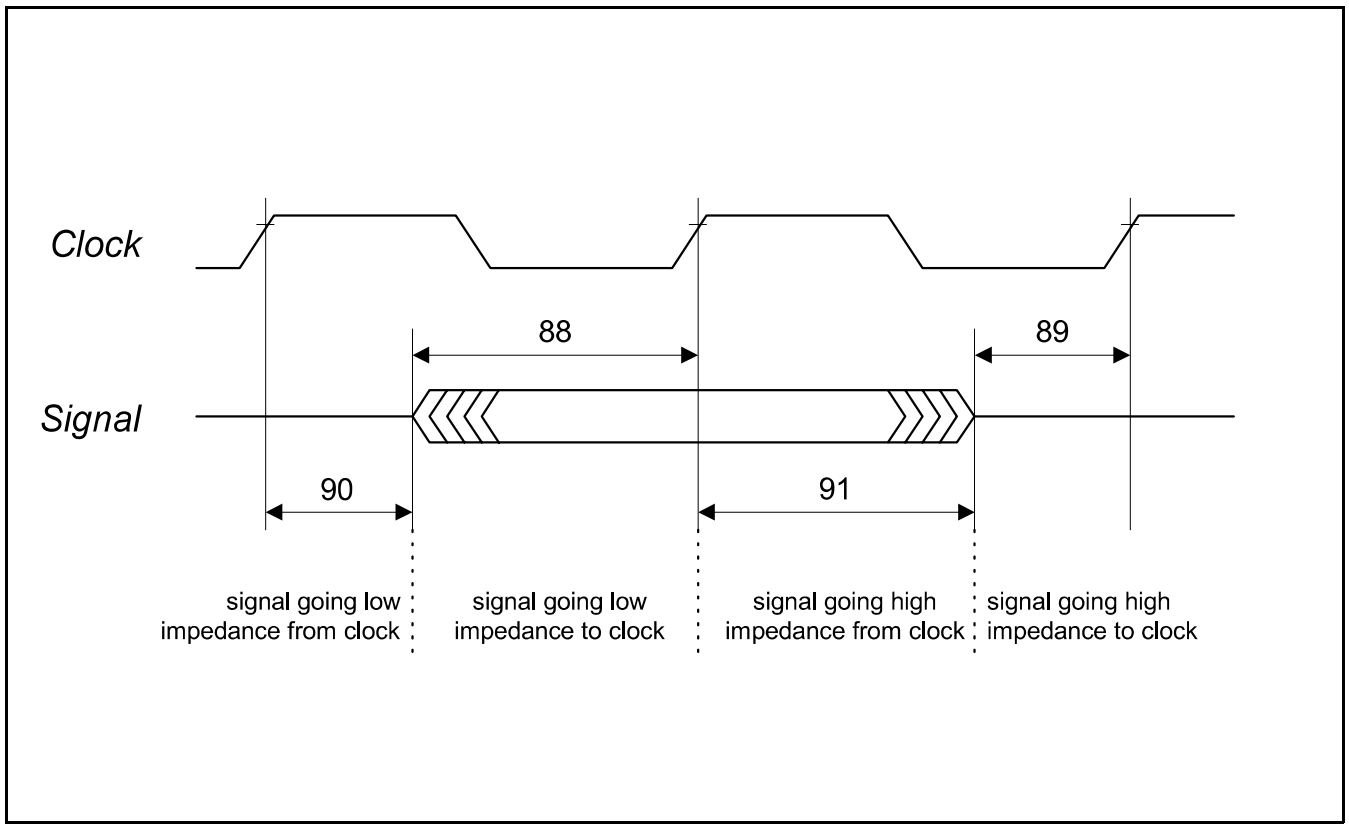


Figure 48 Tristate Timing (Multi-PHY, Multiple Devices Only)

Interface and signal naming conventions:

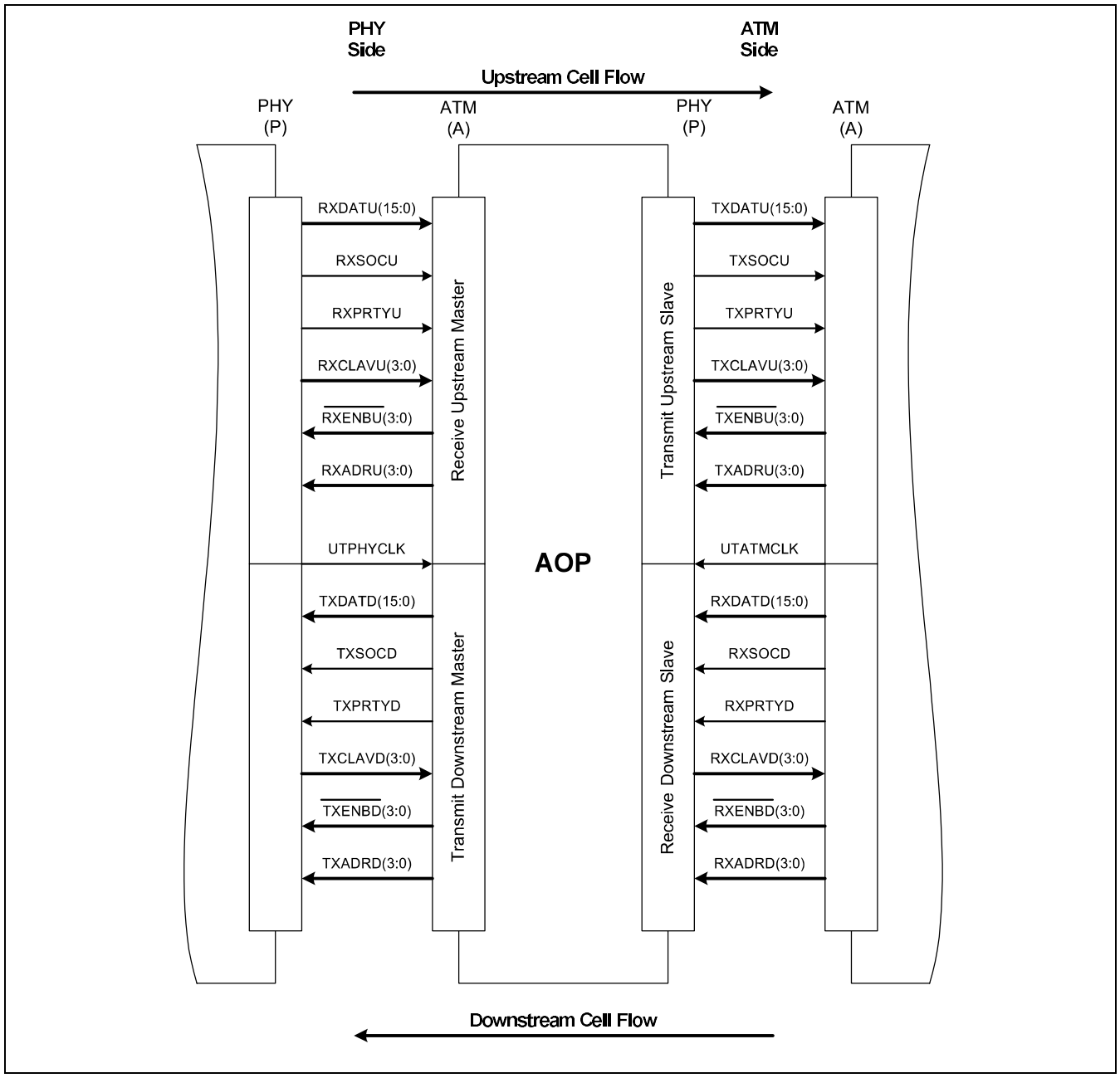


Figure 49 Interface Naming Conventions

In the following tables, A⇒P (column DIR, Direction) defines a signal from the ATM Layer (transmitter, driver) to the PHY Layer (receiver), A⇐P defines a signal from the PHY Layer (transmitter, driver) to the ATM Layer (receiver).

All timings also apply to UTOPIA Level 1 8-bit data bus operation.

The direction notification in the following tables apply to the UTOPIA master interface (AOP to PHY)

Table 15 Transmit Timing Upstream (16-Bit Data Bus, 50 MHz at Cell Interface, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTATMCLK		ATM Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			ATM Clk duty cycle	40	60	%
82			ATM Clk peak-to-peak jitter	-	5	%
83			ATM Clk rise/fall time	-	2	ns
84	TXDATU [15:0], TXSOCU	A<P	Input setup to ATM Clk	4	-	ns
85	TXPRTYU, TXCLAVU[0]		Input hold from ATM Clk	1	-	ns
86	$\overline{\text{TXENBU}}$[0]	A>P	Input setup to ATM Clk	4	-	ns
87			Input hold from ATM Clk	1	-	ns

Table 16 Receive Timing Upstream (16-Bit Data Bus, 50 MHz at Cell Interface, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTPHYCLK		PHY Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			PHY Clk duty cycle	40	60	%
82			PHY Clk peak-to-peak jitter	-	5	%
83			PHY Clk rise/fall time	-	2	ns
84	RXDATU [15:0], RXPRTYU	A<P	Input setup to PHY Clk	5	-	ns
85			Input hold from PHY Clk	1	-	ns
86	RXSOCU, RXCLAVU[0]	A<P	Input setup to PHY Clk	4	-	ns
87			Input hold from PHY Clk	1	-	ns
86	$\overline{\text{RXENBU}}$[0]	A>P	Input setup to PHY Clk	4	-	ns
87			Input hold from PHY Clk	1	-	ns

Table 17 Transmit Timing Downstream (16-Bit Data Bus, 50 MHz at Cell Interface, Singel PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTPHYCLK		PHY Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			PHY Clk duty cycle	40	60	%
82			PHY Clk peak-to-peak jitter	-	5	%
83			PHY Clk rise/fall time	-	2	ns
84	TXDATD [15:0], TXSOCD,	A>P	Input setup to PHY Clk	4	-	ns
85	TXPRTYD, TXENBD[0]		Input hold from PHY Clk	1	-	ns
86	TXCLAVD[0]	A<P	Input setup to PHY Clk	4	-	ns
87			Input hold from PHY Clk	1	-	ns

Table 18 Receive Timing Downstream (16-Bit Data Bus, 50 MHz at Cell Interface, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTATMCLK		ATM Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			ATM Clk duty cycle	40	60	%
82			ATM Clk peak-to-peak jitter	-	5	%
83			ATM Clk rise/fall time	-	2	ns
84	RXDATD [15:0], RXPRTYD	A>P	Input setup to ATM Clk	5	-	ns
85			Input hold from ATM Clk	1	-	ns
86	RXSOCD, RXENBD[0]	A>P	Input setup to ATM Clk	4	-	ns
87			Input hold from ATM Clk	1	-	ns
88	RXCLAVD[0]	A<P	Input setup from ATM Clk	4	-	ns
89			Input hold from ATM Clk	1	-	ns

Table 19 Transmit Timing Upstream (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTATMCLK		ATM Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			ATM Clk duty cycle	40	60	%
82			ATM Clk peak-to-peak jitter	-	5	%
83			ATM Clk rise/fall time	-	2	ns
84	TXDATU [15:0],	A<P	Input setup to ATM Clk	4	-	ns
85	TXSOCU, TXPRTYU		Input hold from ATM Clk	1	-	ns
86	$\overline{\text{TXENBU}}$ [3:0],	A>P	Input setup to ATM Clk	4	-	ns
87	TXADRU [3:0]		Input hold from ATM Clk	1	-	ns
86	TXCLAVU [3:0]	A<P	Input setup to ATM Clk	4	-	ns
87			Input hold from ATM Clk	1	-	ns
88			Signal going low impedance to ATM Clk	4	-	ns
89			Signal going high impedance to ATM Clk	0	-	ns
90			Signal going low impedance from ATM Clk	1	-	ns
91			Signal going high impedance from ATM Clk	1	-	ns

Table 20 Receive Timing Upstream (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTPHYCLK		PHY Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			PHY Clk duty cycle	40	60	%
82			PHY Clk peak-to-peak jitter	-	5	%
83			PHY Clk rise/fall time	-	2	ns
84	$\overline{\text{RXENBU}}$ [3:0],	A>P	Input setup to PHY Clk	4	-	ns
85	RXADRU [3:0]		Input hold from PHY Clk	1	-	ns
86	RXDATU [15:0], RXPRTYU	A<P	Input setup to PHY Clk	5	-	ns
87			Input hold from PHY Clk	1	-	ns
88			Signal going low impedance to PHY Clk	5	-	ns
89			Signal going high impedance to PHY Clk	0	-	ns
90			Signal going low impedance from PHY Clk	1	-	ns
91			Signal going high impedance from PHY Clk	1	-	ns
86	RXSOCU, RXCLAV [3:0]	A<P	Input setup to PHY Clk	4	-	ns
87			Input hold from PHY Clk	1	-	ns
88			Signal going low impedance to PHY Clk	4	-	ns
89			Signal going high impedance to PHY Clk	0	-	ns
90			Signal going low impedance from PHY Clk	1	-	ns
91			Signal going high impedance from PHY Clk	1	-	ns

Table 21 Transmit Timing Downstream (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTPHYCLK		PHY Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			PHY Clk duty cycle	40	60	%
82			PHY Clk peak-to-peak jitter	-	5	%
83			PHY Clk rise/fall time	-	2	ns
84	TXDATD [15:0], TXSOCD,	A>P	Input setup to PHY Clk	4	-	ns
85	$\overline{\text{TXPRTYD}}$, $\overline{\text{TXENBD}}$ [3:0], TXADRD [3:0]		Input hold from PHY Clk	1	-	ns
86	TXCLAVD [3:0]	A<P	Input setup to PHY Clk	4	-	ns
87			Input hold from PHY Clk	1	-	ns
88			Singnal going low impedance to PHY Clk	4	-	ns
89			Singnal going high impedance to PHY Clk	0	-	ns
90			Singnal going low impedance from PHY Clk	1	-	ns
91			Singnal going high impedance from PHY Clk	1	-	ns

Table 22 Receive Timing Downstream (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTATMCLK		ATM Clk frequency (nominal)	$f_{SYSCLK}/2$	52	MHz
81			ATM Clk duty cycle	40	60	%
82			ATM Clk peak-to-peak jitter	-	5	%
83			ATM Clk rise/fall time	-	2	ns
84	$\overline{\text{RXENBD}}$ [3:0]	A>P	Input setup to ATM Clk	4	-	ns
85	RXADRD [3:0]		Input hold from ATM Clk	1	-	ns
86	RXDATD [15:0], RXPRTYD	A<P	Input setup to ATM Clk	5	-	ns
87			Input hold from ATM Clk	1	-	ns
88			Singnal going low impedance to ATM Clk	5	-	ns
89			Singnal going high impedance to ATM Clk	0	-	ns
90			Singnal going low impedance from ATM Clk	1	-	ns
91			Singnal going high impedance from ATM Clk	1	-	ns
86	RXSOCD, RXCLAVD [3:0]	A<P	Input setup from ATM Clk	4	-	ns
87			Input hold from ATM Clk	1	-	ns
88			Singnal going low impedance to ATM Clk	4	-	ns
89			Singnal going high impedance to ATM Clk	0	-	ns
90			Singnal going low impedance from ATM Clk	1	-	ns
91			Singnal going high impedance from ATM Clk	1	-	ns

6.4.3 SSRAM Interface

Timing of the Synchronous Static RAM Interfaces is simplified as all signals are referenced to the rising edge of SYSCLK. In **Figure 50**, it can be seen that all signals output by the PXB 4340 E AOP have identical delay times with reference to the clock. When reading from the RAM, the PXB 4340 E AOP samples the data within a window at the rising clock edge.

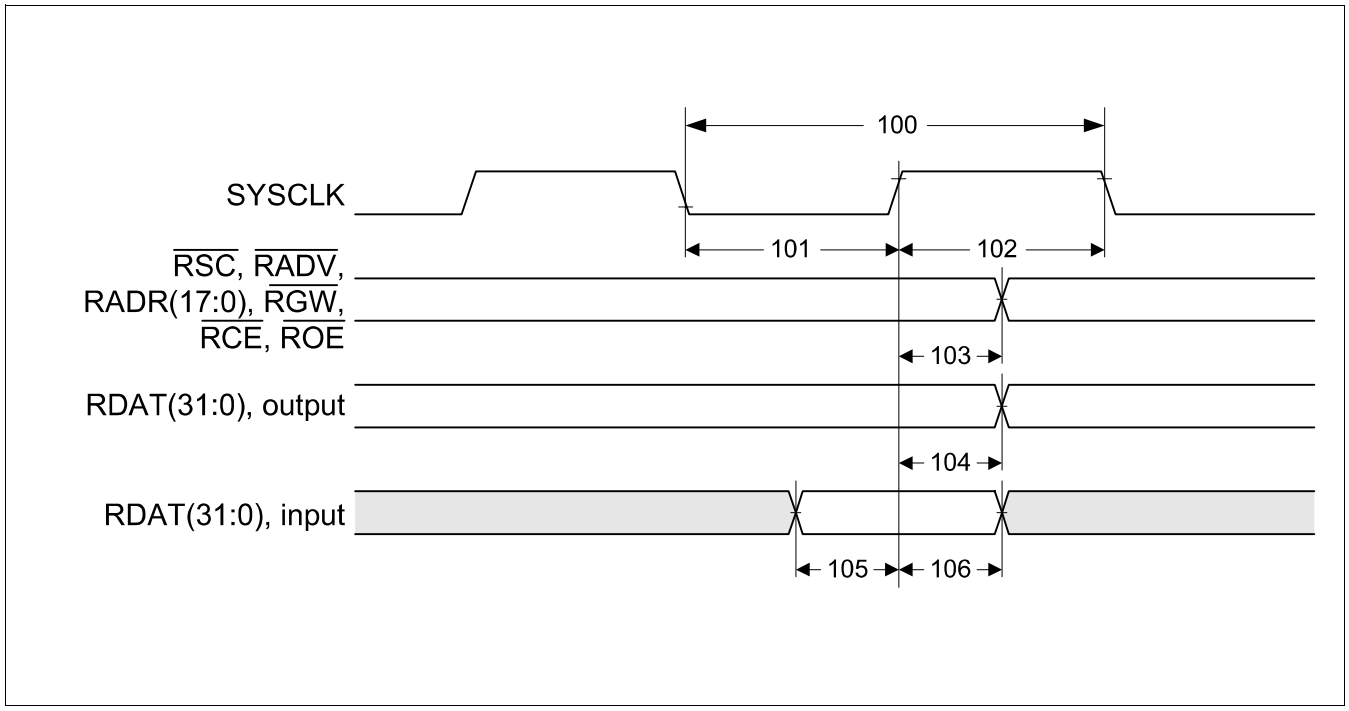


Figure 50 SSRAM Interface Generic Timing Diagram

Table 23 SSRAM Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
100	T_{SYSCLK} : Period SYSCLK	19.2			ns
100A	F_{SYSCLK} : Frequency SYSCLK			52	MHz
101	SYSCLK Low Pulse Width	7			ns
102	SYSCLK High Pulse Width	7			ns
103	Delay SYSCLK rising to $\overline{RSC}$, $\overline{RADV}$, RADR(17:0), $\overline{RGW}$, $\overline{RCE}$, $\overline{ROE}$	2		15	ns
104	Delay SYSCLK rising to RDAT Output	2		15	ns
105	Setup time RDAT Input before SYSCLK rising (read cycles)	6			ns
106	Hold time RDAT Input after SYSCLK rising (read cycles)	1.5			ns

6.4.4 Cell Filter Detector Timing

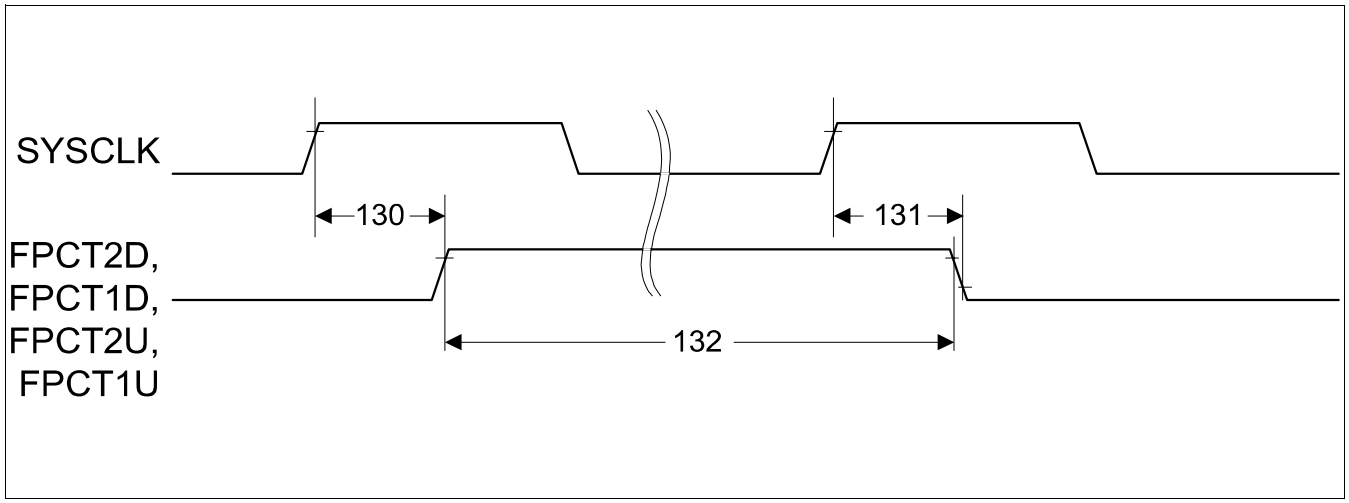


Figure 51 Cell Filter Detector Timing

Table 24 Cell Filter Detecor Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
130	Delay SYSCLK high to FPCT active	4	15	ns
131	Delay SYSCLK high to FPCT inactive	4	15	ns
132	FPCT high time in number of SYSCLK cycles	30		SYSCLK cycles

6.4.5 Reset Timing

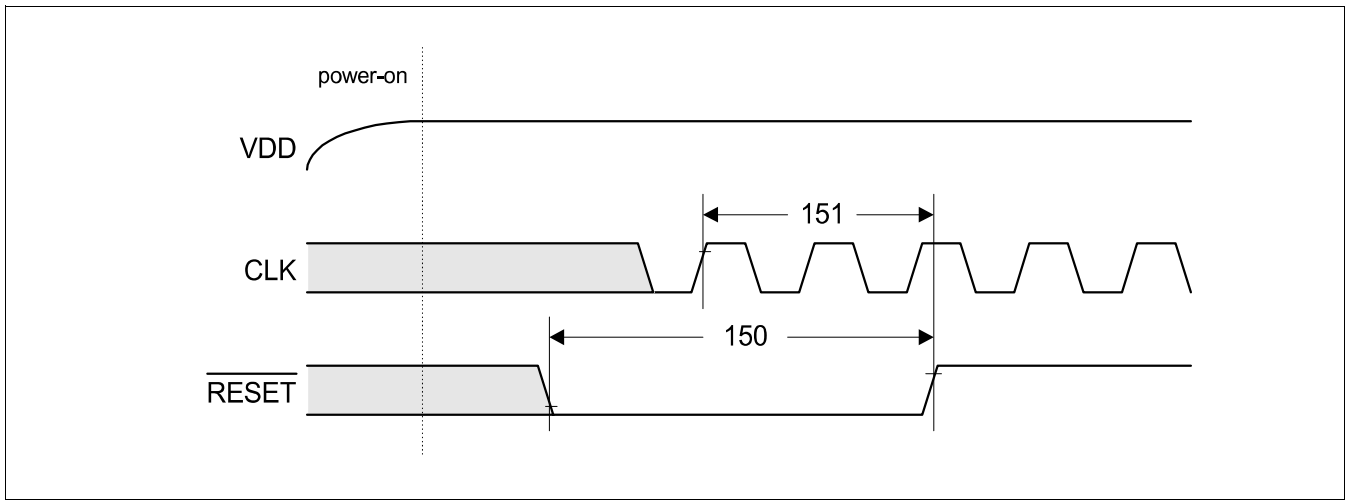


Figure 52 Reset Timing

Table 25 Reset Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
150	RESET pulse width	120		ns
151	Number of SYSCLK cycles during $\overline{\text{RESET}}$ active	3		SYSCLK cycles

Note: $\overline{\text{RESET}}$ may be asynchronous to CLK when asserted or deasserted. $\overline{\text{RESET}}$ may be asserted during power-up or asserted after power-up. Nevertheless, deassertion must be at a clean, bounce-free edge.

6.4.6 Boundary-Scan Test Interface

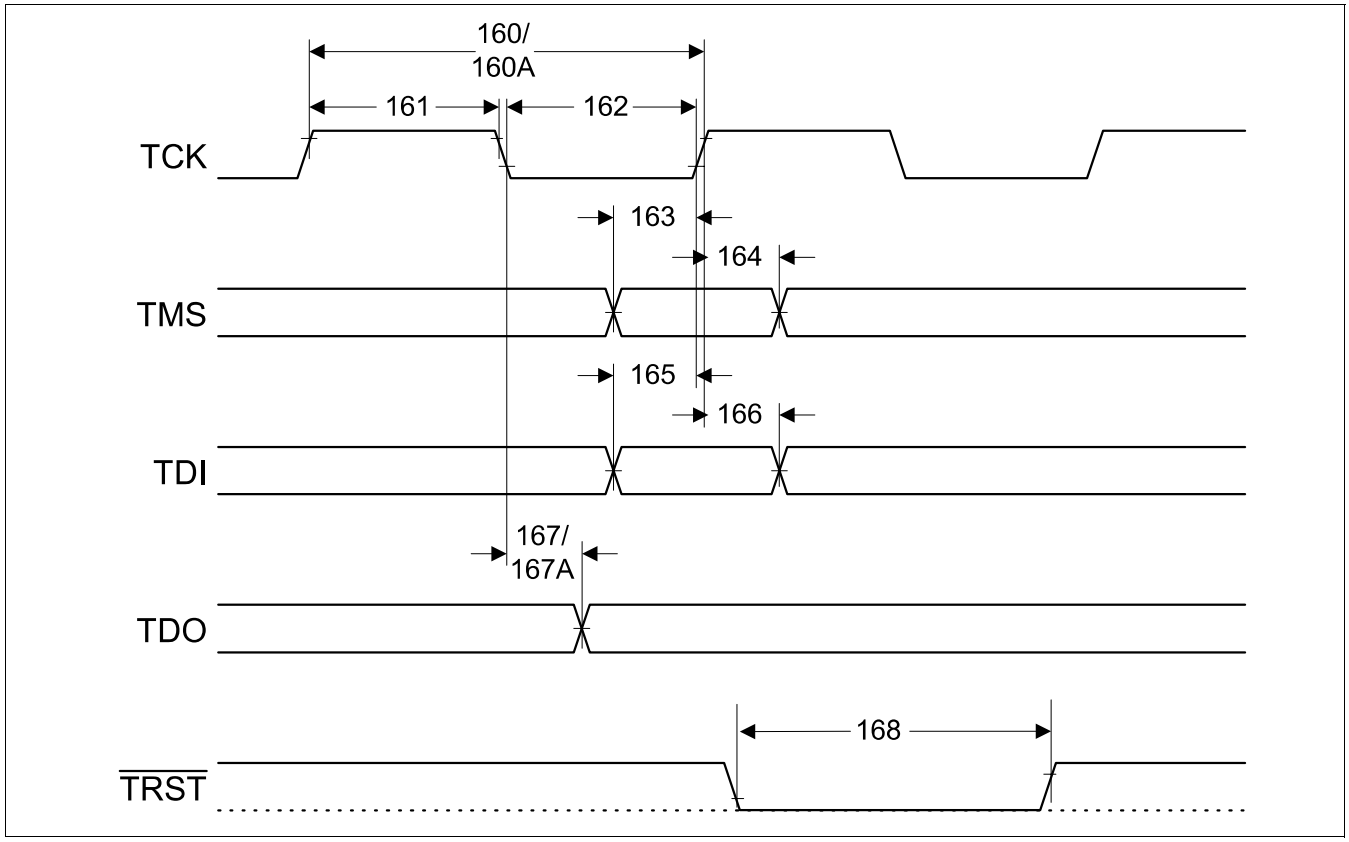


Figure 53 Boundary-Scan Test Interface Timing Diagram

Table 26 Boundary-Scan Test Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
160	T_{TCK} : Period TCK	100			ns
160A	F_{TCK} : Frequency TCK			10	MHz
161	TCK high time	40			ns
162	TCK low time	40			ns
163	Setup time TMS before TCK rising	10			ns
164	Hold time TMS after TCK rising	10			ns
165	Setup time TDI before TCK rising	10			ns
166	Hold time TDI after TCK rising	10			ns
167	Delay TCK falling to TDO valid			30	ns
167A	Delay TCK falling to TDO high impedance			30	ns
168	Pulse width $\overline{\text{TRST}}$ low	200			ns

6.5 Capacitances

Table 27 Capacitances

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input Capacitance	C_{IN}	3	4	pF
Output Capacitance	C_{OUT}	2.5	4	pF
Load Capacitance at: UTOPIA Outputs MPDAT(15:0), MPRDY other outputs	 C_{FO1} C_{FO2} C_{FO3}		 40 50 20	 pF pF pF

6.6 Package Characteristics

Table 28 Thermal Package Characteristics

Parameter		Symbol	Value	Unit
Thermal Package Resistance Junction to Ambient				
Airflow	*Ambient Temperature*			
No airflow	$T_{A=25°C}$	$R_{JA(0,25)}$	17.9	°C/W
Airflow 200 lfpm = 1m/s	$T_{A=25°C}$	$R_{JA(0,25)}$	15.7	°C/W
Airflow 400 lfpm = 2m/s	$T_{A=25°C}$	$R_{JA(0,25)}$	13.2	°C/W
Airflow 600 lfpm = 3m/s	$T_{A=25°C}$	$R_{JA(0,25)}$	12.5	°C/W

7 Package Outlines

P-BGA-352-2
(Plastic Ball Grid Array)

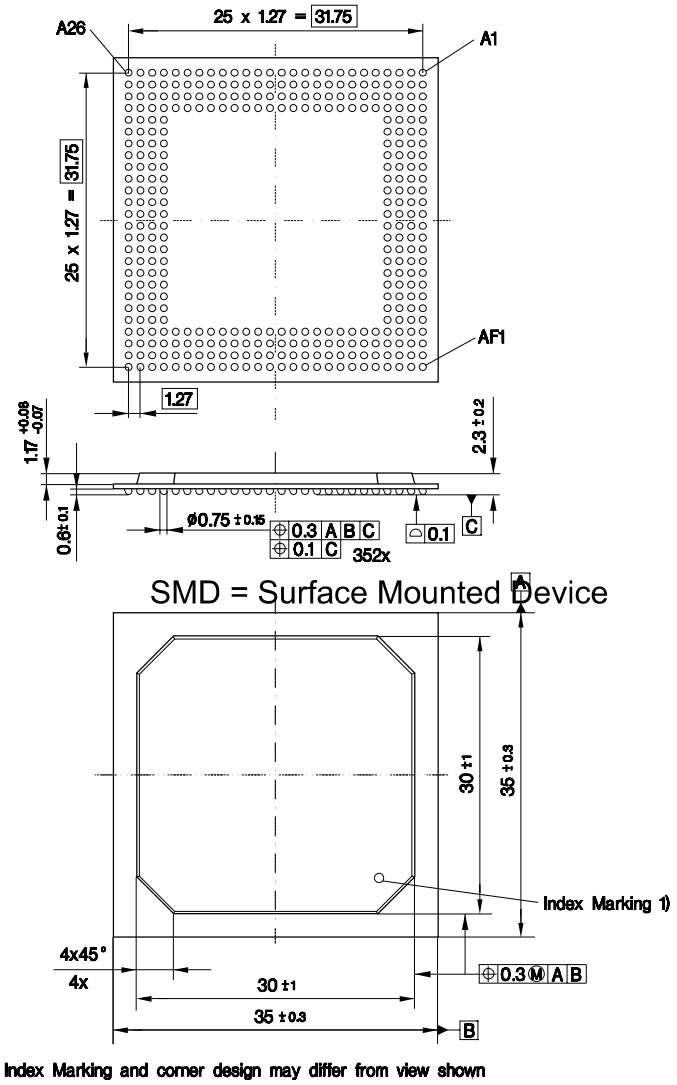


Figure 54 Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

SMD = Surface Mounted Device

Table 29 Thermal Resistance

Parameter	Symbol	Limit Values	Unit
Junction to case	R_{thJC}	3.0	K/W
Junction to ambient air without air flow	R_{thJA}	16.9	K/W
Junction to ambient air with air flow 1.0 m/s	R_{thJA}	14.7	K/W
Junction to ambient air with air flow 2.0 m/s	R_{thJA}	13.7	K/W
Junction to ambient air with air flow 3.0 m/s	R_{thJA}	12.8	K/W

8 Overview Lists

8.1 Layer Point Configurations

The following layer points are defined for both F4 and F5 OAM flows:

- OEP = Originating End Point (end-to-end OAM cell flow)
- TEP = Terminating End Point (end-to-end cell flow)
- OSP = Originating Segment Point (segment cell flow)
- TSP = Terminating Segment Point (segment cell flow)
- IP = Intermediate Point (no origination or termination of OAM flows).

The following table gives an overview over all layer points that can be configured in up- and downstream direction of the AOP:

Table 30 Layer Point Configuration

Layerpoint		Defined for Direction		External RAM Setup					(SCAN internal flags)			Linked layerpt.
F4	F5	Up	Dn	VCON	DIS F4	PIP/ OSP/ TSP	DIS F5	CIP/ OSP/ TSP	F4 Eval	F5 Eval	Flow#	Flow# in opposite direction
(conn disabled)		√	√	0	x	xxx	x	xxx	0	0	0	0
IP	invisible	√	√	1	0	100	x	xxx	1	0	1	1
OSP	invisible	√	√	1	0	110	x	xxx	1	0	2	3
TSP	invisible	√	√	1	0	101	x	xxx	1	0	3	2
OSP+TSP	invisible	√	√	1	0	111	x	xxx	1	0	4	4
-	IP	√	√	1	1	xxx	0	100	0	1	5	5
-	OSP	√	√	1	1	xxx	0	110	0	1	6	7
-	TSP	√	√	1	1	xxx	0	101	0	1	7	6
-	OSP+TSP	√	√	1	1	xxx	0	111	0	1	8	8
TEP	-	√		1	0	0x0	1	xxx	1	0	9	21
TEP	IP	√		1	0	0x0	0	100	1	1	10	22
TEP	OSP	√		1	0	0x0	0	110	1	1	11	24
TEP	TSP	√		1	0	0x0	0	101	1	1	12	23
TEP	OSP+TSP	√		1	0	0x0	0	111	1	1	13	25
TEP+TSP	-	√		1	0	0x1	1	xxx	1	0	14	26
TEP+TSP	IP	√		1	0	0x1	0	100	1	1	15	27
TEP+TSP	OSP	√		1	0	0x1	0	110	1	1	16	29
TEP+TSP	TSP	√		1	0	0x1	0	101	1	1	17	28
TEP+TSP	OSP+TSP	√		1	0	0x1	0	111	1	1	18	30
-	OEP	√		1	1	xxx	0	00x	0	1	19	31
-	OEP+OSP	√		1	1	xxx	0	01x	0	1	20	32
OEP	-		√	1	0	00x	1	xxx	1	0	21	9
OEP	IP		√	1	0	00x	0	100	1	1	22	10
OEP	OSP		√	1	0	00x	0	110	1	1	23	12
OEP	TSP		√	1	0	00x	0	101	1	1	24	11
OEP	OSP+TSP		√	1	0	00x	0	111	1	1	25	13

Table 30 Layer Point Configuration

Layerpoint		Defined for Direction		External RAM Setup					(SCAN internal flags)			Linked layerpt.
F4	F5	Up	Dn	VCON	DIS F4	PIP/ OSP/ TSP	DIS F5	CIP/ OSP/ TSP	F4 Eval	F5 Eval	Flow#	Flow# in opposite direction
OEP+OSP	-		√	1	0	01x	1	xxx	1	0	26	14
OEP+OSP	IP		√	1	0	01x	0	100	1	1	27	15
OEP+OSP	OSP		√	1	0	01x	0	110	1	1	28	17
OEP+OSP	TSP		√	1	0	01x	0	101	1	1	29	16
OEP+OSP	OSP+TSP		√	1	0	01x	0	111	1	1	30	18
-	TEP		√	1	1	xxx	0	0x0	0	1	31	19
-	TEP+TSP		√	1	1	xxx	0	0x1	0	1	32	20

x: no meaning, **use 0 for correct operation!**

Flows have to be adjusted bidirectionally -> in up- and downstream for each originating point in one direction the terminating point in the other direction has to be adjusted.

8.2 OAM Cell Formats

8.2.1 OAM Cell Header Coding

	VCI	PTI	HK*
F4 Segment flow	0003_H	don't care for Rx 000 for Tx	111
F4 End-to-end flow	0004_H	don't care for Rx 000 for Tx	111
F4 Internal Flow (for ICC)*	0003_H	don't care for Rx 000 for Tx	100
F5 Segment flow	don't care for Rx $FFFF_H$ for Tx	100	111
F5 End-to-end flow	don't care for Rx $FFFF_H$ for Tx	101	111
F5 Internal Flow (for ICC)*	don't care for Rx $FFFF_H$ for Tx	100	100

* Proprietary functions, use optional

The following sections describe the payload of the OAM cells supported by the AOP. When generating a cell the complete cell is defined, at detection or loop of OAM cells only those fields are given the AOP uses to detect the respective cell. All other fields are handled transparently.

8.2.2 AIS Cell

Payload byte	Generated AIS Cell			
0..3	10_H	$6A_H$	$6A_H$	$6A_H$
4..7	$6A_H$	$6A_H$	$6A_H$	$6A_H$
8..11	$6A_H$	$6A_H$	$6A_H$	$6A_H$
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	Received AIS Cell			
0..3	10_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

8.2.3 RDI Cell

Payload byte	Generated RDI Cell			
0..3	11_H	$6A_H$	$6A_H$	$6A_H$
4..7	$6A_H$	$6A_H$	$6A_H$	$6A_H$
8..11	$6A_H$	$6A_H$	$6A_H$	$6A_H$
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	Received RDI Cell			
0..3	11_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

8.2.4 CC Cell

Payload byte	Generated CC Cell			
0..3	14_H	$6A_H$	$6A_H$	$6A_H$
4..7	$6A_H$	$6A_H$	$6A_H$	$6A_H$
8..11	$6A_H$	$6A_H$	$6A_H$	$6A_H$
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	Received CC Cell			
0..3	14_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

8.2.5 LB Cell

Payload byte	Generated LB Cell at originating point			
0..3	TMR1L(15:8)	TMR1L(7:0)	TMR2H(15:8)	TMR2H(7:0)
4..7	TMR2L(15:8)	TMR2L(7:0)	TMR3H(15:8)	TMR3H(7:0)
8..11	TMR3L(15:8)	TMR3L(7:0)	TMR4H(15:8)	TMR4H(7:0)
12..15	TMR4L(15:8)	TMR4L(7:0)	TMR5H(15:8)	TMR5H(7:0)
16..19	TMR5L(15:8)	TMR5L(7:0)	TMR6H(15:8)	TMR6H(7:0)
20..23	TMR6L(15:8)	TMR6L(7:0)	TMR7H(15:8)	TMR7H(7:0)
24..27	TMR7L(15:8)	TMR7L(7:0)	TMR8H(15:8)	TMR8H(7:0)
28...31	TMR8L(15:8)	TMR8L(7:0)	TMR9H(15:8)	TMR9H(7:0)
32..35	TMR9L(15:8)	TMR9L(7:0)	TMR10H(15:8)	TMR10H(7:0)
36..39	TMR10L(15:8)	TMR10L(7:0)	TMR11H(15:8)	TMR11H(7:0)
40..43	TMR11L(15:8)	TMR11L(7:0)	TMR12H(15:8)	TMR12H(7:0)
44..47	TMR12L(15:8)	TMR12L(7:0)	000000 : CRC-10(9:0)	

TMRxx = Registers for Insertion Buffer access

Payload byte	Received Loopback Cell at loopback and at terminating point			
0..3	18_H	01_H		
4..7			Location ID #15	Location ID #14
8..11	Location ID #13	Location ID #12	Location ID #11	Location ID #10
12..15	Location ID #9	Location ID #8	Location ID #7	Location ID #6
16..19	Location ID #5	Location ID #4	Location ID #3	Location ID #2
20..23	Location ID #1	Location ID #0	Source ID #15	Source ID #14
24..27	Source ID #13	Source ID #12	Source ID #11	Source ID #10
28...31	Source ID #9	Source ID #8	Source ID #7	Source ID #6
32..35	Source ID #5	Source ID #4	Source ID #3	Source ID #2
36..39	Source ID #1	Source ID #0		
40..43				
44..47			xxxxxx : CRC-10(9:0)	

Payload byte	Generated LB Cell at loopback point			
0..3	18_H	00_H		
4..7				
8..11				
12..15				
16..19				
20..23		**byte 2..45 and byte 46(7:2)**		
24..27		**are copied from received**		
28...31		**LB cell**		
32..35				
36..39				
40..43				
44..47			000000 : CRC-10(9:0)	

8.2.6 FM Cell

Payload byte	Generated FM Cell			
0..3	20_H	MCSN	TUC_{0+1}(15:8)	TUC_{0+1}(7:0)
4..7	BEDC(15:8)	BEDC(7:0)	TUC_0(15:8)	TUC_0(7:0)
8..11	FF_H	FF_H	FF_H	FF_H
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	Received FM Cell			
0..3	20_H	MCSN	TUC_{0+1}(15:8)	TUC_{0+1}(7:0)
4..7	BEDC(15:8)	BEDC(7:0)	TUC_0(15:8)	TUC_0(7:0)
8..11				
12..15				
16..19				
20..23		**byte 8..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

8.2.7 BR Cell

Payload byte	Generated BR Cell			
0..3	21_H	MCSN	TUC_{0+1}(15:8)*	TUC_{0+1}(7:0)*
4..7	BEDC(15:8)	BEDC(7:0)	TUC_0(15:8)*	TUC_0(7:0)*
8..11	FF_H	FF_H	FF_H	FF_H
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$TRCC_0$(15:8)	$TRCC_0$(7:0)	BLER
44..47	$TRCC_{0+1}$(15:8)	$TRCC_{0+1}$(7:0)	000000 : CRC-10(9:0)	

* TUC_0 and TUC_{0+1} are copied from the received FM cell

Payload byte	Received BR Cell			
0..3	21_H	MCSN	TUC_{0+1}(15:8)	TUC_{0+1}(7:0))
4..7			TUC_0(15:8)	TUC_0(7:0))
8..11				
12..15				
16..19		**byte 4, 5 and**		
20..23		**byte 8..40 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43		$TRCC_0$(15:8)	$TRCC_0$(7:0)	BLER
44..47	$TRCC_{0+1}$(15:8)	$TRCC_{0+1}$(7:0)	xxxxxx : CRC-10(9:0)	

8.2.8 PM/CC Activation/deactivation Cell

Payload byte	Generated PM/CC activation/deactivation Cell			
0..3	TMR1L(15:8)	TMR1L(7:0)	TMR2H(15:8)	TMR2H(7:0)
4..7	TMR2L(15:8)	TMR2L(7:0)	TMR3H(15:8)	TMR3H(7:0)
8..11	TMR3L(15:8)	TMR3L(7:0)	TMR4H(15:8)	TMR4H(7:0)
12..15	TMR4L(15:8)	TMR4L(7:0)	TMR5H(15:8)	TMR5H(7:0)
16..19	TMR5L(15:8)	TMR5L(7:0)	TMR6H(15:8)	TMR6H(7:0)
20..23	TMR6L(15:8)	TMR6L(7:0)	TMR7H(15:8)	TMR7H(7:0)
24..27	TMR7L(15:8)	TMR7L(7:0)	TMR8H(15:8)	TMR8H(7:0)
28...31	TMR8L(15:8)	TMR8L(7:0)	TMR9H(15:8)	TMR9H(7:0)
32..35	TMR9L(15:8)	TMR9L(7:0)	TMR10H(15:8)	TMR10H(7:0)
36..39	TMR10L(15:8)	TMR10L(7:0)	TMR11H(15:8)	TMR11H(7:0)
40..43	TMR11L(15:8)	TMR11L(7:0)	TMR12H(15:8)	TMR12H(7:0)
44..47	TMR12L(15:8)	TMR12L(7:0)	000000 : CRC-10(9:0)	

TMRxx = Registers for Insertion Buffer access

Payload byte	Received activation/deactivation PM Cell at terminating point			
0..3	80_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and byte 46(7:2)**		
24..27		**are don't care**		
28...31				
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

Payload byte	Received activation/deactivation CC Cell at terminating point			
0..3	81_H			
4..7				
8..11				
12..15				
16..19				
20..23		byte 1..45 and byte 46(7:2)		
24..27		are don't care		
28...31				
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

8.3 References

1. UTOPIA Level 1 Specification Version 2.01, March 21, 1994, ATM Forum
2. UTOPIA Level 2 Specification Version 1.0, June 1995, ATM Forum
3. IEEE 1596.3 Standard for Low-Voltage Differential Signals for SCI, Draft 1.3, Nov. 95
4. Joint Test Action Group JTAG standard IEEE Std. 1149.1
5. 'ATM Networks: Concepts, Protocols, Applications', Händel, Schröder, Huber, Addison-Wesley, 1994, ISBN 0-201-42274-3
6. ITU-T Recommendation I.610 „B-ISDN Operation and Maintenance Principles and Functions", 11/94
7. Bellcore TA-NWT 1248 CORE „Generic Requirements for Operations of ATM Network Elements"

8.4 Acronyms

ABM	PXB 4330 E **A**TM **B**uffer **M**anager
AIS	**A**larm **I**ndication **S**ignal (I.610)
ALP	PXB 4350 E **A**TM **L**ayer **P**rocessor
AOP	PXB 4340 E **A**TM **O**AM **P**rocessor
BEDC	**B**lock **E**rror **D**etection **C**ode (I.610)
BIP-16	**B**it **I**nterleaved **P**arity, 16 bit
BLER	**Bl**ock **E**rror **R**esult (I.610)
BR	**B**ackward **R**eporting (PM function)
byte	octet = 8 bit
CC	**C**ontinuity **C**heck (I.610)
CLP	**C**ell **L**oss **P**riority of standardized ATM cell
CRC-10	**C**yclic **R**edundancy **C**heck; uses polynomial $1+x+x^4+x^5+x^9+x^{10}$
double word	32 bit
EDC	**E**rror **D**etection **C**ode of OAM cells (I.610), uses CRC-10
FM	**F**orward **M**onitoring (PM cell type)
HK	**H**ouse**K**eeping bits of UDF1 field in UTOPIA cell format
HT	**H**eader **T**ranslation
I/O	**I**nput / **O**utput
ICC	**I**nternal **C**ontinuity **C**heck (proprietary I.610)
ITU-T	**I**nternational **T**elecommunications **U**nion - Telecommunications standardization sector
IWE8	PXB 4220 **I**nter**W**orking **E**lement for 8 channels
LB	**L**oop**b**ack (I.610)
LCI	**L**ocal **C**onnection **I**dentifier
LIC	**L**ine **I**nterface **C**ard or **L**ine **I**nterface **C**ircuit
LOC	**L**oss **O**f **C**ontinuity (I.610)
LPS	**L**ine **P**rotection **S**witching
LSB	**L**east **S**ignificant **B**it

octet	byte = 8 bit
OAM	**O**peration **A**nd **M**aintenance
OEP	**O**riginating **E**nd **P**oint
OSP	**O**riginating **S**egment **P**oint
PM	**P**erformance **M**onitoring (I.610)
PN	**P**ort **N**umber
PTI	**P**ayload **T**ype **I**ndication field of standardized ATM cell
RDI	**R**emote **D**efect **I**ndication (I.610)
SSRAM	**S**ynchronous **S**tatic **RAM**
tbd	**t**o **b**e **d**efined
TEP	**T**erminating **E**nd **P**oint
TM	**T**raffic **M**anagement
TSP	**T**erminating **S**egment **P**oint
UTOPIA	**U**niversal **T**est and **Op**eration **I**nterface for **A**TM
VC-	**V**irtual **C**hannel specific
VCC	**V**irtual **C**hannel **C**onnection
VCI	**V**irtual **C**hannel **I**dentifier of standardized ATM cell
VP-	**V**irtual **P**ath specific
VPC	**V**irtual **P**ath **C**onnection
VPI	**V**irtual **P**ath **I**dentifier of standardized ATM cell
word	16 bit