HARRIS SEMICONDUCTOR

CD74LPT16501

December 1996

Fast CMOS 18-Bit Registered Transceiver

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74LPT16501AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16501ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16501MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16501SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

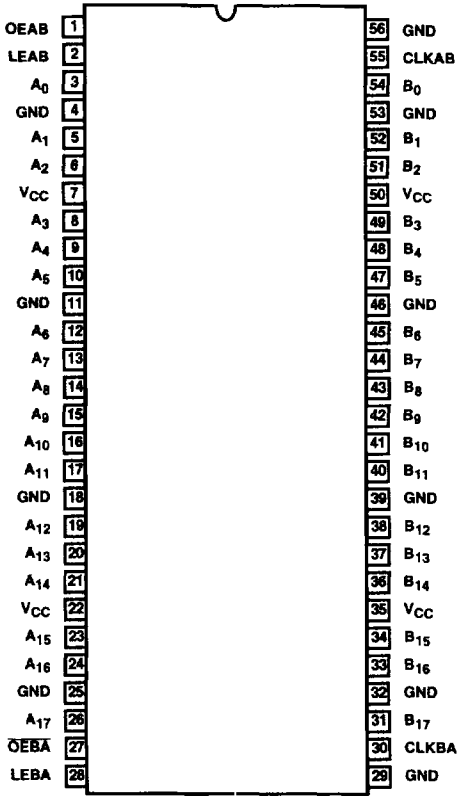
Description

The CD74LPT16501 is an 18-bit registered bus transceiver designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and $\overline{OEBA}$), Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using $\overline{OEBA}$, LEBA and CLKBA. This high-speed, low power device offers a flow-through organization for ease of board layout.

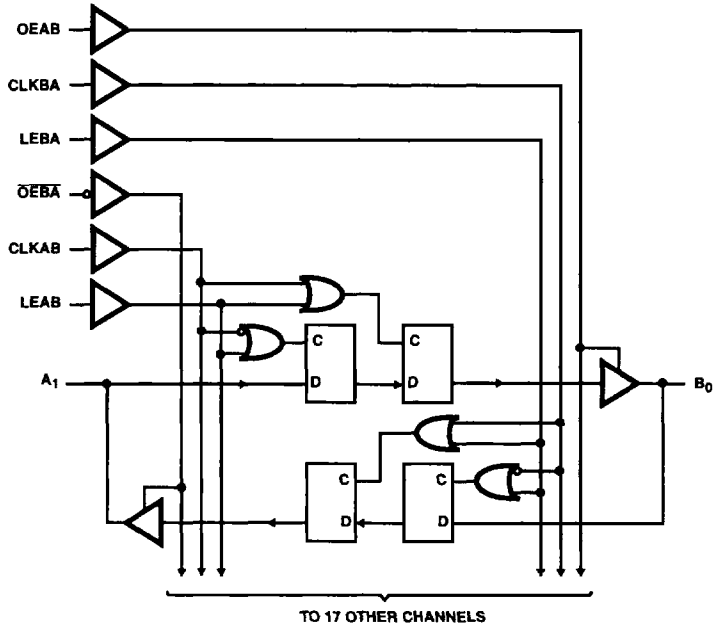
The CD74LPT16501 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.

Pinout

CD74LPT16501
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 4)

INPUTS				OUTPUTS
OEAB	**LEAB**	**CLKAB**	**A_X**	**B_X**
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B (Note 2)
H	L	H	X	B (Note 3)

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A_X	A-to-B Data Inputs or B-to-A Three-State Outputs
B_X	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 8)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 8)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 10)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V
Short Circuit Current (Note 9)	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		-	-	±100	µA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 11)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 11)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 12)	-	2.0	30	µA
Dynamic Power Supply Current (Note 13)	I_{CCD}	V_{CC} = Max, Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 15)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB), 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND, f_i = 5MHz One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB), 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND, f_i = 2.5MHz Eighteen Bits Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 14)	mA

Switching Specifications Over Operating Range (Note 16)

PARAMETER	SYMBOL	(NOTE 17) TEST CONDITIONS	CD74LPT16501		CD74LPT16501A		UNITS
			(NOTE 18) MIN	MAX	(NOTE 18) MIN	MAX	
CLKAB or CLKBA frequency	t_{MAX}	C_L = 50pF R_L = 500Ω	-	100	-	150	ns
Propagation Delay A_X to B_X or B_X to A_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.1	ns
Propagation Delay LEBA to A_X, LEAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	5.6	ns
Propagation Delay CLKBA to A_X, CLKAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	5.6	ns
Output Enable Time $\overline{OEBA}$ to A_X, OEAB to Bx	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	6.0	ns
Output Disable Time (Note 19) $\overline{OEBA}$ to A_X, OEAB to B_X	t_{PHZ} t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	5.6	ns

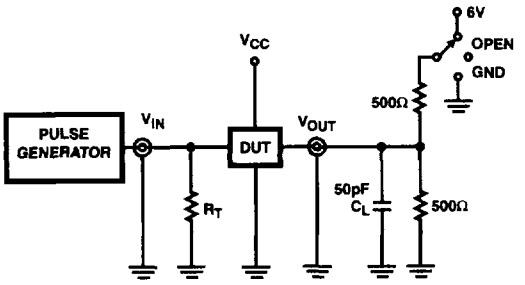
Switching Specifications Over Operating Range (Note 16) **(Continued)**

PARAMETER	SYMBOL	(NOTE 17) TEST CONDITIONS	CD74LPT16501		CD74LPT16501A		UNITS
			(NOTE 18) MIN	MAX	(NOTE 18) MIN	MAX	
Setup Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	ns
Hold Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_H	C_L = 50pF R_L = 500Ω	0	-	0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock HIGH	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock LOW	t_{SU}	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	ns
Hold Time HIGH or LOW, Ax to LEAB, Bx to LEBA	t_H	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	ns
LEAB or LEBA Pulse Width HIGH (Note 19)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 19)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	ns
Output Skew (Note 20)	$t_{SK(O)}$	C_L = 50pF R_L = 500Ω	-	0.5	-	0.5	ns

NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading, except as noted.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. This parameter is guaranteed but not tested.
10. $V_{OH} = V_{CC}$ - 0.6V at rated current.
11. This parameter is determined by device characterization but is not production tested.
12. Per TTL driven input; all other inputs at V_{CC} or GND.
13. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
14. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
15. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
16. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
17. See test circuit and wave forms.
18. Minimum limits are guaranteed but not tested on Propagation Delays.
19. This parameter is guaranteed but not production tested.
20. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

21. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

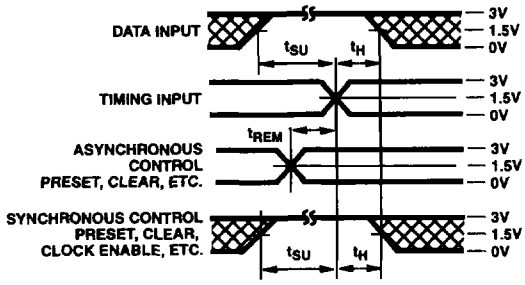


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

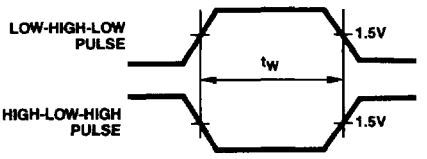


FIGURE 3. PULSE WIDTH

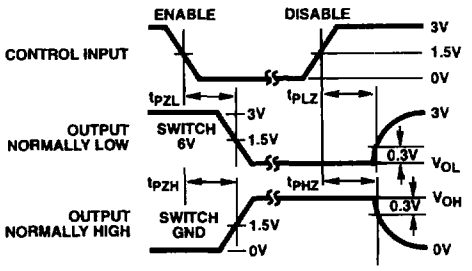


FIGURE 4. ENABLE AND DISABLE TIMING

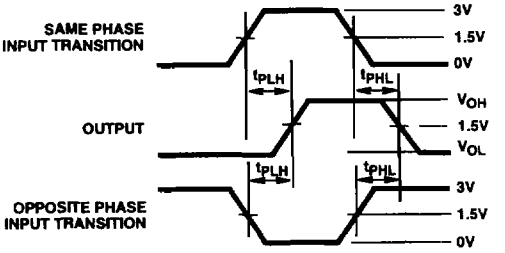


FIGURE 5. PROPAGATION DELAY