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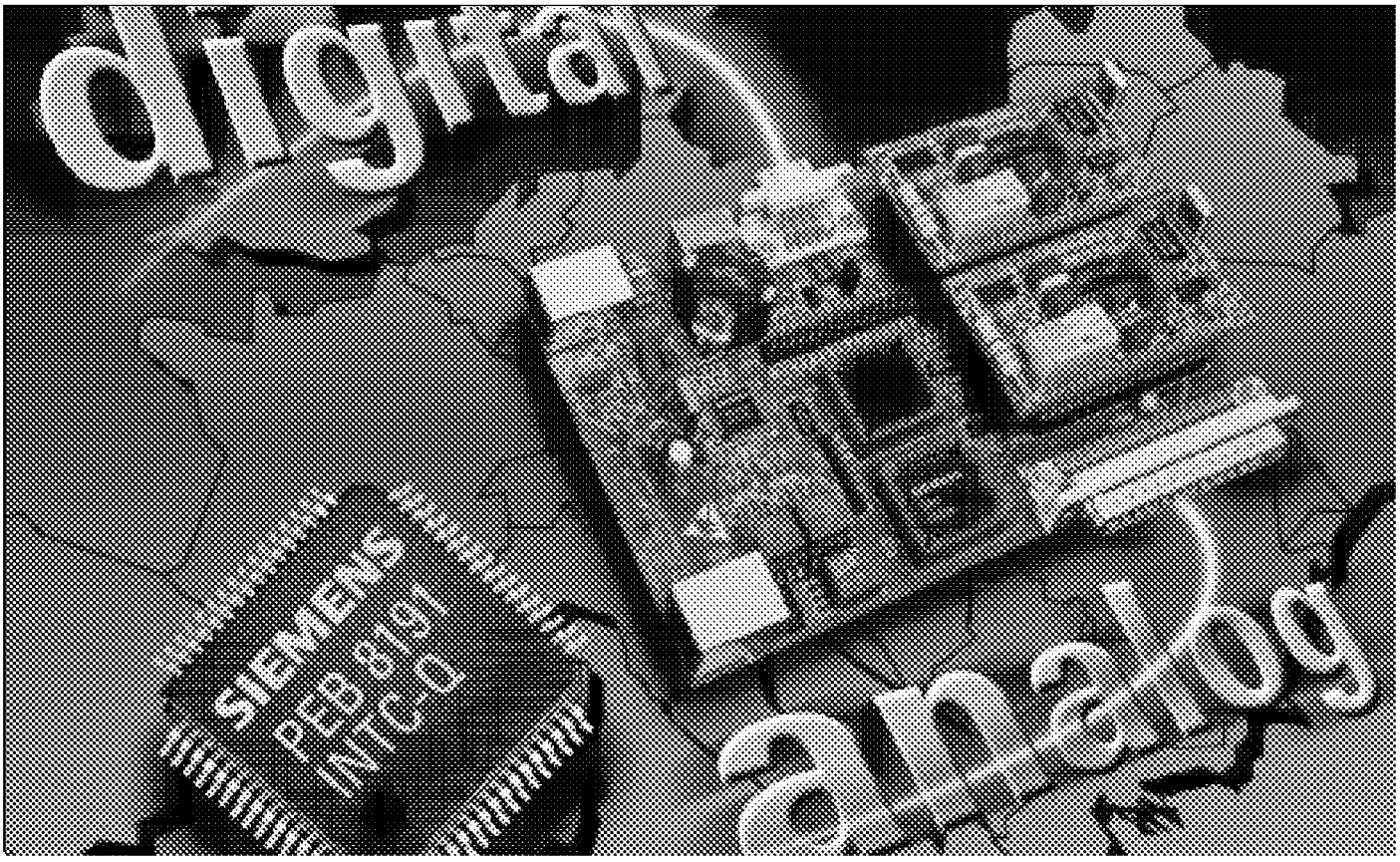

ICs for Communications

Intelligent Network Termination Controller
INTC-Q

PEB 8191

PEF 8191

Version 1.1

Product Overview 02.97

T8191-XV11-O1-7600

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1 Overview

The Intelligent Network Termination Controller (INTC-Q) is a one-chip NT for the Integrated Services Digital Network. The INTC-Q is used for Intelligent NT[1]s, NT1s and U- or S-terminals as well as terminal adaptors (TA). It combines the devices PSB 21910 (IEC-Q NTE), the PEB 2081 (SBCX) and the PEB 2070 (ICC). The INTC-Q provides the 2B1Q-U-interface as defined by ETSI ETR 080 1995 and ANSI T1.601 1992 together with the S/T-interface as of ITU Rec. I.430.

In µP mode the INTC-Q is perfectly suited for intelligent NTs as well as for ISDN-terminals and terminal adaptors (TA) with U- or S-interface. An integrated HDLC controller and a parallel or serial microcontroller interface give access to the D-channel and allow the microcontroller to control the U- and S-transceivers. High level support of the layer-2 protocol (LAPD) is possible.

An extended IOM®-2 interface allows the intelligent NT or TA to feature analog telephone lines or data terminals. Codec filter devices like the PSB 2161 (ARCOFI®-BA), the PSB 2132 (SICOFI®-2 TE[2]), the PSB 2134 (SICOFI®-4 TE[3]) or standard codecs may be connected to the extended IOM®-2 interface as well as communication controllers such as PSB 2110 (ITAC) or PSB 21525 (HSCX-TE).

Internal switching functions allow the expansion of the intelligent NT with local S-interface switching.

In NT1 mode the INTC-Q works as a stand-alone NT1 with completely automatic handling of all layer-1 procedures without a microcontroller. In this mode the INTC-Q is pin-to-pin and function compatible to the PEB 8091, NTC-Q.

The INTC-Q is a CMOS device that comes in a T-QFP 64 package. It operates from a single +5V supply and features S-only as well as U-only operation with very low power consumption.

1 'Intelligent NT's are also known as 'Smart NT's or 'NT plus'
2 PSB 2132, SICOFI®-2 TE is a two channel terminal derivative of the PEB 2466, SICOFI®-4µC
3 PSB 2134, SICOFI®-4 TE is a pin-to-pin compatible terminal derivative of the PEB 2466, SICOFI®-4µC

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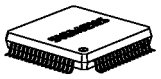
Intelligent Network Termination Controller INTC-Q

PEB 8191
PEF 8191

Product Overview **CMOS**

1.1 Features



T-QFP 64

- Single chip solution including U-, S-transceiver and D-channel controller
- Stand-alone mode for ISDN NT1 applications compatible to PEB8091, NTC-Q
- U-interface (2B1Q) conform to ANSI T1.601, ETSI ETR 080 and CNET ST/LAA/ELR/DNP/822:
  - Meets and exceeds all transmission requirements on all ANSI, ETSI and CNET loops
  - MLT input and decode logic (ANSI)
  - function compatible to IEC-Q NTE
- S/T-interface conform to ITU Rec. I.430, ETS 300 012 and ANSI T1.605
  - Meets and exceeds all transmission requirements
  - S/T interface in NT and TE mode
  - function compatible to SBCX
- Activation status LED supported
- Integrated ICC-compatible D-channel controller
  - 64-byte FIFO storage of HDLC data per direction
  - Support of LAPD protocol
  - Automatic D-channel arbitration between S-bus and local HDLC controller using S-bus arbitration principle
- IOM®-2 interface for connection of SICOFI®-2/4TE, ARCOFI®, ITAC, HSCX-TE, ISAR
- Bit clock and two programmable frame strobes to connect standard codecs
- Parallel or serial microprocessor interface and watch dog
- µP access to B-channels and intercommunication channels
- µP access to IOM®-2 Monitor-channels and C/I-channels
- Microcontroller clock source; clock rate adjustable between 0.96MHz and 7.68MHz
- Single 5 Volt power supply
- Low power CMOS technology with power-down mode

Type	Ordering Code	Package
PEB 8191		T-QFP 64
PEF 8191		T-QFP 64

1.2 Logic Symbol µP mode

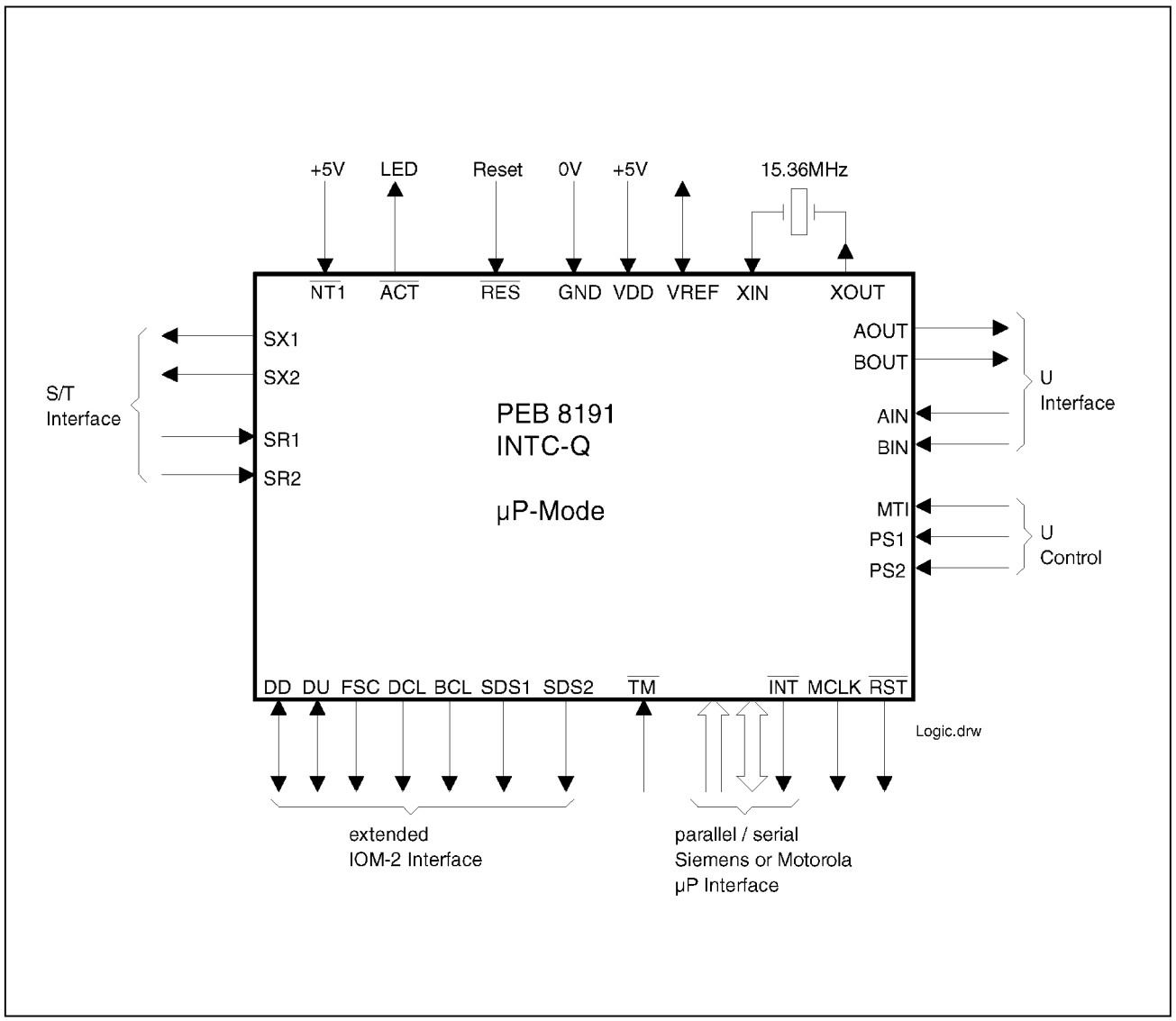


Figure 1
Logic Symbol µP mode

1.3 Logic Symbol NT1 mode

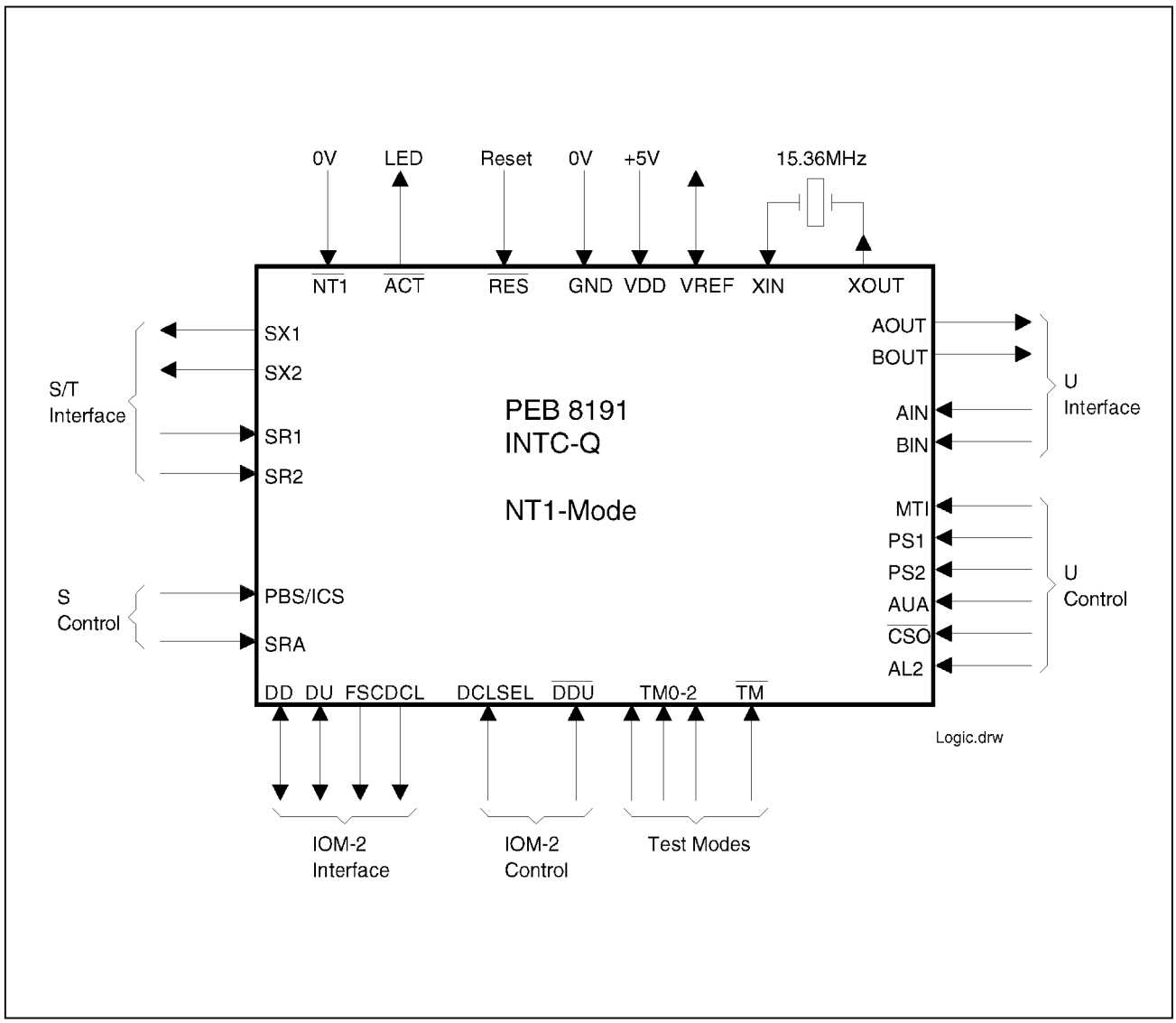


Figure 2
Logic Symbol NT1 mode

1.4 Pin Configuration

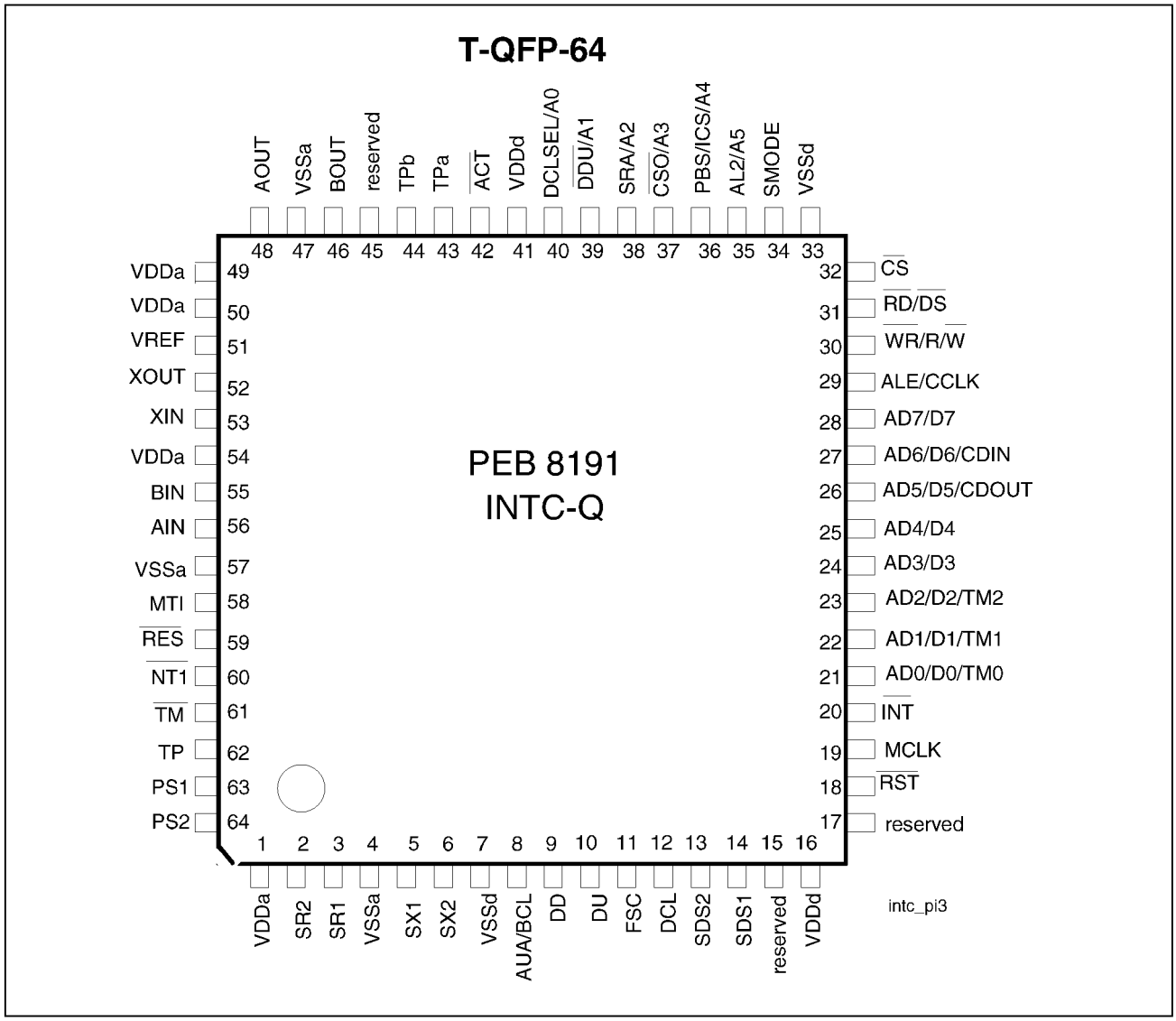


Figure 3
Pin Configuration

1.5 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type and a brief description of the function

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
Power Supply Pins				
1, 49, 50, 54 16, 41	VDD_A1..4 VDD_D1,2	VDD_A1..4 VDD_D1,2		+5V +/-5% supply voltage, analog +5V +/-5% supply voltage, digital
4, 47, 57 7, 33	VSS_A1..3 VSS_D1,2	VSS_A1..3 VSS_D1,2		Analog GND Digital GND
(extended) IOM®-2 interface				
9	DD	DD	I/O	**Data Downstream.** IOM®-2 data downstream synchronous to DCL clock. Tristate or open-drain (default) in µP mode (programmable). Push-pull, open-drain or high Z in NT1 mode (see chapter 2.2.2).
10	DU	DU	I/O	**Data Upstream.** IOM®-2 data upstream synchronous to DCL clock. Tristate or open-drain (default) in µP mode (programmable). Push-pull, open-drain or high Z in NT1 mode (see chapter 2.2.2).
11	FSC	FSC	O	**Frame synchronization clock.** The start of the B1 channel in time slot 0 is marked.
12	DCL	DCL	O	**Data clock.** 512 kHz (NT1mode) or 1.536 MHz data clock (NT mode, TE mode, NT1 mode).
13	SDS2	reserved	O	**Serial Data Strobe 2.** Programmable strobe signal. High during the time the data of B1, B2, IC1 or IC2 channel is active on the IOM®-2 interface. Leave open in NT1 mode.

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
14	SDS1	reserved	O	**Serial Data Strobe 1.** Programmable strobe signal. High during the time the data of B1, B2, IC1 or IC2 channel is active on the IOM®-2 interface. Leave open in NT1 mode.
8	BCL	AUA	I/O (PU)	**Bit Clock.** 768 kHz bit clock. **Auto U Activation.** Used in NT1 Mode only. '1' sets the U-transceiver to 'NT-AUTO' Mode where automatic activation of the U-interface after reset is provided. Internal Pull-up

U-Interface

48	AOUT	AOUT	O	Differential U-interface output
46	BOUT	BOUT	O	Differential U-interface output
56	AIN	AIN	I	Differential U-interface input
55	BIN	BIN	I	Differential U-interface input

S/T-Interface

5	SX1	SX1	O	S/T-interface positive transmit output
6	SX2	SX2	O	S/T-interface negative transmit output
3	SR1	SR1	I	Differential S/T-interface receive input
2	SR2	SR2	I	Differential S/T-interface receive input

Microcontroller Interface

32	$\overline{CS}$	reserved	I	**Chip Select.** Enable to read or write data, active low.
40	A0	DCLSEL	I	**Address 0.** Address pin in the parallel, non-multiplexed µP interface mode. **DCL Select.** Selects between 512 kHz (1) and 1.536 MHz (0) DCL clock rate for test purposes.

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
39	A1	$\overline{\text{DDU}}$	I	**Address 1.** Address pin in the parallel, nonmultiplexed µP interface mode. **Disconnect DU.** '0' disconnects DU between S- and U-transceiver for test purposes. Normal operation if '1'.
38	A2	SRA	I	**Address 2.** Address pin in the parallel, nonmultiplexed µP interface mode. **S-Receiver Amplifier.** '1' selects 1:1 amplifier ratio (2:1 transformer). '0' selects 2:1 amplifier ratio (external capacitive coupling).
37	A3	$\overline{\text{CSO}}$	I (PU)	**Address 3.** Address pin in the parallel, nonmultiplexed µP interface mode. Internal pull-up. **Cold Start Only.** '0' selects CSO-bit to '1'. '1' selects CSO-bit to '0'. The U-transceiver always performs a warm start. Internal pull-up.
36	A4	PBS ICS	I (PU)	**Address 4.** Address pin in the parallel, nonmultiplexed µP interface mode. Internal pull-up. **Point- Bus Selection.** Selects between point-to-point (1) and bus (0) mode of S-receiver. Internal pull-up. **IOM®-2 channel S-transceiver** Applies only when DCL = 1.536 MHz (i.e. DCLSEL='0'). '0' on this pin maps S-transceiver to IOM®-2 channel 1, '1' maps it to channel 0. Internal pull-up

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
35	A5 AL2		I (PU)	**Address 5.** Address pin in the parallel, nonmultiplexed µP interface mode. Internal pull-up. **ACT-bit Loop 2.** '1' selects the control of loop 2 according to ETSI, '0' sets it according to ANSI. Internal pull-up.
34	SMODE	reserved	I	**Serial Mode.** Selects serial µP interface mode if tied to '1'. Tie to '0' in parallel µP interface mode. Tie to '1' in NT1 mode.
28	AD7 D7	reserved	I/O	**Address/Data 7.** Bus pin 7 in the multiplexed µP interface mode. **Data 7.** Data pin 7 in non-multiplexed µP interface mode. Tie to '1' in the serial µP interface mode and in NT1 mode.
27	AD6 D6 CDIN	reserved	I/O	**Address/Data 6.** Bus pin 6 in the multiplexed µP interface mode. **Data 6.** Data pin 6 in non-multiplexed µP interface mode. **Controller Data In.** Controller data in in serial processor mode. CCLK determines the data rate. Tie to '1' in NT1 mode.

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
26	AD5 D5 CDOUT	reserved	I/O	**Address/Data 5.** Bus pin 5 in the multiplexed µP interface mode. **Data 5.** Data pin 5 in non-multiplexed µP interface mode. **Controller Data Out.** CCLK determines the data rate. CDOUT is 'high Z' if no data is transmitted. Tie to '1' in NT1 mode.
25	AD4 D4	reserved	I/O	**Address/Data 4.** Bus pin 4 in the multiplexed µP interface mode. **Data 4.** Data pin 4 in non-multiplexed µP interface mode. Tie to '1' in the serial µP interface mode and in NT1 mode.
24	AD3 D3	reserved	I/O	**Address/Data 3.** Bus pin 3 in the multiplexed µP interface mode. **Data 3.** Data pin 3 in non-multiplexed µP interface mode. Tie to '1' in the serial µP interface mode and in NT1 mode.
23	AD2 D2 TM2	 TM2	I/O (PU)	**Address/Data 2.** Bus pin 2 in the multiplexed µP interface mode. Internal pull-up. **Data 2.** Data pin 2 in non-multiplexed µP interface mode. Internal pull-up. **Test Mode 2.** Selects test modes if $\overline{TM}$ = 0. Internal pull-up.

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
22	AD1 D1 TM1	 TM1	I/O (PU)	**Address/Data 1.** Bus pin 1 in the multiplexed µP interface mode. Internal pull-up. **Data 1.** Data pin 1 in non-multiplexed µP interface mode. Internal pull-up. **Test Mode 1.** Selects test modes if $\overline{TM}$ = 0. Internal pull-up
21	AD0 D0 TM0	 TM0	I/O (PU)	**Address/Data 0.** Bus pin 0 in the multiplexed µP interface mode. Internal pull-up. **Data 0.** Data pin 0 in non-multiplexed µP interface mode. Internal pull-up. **Test Mode 0.** Selects test modes if $\overline{TM}$ = 0. Internal pull-up
31	$\overline{RD}$ $\overline{DS}$	reserved	I	**Read (Siemens/Intel modes).** Indicates a read operation, active low. **Data Strobe (Motorola mode).** Indicates a data transfer, active low. Tie to '1' in serial µP interface mode and in NT1 mode.
30	$\overline{WR}$ R/$\overline{W}$	reserved	I	**Write (Siemens/Intel modes).** Indicates a write operation, active low. **Read/Write (Motorola mode):** Indicates a read (high) or write (low) operation. Tie to '1' in serial µP interface mode and in NT1 mode.
20	$\overline{INT}$	reserved	O	**Interrupt Request.** The signal is activated when the INTC-Q requests an interrupt. Active low. Open drain. Leave open in NT1 mode.

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
29	ALE CCLK	reserved	I	**Address Latch Enable.** Siemens/Intel **multiplexed** bus type:A high on this pin indicates an address on the external address/data bus. Siemens/Intel **non-multiplexed**: tie to '0'. Motorola bus type: tie to '1'. **Controller Data Clock.** Connect up to 7.68 MHz clock to shift data from or to the device in the serial mode. Tie to '1' in NT1 mode.
18	$\overline{\text{RST}}$	reserved	O	**Reset Output.** Active low. Set to '0', when internal watchdog, $\overline{\text{RES}}$ or power-on reset are active. Leave open in NT1 mode.
19	MCLK	reserved	O	**Microcontroller Clock.** Programmable 0.96 MHz to 7.68 MHz clock. Leave open in NT1 mode.

Control and Status Pins

58	MTI	MTI	I	**Metallic Termination Input.** Input to evaluate Metallic Termination pulses. Tie to '1' if not used.
63	PS1	PS1	I (PD)	**Power Status (primary).** The pin value is passed to the overhead bit 'PS1' in the U frame to signalize the status of the primary power supply. Internal pull-down.
64	PS2	PS2	I	**Power Status (secondary).** The pin value is passed to the overhead bit 'PS2' in the U frame to signalize the status of the secondary power supply.
42	$\overline{\text{ACT}}$	$\overline{\text{ACT}}$	O	**Activation LED.** Low Active. Programmable in µP-mode. Indicates the activation status of U- and S-transceiver in NT1 mode. Can directly drive an LED. Open-drain.

Pin No.	Symbol µP mode	Symbol NT1 mode	I/O	Description
Test Pins and Miscellaneous Pins				
61	$\overline{TM}$	$\overline{TM}$	I (PU)	**Test Mode**. Activates test mode of pins TM2-0 (AD2-0) if tied to VSS. Internal pull-up.
62	TP	TP	I (PD)	**Test Pin.** Used for factory device test. Internal pull-down. Do not connect.
43	TPa	TPa	I	**Test Pin a.** Used for factory device test. Tie to '0'
44	TPb	TPb	I	**Test Pin b.** Used for factory device test. Tie to '0'
60	$\overline{NT1}$	$\overline{NT1}$	I	**NT1 Mode Select.** Selects NT1 mode (0) or µP mode (1).
59	$\overline{RES}$	$\overline{RES}$	I	**Reset Input.** Active low. Tie to '1' if not used.
53	XIN	XIN	I	**Crystal IN.** Connect 15.36 MHz clock input or 15.36 MHz crystal .
52	XOUT	XOUT	O	**Crystal OUT.** Connect 15.36 MHz crystal. Leave open if not used.
51	VREF	VREF	I/O	**Reference Voltage.** Connect 100nF vs. VSS_A to buffer internally generated reference voltage.
15	reserved	reserved	I	Tie to '1'.
17	reserved	reserved	O	Used for factory device test. Do not connect.
45	reserved	reserved	I	Tie to '1'.

1.6 System Integration

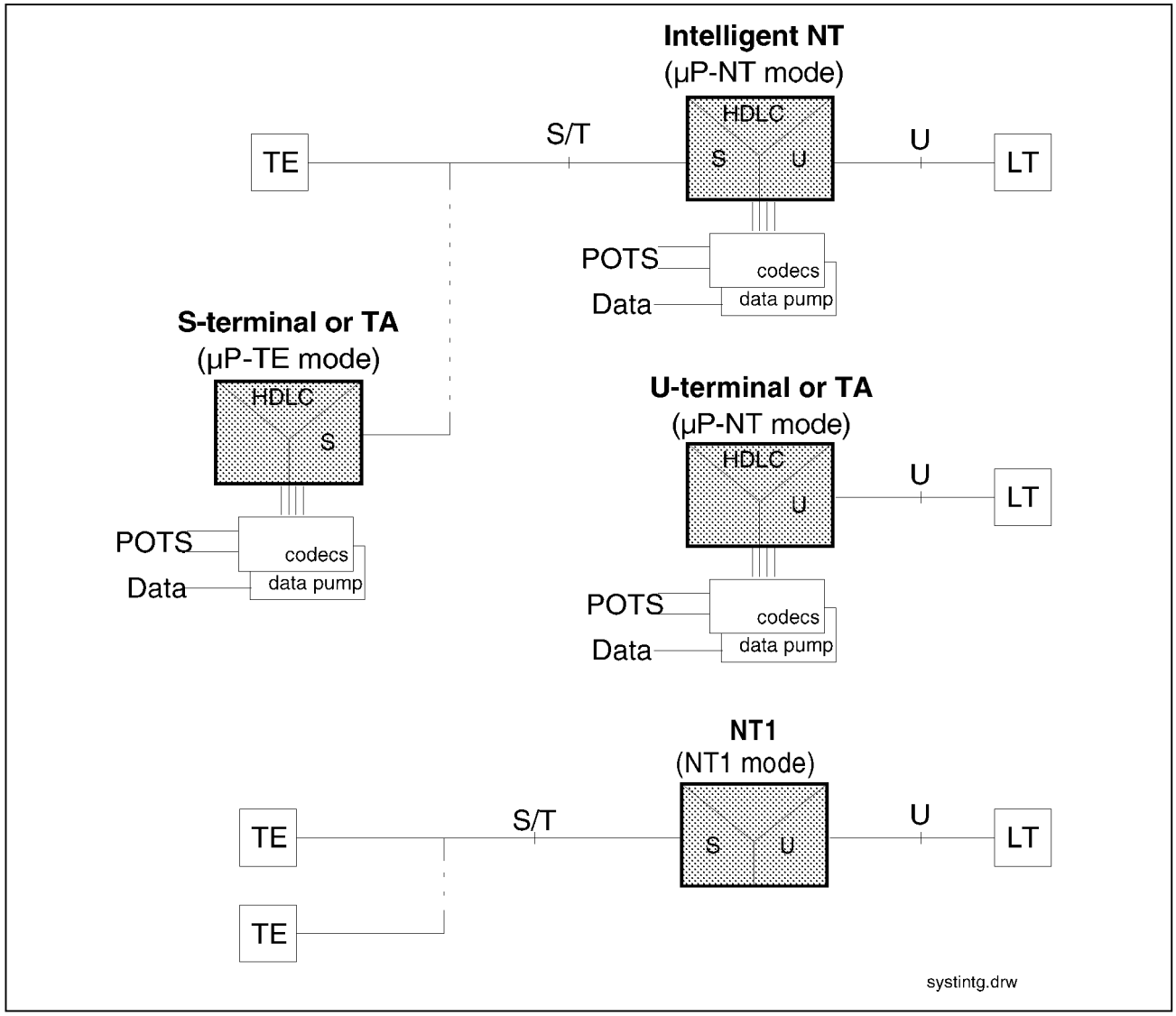


Figure 4
System Integration

A modular architecture allows configuration of the INTC-Q for various applications. Blocks like the S- and U-transceivers, the HDLC controller, the IOM®-2 interface and the D-channel arbitration unit can be configured individually and be enabled and disabled separately. The power consumption of disabled blocks is minimized. **Figure 4** shows configurations for the most common applications. However, other configurations to address further applications are also possible.

1.6.1 Intelligent NT with POTS interface

The INTC-Q is in µP-NT mode. The microcontroller accesses the D-channel in the upstream direction (to the LT). The HDLC controller offers different modes of address handling and support of the LAPD protocol. Hence, an 8-bit microcontroller is sufficient.

The INTC-Q features the IOM®-2 TIC-bus as well as an enhanced algorithm that arbitrates the D-channel between the S-bus and the local HDLC controller. Therefore, the D-channel software is liberated from monitoring the D-channel packets coming from the S-bus.

The IOM®-2 interface issues 1.536 MHz and uses the TE structure with 3 IOM®-2 channels. It allows the connection of a variety of devices, e.g. the SICOFI®-2 TE, the SICOFI®-4 TE, the ARCOFI®-BA, the ITAC or the HSCX-TE. Two programmable frame strobes and a bit clock (BCL) support also non-IOM®-2 devices, e.g. standard codecs.

The U-transceiver is in TE mode and uses IOM®-2 channel 0. Activation and deactivation is controlled via the microprocessor interface.

The S-transceiver is in LT-S mode applying the NT state machine. It is programmed to operate in IOM®-2 channel 1. Individual bits allow the mapping of the B- and D-channels to IOM®-2 channel 0 which enables a transparent data flow between the U- and the S-interface. Activation and deactivation is controlled via the microprocessor interface.

For US applications, the metallic loop termination state machine is included which evaluates the signal provided on the MTI-input and automatically sets the proper test modes. In addition, a C/I-interrupt is generated and the state of the MTI evaluation can be read from a register.

Figure 5 illustrates the connection of the PSB 2132 SICOFI®-2 TE. SLIC-control and monitoring is handled via the serial µP-interface and the SICOFI®-2 TE. Hence, no microcontroller pins are required for SLIC control. The time slots of the SICOFI®-2 TE can individually be programmed to fit the B1, B2 or IC1, IC2-channel of the IOM®-2 interface. The SICOFI®-2/4TE provides internal switching via the IOM®-2/PCM interface.

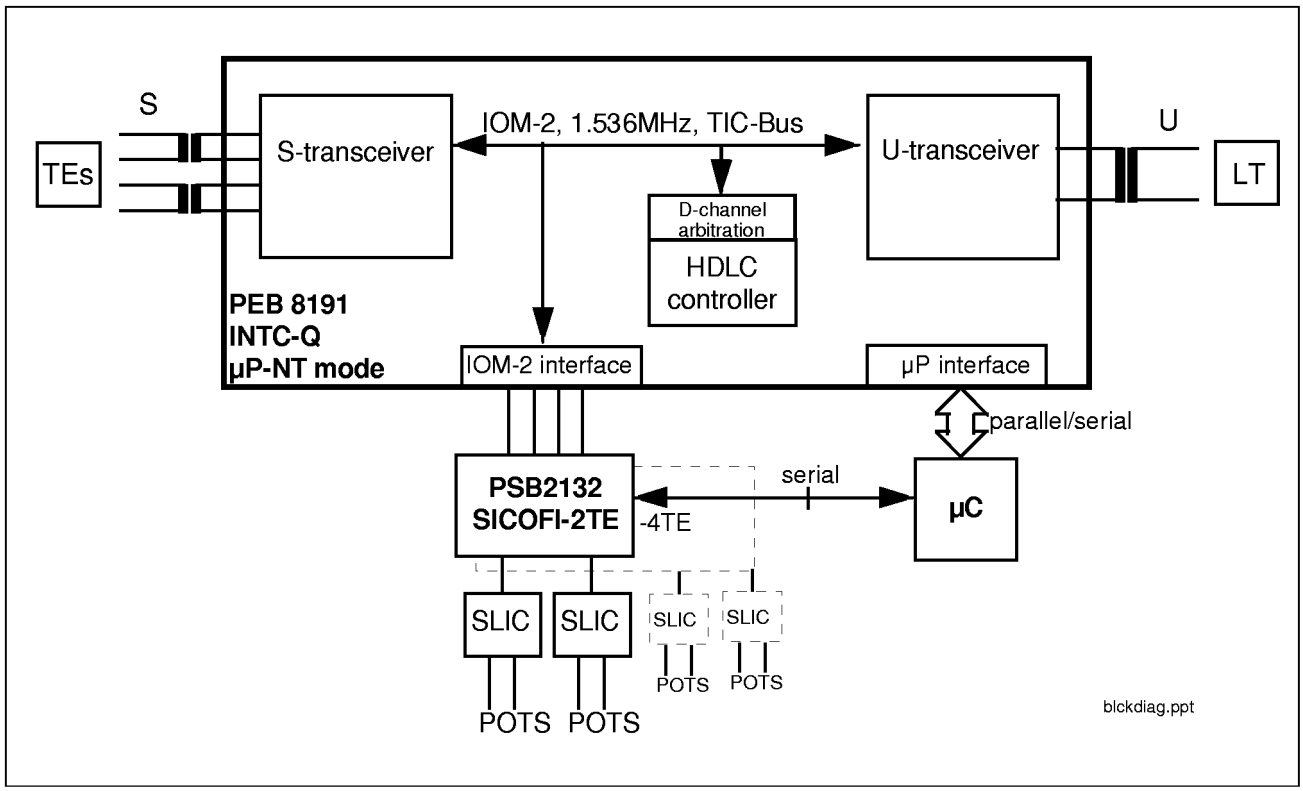


Figure 5
NT + 2 POTS application with SICOFI®-2 TE

Figure 6 illustrates an application with two standard codecs. The active B-channels of the IOM®-2 TE structure are disclosed to the codecs via the frame strobes SDS1 and SDS2. The two frame strobe signals can be assigned to the B1-, B2-, IC1-, or IC2-channel of the IOM®-2 interface via register programming. SLIC control and monitoring is handled via dedicated I/O pins of the microcontroller.

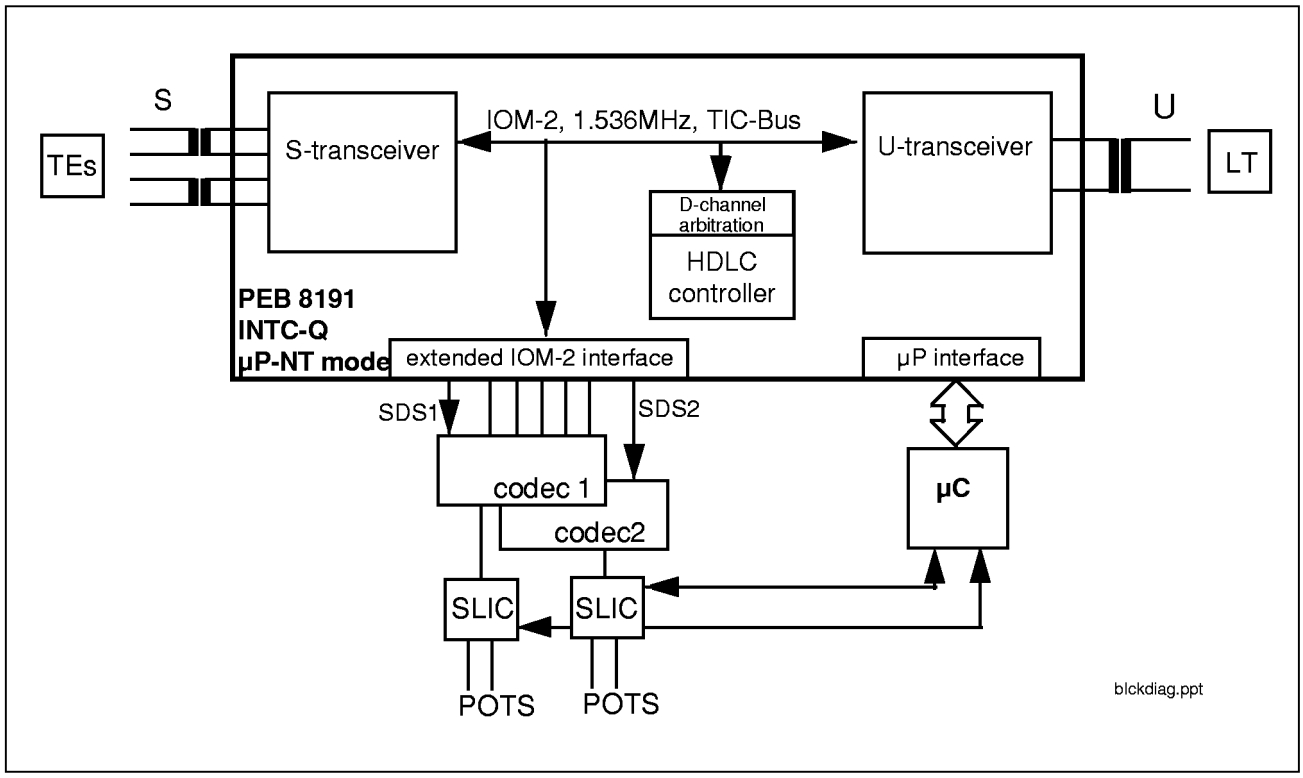


Figure 6
NT + 2 POTS application with standard codecs using programmable frame strobes

1.6.2 Intelligent NT with switching (PBX functionality)

Connecting analog or digital terminals with each other without using the trunk line allows building of a small PBX.

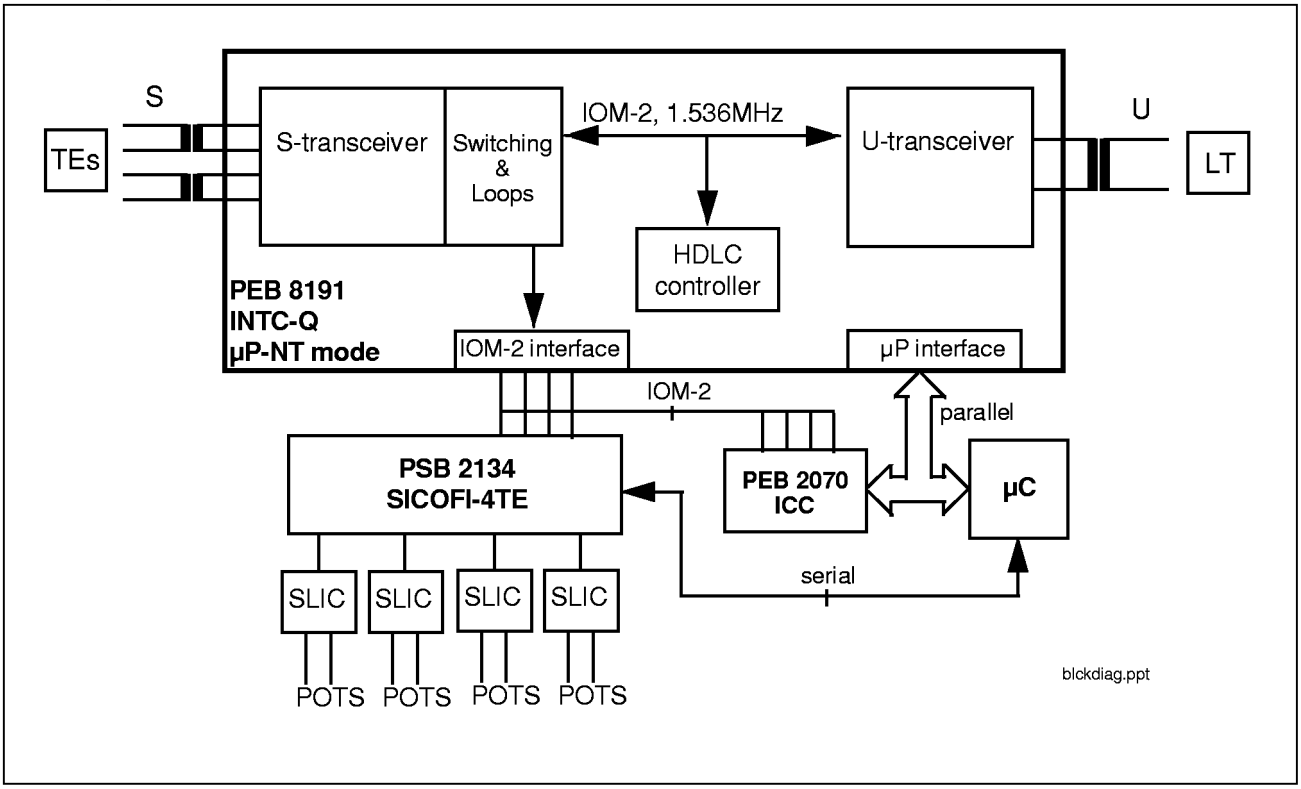


Figure 7
Intelligent NT as small PBX

An additional PEB 2070 (ICC) can be used to perform the D-Channel signalling to the terminals on the S-interface. The HDLC controller of the INTC-Q establishes the link to the exchange. See **Figure 7** for an example with the PSB 2134 SICOFI®-4 TE as codec. In this case, four analog terminals can be connected, two of them having access to the ISDN simultaneously.

Alternatively to the additional ICC the signalling towards the S-bus can also be implemented purely in software. The INTC-Q provides the microcontroller with access to the downstream D-channel via the µP-interface.

Internal communication between terminals on the S-interface and the POTS is possible using the switching functions inside the S-transceiver and the SICOFI®-2/4TE. The D-channel arbitration is disabled and the S-transceiver lies completely in IOM®-2 channel 1. This separates the B-channels and the D-channel from U and S. The voice or data channels of U, S and the POTS can be switched together individually via register programming following the principle of the three-chip solution (IEC-Q NTE, SBCX, ICC). Access to the B- and IC-channels is possible via the µP interface.

1.6.3 Dual Mode S/U-Terminal and TA

In terminal or terminal adaptor (TA) applications only one of the two INTC-Q transceivers is active while the other is disabled and powered down. With the INTC-Q it is possible to cover both, the S and the U-interface with a single layer-1/2 device in the terminal or TA equipment (**Figure 8**).

For terminals connected to the U-interface the INTC-Q is set to µP-NT mode. The U-transceiver is then in TE mode which means it delivers IOM®-2 clocks synchronous to the U-interface. The S-transceiver is disabled.

For terminals connected to the S-interface the INTC-Q is set to µP-TE mode. The S-transceiver is then in TE mode which means it delivers IOM®-2 clocks synchronous to the S-interface. The U-transceiver is disabled.

Both modes are software programmable. The active transceiver and the HDLC controller communicate via the IOM®-2 interface with 1.536 MHz DCL-clock and TE-structure. Direct access is given to this link via the DCL, FSC, DD and DU pins of the IOM®-2 interface. The IOM®-2 interface allows the connection of a wide variety of devices to implement analog or digital voice or data transfer.

Two programmable frame strobe signals (pins SDS1 and SDS2) and a 768 kHz bit clock (pin BCL) are provided to connect up to two non-IOM®-2 devices.

For US applications, the metallic loop termination state machine is included.

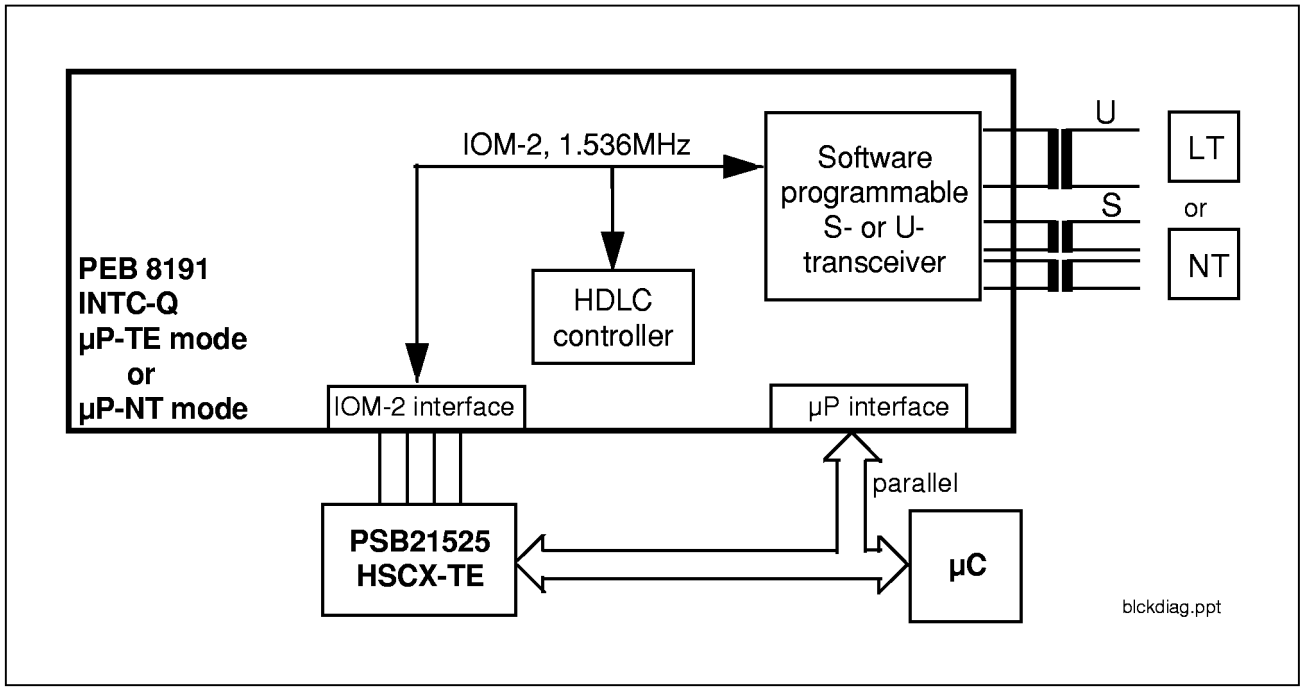


Figure 8
Dual Mode terminal with HSCX-TE

1.6.4 Standard NT1

In NT1 mode the INTC-Q is pin-to-pin compatible to the PEB8091, NTC-Q. It provides NT1 functionality without a microcontroller being necessary. The internal HDLC controller and the microprocessor interface are disabled. The default state of all relevant registers is such that operation of an NT1 is provided. **Figure 9** shows a block diagram of the INTC-Q in NT1 mode.

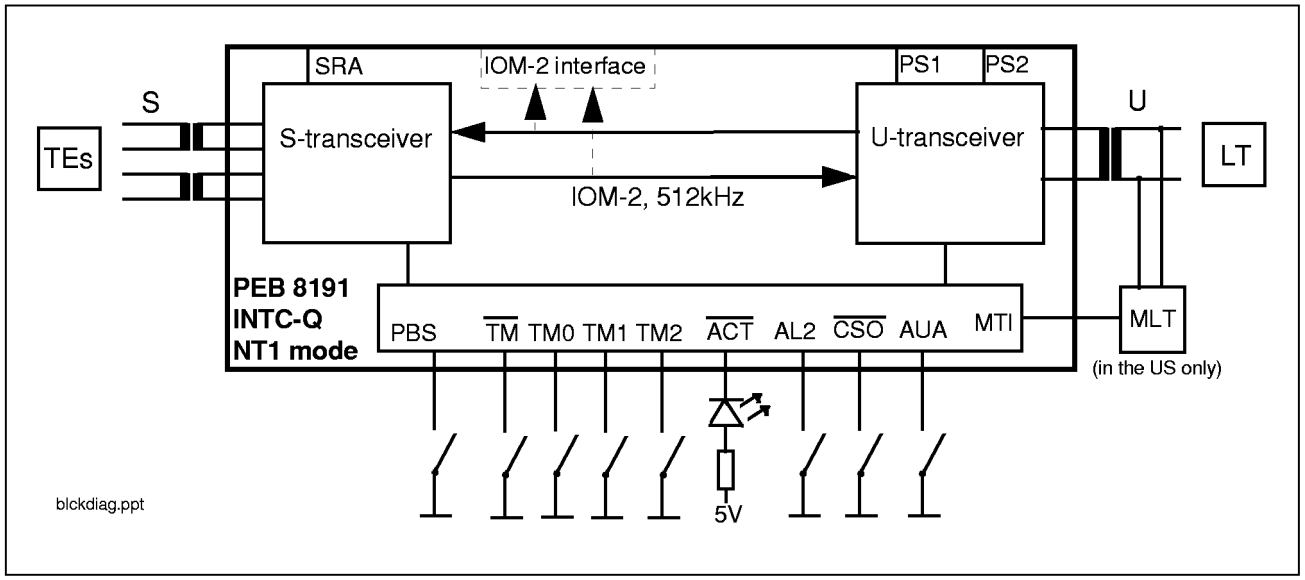


Figure 9
Standard NT1 Block Diagram

Pin AUA is used to select automatic activation of the U-transceiver after power-on and reset. Additional pins control the state of the CSO-bit, ACT-bit during Loop2 and the PS1 and PS2 bits in the U-frame. U-only activation is supported by the U-part. The test modes 'quiet mode', 'send single pulses' and 'data through' can be selected via pins $\overline{TM}$ and TM0-2.

The S-transceiver timing mode may be switched between point-to-point and bus configuration. The amplifier of the S-receiver is configurable to a 2:1ratio which allows the use of capacitive coupling for the receiver. Two test patterns (2 kHz, 96kHz) can be generated via pin strapping of $\overline{TM}$ and TM0-2.

All configuration pins which are intended for connection of a switch have internal pull-up resistors. An LED can be connected to indicate the activation status of the U- and the S-transceiver.

The communication between the S-transceiver and the U-transceiver can be monitored on a 512 kHz IOM®-2 interface. Both transceivers are in NT mode. The IOM®-2 interface can be disabled to reduce power consumption. In addition to the 512 kHz mode, the 1.536 MHz IOM®-2 mode may be selected via pin strapping for test purposes. The S-transceiver may then be configured to IOM®-2 channel 0 or channel 1. If 1.536 MHz are

selected the S-transceiver is in LT-S mode with NT state machine and the U-transceiver is in TE mode.

For US-applications, the metallic loop termination state machine is included which evaluates the signal provided on the MTI-input and automatically sets the INTC-Q in the proper test mode.

In addition to a traditional configuration with transformers on the S-interface, the combination of INTC-Q, PEB 3023 ISFC and PEB 2023 IDCC allows a transformerless S-interface design (**Figure 10**). The ISFC performs polarity reversal to indicate restricted power mode feeding conditions and current limitation.

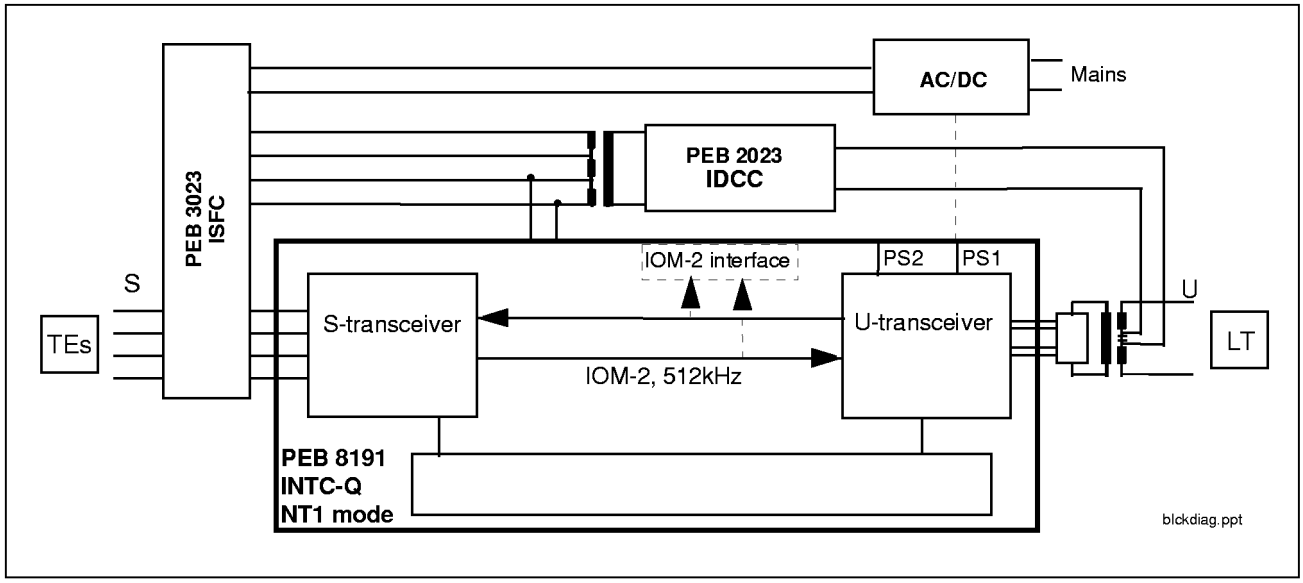


Figure 10
Standard NT1 with ISFC and IDCC

2 Operational Description

2.1 Operational Modes

The default configuration after power-on or reset depends on the state of the $\overline{\text{NT1}}$ pin. Two cases are to be distinguished:

µP mode ($\overline{\text{NT1}}$ tied to VDD)

After power on or reset the INTC-Q is in µP-NT mode. The S-transceiver is disabled to avoid any automatic actions before initialization has been performed. The U-transceiver (NT mode) and the HDLC controller are enabled.

The µP-TE mode can be selected via register programming. In this mode the S-transceiver is enabled (TE mode) and the U-transceiver is disabled.

The internal IOM®-2 interface between the U-part and the S-part works on a 1.536 MHz DCL base. The data on DD, DU, DCL and FSC lines is available on the corresponding pins.

NT1 mode ($\overline{\text{NT1}}$ tied to GND)

After applying power or after reset the INTC-Q enters NT1 mode.

2.2 Test Modes

2.2.1 µP Mode

In µP mode the test modes can either be programmed with the UMOD register and the SMOD register or be set via pin strapping as follows:

Pin $\overline{TM}$ tied to GND enables the test modes and disables the access to the µP interface. The pins TM0-2 are then used to select the different test modes as given in **table 1**. They are valid for both the µP-NT mode and the µP-TE mode. If the selected test mode differs from normal operation the pin setting overwrites the register content.

Table 1
Tests Modes µP Mode

$\overline{TM}$	TM0	TM1	TM2	U-transceiver	S-transceiver
1	AD0	AD1	AD2	normal operation, µP interface enabled	
0	0	0	0	Quiet Mode	normal operation
0	0	0	1	reserved	
0	0	1	0	normal operation	Test Mode 2
0	0	1	1		Test Mode 1
0	1	0	0	reserved	
0	1	0	1	Data Through	normal operation
0	1	1	0	Send Single Pulses	
0	1	1	1	normal operation, µP interface disabled	

In Test Mode 1 the S-transceiver transmits pseudo-ternary pulses at a rate of 2 kHz. In Test Mode 2 pseudo-ternary pulses at a rate of 96 kHz are transmitted.

Send Single Pulses requests the transmission of single pulses on the U-interface. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs.

Data Through forces the U-transceiver into the transparent state where it transmitts signal SN3T.

Quiet Mode sets the U-transceiver in Quiet Mode as defined in ANSI T1.601.

The IOM®-2 interface can be enabled and disabled via register OM. The data outputs can be programmed to be either open drain or tristate in the ADF2 register.

2.2.2 NT1 Mode

Pin $\overline{TM}$ tied to GND enables the test modes and pins TM0-2 are used to select the different test modes as given in **table 1**.

Table 2
Test Modes NT1 Mode

$\overline{TM}$	TM0	TM1	TM2	U-transceiver	S-transceiver
1	x[1)]	x	x	normal operation, IOM®-2 interface disabled	
0	0	0	0	Quiet Mode	normal operation
0	0	0	1	reserved	
0	0	1	0	normal operation	Test Mode 2
0	0	1	1		Test Mode 1
0	1	0	0	reserved	
0	1	0	1	Data Through	normal operation
0	1	1	0	Send Single Pulses	
0	1	1	1	normal operation, IOM®-2 interface active	

1) 'x' means: don't care

The status of the IOM®-2 interface depends on the setting of pin DCLSEL.

DCL = 512 kHz (pin DCLSEL = 1)

The IOM®-2 interface is generally disabled to minimize power consumption. The data lines DD and DU can be left open. $\overline{TM}$=0 and TM0-2='111' enable the IOM®-2 interface for test purposes. Two cases are to be distinguished:

a) Pin $\overline{DDU}$ = 1
The IOM®-2 pins DD and DU are output pins (push-pull). This allows monitoring of the communication between the U- and the S-transceiver in an NT1 application.

b) Pin $\overline{DDU}$ = 0
IOM®-2 pin DD is an output (push-pull) and DU is an input. The chip-internal data output of the S-transceiver is disabled. In this configuration the U-transceiver of the INTC-Q is controlled via the IOM®-2 interface. Therefore, it is possible to test the U-transceiver (e.g. bit error rates) with the same test equipment as used for the IEC-Q. Internal registers of the U-transceiver can be programmed and read via the Monitor channel of the IOM®-2 interface.

DCL = 1.536 MHz (pin DCLSEL = 0)

The IOM®-2 interface is always active if DCLSEL = 0. The IOM®-2 data lines DD and DU are open drain in/outputs. Pin ICS selects the IOM®-2 channel of the S-transceiver. ICS=0 maps the S-transceiver to IOM®-2 channel 1, ICS=1 maps it to channel 0.

2.3 Microprocessor Interface

The parallel/serial microprocessor interface can be selected to be either of the

1. Siemens/Intel **non-multiplexed** bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$
2. Siemens/Intel **multiplexed** address/data bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE
3. Motorola type with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$
4. Serial mode using control signals CDIN, CDOUT, CCLK and $\overline{CS}$.

The selection is performed via pins ALE/CCLK and SMODE as follows:

ALE tied to GND => 1.

ALE tied to VDD => 3.

Edge on ALE => 2. (pin SMODE tied to GND) or 4. (pin SMODE tied to VDD)

The occurrence of an edge on ALE/CCLK, either positive or negative, at any time during the operation immediately selects interface type 2 or 4. A return to one of the other interface types is possible only if a hardware reset is issued.

2.3.1 Microprocessor Clock Output

The microprocessor clock is provided in µP mode on the MCLK-output. Four clock rates are provided by a programmable prescaler. These are 7.68 MHz, 3.84 MHz, 1.92 MHz and 0.96 MHz. Switching between the clock rates is realized without spikes. The oscillator remains active all the time. The clock is synchronized to the 15.36 MHz clock at the XIN pin.

2.3.2 Reset Logic and Watchdog Timer

The INTC-Q provides a low active reset output (pin $\overline{RST}$) which is controlled by a watchdog timer, the power-on reset and the reset input (pin $\overline{RES}$).

After the microcontroller has enabled the watchdog timer it has to write the bit patterns ’10” and ’01” in a register within a period of 128 ms. If it fails to do so, a reset signal at pin $\overline{RST}$ and an interrupt are generated. The clock at pin MCLK remains active during this reset.

2.4 LED

An LED can be connected to pin $\overline{\text{ACT}}$ to display four different states (off, slow flashing, fast flashing, on).

In µP mode the LED status is programmable via two bits. It may be used to display the activation status, the power availability or for any customer specific purposes.

In NT1 mode the LED displays the activation status of the U-and S-transceiver according to **table 3**.

Table 3
LED states in NT1 mode

Pin $\overline{\text{ACT}}$	LED	U- and S-interface states
high Z	off	S- and U-interface deactivated
8Hz	8Hz	U activating or problem on U
1Hz	1Hz	U active; S activating or problem on S
GND	on	S and U activated

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEB PEF	T_A T_A	0 to 70 – 40 to 85	°C °C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Power Consumption

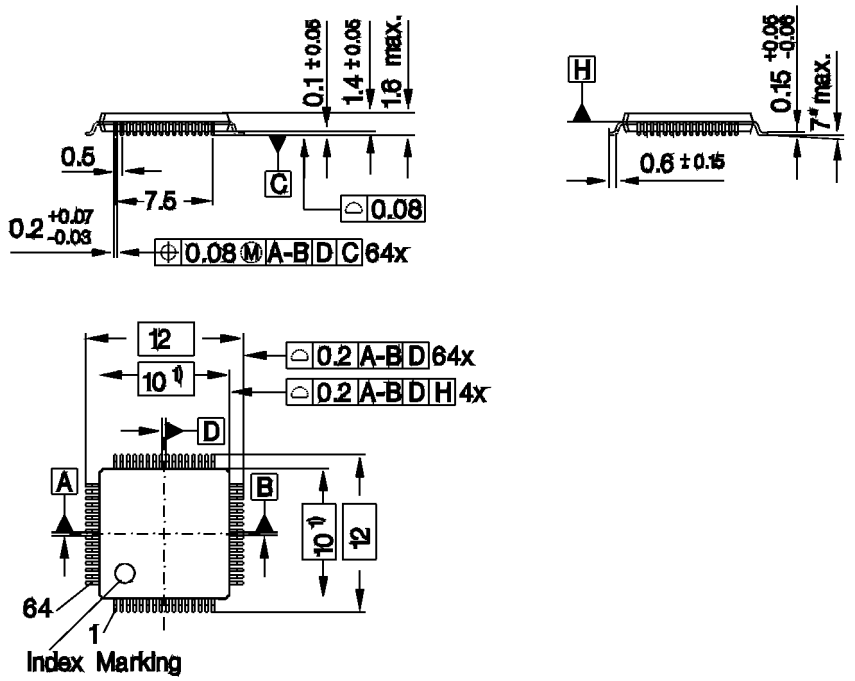
All values are preliminary.

Power Consumption

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
Intelligent NT application all interfaces and functions enabled (S, U, HDLC, IOM®-2 , µP) Operational Power Down		 380 47		 mW mW	VDD=5V, VSS=0V. Inputs at VSS/VDD, No output loads except SX1,2 (50Ohm) and AOUT,BOUT (98Ohm), 50% bin. zeros no LED connected, pin MTI open
Intelligent NT, restricted power (S disabled, others enabled) Operational		 325		 mW	
NT1 (only S and U enabled) Operational Power Down		 355 41		 mW mW	

4 Package Outlines

Plastic Package, T-QFP 64
(Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.
SMD = Surface Mounted Device

Dimensions in mm