RX21A Group
Renesas MCUs

R01DS0129EJ0110
Rev.1.10
Aug 28, 2014

50-MHz 32-bit RX MCUs, 78 DMIPS, 24-bit ΔΣ A/D Converter, up to 512-KB flash memory, IrDA, 10-bit A/D, 10-bit D/A, DEU, ELC, MPC, RTC; up to 9 comms interfaces

Features

■ 32-bit RX CPU core
- Max. operating frequency: 50 MHz
  Capable of 78 DMIPS in operation at 50 MHz
- Accumulator handles 64-bit results (for a single instruction) from 32- × 32-bit operations
- Multiplication and division unit handles 32- × 32-bit operations (multiplication instructions take one CPU clock cycle)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- Memory protection unit
- On-chip debugging circuit

■ Low power design and architecture
- Operation from a single 1.8-V to 3.6-V supply
  (2.7 V to 3.6 V for the ΔΣ A/D converter operating voltage)
- Deep software standby mode with RTC remaining usable
- Four low power modes

■ 24-bit ΔΣ A/D Converter
- SNDR = 85dB
- Seven ΔΣ converter units available. Seven channels can be operated simultaneously or independently.
- Up to x 64 PGA gain for differential input

■ On-chip flash memory for code, no wait states
- 50-MHz operation, 20-ns read cycle
- No wait states for reading at full CPU speed
- 256-K to 512-Kbyte capacities
- User code programmable via the SCI
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory
- 8 Kbytes
  (Number of times of reprogramming: 100,000)
- Erasing and programming impose no load on the CPU.

■ On-chip SRAM, no wait states
- 32-K to 64-Kbyte size capacities

■ DMA
- DMAC: Incorporates four channels
- DTC: Four transfer modes

■ Reset and supply management
- Nine types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- Frequency of external clock: Up to 20 MHz
- Frequency of the oscillator for sub-clock generation: 32.768 kHz
- PLL circuit input: 4 MHz to 12.5 MHz
- On-chip low- and high-speed oscillators, dedicated on-chip low-speed oscillator for the IWDT
- Generation of a dedicated 32.768-kHz clock for the RTC
- Clock frequency accuracy measurement circuit (CAC)

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Year and month display or 32-bit second display (binary counter) is selectable
- Time capture on event-signal input through external pins
- RTC capable of initiating return from deep software standby mode

PLQP0100KB-A 14 × 14 mm, 0.5-mm pitch
PLQP0080KB-A 12 × 12 mm, 0.5-mm pitch
PLQP0064KB-A 10 × 10 mm, 0.5-mm pitch
PTLG0100JA-A 7×7mm, 0.65-mm pitch

■ Independent watchdog timer
- 125-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock-frequency accuracy-measurement circuit, independent watchdog timer, functions to assist in RAM testing, etc.

■ Up to nine communications channels
- SCI with many useful functions (up to five channels)
  Asynchronous mode, clock synchronous mode, smart card interface
- IrDA Interface (one channel, in cooperation with the SCI5)
- I^2C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (two channels)
- RSPI (two channels)

■ Up to 14 extended-function timers
- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (four channels)

■ 10-bit A/D converter
- Conversion time 2.0 µs
- Self-diagnostic function and analog input disconnection detection assistance function

■ 10-bit D/A converter

■ Analog comparator

■ General I/O ports
- 5-V tolerant, open drain, input pull-up, switching of driving ability

■ MPC
- Multiple locations are selectable for I/O pins of peripheral functions

■ ELC
- Module operation can be initiated by event signals without going through interrupts.
- Modules can operate while the CPU is sleeping.

■ DEU
- Encryption and decryption of AES
- 128-, 192-, or 256-bit key length
- ECB/CBC Mode

■ Temperature sensor

■ Operating temp. range
- –40°C to +85°C
- –40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 shows the outline of the specifications and Table 1.2 shows the comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
Memory	ROM	• Capacity: 256 K/384 K/512 Kbytes • 50 MHz, no-wait memory access • On-board programming: 3 types
	RAM	• Capacity:32 K/64 Kbytes • 50 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLK):25 MHz (at max.) The flash peripheral circuit runs in synchronization with the flash peripheral clock (FCLK): 25 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 2 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 9 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 9 levels
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A, middle-speed operating mode 2B, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 122 • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (2 / 4)

Classification	Module/Function	Description
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin/80-pin/64-pin • I/O pin: 66/51/38 • Input: 1/1/1 • Pull-up resistors: 66/51/38 • Open-drain outputs: 47/37/28 • 5-V tolerance: 6/6/2
Event link controller (ELC)		• Event signals of 69 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		• Capable of selecting input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits x 6 channels) x 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels. • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion
	Port output enable2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	8-bit timer (TMR)	• (8 bits x 2 channels) x 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5 and SCI6
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits x 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits x 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCc)	• Clock source: Sub-clock • Time count or 32-bit binary count in second units basis selectable • Time/calendar • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values

Table 1.1 Outline of Specifications (3 / 4)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIc)	• 5 channels (channel 1, 5, 6, 8, 9) (including one channel for IrDA) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5 and SCI6) • Simple IIC • Simple SPI
	IrDA interface (IRDA)	• 1 channel (SCI5 is used) • Supports encoding/decoding the waveforms conforming to the IrDA specification version 1.0
	I^2C bus interface (RIIC)	• 2 channels • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the fast mode
	Serial peripheral interface (RSPI)	• 2 channels • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
24-bit ΔΣ A/D converter (DSAD)		• 7 channels: 4-channel differential input for current; 3-channel single-ended input for voltage • x 1 to x 64 PGA for differential input side for current and x 1 to x 4 PGA for single-ended input side for voltage • Minimum conversion time: 81.92 µs (A/D conversion clock: 25 MHz)
10-bit A/D converter (AD)		• 10 bits (7 channels x 1 unit) • 10-bit resolution • Conversion time: 2.0 µs per channel (A/D conversion clock: 25 MHz) • Operating modes Scan mode (single scan mode and continuous scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • A/D conversion start conditions Conversion can be started by software, a conversion start trigger from a timer (MTU), an external trigger signal, a temperature sensor or ELC.
Temperature sensor (TEMPSa)		• Outputs the voltage that changes depending on the temperature • PGA gain switchable: Three levels according to the voltage range
D/A converter (DA)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Data encryption unit (DEU)*1		• Encryption and decryption of AES • 128-, 192-, or 256-bit key length • ECB or CBC mode
Comparator A (CMPA)		• 2 channels • Comparison of reference voltage and analog input voltage
Comparator B (CMPB)		• 2 channels • Comparison of reference voltage and analog input voltage
Data operating circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltage/ Operating frequency		VCC = 1.8 to 3.6 V: 25 MHz, VCC = 2.7 to 3.6 V: 50 MHz
Supply current		8.6mA@50MHz (typ)
Operating temperature		D version: –40 to +85°C, G version: –40 to +105°C*2, *3

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
Package		100-pin LQFP (PLQP0100KB-A) 14 x 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 x 12mm, 0.5-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 x 10mm, 0.5-mm pitch 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch
On-chip debugging system		E1 emulator (FINE interfaces)

Note 1. Contact a Renesas Electronics sales office for more information.
Note 2. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 3. The unique ID specification and the calibration functions of the temperature sensor and the 24-Bit ΔΣ A/D converter of these products differ from other products. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
Section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
Section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
Section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
Section 37.3, Using the Temperature Sensor
Section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX21A Group		
		100 Pins	80 Pins	64 Pins
Interrupt	External interrupts	NMI, IRQ0 to IRQ7		NMI, IRQ0 to IRQ2, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)		
	Data transfer controller	Supported		
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)		
	Port output enable 2	POE0# to POE3#, POE8#		
	8-bit timer	2 channels × 2 units		
	Compare match timer	2 channels × 2 units		
	Realtime clock	Supported		
	Watchdog timer	Supported		
	Independent watchdog timer	Supported		
Communication function	Serial communications interface	5 channels (SCI1, 5, 6, 8, 9) (including one channel for IrDA)		
	I^2C bus interface	2 channels		1 channel
	Serial peripheral interface	2 channels		
24-bit ΔΣ A/D converter		7 channels	4 channels	3 channels
10-bit A/D converter		7 channels (AN0 to AN6)		4 channels (AN0, AN1, AN4, AN5)
Temperature sensor		Supported		
D/A converter		2 channels		—
CRC calculator		Supported		
Data encryption unit		Supported		
Event link controller		Supported		
Comparator A		2 channels		1 channel
Comparator B		2 channels		
Package		100-pin LQFP 100-pin TFLGA	80-pin LQFP	64-pin LQFP

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating temperature
RX21A	R5F521A8BDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F521A8BDFN	PLQP0080KB-A					
	R5F521A8BDFM	PLQP0064KB-A					
	R5F521A8BDLJ	PTLG0100JA-A					
	R5F521A7BDFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BDFN	PLQP0080KB-A					
	R5F521A7BDFM	PLQP0064KB-A					
	R5F521A7BDLJ	PTLG0100JA-A					
	R5F521A6BDFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BDFN	PLQP0080KB-A					
	R5F521A6BDFM	PLQP0064KB-A					
	R5F521A6BDLJ	PTLG0100JA-A					
	R5F521A8BGFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +105°C *1, *2
	R5F521A8BGFN	PLQP0080KB-A					
	R5F521A8BGFM	PLQP0064KB-A					
	R5F521A7BGFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BGFN	PLQP0080KB-A					
	R5F521A7BGFM	PLQP0064KB-A					
	R5F521A6BGFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BGFN	PLQP0080KB-A					
	R5F521A6BGFM	PLQP0064KB-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 2. The unique ID specification and the calibration functions of the temperature sensor and the 24-Bit ΔΣ A/D converter of these products differ from other products. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
section 37.3, Using the Temperature Sensor
section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

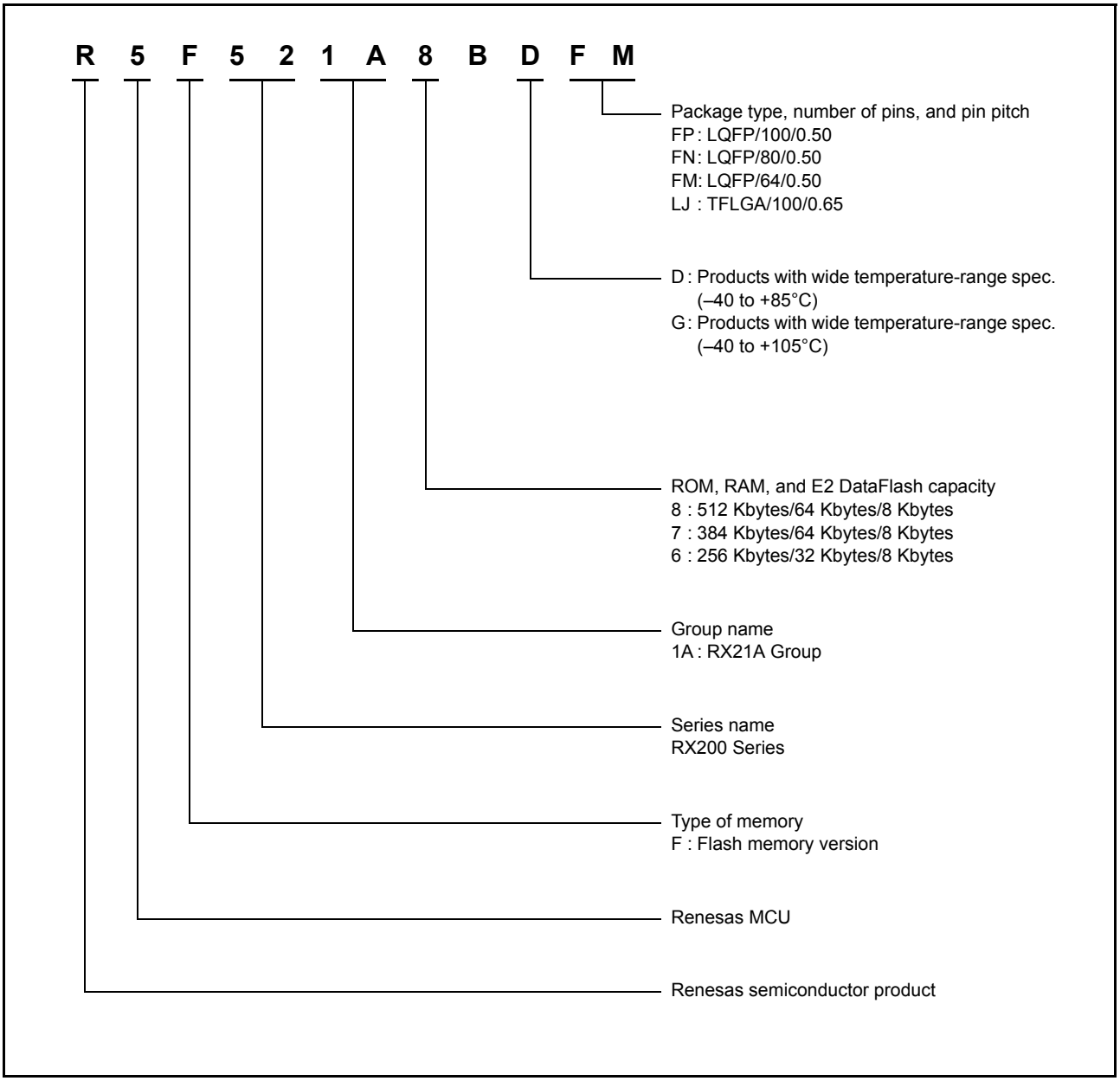
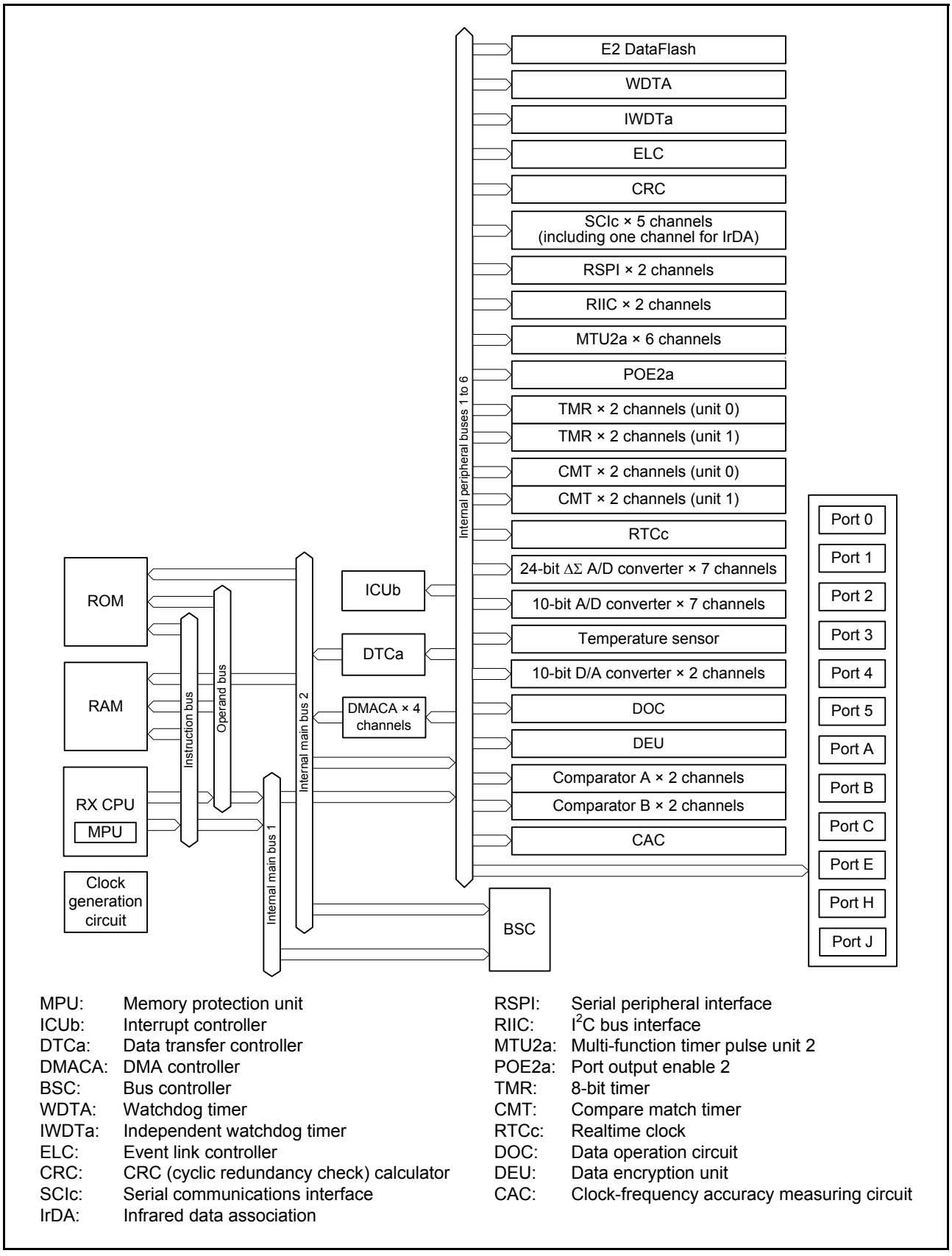


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.3 Block Diagram

Figure 1.2 shows a block diagram (100-pin package).



MPU: Memory protection unit
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIc: Serial communications interface
IrDA: Infrared data association

RSPI: Serial peripheral interface
RIIC: I^2C bus interface
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTCc: Realtime clock
DOC: Data operation circuit
DEU: Data encryption unit
CAC: Clock-frequency accuracy measuring circuit

Figure 1.2 Block Diagram (100-Pin Package)

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 0.1 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.
Realtime clock	RTCOUT	Output	Output pin for 1-Hz, 64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.

Table 1.4 Pin Functions (2 / 3)

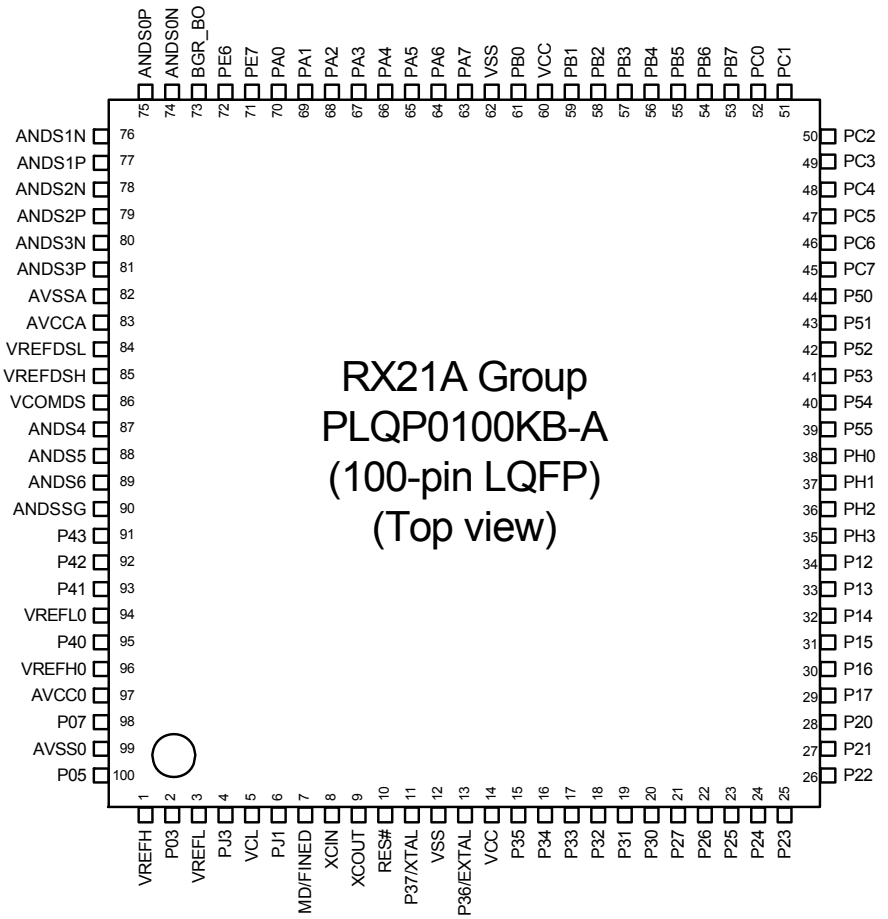
Classifications	Pin Name	I/O	Description
Serial communications interface	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data
	TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data
	CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception
	RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock
	SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmission of data
	SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmission of data
	SS1#, SS5#, SS6#, SS8#, SS9#	Input	Chip-select input pins
	• IrDA Interface		
	IRTXD5	Output	Data output pin in the IrDA format
	IRRXD5	Input	Data input pin in the IrDA format
I^2C bus interface	SCL0, SCL1	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open-drain output.
	SDA0, SDA1	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open-drain output.
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pin for the RSPI.
	MOSIA, MOSIB	I/O	Input or output data output from the master for the RSPI.
	MISOA, MISOB	I/O	Input or output data output from the slave for the RSPI.
	SSLA0, SSLB0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins to select the slave for the RSPI.
24-bit ΔΣ A/D converter	ANDS0N to ANDS3N, ANDS0P to ANDS3P	Input	Analog differential input pins for the ΔΣ A/D converter
	ANDS4 to ANDS6	Input	Analog single-ended input pins for the ΔΣ A/D converter
	ANDSSG	Input	Common signal ground pin for the analog single-ended inputs (ANDS4 to ANDS6) for the ΔΣ A/D converter
10-bit A/D converter	AN0 to AN6	Input	Input pin for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.

Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signals.
	CMPA2	Input	Input pin for the comparator A2 analog signals.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signals.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signals.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH0	Input	Reference voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
	AVCCA	Input	Analog voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VCC if the 24-bit ΔΣ A/D converter is not to be used.
	AVSSA	Input	Analog ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSH	—	Reference voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VREFDSL pin via a 1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSL	Input	Reference voltage ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VCOMDS	—	Common mode voltage pin for the 24-bit ΔΣ A/D converter. Connect this pin to the AVSSA pin via a 0.1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	BGR_BO	Input	Internal reference voltage input pin for the 24-bit ΔΣ A/D converter. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pins)
	P40 to P43	I/O	4-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE6, PE7	I/O	2-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3	I/O	2-bit input/output pins.

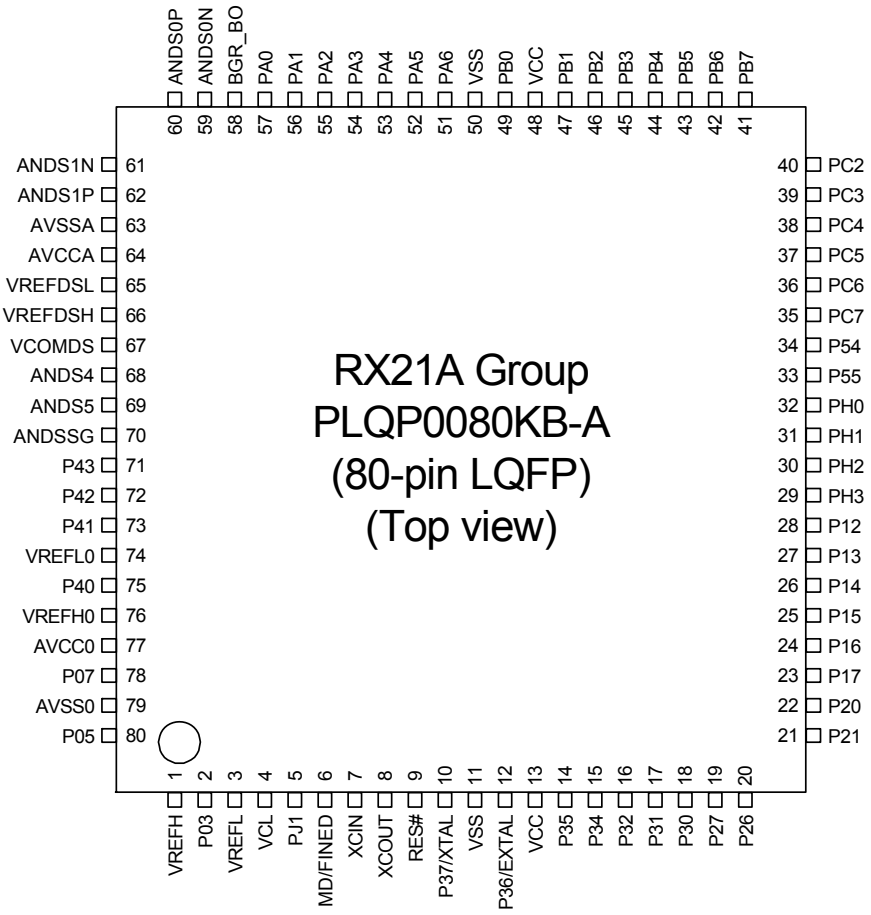
1.5 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments. Table 1.5 to Table 1.7 show the lists of pins and pin functions.



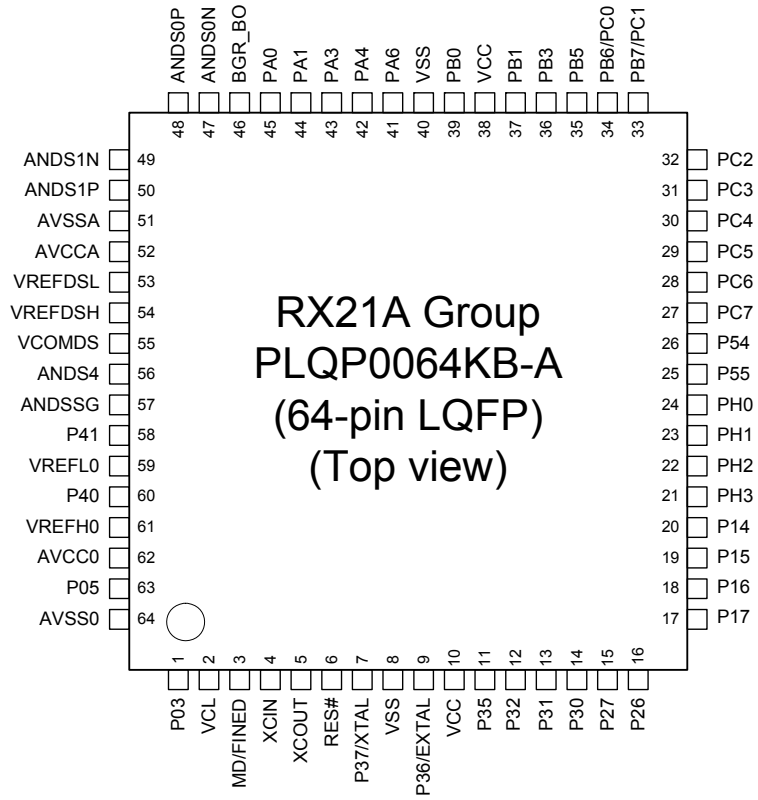
Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LQFP)”.

Figure 1.3 Pin Assignments of the 100-Pin LQFP



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LQFP)”.

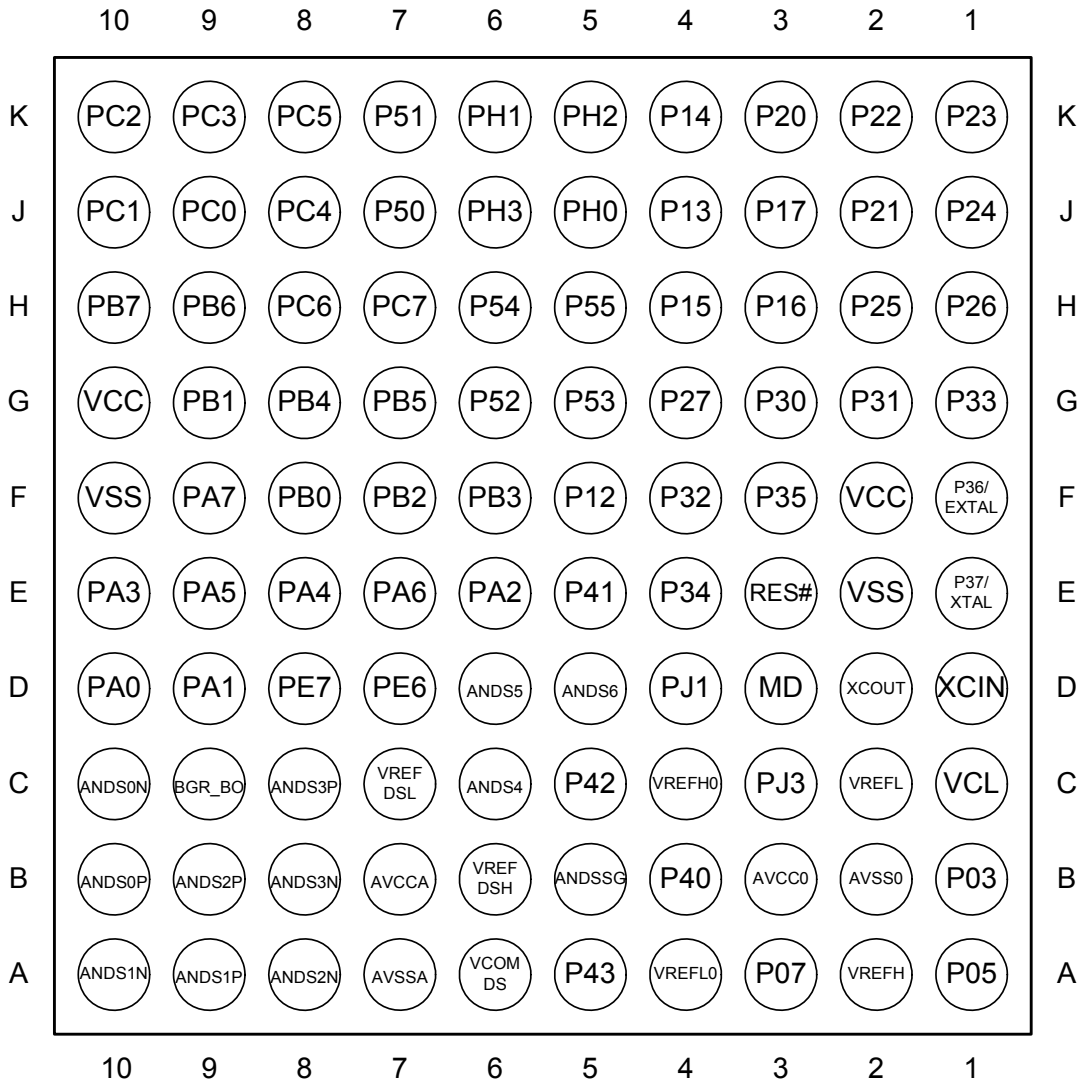
Figure 1.4 Pin Assignments of the 80-Pin LQFP



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LQFP)”.

Figure 1.5 Pin Assignments of the 64-Pin LQFP

RX21A Group
PTLG0100JA-A
(100-pin TFLGA)
(Upper perspective view)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
1	VREFH				
2		P03			AN4/DA0
3	VREFL				
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL				
6		PJ1	MTIOC3A		
7	MD				FINED
8	XCIN				
9	XCOUT				
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		P35			NMI
16		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
17		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
19		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
20		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS/RTCIC0
21		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
22		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB	
23		P25	MTIOC4C/MTCLKB		ADTRG0#
24		P24	MTIOC4A/MTCLKA/TMRI1		
25		P23	MTIOC3D/MTCLKD		
26		P22	MTIOC3B/MTCLKC/TMO0		
27		P21	MTIOC1B/TMCI0	SCL1	
28		P20	MTIOC1A/TMRI0	SDA1	
29		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
30		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0-DS	IRQ6/RTCOUT/ ADTRG0#
31		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13	MTIOC0B/TMO3	SDA0	IRQ3
34		P12	TMCI1	SCL0	IRQ2
35		PH3	TMCI0		
36		PH2	TMRI0		IRQ1
37		PH1	TMO0		IRQ0
38		PH0			CACREF
39		P55	MTIOC4D/TMO3		
40		P54	MTIOC4B/TMCI1		
41		P53			

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
42		P52		SSLB3	
43		P51		SSLB2	
44		P50		SSLB1	
45		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
47		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/ IRTXD5	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	
51		PC1	MTIOC3A	SCK5/SSLA2	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
56		PB4		CTS9#/RTS9#/SS9#	
57		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
58		PB2		CTS6#/RTS6#/SS6#	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
60	VCC				
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
62	VSS				
63		PA7		MISOA	
64		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
65		PA5		RSPCKA	
66		PA4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
68		PA2		RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	CMPA2
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
71		PE7		MISOB	IRQ7-DS
72		PE6		MOSIB	IRQ6
73	BGR_BO				
74					ANDS0N
75					ANDS0P
76					ANDS1N
77					ANDS1P
78					ANDS2N

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
79					ANDS2P
80					ANDS3N
81					ANDS3P
82	AVSSA				
83	AVCCA				
84	VREFDSL				
85	VREFDSH				
86	VCOMDS				
87					ANDS4
88					ANDS5
89					ANDS6
90	ANDSSG				
91		P43			AN3
92		P42			AN2
93		P41			AN1
94	VREFL0				
95		P40			AN0
96	VREFH0				
97	AVCC0				
98		P07			AN6/ADTRG0#
99	AVSS0				
100		P05			AN5/DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
1	VREFH				
2		P03			AN4/DA0
3	VREFL				
4	VCL				
5		PJ1	MTIOC3A		
6	MD				FINED
7	XCIN				
8	XCOUT				
9	RES#				
10	XTAL	P37			
11	VSS				
12	EXTAL	P36			
13	VCC				
14		P35			NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/MISOB	IRQ0-DS/RTCIC0
19		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/MOSIB	
21		P21	MTIOC1B/TMCI0	SCL1	
22		P20	MTIOC1A/TMRI0	SDA1	
23		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
24		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0-DS	IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
27		P13	MTIOC0B/TMO3	SDA0	IRQ3
28		P12	TMCI1	SCL0	IRQ2
29		PH3	TMCI0		
30		PH2	TMRI0		IRQ1
31		PH1	TMO0		IRQ0
32		PH0			CACREF
33		P55	MTIOC4D/TMO3		
34		P54	MTIOC4B/TMCI1		
35		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
37		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
38		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	
41		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
42		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
44		PB4		CTS9#/RTS9#/SS9#	
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
46		PB2		CTS6#/RTS6#/SS6#	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
48	VCC				
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	CMPB0
50	VSS				
51		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
52		PA5		RSPCKA	
53		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0	IRQ5-DS/CVREFB1
54		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/IRRXD5	IRQ6-DS/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	CMPA2
56		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
57		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
58	BGR_BO				
59					ANDS0N
60					ANDS0P
61					ANDS1N
62					ANDS1P
63	AVSSA				
64	AVCCA				
65	VREFDSL				
66	VREFDSH				
67	VCOMDS				
68					ANDS4
69					ANDS5
70	ANDSSG				
71		P43			AN3
72		P42			AN2
73		P41			AN1
74	VREFL0				
75		P40			AN0
76	VREFH0				
77	AVCC0				
78		P07			AN6/ADTRG0#
79	AVSS0				
80		P05			AN5/DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.7 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, RSPI, RIIC)	Others
1		P03			AN4
2	VCL				
3	MD				FINED
4	XCIN				
5	XCOUT				
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		P35			NMI
12		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
13		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
14		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS/RTCIC0
15		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB	
17		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
18		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0-DS	IRQ6/RTCOUT/ ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
21		PH3	TMCI0		
22		PH2	TMRI0		IRQ1
23		PH1	TMO0		IRQ0
24		PH0			CACREF
25		P55	MTIOC4D/TMO3		
26		P54	MTIOC4B/TMCI1		
27		PC7	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
29		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
30		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/ IRTXD5	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	
33		PB7/PC1	MTIOC3B	TXD9/SMOSI9/SSDA9	
34		PB6/PC0	MTIOC3D	RXD9/SMISO9/SSCL9	
35		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
36		PB3	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	

Table 1.7 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, RSPI, RIIC)	Others
37		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
38	VCC				
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
40	VSS				
41		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
42		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
45		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
46	BGR_BO				
47					ANDS0N
48					ANDS0P
49					ANDS1N
50					ANDS1P
51	AVSSA				
52	AVCCA				
53	VREFDSL				
54	VREFDSH				
55	VCOMDS				
56					ANDS4
57	ANDSSG				
58		P41			AN1
59	VREFL0				
60		P40			AN0
61	VREFH0				
62	AVCC0				
63		P05			AN5
64	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
A1		P05			AN5/DA1
A2	VREFH				
A3		P07			AN6/ADTRG0#
A4	VREFL0				
A5		P43			AN3
A6	VCOMDS				
A7	AVSSA				
A8					ANDS2N
A9					ANDS1P
A10					ANDS1N
B1		P03			AN4/DA0
B2	AVSS0				
B3	AVCC0				
B4		P40			AN0
B5	ANDSSG				
B6	VREFDSH				
B7	AVCCA				
B8					ANDS3N
B9					ANDS2P
B10					ANDS0P
C1	VCL				
C2	VREFL				
C3		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	
C4	VREFH0				
C5		P42			AN2
C6					ANDS4
C7	VREFDSL				
C8					ANDS3P
C9	BGR_BO				
C10					ANDS0N
D1	XCIN				
D2	XCOUT				
D3	MD				FINED
D4		PJ1	MTIOC3A		
D5					ANDS6
D6					ANDS5
D7		PE6		MOSIB	IRQ6
D8		PE7		MISOB	IRQ7-DS
D9		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D10		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
E1	XTAL	P37			
E2	VSS				
E3	RES#				
E4		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
E5		P41			AN1

Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
E6		PA2		RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	CMPA2
E7		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
E8		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
E9		PA5		RSPCKA	
E10		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
F1	EXTAL	P36			
F2	VCC				
F3		P35			NMI
F4		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
F5		P12	TMCI1	SCL0	IRQ2
F6		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
F7		PB2		CTS6#/RTS6#/SS6#	
F8		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
F9		PA7		MISOA	
F10	VSS				
G1		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
G2		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
G3		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS/RTCIC0
G4		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
G5		P53			
G6		P52		SSLB3	
G7		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
G8		PB4		CTS9#/RTS9#/SS9#	
G9		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
G10	VCC				
H1		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB	
H2		P25	MTIOC4C/MTCLKB		ADTRG0#
H3		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0-DS	IRQ6/RTCOUT/ ADTRG0#
H4		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
H5		P55	MTIOC4D/TMO3		
H6		P54	MTIOC4B/TMCI1		
H7		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
H8		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
H9		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
H10		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
J1		P24	MTIOC4A/MTCLKA/TMRI1		

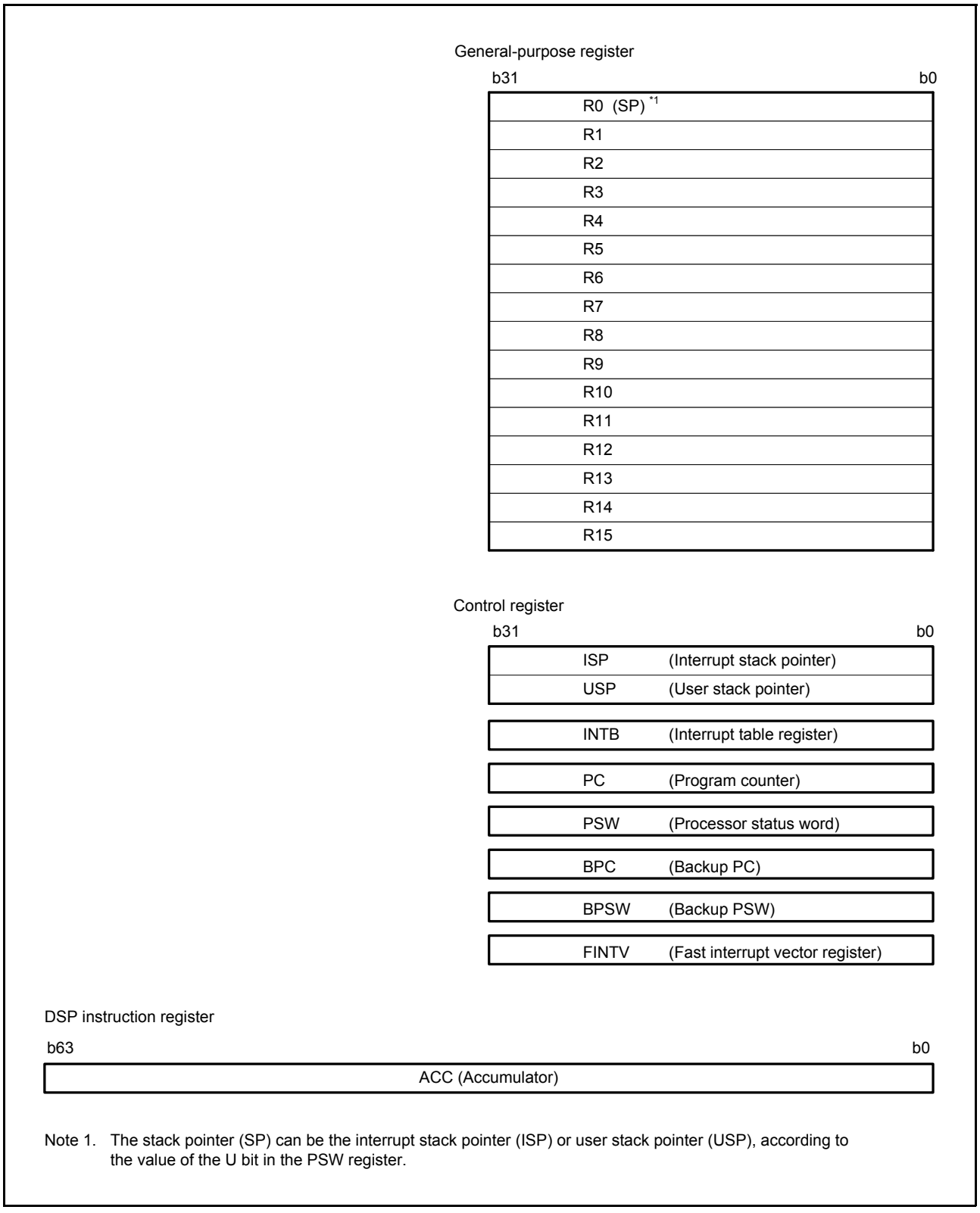
Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
J2		P21	MTIOC1B/TMCI0	SCL1	
J3		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
J4		P13	MTIOC0B/TMO3	SDA0	IRQ3
J5		PH0			CACREF
J6		PH3	TMCI0		
J7		P50		SSLB1	
J8		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
J9		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
J10		PC1	MTIOC3A	SCK5/SSLA2	
K1		P23	MTIOC3D/MTCLKD		
K2		P22	MTIOC3B/MTCLKC/TMO0		
K3		P20	MTIOC1A/TMRI0	SDA1	
K4		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
K5		PH2	TMRI0		IRQ1
K6		PH1	TMO0		IRQ0
K7		P51		SSLB2	
K8		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
K9		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/ IRTXD5	
K10		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

This CPU has the following eight control registers.

(1) Interrupt Stack Pointer (ISP) / User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

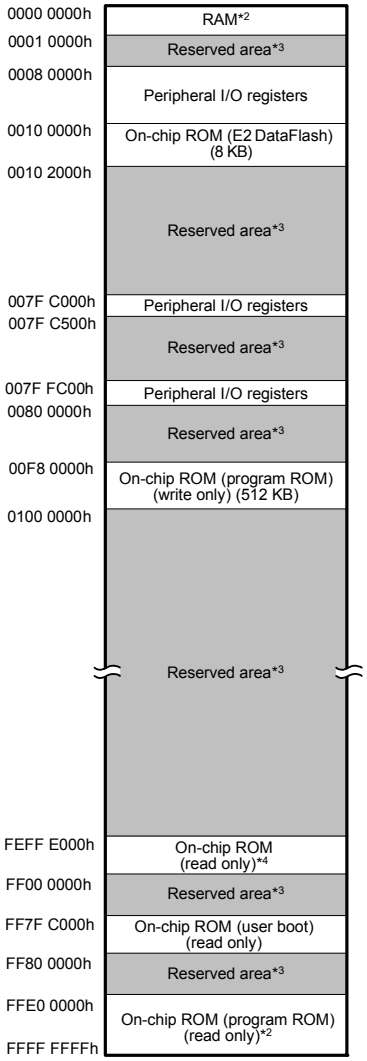
The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory map.

Single-chip mode*1



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh

Note:•See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.
Note 4. Only some specific addresses are usable. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
Section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
Section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
Section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
Section 37.3, Using the Temperature Sensor
Section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

Figure 3.1 Memory Map

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DMAC or DTC).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16		3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16		3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16		3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16		3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32		3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32		3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32		3 ICLK
0008 001Ch	SYSTEM	Module stop control register D	MSTPCRD	32	32		3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32		3 ICLK
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16		3 ICLK
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16		3 ICLK
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8		3 ICLK
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8		3 ICLK
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8		3 ICLK
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8		3 ICLK
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8		3 ICLK
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8		3 ICLK
0008 0037h	SYSTEM	High-speed on-chip oscillator control register 2	HOCOCR2	8	8		3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8		3 ICLK
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8		3 ICLK
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8		3 ICLK
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8		3 ICLK
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8		3 ICLK
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8		3 ICLK
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8		3 ICLK
0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8		3 ICLK
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8		3 ICLK
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16		3 ICLK
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8		3 ICLK
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8		3 ICLK
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8		3 ICLK
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8		3 ICLK
0008 03FEh	SYSTEM	Protect register	PRCR	16	16		3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8		2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8		2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8		2 ICLK
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (2 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32		2 ICLK
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16		2 ICLK
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8		2 ICLK
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8		2 ICLK
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32		2 ICLK
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16		2 ICLK
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8		2 ICLK
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8		2 ICLK
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32		2 ICLK
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32		2 ICLK
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16		2 ICLK
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8		2 ICLK
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8		2 ICLK
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2200h	DMAC	DMA module activation register	DMAST	8	8		2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8		2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32		2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8		2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8		2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16		2 ICLK
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32		1 ICLK
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32		1 ICLK
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32		1 ICLK
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32		1 ICLK
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32		1 ICLK
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32		1 ICLK
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32		1 ICLK
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32		1 ICLK
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32		1 ICLK
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32		1 ICLK
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32		1 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 642Ch	MPU	Region-5 end page number register	REPAGE5	32	32		1 ICLK
0008 6430h	MPU	Region-6 start page number register	RSPAGE6	32	32		1 ICLK
0008 6434h	MPU	Region-6 end page number register	REPAGE6	32	32		1 ICLK
0008 6438h	MPU	Region-7 start page number register	RSPAGE7	32	32		1 ICLK
0008 643Ch	MPU	Region-7 end page number register	REPAGE7	32	32		1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32		1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32		1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32		1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32		1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32		1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32		1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16		1 ICLK
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16		1 ICLK
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32		1 ICLK
0008 652Ch	MPU	Data-hit region register	MHITD	32	32		1 ICLK
0008 7010h	ICU	Interrupt request register 016	IR016	8	8		2 ICLK
0008 7015h	ICU	Interrupt request register 021	IR021	8	8		2 ICLK
0008 7017h	ICU	Interrupt request register 023	IR023	8	8		2 ICLK
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8		2 ICLK
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8		2 ICLK
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8		2 ICLK
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8		2 ICLK
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8		2 ICLK
0008 7020h	ICU	Interrupt request register 032	IR032	8	8		2 ICLK
0008 7021h	ICU	Interrupt request register 033	IR033	8	8		2 ICLK
0008 7022h	ICU	Interrupt request register 034	IR034	8	8		2 ICLK
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8		2 ICLK
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8		2 ICLK
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8		2 ICLK
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8		2 ICLK
0008 7030h	ICU	Interrupt request register 048	IR048	8	8		2 ICLK
0008 7031h	ICU	Interrupt request register 049	IR049	8	8		2 ICLK
0008 7032h	ICU	Interrupt request register 050	IR050	8	8		2 ICLK
0008 7033h	ICU	Interrupt request register 051	IR051	8	8		2 ICLK
0008 7039h	ICU	Interrupt request register 057	IR057	8	8		2 ICLK
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8		2 ICLK
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8		2 ICLK
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8		2 ICLK
0008 7040h	ICU	Interrupt request register 064	IR064	8	8		2 ICLK
0008 7041h	ICU	Interrupt request register 065	IR065	8	8		2 ICLK
0008 7042h	ICU	Interrupt request register 066	IR066	8	8		2 ICLK
0008 7043h	ICU	Interrupt request register 067	IR067	8	8		2 ICLK
0008 7044h	ICU	Interrupt request register 068	IR068	8	8		2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8		2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8		2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8		2 ICLK
0008 7058h	ICU	Interrupt request register 088	IR088	8	8		2 ICLK
0008 7059h	ICU	Interrupt request register 089	IR089	8	8		2 ICLK
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8		2 ICLK
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8		2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (4 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8		2 ICLK
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8		2 ICLK
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8		2 ICLK
0008 706Dh	ICU	Interrupt request register 109	IR109	8	8		2 ICLK
0008 7072h	ICU	Interrupt request register 114	IR114	8	8		2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8		2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8		2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8		2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8		2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8		2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8		2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8		2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8		2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8		2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8		2 ICLK
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8		2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8		2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8		2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8		2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8		2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8		2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8		2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8		2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8		2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8		2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8		2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8		2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8		2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8		2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8		2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8		2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8		2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8		2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8		2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8		2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8		2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8		2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8		2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8		2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8		2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8		2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8		2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8		2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8		2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8		2 ICLK
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8		2 ICLK
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8		2 ICLK
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8		2 ICLK
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8		2 ICLK
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8		2 ICLK
0008 70CEh	ICU	Interrupt request register 206	IR206	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (5 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 70CFh	ICU	Interrupt request register 207	IR207	8	8		2 ICLK
0008 70D0h	ICU	Interrupt request register 208	IR208	8	8		2 ICLK
0008 70D1h	ICU	Interrupt request register 209	IR209	8	8		2 ICLK
0008 70D2h	ICU	Interrupt request register 210	IR210	8	8		2 ICLK
0008 70D3h	ICU	Interrupt request register 211	IR211	8	8		2 ICLK
0008 70D4h	ICU	Interrupt request register 212	IR212	8	8		2 ICLK
0008 70D5h	ICU	Interrupt request register 213	IR213	8	8		2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8		2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8		2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8		2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8		2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8		2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8		2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8		2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8		2 ICLK
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8		2 ICLK
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8		2 ICLK
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8		2 ICLK
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8		2 ICLK
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8		2 ICLK
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8		2 ICLK
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8		2 ICLK
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8		2 ICLK
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8		2 ICLK
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8		2 ICLK
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8		2 ICLK
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8		2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8		2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8		2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8		2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8		2 ICLK
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8		2 ICLK
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8		2 ICLK
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8		2 ICLK
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8		2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8		2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8		2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8		2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8		2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8		2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8		2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8		2 ICLK
0008 7131h	ICU	DTC activation enable register 049	DTCER049	8	8		2 ICLK
0008 7132h	ICU	DTC activation enable register 050	DTCER050	8	8		2 ICLK
0008 713Ah	ICU	DTC activation enable register 058	DTCER058	8	8		2 ICLK
0008 713Bh	ICU	DTC activation enable register 059	DTCER059	8	8		2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8		2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8		2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8		2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8		2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8		2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8		2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8		2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8		2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8		2 ICLK
0008 716Bh	ICU	DTC activation enable register 107	DTCER107	8	8		2 ICLK
0008 716Ch	ICU	DTC activation enable register 108	DTCER108	8	8		2 ICLK
0008 716Dh	ICU	DTC activation enable register 109	DTCER109	8	8		2 ICLK
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8		2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8		2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8		2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8		2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8		2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8		2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8		2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8		2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8		2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8		2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8		2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8		2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8		2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8		2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8		2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8		2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8		2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8		2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8		2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8		2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8		2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8		2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8		2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8		2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8		2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8		2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8		2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8		2 ICLK
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8		2 ICLK
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8		2 ICLK
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8		2 ICLK
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8		2 ICLK
0008 71CFh	ICU	DTC activation enable register 207	DTCER207	8	8		2 ICLK
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8		2 ICLK
0008 71D1h	ICU	DTC activation enable register 209	DTCER209	8	8		2 ICLK
0008 71D2h	ICU	DTC activation enable register 210	DTCER210	8	8		2 ICLK
0008 71D3h	ICU	DTC activation enable register 211	DTCER211	8	8		2 ICLK
0008 71D4h	ICU	DTC activation enable register 212	DTCER212	8	8		2 ICLK
0008 71D5h	ICU	DTC activation enable register 213	DTCER213	8	8		2 ICLK
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8		2 ICLK
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8		2 ICLK
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8		2 ICLK
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8		2 ICLK
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8		2 ICLK
0008 71E7h	ICU	DTC activation enable register 231	DTCER231	8	8		2 ICLK
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8		2 ICLK
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8		2 ICLK
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8		2 ICLK
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8		2 ICLK
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8		2 ICLK
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8		2 ICLK
0008 71FCh	ICU	DTC activation enable register 252	DTCER252	8	8		2 ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8		2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8		2 ICLK
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8		2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8		2 ICLK
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8		2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8		2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8		2 ICLK
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8		2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8		2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8		2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8		2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8		2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8		2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8		2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8		2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8		2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8		2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8		2 ICLK
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8		2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8		2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8		2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8		2 ICLK
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8		2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8		2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8		2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8		2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16		2 ICLK
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8		2 ICLK
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8		2 ICLK
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8		2 ICLK
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8		2 ICLK
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8		2 ICLK
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8		2 ICLK
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8		2 ICLK
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8		2 ICLK
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8		2 ICLK
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8		2 ICLK
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8		2 ICLK
0008 732Ch	ICU	Interrupt source priority register 044	IPR044	8	8		2 ICLK
0008 7330h	ICU	Interrupt source priority register 048	IPR048	8	8		2 ICLK
0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 733Ah	ICU	Interrupt source priority register 058	IPR058	8	8		2 ICLK
0008 733Bh	ICU	Interrupt source priority register 059	IPR059	8	8		2 ICLK
0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8		2 ICLK
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8		2 ICLK
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8		2 ICLK
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8		2 ICLK
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8		2 ICLK
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8		2 ICLK
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8		2 ICLK
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8		2 ICLK
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8		2 ICLK
0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8		2 ICLK
0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8		2 ICLK
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8		2 ICLK
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8		2 ICLK
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8		2 ICLK
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8		2 ICLK
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8		2 ICLK
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8		2 ICLK
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8		2 ICLK
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8		2 ICLK
0008 7376h	ICU	Interrupt source priority register 118	IPR118	8	8		2 ICLK
0008 7379h	ICU	Interrupt source priority register 121	IPR121	8	8		2 ICLK
0008 737Bh	ICU	Interrupt source priority register 123	IPR123	8	8		2 ICLK
0008 737Dh	ICU	Interrupt source priority register 125	IPR125	8	8		2 ICLK
0008 737Fh	ICU	Interrupt source priority register 127	IPR127	8	8		2 ICLK
0008 7381h	ICU	Interrupt source priority register 129	IPR129	8	8		2 ICLK
0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8		2 ICLK
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8		2 ICLK
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8		2 ICLK
0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8		2 ICLK
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8		2 ICLK
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8		2 ICLK
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8		2 ICLK
0008 73CFh	ICU	Interrupt source priority register 207	IPR207	8	8		2 ICLK
0008 73D0h	ICU	Interrupt source priority register 208	IPR208	8	8		2 ICLK
0008 73D1h	ICU	Interrupt source priority register 209	IPR209	8	8		2 ICLK
0008 73D2h	ICU	Interrupt source priority register 210	IPR210	8	8		2 ICLK
0008 73D3h	ICU	Interrupt source priority register 211	IPR211	8	8		2 ICLK
0008 73D4h	ICU	Interrupt source priority register 212	IPR212	8	8		2 ICLK
0008 73D5h	ICU	Interrupt source priority register 213	IPR213	8	8		2 ICLK
0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8		2 ICLK
0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8		2 ICLK
0008 73FBh	ICU	Interrupt source priority register 251	IPR251	8	8		2 ICLK
0008 73FCh	ICU	Interrupt source priority register 252	IPR252	8	8		2 ICLK
0008 73FDh	ICU	Interrupt source priority register 253	IPR253	8	8		2 ICLK
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8		2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8		2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8		2 ICLK
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8		2 ICLK
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	8	8		2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK
0008 8036h	IWDT	IWDT reset control register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8038h	IWDT	IWDT count stop control register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK
0008 80C0h	DA	D/A data register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK
0008 80C2h	DA	D/A data register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK
0008 80C4h	DA	D/A control register	DACR	8	8	2, 3 PCLKB	2 ICLK
0008 80C5h	DA	DADRm format select register	DADPR	8	8	2, 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer counter control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time constant register A	TCORA	8	8*1	2, 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time constant register B	TCORB	8	8*1	2, 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer counter	TCNT	8	8*1	2, 3 PCLKB	2 ICLK
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8*1	2, 3 PCLKB	2 ICLK
0008 820Ch	TMR0	Time count start register	TCSTR	8	8	2, 3 PCLKB	2 ICLK
0008 8210h	TMR2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8211h	TMR3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
0008 8215h	TMR3	Time constant register A	TCORA	8	8*1	2, 3 PCLKB	2 ICLK
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
0008 8217h	TMR3	Time constant register B	TCORB	8	8*1	2, 3 PCLKB	2 ICLK
0008 8218h	TMR2	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
0008 8219h	TMR3	Timer counter	TCNT	8	8*1	2, 3 PCLKB	2 ICLK
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8*1	2, 3 PCLKB	2 ICLK
0008 821Ch	TMR2	Time count start register	TCSTR	8	8	2, 3 PCLKB	2 ICLK
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Timeout internal counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Timeout internal counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8320h	RIIC1	I2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
0008 8321h	RIIC1	I2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8322h	RIIC1	I2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
0008 8323h	RIIC1	I2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
0008 8324h	RIIC1	I2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
0008 8325h	RIIC1	I2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
0008 8326h	RIIC1	I2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
0008 8327h	RIIC1	I2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
0008 8328h	RIIC1	I2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
0008 8329h	RIIC1	I2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Timeout internal counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Timeout internal counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8330h	RIIC1	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8331h	RIIC1	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8332h	RIIC1	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8333h	RIIC1	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA control register	IRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK
0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK
0008 8632h	MTU	Timer buffer transfer set register	TBTER	8	8	2, 3 PCLKB	2 ICLK
0008 8634h	MTU	Timer dead time enable register	TDER	8	8	2, 3 PCLKB	2 ICLK
0008 8636h	MTU	Timer output level buffer register	TOLBR	8	8	2, 3 PCLKB	2 ICLK
0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2, 3 PCLKB	2 ICLK
0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2, 3 PCLKB	2 ICLK
0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2, 3 PCLKB	2 ICLK
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK
0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK
0008 8724h	MTU0	Timer interrupt enable register 2	TIER2	8	8	2, 3 PCLKB	2 ICLK
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK
0008 8900h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8902h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8908h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK
0008 9800h	AD	A/D control register	ADCSR	16	16	2, 3 PCLKB	2 ICLK
0008 9804h	AD	A/D channel select register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK
0008 9808h	AD	A/D-converted value addition mode select register	ADADS	16	16	2, 3 PCLKB	2 ICLK
0008 980Ch	AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK
0008 980Eh	AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK
0008 9810h	AD	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK
0008 9812h	AD	A/D-converted extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK
0008 981Ah	AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK
0008 981Ch	AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK
0008 981Eh	AD	A/D self-diagnosis data register	ADRD	16	16	2, 3 PCLKB	2 ICLK
0008 9820h	AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK
0008 9822h	AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK
0008 9824h	AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK
0008 9826h	AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK
0008 9828h	AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK
0008 982Ah	AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK
0008 982Ch	AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK
0008 9860h	AD	A/D sampling state register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK
0008 9870h	AD	A/D sampling state register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK
0008 9871h	AD	A/D sampling state register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK
0008 9873h	AD	A/D sampling state register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK
0008 9874h	AD	A/D sampling state register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK
0008 9875h	AD	A/D sampling state register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK
0008 9876h	AD	A/D sampling state register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK
0008 9877h	AD	A/D sampling state register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK
0008 9878h	AD	A/D sampling state register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 907Ah	AD	A/D disconnecting detection control register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A029h	SCI1	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ah	SCI1	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C9h	SCI6	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B101h	ELC	Event link setting register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B106h	ELC	Event link setting register 5	ELSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event link setting register 14	ELSR14	8	8	2, 3 PCLKB	2 ICLK
0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (17 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 B11Bh	ELC	Event link setting register 26	ELSR26	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ch	ELC	Event link setting register 27	ELSR27	8	8	2, 3 PCLKB	2 ICLK
0008 B11Dh	ELC	Event link setting register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK
0008 B11Eh	ELC	Event link setting register 29	ELSR29	8	8	2, 3 PCLKB	2 ICLK
0008 B11Fh	ELC	Event link option setting register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK
0008 B120h	ELC	Event link option setting register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK
0008 B121h	ELC	Event link option setting register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK
0008 B122h	ELC	Event link option setting register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK
0008 B123h	ELC	Port group setting register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK
0008 B124h	ELC	Port group setting register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK
0008 B125h	ELC	Port group control register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK
0008 B126h	ELC	Port group control register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK
0008 B127h	ELC	Port buffer register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK
0008 B128h	ELC	Port buffer register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK
0008 B129h	ELC	Event link port setting register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK
0008 B12Ah	ELC	Event link port setting register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK
0008 B12Bh	ELC	Event link port setting register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK
0008 B12Ch	ELC	Event link port setting register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK
0008 B12Dh	ELC	Event link software event generation register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK
0008 B130h	ELC	Event link port setting register 30	ELSR30	8	8	2, 3 PCLKB	2 ICLK
0008 B131h	ELC	Event link port setting register 31	ELSR31	8	8	2, 3 PCLKB	2 ICLK
0008 B132h	ELC	Event link port setting register 32	ELSR32	8	8	2, 3 PCLKB	2 ICLK
0008 B133h	ELC	Event link port setting register 33	ELSR33	8	8	2, 3 PCLKB	2 ICLK
0008 B134h	ELC	Event link port setting register 34	ELSR34	8	8	2, 3 PCLKB	2 ICLK
0008 B135h	ELC	Event link port setting register 35	ELSR35	8	8	2, 3 PCLKB	2 ICLK
0008 B136h	ELC	Event link port setting register 36	ELSR36	8	8	2, 3 PCLKB	2 ICLK
0008 B401h	DSAD	ΔΣ A/D reset register	DSADRSTR	8	8	2, 3 PCLKB	2 ICLK
0008 B402h	DSAD	ΔΣ A/D reference control register	DSADRCR	8	8	2, 3 PCLKB	2 ICLK
0008 B403h	DSAD	ΔΣ A/D control expansion register	DSADCER	8	8	2, 3 PCLKB	2 ICLK
0008 B410h	DSAD	ΔΣ A/D control register 0	DSADCR0	8	8	2, 3 PCLKB	2 ICLK
0008 B411h	DSAD	ΔΣ A/D control/status register 0	DSADCSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B412h	DSAD	ΔΣ A/D gain select register 0	DSADGSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B413h	DSAD	ΔΣ A/D overwrite flag register 0	DSADFR0	8	8	2, 3 PCLKB	2 ICLK
0008 B414h	DSAD	ΔΣ A/D data register 0	DSADDR0	32	32	2, 3 PCLKB	2 ICLK
0008 B418h	DSAD	ΔΣ A/D input select register 0	DSADISR0	8	8	2, 3 PCLKB	2 ICLK
0008 B420h	DSAD	ΔΣ A/D control register 1	DSADCR1	8	8	2, 3 PCLKB	2 ICLK
0008 B421h	DSAD	ΔΣ A/D control/status register 1	DSADCSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B422h	DSAD	ΔΣ A/D gain select register 1	DSADGSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B423h	DSAD	ΔΣ A/D overwrite flag register 1	DSADFR1	8	8	2, 3 PCLKB	2 ICLK
0008 B424h	DSAD	ΔΣ A/D data register 1	DSADDR1	32	32	2, 3 PCLKB	2 ICLK
0008 B428h	DSAD	ΔΣ A/D input select register 1	DSADISR1	8	8	2, 3 PCLKB	2 ICLK
0008 B430h	DSAD	ΔΣ A/D control register 2	DSADCR2	8	8	2, 3 PCLKB	2 ICLK
0008 B431h	DSAD	ΔΣ A/D control/status register 2	DSADCSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B432h	DSAD	ΔΣ A/D gain select register 2	DSADGSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B433h	DSAD	ΔΣ A/D overwrite flag register 2	DSADFR2	8	8	2, 3 PCLKB	2 ICLK
0008 B434h	DSAD	ΔΣ A/D data register 2	DSADDR2	32	32	2, 3 PCLKB	2 ICLK
0008 B438h	DSAD	ΔΣ A/D input select register 2	DSADISR2	8	8	2, 3 PCLKB	2 ICLK
0008 B440h	DSAD	ΔΣ A/D control register 3	DSADCR3	8	8	2, 3 PCLKB	2 ICLK
0008 B441h	DSAD	ΔΣ A/D control/status register 3	DSADCSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B442h	DSAD	ΔΣ A/D gain select register 3	DSADGSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B443h	DSAD	ΔΣ A/D overwrite flag register 3	DSADFR3	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 B444h	DSAD	ΔΣ A/D data register 3	DSADDR3	32	32	2, 3 PCLKB	2 ICLK
0008 B448h	DSAD	ΔΣ A/D input select register 3	DSADISR3	8	8	2, 3 PCLKB	2 ICLK
0008 B450h	DSAD	ΔΣ A/D control register 4	DSADCR4	8	8	2, 3 PCLKB	2 ICLK
0008 B451h	DSAD	ΔΣ A/D control/status register 4	DSADCSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B452h	DSAD	ΔΣ A/D gain select register 4	DSADGSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B453h	DSAD	ΔΣ A/D overwrite flag register 4	DSADFR4	8	8	2, 3 PCLKB	2 ICLK
0008 B454h	DSAD	ΔΣ A/D data register 4	DSADDR4	32	32	2, 3 PCLKB	2 ICLK
0008 B458h	DSAD	ΔΣ A/D input select register 4	DSADISR4	8	8	2, 3 PCLKB	2 ICLK
0008 B460h	DSAD	ΔΣ A/D control register 5	DSADCR5	8	8	2, 3 PCLKB	2 ICLK
0008 B461h	DSAD	ΔΣ A/D control/status register 5	DSADCSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B462h	DSAD	ΔΣ A/D gain select register 5	DSADGSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B463h	DSAD	ΔΣ A/D overwrite flag register 5	DSADFR5	8	8	2, 3 PCLKB	2 ICLK
0008 B464h	DSAD	ΔΣ A/D data register 5	DSADDR5	32	32	2, 3 PCLKB	2 ICLK
0008 B468h	DSAD	ΔΣ A/D input select register 5	DSADISR5	8	8	2, 3 PCLKB	2 ICLK
0008 B470h	DSAD	ΔΣ A/D control register 6	DSADCR6	8	8	2, 3 PCLKB	2 ICLK
0008 B471h	DSAD	ΔΣ A/D control/status register 6	DSADCSR6	8	8	2, 3 PCLKB	2 ICLK
0008 B472h	DSAD	ΔΣ A/D gain select register 6	DSADGSR6	8	8	2, 3 PCLKB	2 ICLK
0008 B473h	DSAD	ΔΣ A/D overwrite flag register 6	DSADFR6	8	8	2, 3 PCLKB	2 ICLK
0008 B474h	DSAD	ΔΣ A/D data register 6	DSADDR6	32	32	2, 3 PCLKB	2 ICLK
0008 B478h	DSAD	ΔΣ A/D input select register 6	DSADISR6	8	8	2, 3 PCLKB	2 ICLK
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C011h	PORTH	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C031h	PORTH	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C040h	PORT0	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C041h	PORT1	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

Table 4.1 List of I/O Registers (Address Order) (19 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C042h	PORT2	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C043h	PORT3	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C044h	PORT4	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C045h	PORT5	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C051h	PORTH	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C052h	PORTJ	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D1h	PORTH	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E1h	PORT1	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E2h	PORT2	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E3h	PORT3	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E5h	PORT5	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EAh	PORTA	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EBh	PORTB	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0ECh	PORTC	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EEh	PORTE	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F1h	PORTH	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F2h	PORTJ	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK
0008 C121h	PORT	Port switching register A	PSRA	8	8	2, 3 PCLKB	2 ICLK
0008 C143h	MPC	P03 pin function control register	P03PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C145h	MPC	P05 pin function control register	P05PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C147h	MPC	P07 pin function control register	P07PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ah	MPC	P12 pin function control register	P12PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Bh	MPC	P13 pin function control register	P13PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ch	MPC	P14 pin function control register	P14PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Dh	MPC	P15 pin function control register	P15PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Eh	MPC	P16 pin function control register	P16PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Fh	MPC	P17 pin function control register	P17PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C150h	MPC	P20 pin function control register	P20PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C151h	MPC	P21 pin function control register	P21PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C168h	MPC	P50 pin function control register	P50PFS	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (21 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C169h	MPC	P51 pin function control register	P51PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ah	MPC	P52 pin function control register	P52PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ch	MPC	P54 pin function control register	P54PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 pin function control register	PH0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 pin function control register	PH1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 pin function control register	PH2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 pin function control register	PH3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D1h	MPC	PJ1 pin function control register	PJ1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Fh	SYSTEM	Flash HOCO software standby control register	FHSSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C294h	SYSTEM	High-speed clock oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C295h	SYSTEM	PLL power control register	PLLPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C297h	SYSTEM	Voltage monitoring circuit/comparator A control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK

Table 4.1 List of I/O Registers (Address Order) (22 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to DPSBKR31	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK
0008 C402h	RTC	Second counter/Binary counter 0	RSECCNT/ BCNT0	8	8	2, 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute counter/Binary counter 1	RMINCNT/ BCNT1	8	8	2, 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour counter/Binary counter 2	RHRCNT/ BCNT2	8	8	2, 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-week counter/Binary counter 3	RWKCNT/ BCNT3	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK
0008 C410h	RTC	Second alarm register/Binary counter 0 alarm register	RSECAR/ BCNT0AR	8	8	2, 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute alarm register/Binary counter 1 alarm register	RMINAR/ BCNT1AR	8	8	2, 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour alarm register/Binary counter 2 alarm register	RHRAR/ BCNT2AR	8	8	2, 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-week alarm register/Binary counter 3 alarm register	RWKAR/ BCNT3AR	8	8	2, 3 PCLKB	2 ICLK
0008 C418h	RTC	Date alarm register/Binary counter 0 alarm enable register	RDAYAR/ BCNT0AER	8	8	2, 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month alarm register/Binary counter 1 alarm enable register	RMONAR/ BCNT1AER	8	8	2, 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year alarm register/Binary counter 2 alarm enable register	RYRAR/ BCNT2AER	16	16	2, 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year alarm enable register/Binary counter 3 alarm enable register	RYRAREN/ BCNT3AER	8	8	2, 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK
0008 C452h	RTC	Second capture register 0/BCNT0 capture register 0	RSECCP0/ BCNT0CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C454h	RTC	Minute capture register 0/BCNT1 capture register 0	RMINCP0/ BCNT1CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C456h	RTC	Hour capture register 0/BCNT2 capture register 0	RHRCP0/ BCNT2CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C45Ah	RTC	Date capture register 0/BCNT3 capture register 0	RDAYCP0/ BCNT3CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK
0008 C462h	RTC	Second capture register 1/BCNT0 capture register 1	RSECCP1/ BCNT0CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C464h	RTC	Minute capture register 1/BCNT1 capture register 1	RMINCP1/ BCNT1CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C466h	RTC	Hour capture register 1/BCNT2 capture register 1	RHRCP1/ BCNT2CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C46Ah	RTC	Date capture register 1/BCNT3 capture register 1	RDAYCP1/ BCNT3CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK
0008 C472h	RTC	Second capture register 2/BCNT0 capture register 2	RSECCP2/ BCNT0CP2	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (23 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C474h	RTC	Minute capture register 2/BCNT1 capture register 2	RMINCP2/ BCNT1CP2	8	8	2, 3 PCLKB	2 ICLK
0008 C476h	RTC	Hour capture register 2/BCNT2 capture register 2	RHRCP2/ BCNT2CP2	8	8	2, 3 PCLKB	2 ICLK
0008 C47Ah	RTC	Date capture register 2/BCNT3 capture register 2	RDAYCP2/ BCNT3CP2	8	8	2, 3 PCLKB	2 ICLK
0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK
0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C580h	CMPB	Comparator B control register 1	CPBCNT1	8	8	2, 3 PCLKB	2 ICLK
0008 C582h	CMPB	Comparator B flag register	CPBFLG	8	8	2, 3 PCLKB	2 ICLK
0008 C583h	CMPB	Comparator B interrupt control register	CPBINT	8	8	2, 3 PCLKB	2 ICLK
0008 C584h	CMPB	Comparator B filter select register	CPBF	8	8	2, 3 PCLKB	2 ICLK
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2 ICLK
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2 ICLK
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2 ICLK
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2 ICLK
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2 ICLK
007F C450h	FLASH	E2 DataFlash programming/erasure enable register 0	DFLWE0	16	16	2, 3 FCLK	2 ICLK
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2 ICLK
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2 ICLK
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2 ICLK
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2 ICLK
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2 ICLK
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2 ICLK
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2 ICLK
007F FFCAh	FLASH	E2 DataFlash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2 ICLK
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2 ICLK
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2 ICLK
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2 ICLK
FEFF FAC0h	FLASH	Unique ID register 0*3	UIDR0	32	32	1ICLK	
FEFF FAC4h	FLASH	Unique ID register 1*3	UIDR1	32	32	1ICLK	
FEFF FAC8h	FLASH	Unique ID register 2*3	UIDR2	32	32	1ICLK	
FEFF FACCh	FLASH	Unique ID register 3*3	UIDR3	32	32	1ICLK	
FEFF FAD0h	TEMPS	Temperature sensor calibration data register 0*3	TSCDR0	32	32	1ICLK	
FEFF FAD4h	TEMPS	Temperature sensor calibration data register 1*3	TSCDR1	32	32	1ICLK	
FEFF FADCh	TEMPS	Temperature sensor calibration data register 3*3	TSCDR3	32	32	1ICLK	
FEFF FB30h	DSAD	ΔΣA/D gain calibration data register 0 X1*3	DSADG0X1	32	32	1ICLK	
FEFF FB34h	DSAD	ΔΣA/D gain calibration data register 1 X1*3	DSADG1X1	32	32	1ICLK	
FEFF FB38h	DSAD	ΔΣA/D gain calibration data register 2 X1*3	DSADG2X1	32	32	1ICLK	
FEFF FB3Ch	DSAD	ΔΣA/D gain calibration data register 3 X1*3	DSADG3X1	32	32	1ICLK	
FEFF FB40h	DSAD	ΔΣA/D gain calibration data register 4 X1*3	DSADG4X1	32	32	1ICLK	
FEFF FB44h	DSAD	ΔΣA/D gain calibration data register 5 X1*3	DSADG5X1	32	32	1ICLK	
FEFF FB48h	DSAD	ΔΣA/D gain calibration data register 6 X1*3	DSADG6X1	32	32	1ICLK	
FEFF FB50h	DSAD	ΔΣA/D gain calibration data register 0 X2*3	DSADG0X2	32	32	1ICLK	
FEFF FB54h	DSAD	ΔΣA/D gain calibration data register 1 X2*3	DSADG1X2	32	32	1ICLK	
FEFF FB58h	DSAD	ΔΣA/D gain calibration data register 2 X2*3	DSADG2X2	32	32	1ICLK	
FEFF FB5Ch	DSAD	ΔΣA/D gain calibration data register 3 X2*3	DSADG3X2	32	32	1ICLK	
FEFF FB60h	DSAD	ΔΣA/D gain calibration data register 4 X2*3	DSADG4X2	32	32	1ICLK	
FEFF FB64h	DSAD	ΔΣA/D gain calibration data register 5 X2*3	DSADG5X2	32	32	1ICLK	
FEFF FB68h	DSAD	ΔΣA/D gain calibration data register 6 X2*3	DSADG6X2	32	32	1ICLK	
FEFF FB70h	DSAD	ΔΣA/D gain calibration data register 0 X4*3	DSADG0X4	32	32	1ICLK	

Table 4.1 List of I/O Registers (Address Order) (24 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
FEFF FB74h	DSAD	ΔΣA/D gain calibration data register 1 X4*3	DSADG1X4	32	32		1ICLK
FEFF FB78h	DSAD	ΔΣA/D gain calibration data register 2 X4*3	DSADG2X4	32	32		1ICLK
FEFF FB7Ch	DSAD	ΔΣA/D gain calibration data register 3 X4*3	DSADG3X4	32	32		1ICLK
FEFF FB80h	DSAD	ΔΣA/D gain calibration data register 4 X4*3	DSADG4X4	32	32		1ICLK
FEFF FB84h	DSAD	ΔΣA/D gain calibration data register 5 X4*3	DSADG5X4	32	32		1ICLK
FEFF FB88h	DSAD	ΔΣA/D gain calibration data register 6 X4*3	DSADG6X4	32	32		1ICLK
FEFF FB90h	DSAD	ΔΣA/D gain calibration data register 0 X8*3	DSADG0X8	32	32		1ICLK
FEFF FB94h	DSAD	ΔΣA/D gain calibration data register 1 X8*3	DSADG1X8	32	32		1ICLK
FEFF FB98h	DSAD	ΔΣA/D gain calibration data register 2 X8*3	DSADG2X8	32	32		1ICLK
FEFF FB9Ch	DSAD	ΔΣA/D gain calibration data register 3 X8*3	DSADG3X8	32	32		1ICLK
FEFF FBA0h	DSAD	ΔΣA/D gain calibration data register 0 X16*3	DSADG0X16	32	32		1ICLK
FEFF FBA4h	DSAD	ΔΣA/D gain calibration data register 1 X16*3	DSADG1X16	32	32		1ICLK
FEFF FBA8h	DSAD	ΔΣA/D gain calibration data register 2 X16*3	DSADG2X16	32	32		1ICLK
FEFF FBACh	DSAD	ΔΣA/D gain calibration data register 3 X16*3	DSADG3X16	32	32		1ICLK
FEFF FBB0h	DSAD	ΔΣA/D gain calibration data register 0 X32*3	DSADG0X32	32	32		1ICLK
FEFF FBB4h	DSAD	ΔΣA/D gain calibration data register 1 X32*3	DSADG1X32	32	32		1ICLK
FEFF FBB8h	DSAD	ΔΣA/D gain calibration data register 2 X32*3	DSADG2X32	32	32		1ICLK
FEFF FBBCh	DSAD	ΔΣA/D gain calibration data register 3 X32*3	DSADG3X32	32	32		1ICLK
FEFF FBD0h	DSAD	ΔΣA/D input impedance calibration data register*3	DSADIIC	32	32		1ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 24.4 lists register allocation for 16-bit access.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register. Table 31.3 lists register allocation for 16-bit access.
Note 3. Only G version products have these registers.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +6.5	V
Input voltage (except for ports for 5 V tolerant*1)	V_{in}	–0.3 to VCC + 0.3*3	V
Input voltage (ports for 5 V tolerant*1)	V_{in}	–0.3 to +6.5	V
Reference power supply voltage	VREFH, VREFH0	–0.3 to VCC + 0.3*3	V
Analog power supply voltage	AVCC0, AVCCA, BGR_BO*2	–0.3 to +6.5	V
A/D converter analog input voltage	V_{AN}	–0.3 to VCC + 0.3*3	V
ΔΣ A/D converter analog input voltage	V_{ANDS}	–0.6 to VCC + 0.3*3	V
Operating temperature	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interferences, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, the AVCCA and AVSSA pins, and between the VREFH0 and VREFL0 pins. Place capacitors of 0.1 µF or so as close to every power pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 0.1 µF (±20% accuracy) capacitor. The capacitor must be placed as close to the pin as possible.

Note 1. Ports 12, 13, 16, 17, 20, and 21 are 5 V tolerant.

Note 2. Set AVCC0 and AVCCA to the same potential as VCC. When neither the A/D converter, the D/A converter, nor ΔΣ A/D converter is in use, do not leave the AVCC0, VREFH, AVCCA, VREFH0, AVSS0, VREFL, AVSSA, and VREFL0 pins open. Connect the AVCC0, VREFH, AVCCA, and VREFH0 pins to VCC, and the AVSS0, VREFL, AVSSA, and VREFL0 pins to VSS, respectively.

Note 3. The maximum value is 6.5 V.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 12, 13, 16, 17, 20, and 21 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 0, 14, 15, 22, 23, 24, 25, 26, 27, 3, 4, 5, A, B, C, E, H, J, and RES#		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Other than RIIC input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Other than RIIC input pin		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD pin	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD pin	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 5.3 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 2.7 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, 17, 20, and 21 (5 V tolerant)		V_{IH}	VCC × 0.8	—	5.8	V	
	Ports 0, 14, 15, 22, 23, 24, 25, 26, 27, 3, 4, 5, A, B, C, E, H, J, and RES#			VCC × 0.8	—	VCC + 0.3		
	All input pins		V_{IL}	–0.3	—	VCC × 0.2		
	Ports 0 to 5, ports A to J	VCC ≥ 2.2 V	ΔV_T	VCC × 0.05	—	—		
		VCC < 2.2 V		VCC × 0.03				
	RES#			VCC × 0.1				
Input level voltage (except for Schmitt trigger input pins)	MD pin		V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL			VCC × 0.8	—	VCC + 0.3		
	MD pin		V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL			–0.3	—	VCC × 0.2		

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 0, 12, 13, 16, 17, 20, 21, port 4, ports A0, A1, A2, A3, A4, A6, and port B0)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 0, 12, 13, 16, 17, 20, 21, port 4, ports A0, A1, A2, A3, A4, A6, and port B0		—	—	30		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC				Unit	Test Conditions
			1.8 to 2.7 V		2.7 to 3.6 V			
			Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	|5|	|150|	|10|	|200|	µA	V_{in} = 0 V

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*3	ICLK = 50 MHz	I_{CC}	8.6	—	mA	
			All peripheral operation: Normal*4	ICLK = 50 MHz		13	—		
			All peripheral operation: Max.*5	ICLK = 50 MHz		—	59		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.9	—		
			All peripheral operation: Normal	ICLK = 50 MHz		9.0	—		
		All-module clock stop mode		ICLK = 50 MHz		3.9	—		
		Increase during BGO operation*2				23	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. PCLKA is ICLK divided by 1. FCLK, PCLKB, PCLKC, and PCLKD are ICLK divided by 2.

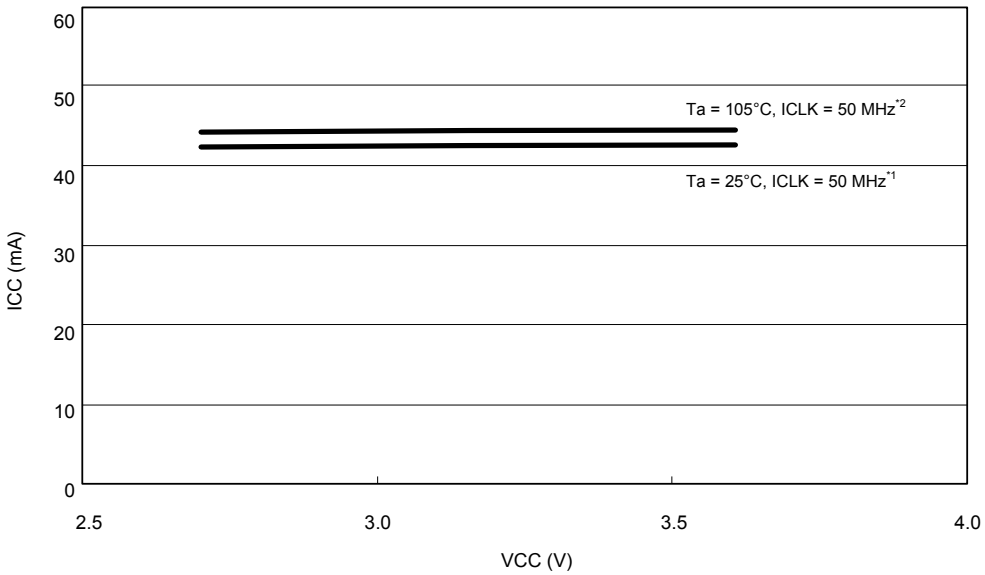
Table 5.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Medium-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation*3	ICLK = 25 MHz	I_{CC}	5.9	—	mA	
			All peripheral operation: Normal*4	ICLK = 25 MHz		8.0	—		
			All peripheral operation: Max.*5	ICLK = 25 MHz		—	38		
		Sleep mode	No peripheral operation	ICLK = 25 MHz		4.1	—		
			All peripheral operation: Normal	ICLK = 25 MHz		6.2	—		
		All-module clock stop mode		ICLK = 25 MHz		3.6	—		
		Increase during BGO operation*2	Medium-speed operating mode 1A			23	—		
			Medium-speed operating mode 1B			20	—		
	Medium-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*3	ICLK = 25 MHz		5.4	—		
				ICLK = 12.5 MHz		3.9	—		
			All peripheral operation: Normal*4	ICLK = 25 MHz		7.4	—		
				ICLK = 12.5 MHz		5.0	—		
			All peripheral operation: Max.*5	ICLK = 25 MHz		—	37		
		Sleep mode	No peripheral operation	ICLK = 25 MHz		3.5	—		
				ICLK = 12.5 MHz		3.0	—		
			All peripheral operation: Normal	ICLK = 25 MHz		5.6	—		
				ICLK = 12.5 MHz		4.1	—		
		All-module clock stop mode		ICLK = 25 MHz		3.0	—		
				ICLK = 12.5 MHz		2.7	—		
		Increase during BGO operation*2	Medium-speed operating mode 2A			23	—		
			Medium-speed operating mode 2B			20	—		

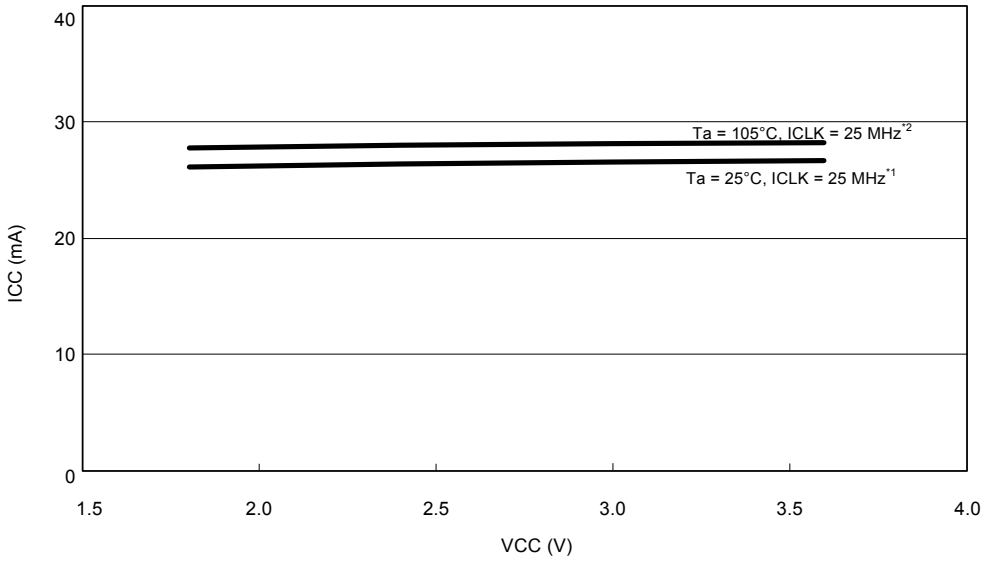
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*6	ICLK = 8 MHz	I_{CC}	1.9	—	mA	
				ICLK = 4 MHz		1.2	—		
			All peripheral operation: Normal*7	ICLK = 8 MHz		2.5	—		
				ICLK = 4 MHz		1.7	—		
			All peripheral operation: Max.*8	ICLK = 8 MHz		—	12		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.3	—		
				ICLK = 4 MHz		0.9	—		
			All peripheral operation: Normal	ICLK = 8 MHz		1.9	—		
				ICLK = 4 MHz		1.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.1	—		
				ICLK = 4 MHz		0.9	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.027	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.030	—		
			All peripheral operation: Max.*11	ICLK = 32 kHz		—	1.0		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.025	—		
		All-module clock stop mode		ICLK = 32 kHz		0.022	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are ICLK divided by 1.
Note 6. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are ICLK divided by 1.



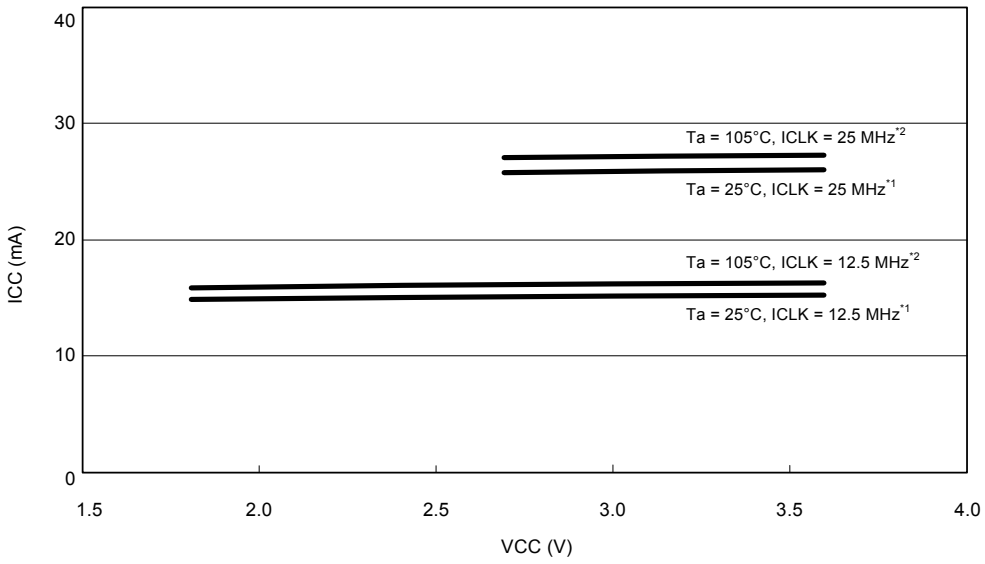
Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



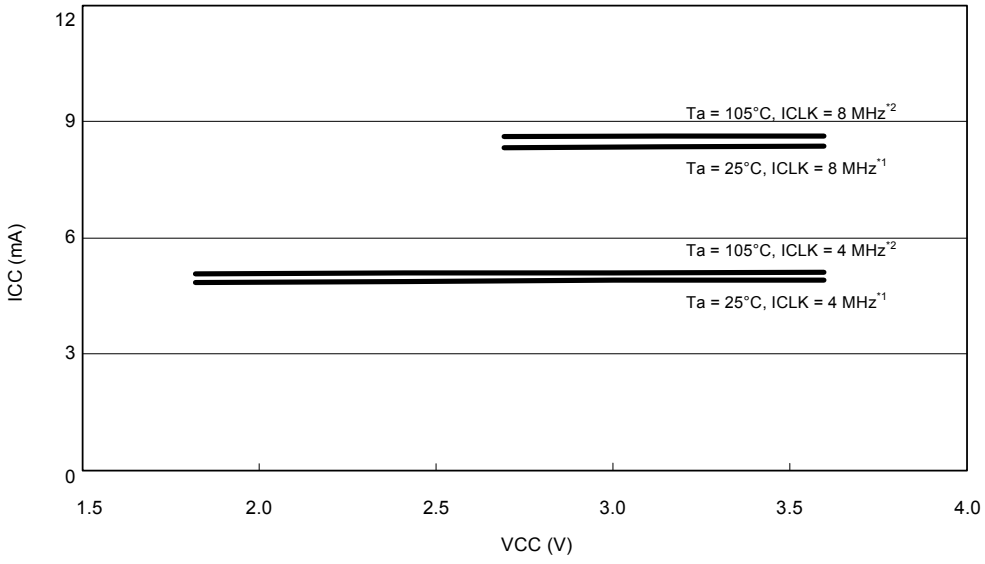
Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Medium-Speed Operating Modes 1A and 1B (Reference Data)



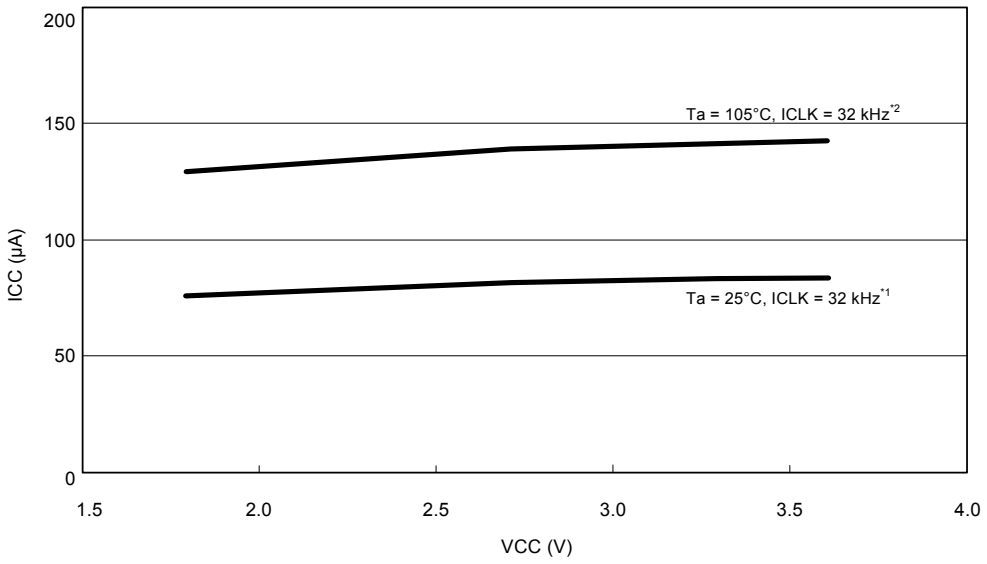
Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Medium-Speed Operating Modes 2A and 2B (Reference Data)



Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data)



Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

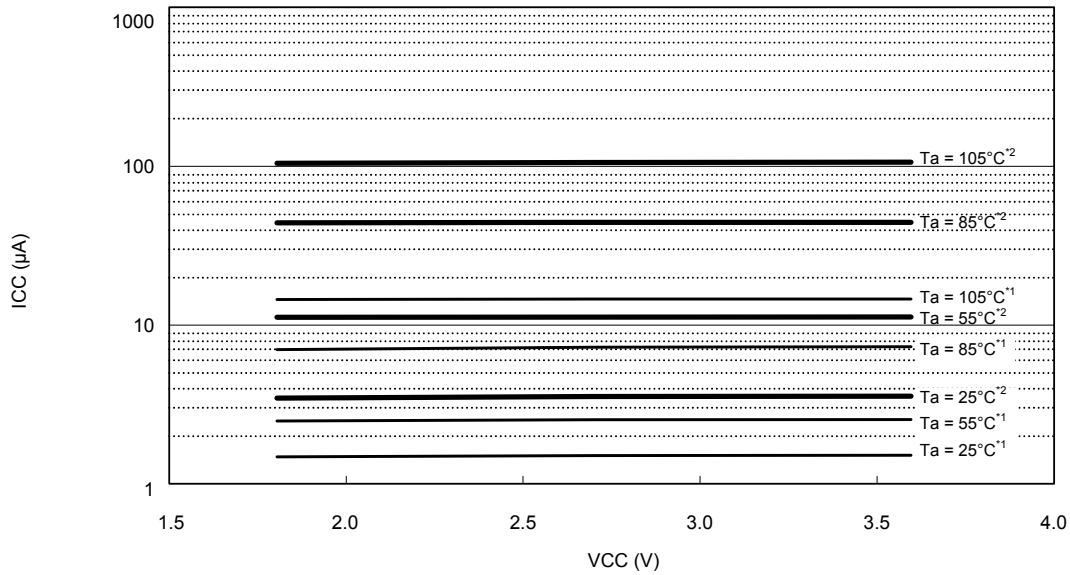
Figure 5.5 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data)

Table 5.8 DC Characteristics (7)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

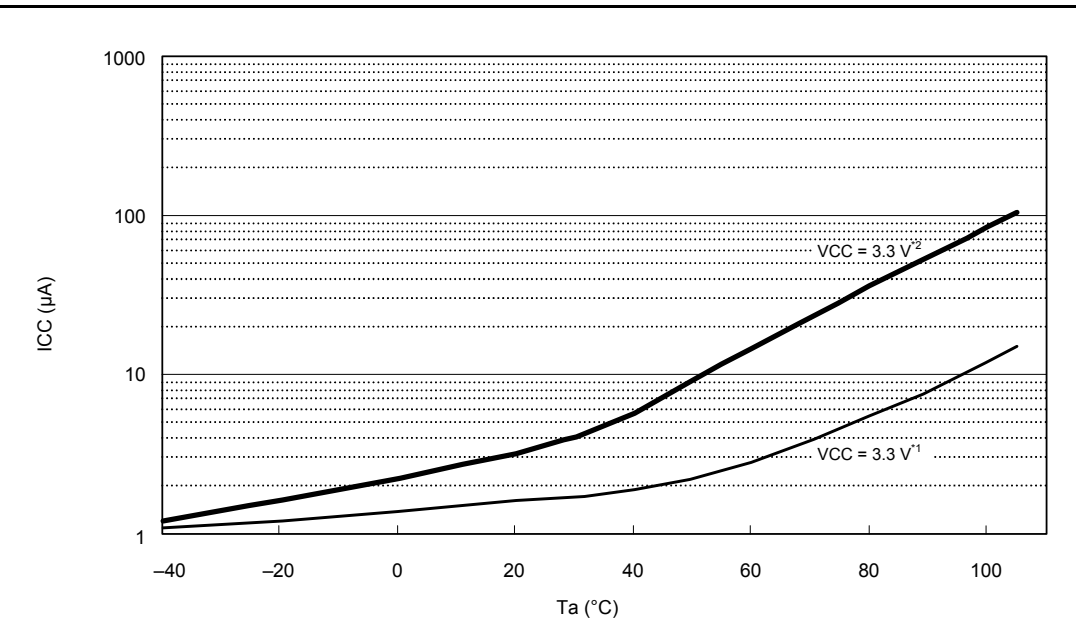
Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	10	20	µA	
			T_a = 55°C		12	41		
			T_a = 85°C		18	113		
			T_a = 105°C		29	233		
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		1.7	7.9		
			T_a = 55°C		2.7	25		
			T_a = 85°C		7.0	86		
			T_a = 105°C		16	189		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled	T_a = 25°C		0.3	0.8		
			T_a = 55°C		0.4	1.1		
			T_a = 85°C		0.8	2.2		
			T_a = 105°C		1.3	4.7		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.2	—		
	Increment for RTC operation (low CL)				0.6	—		
	Increment for RTC operation (standard CL)				1.4	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.



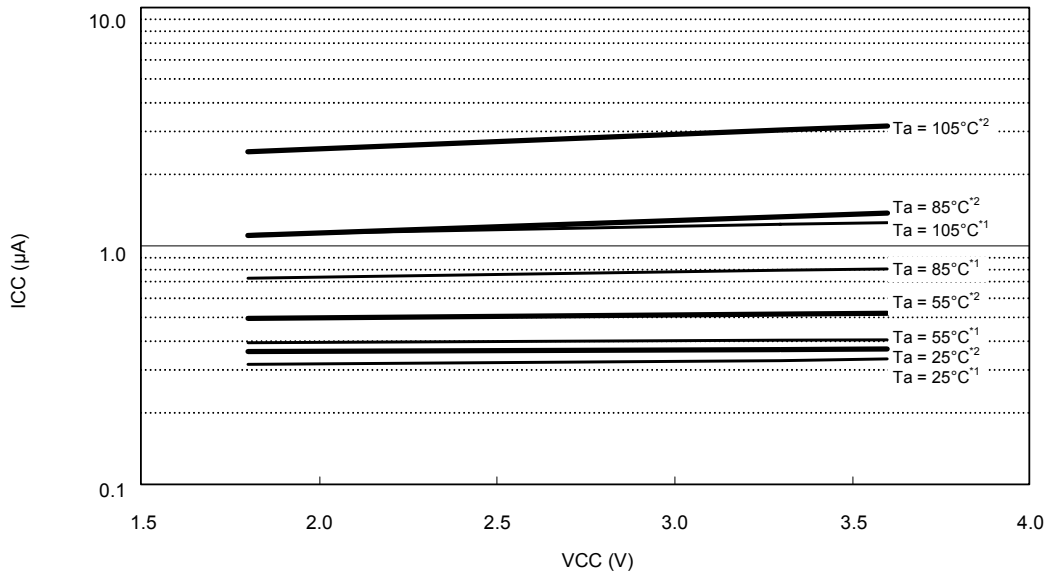
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.6 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data)



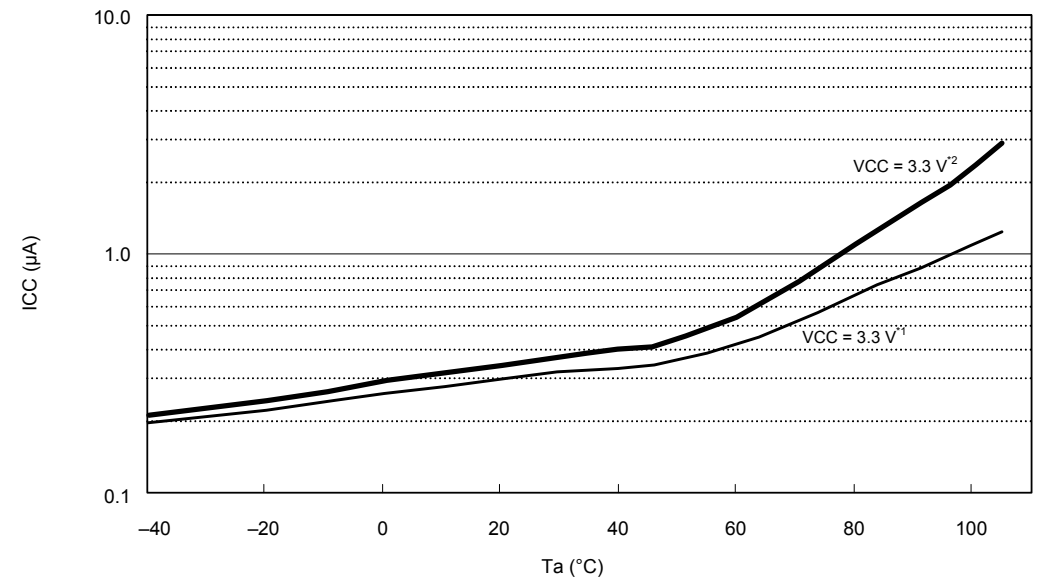
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.7 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.8 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data)

Table 5.9 DC Characteristics (8)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	P_d	—	350	mW	Ta = –40 to 85°C
		—	150		85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.10 DC Characteristics (9)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VREFH = 1.8 to AVCC0, VREFH0 = 1.8 to AVCC0, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	Conversion time = 2 µs	I_{AVCC0}	—	0.65	1.1	mA	
	Temperature sensor enabled while waiting for A/D conversion			—	60	150	µA	
	During D/A conversion (per channel)		I_{VREFH}*1	—	0.25	0.45	mA	
	Waiting for A/D, D/A conversion (all units)*2		—	—	0.2	2.0	µA	
Reference power supply current	During A/D conversion	Conversion time = 2 µs	I_{VREFH0}	—	0.05	0.1	mA	
	Waiting for A/D conversion			—	0.2	0.4	µA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. The values are the sum of I_{AVCC0} and I_{REFH}.

Table 5.11 DC Characteristics (10)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During ΔΣ A/D conversion (per channel)	AI_{CCA}	—	0.9	1.4	mA	
	ΔΣ A/D bias circuit operating current		—	90	130	µA	
	When ΔΣ A/D conversion is stopped (all units)		—	0.07	1.8		

Table 5.12 DC Characteristics (11)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.13 DC Characteristics (12)

Conditions: VCC = AVCC0 = AVCCA = 0 to 3.6 V, VREFH = VREFH0 = 0 to AVCC0, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	At cold start

Table 5.14 DC Characteristics (13)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $fr_{(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).
When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$fr_{(VCC)}$	—	—	10	kHz	Figure 5.10 VCC × 0.1 < $V_{r(VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	Figure 5.10 VCC × 0.05 < $V_{r(VCC)}$ ≤ VCC × 0.1
		—	—	10	MHz	Figure 5.10 $V_{r(VCC)}$ ≤ VCC × 0.05
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

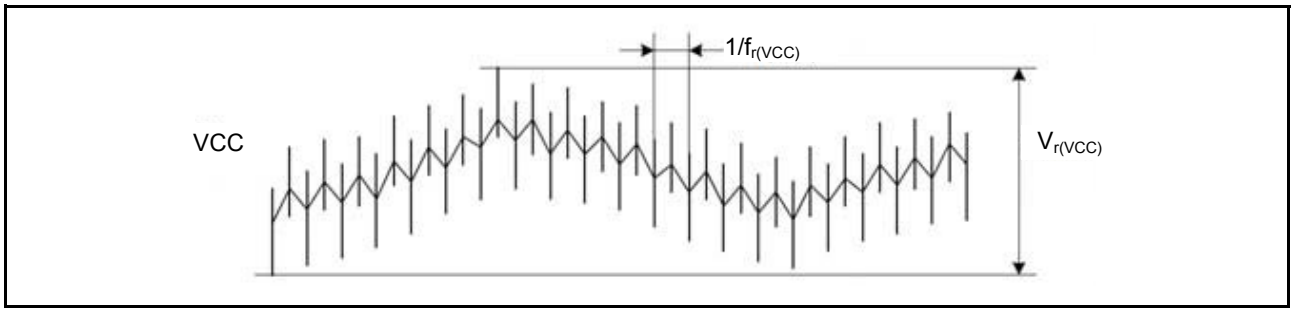


Figure 5.10 Ripple Waveform

Table 5.15 Permissible Output Currents (1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
when total power (mW) < 1000 – 10 × Ta

Item		Symbol	Max.	Unit
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OL}	4.0	mA
	High-drive output mode		8.0	
Permissible output low current (total)	Total of all output pins	I_{OL}	60	
Permissible output high current (maximum value per 1 pin)	Normal output mode	I_{OH}	–4.0	
	High-drive output mode		–8.0	
Permissible output high current (total)	Total of all output pins	I_{OH}	–60	

Table 5.16 Permissible Output Currents (2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
when total power (mW) ≥ 1000 – 10 × Ta

Item		Symbol	Max.	Unit
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OL}	2.0	mA
	High-drive output mode		4.0	
Permissible output low current (total)	Total of all output pins	I_{OL}	30	
Permissible output high current (maximum value per 1 pin)	Normal output mode	I_{OH}	–2.0	
	High-drive output mode		–4.0	
Permissible output high current (total)	Total of all output pins	I_{OH}	–30	

Table 5.17 Output Values of Voltage (1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 2.7 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.4	V	I_{OL} = 0.5 mA
		High-drive output mode		—	0.4		I_{OL} = 1.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.4	—	V	I_{OL} = –0.5 mA
		High-drive output mode		VCC – 0.4	—		I_{OL} = –1.0 mA

Table 5.18 Output Values of Voltage (2)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL =0 V,
T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	1.0	V	I_{OL} = 3.0 mA
		High-drive output mode		—	1.0		I_{OL} = 5.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 1.0	—	V	I_{OL} = –3.0 mA
		High-drive output mode		VCC – 1.0	—		I_{OL} = –5.0 mA

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.11 to Figure 5.15 show the characteristics when normal output is selected by the drive capacity control register.

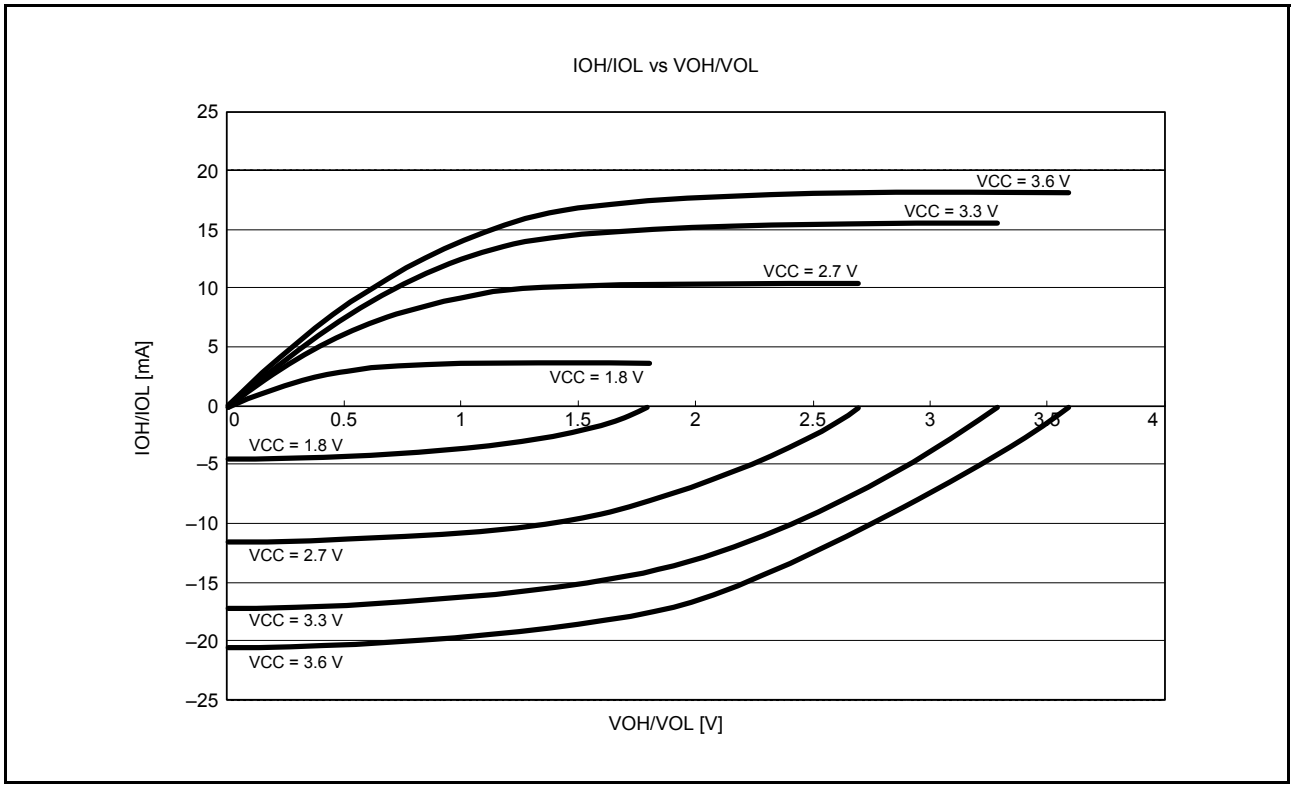


Figure 5.11 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

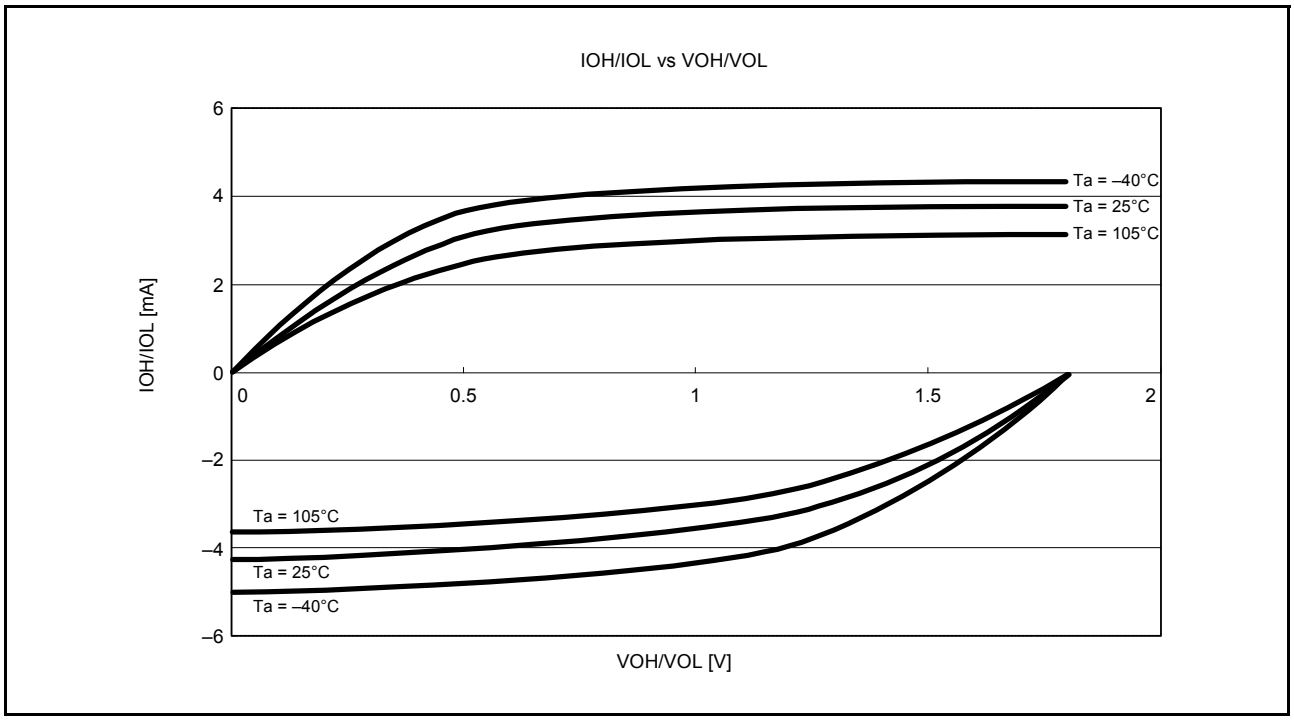


Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.8 V when Normal Output is Selected (Reference Data)

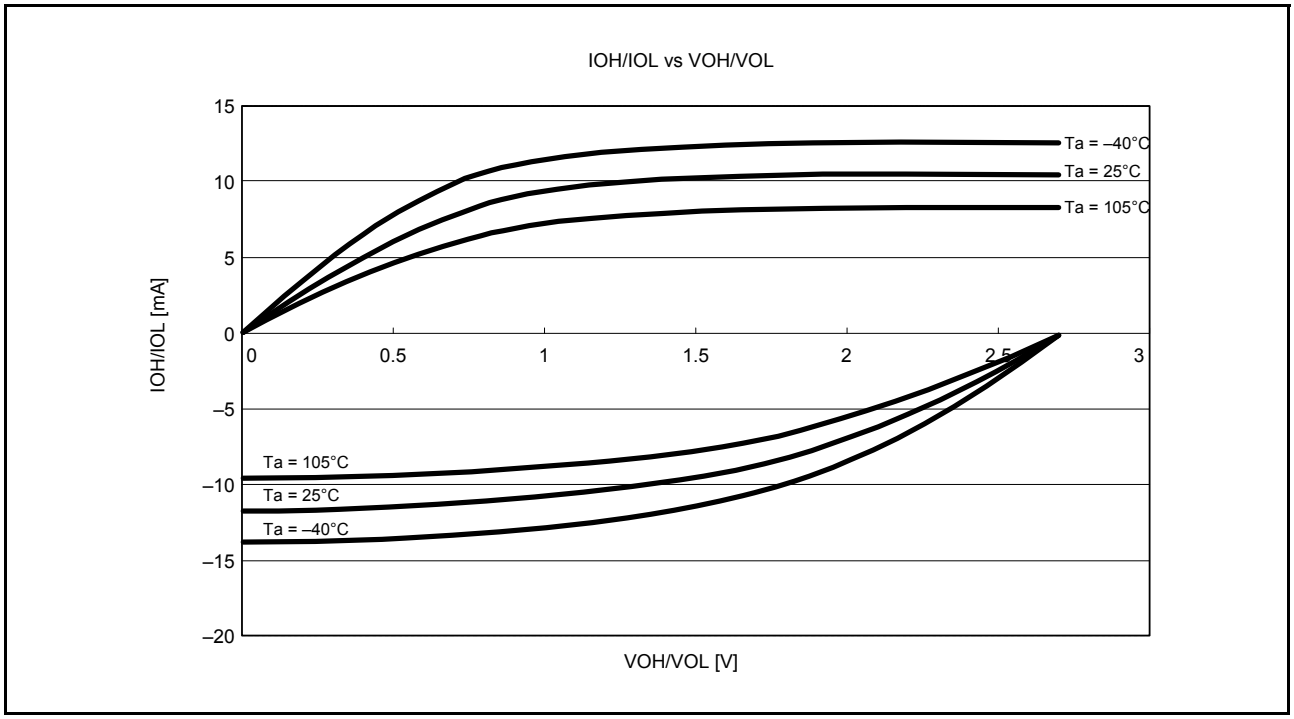


Figure 5.13 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

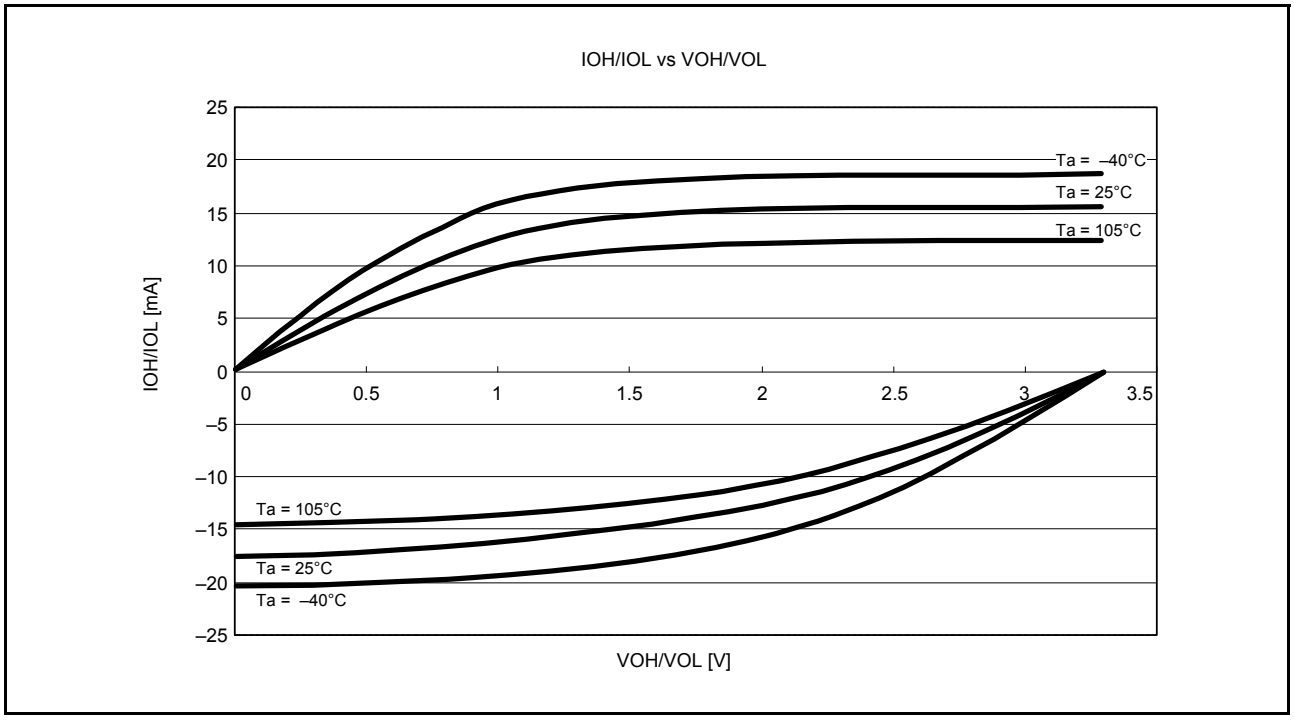


Figure 5.14 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when Normal Output is Selected (Reference Data)

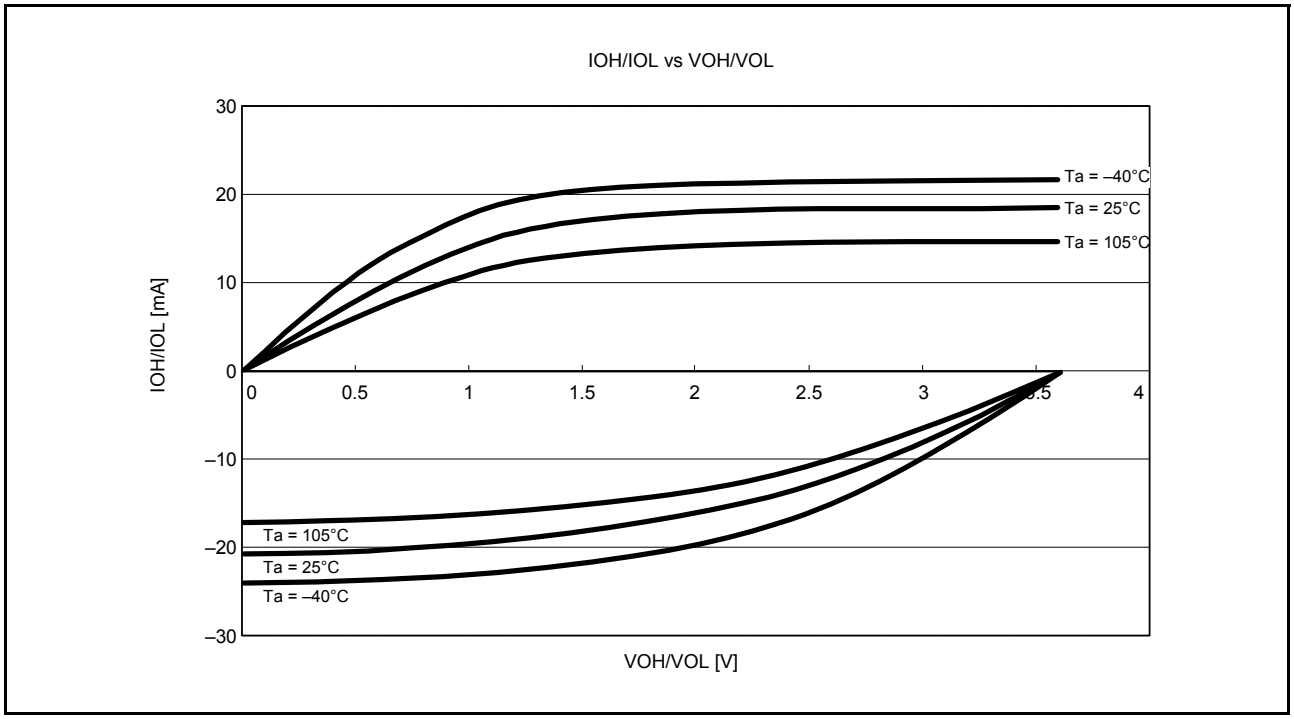


Figure 5.15 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.6 V when Normal Output is Selected (Reference Data)

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.16 to Figure 5.20 show the characteristics when high-drive output is selected by the drive capacity control register.

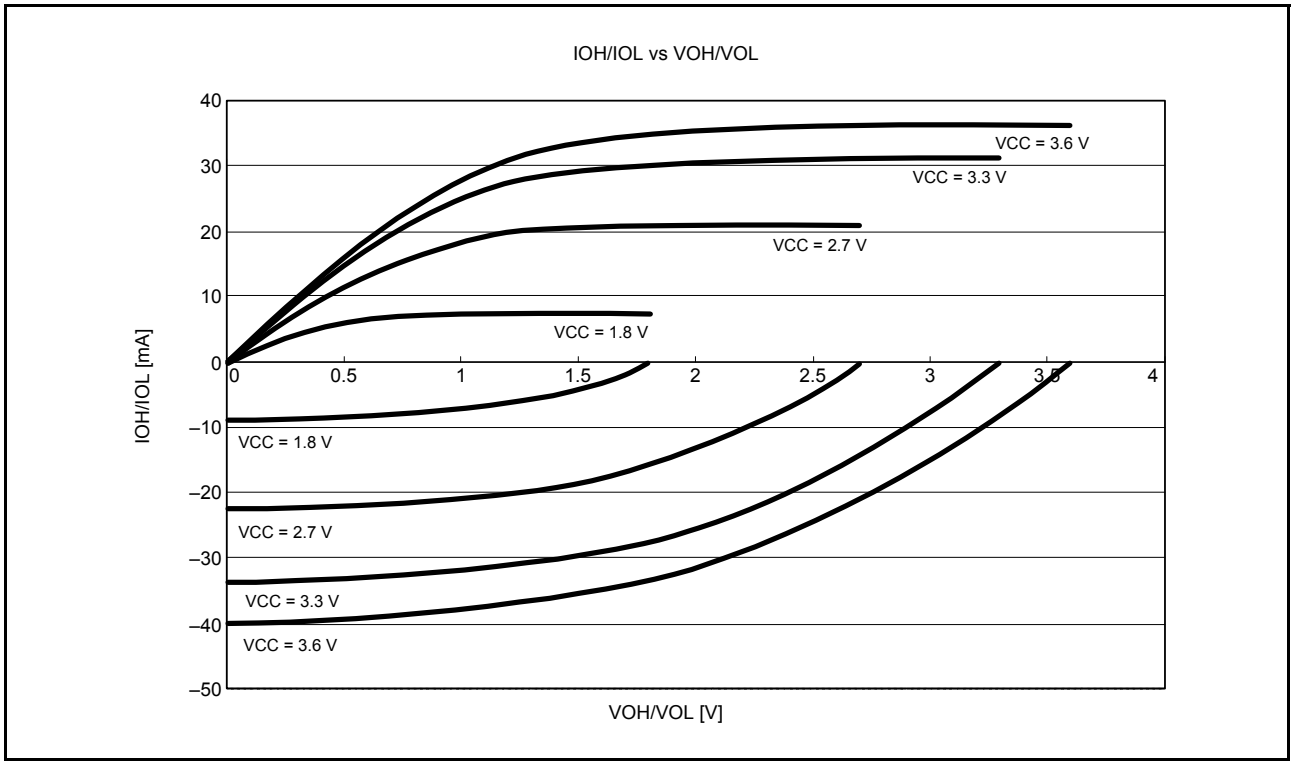


Figure 5.16 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when High-Drive Output is Selected (Reference Data)

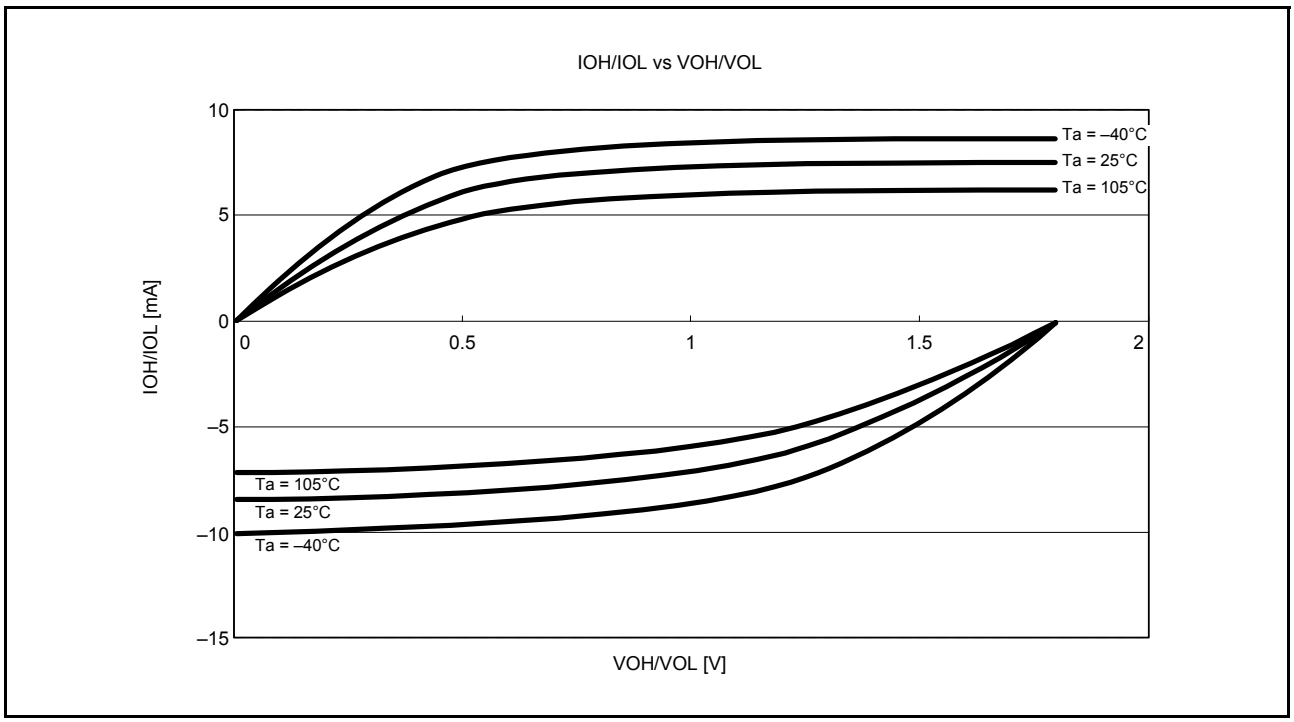


Figure 5.17 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.8 V when High-Drive Output is Selected (Reference Data)

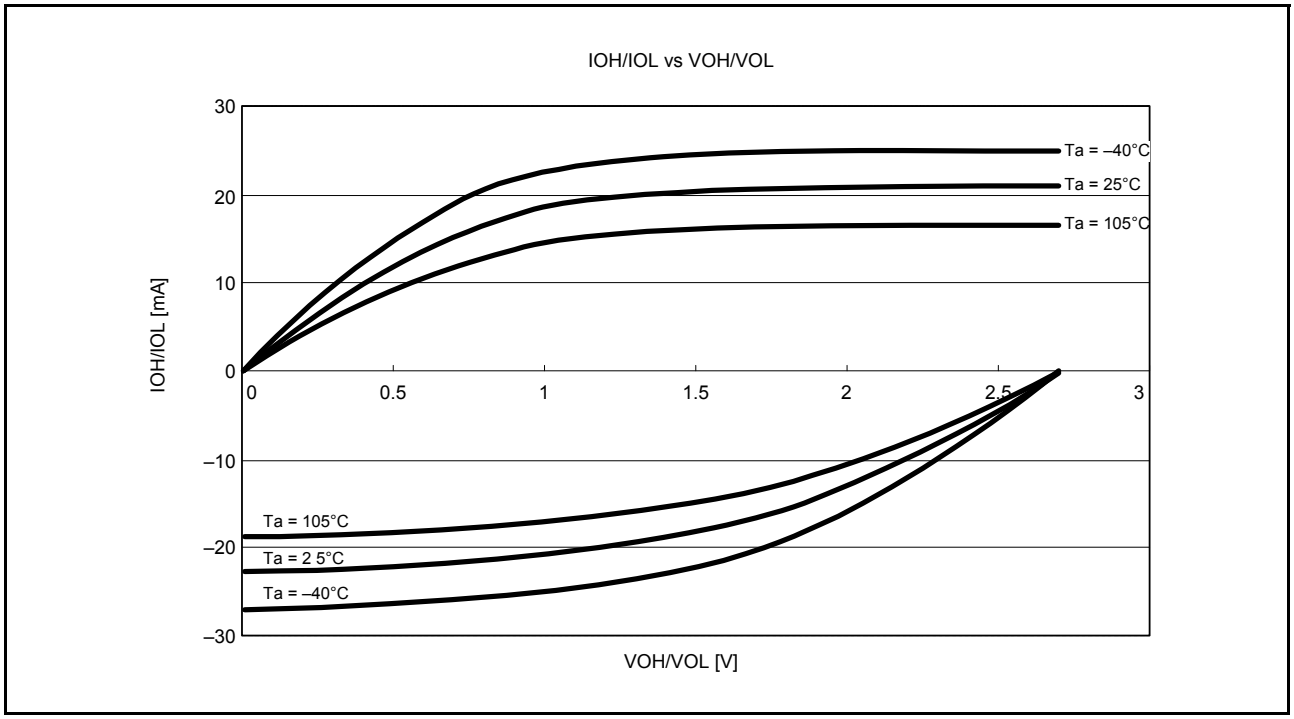


Figure 5.18 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when High-Drive Output is Selected (Reference Data)

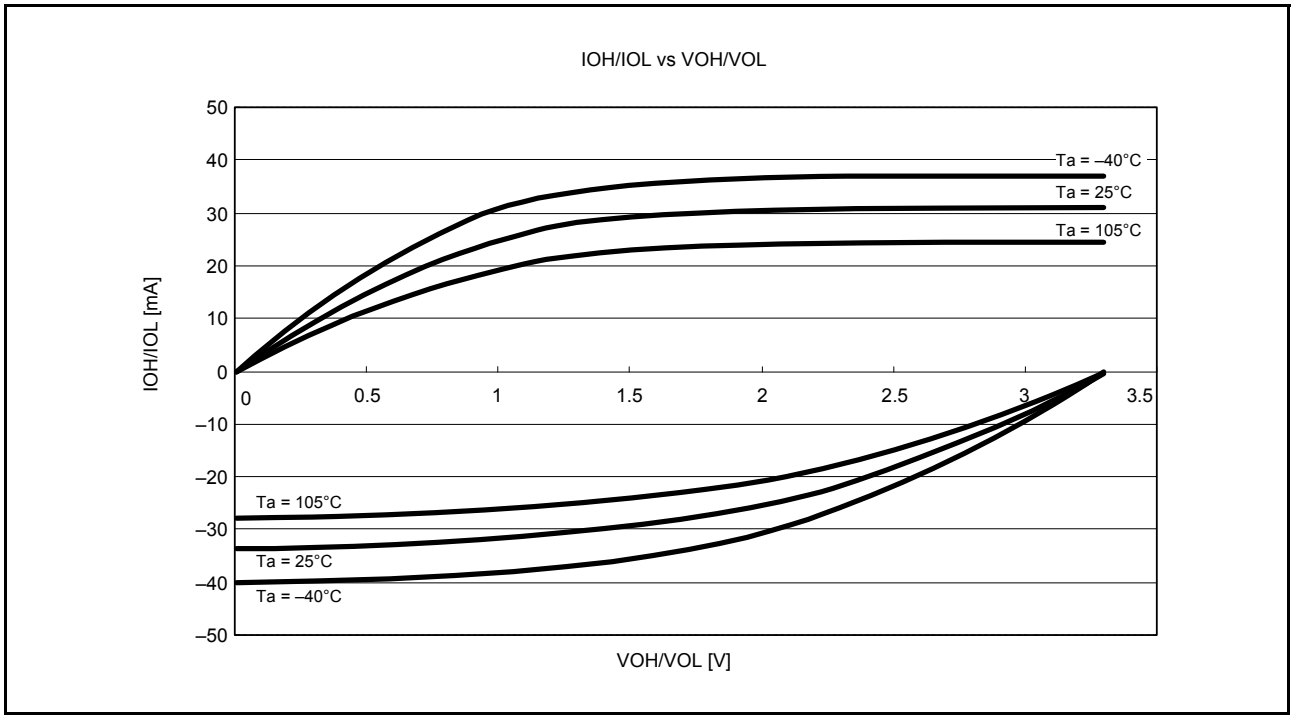


Figure 5.19 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when High-Drive Output is Selected (Reference Data)

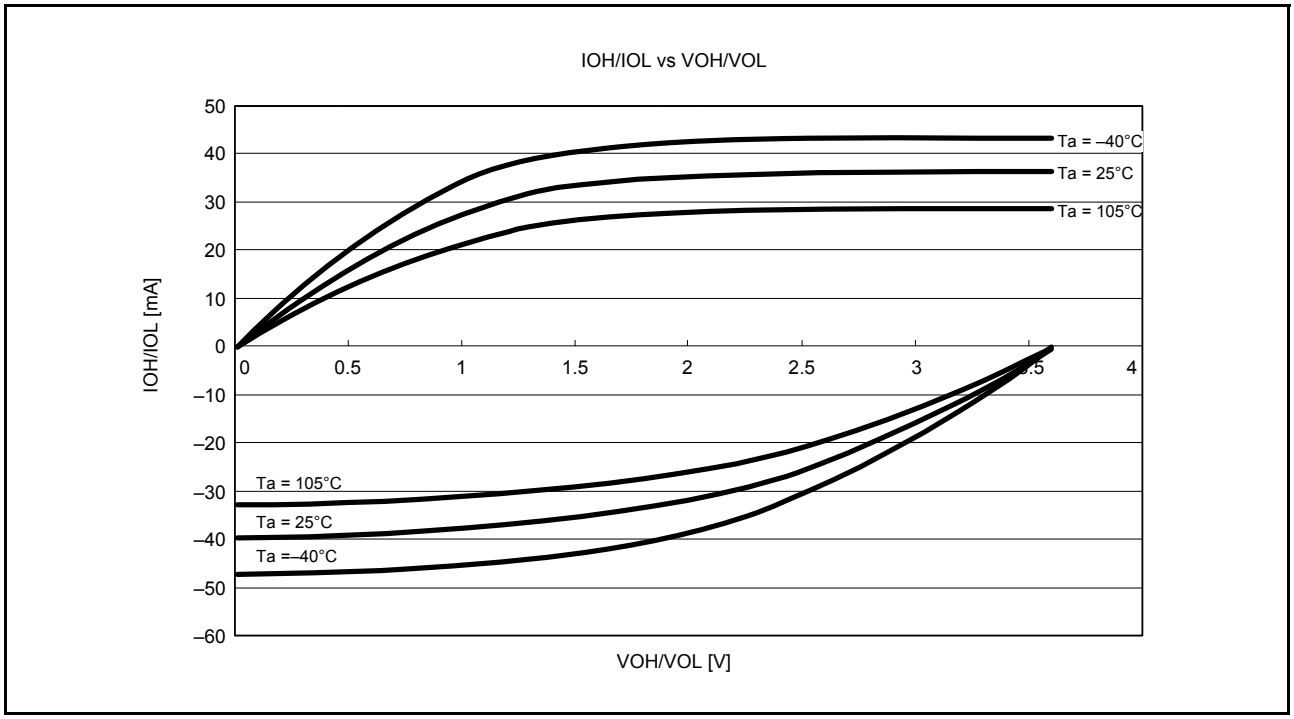


Figure 5.20 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.6 V when High-Drive Output is Selected (Reference Data)

5.2.3 RIIC Pin Output Characteristics

Figure 5.21 to Figure 5.24 show the output characteristics of the RIIC pin.

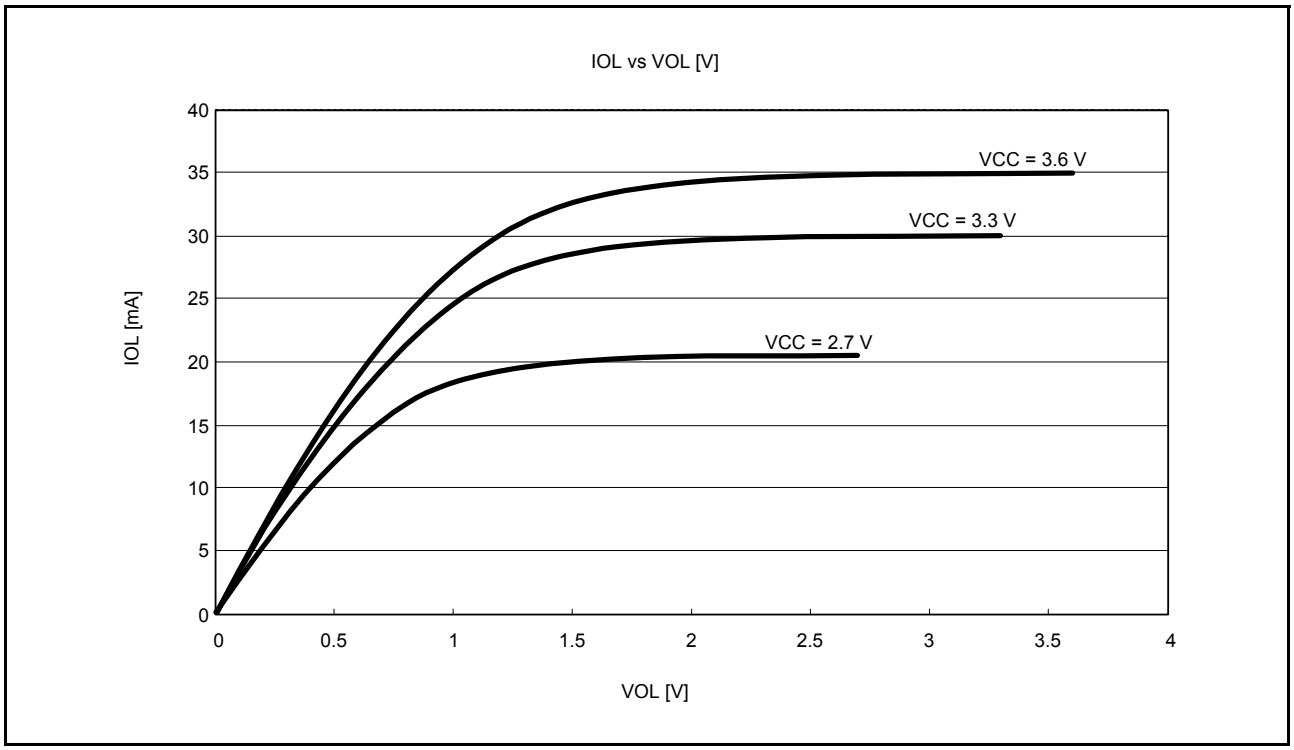


Figure 5.21 VOH and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)

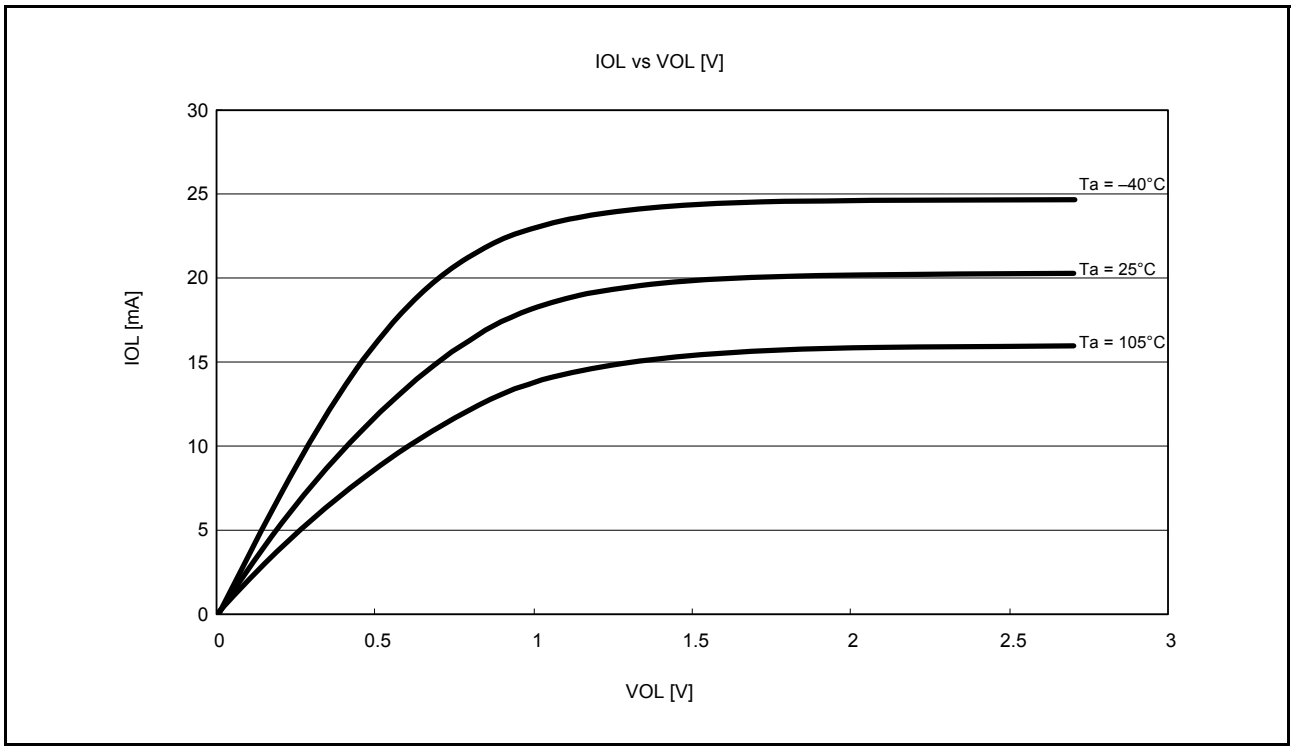


Figure 5.22 VOH and IOL Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

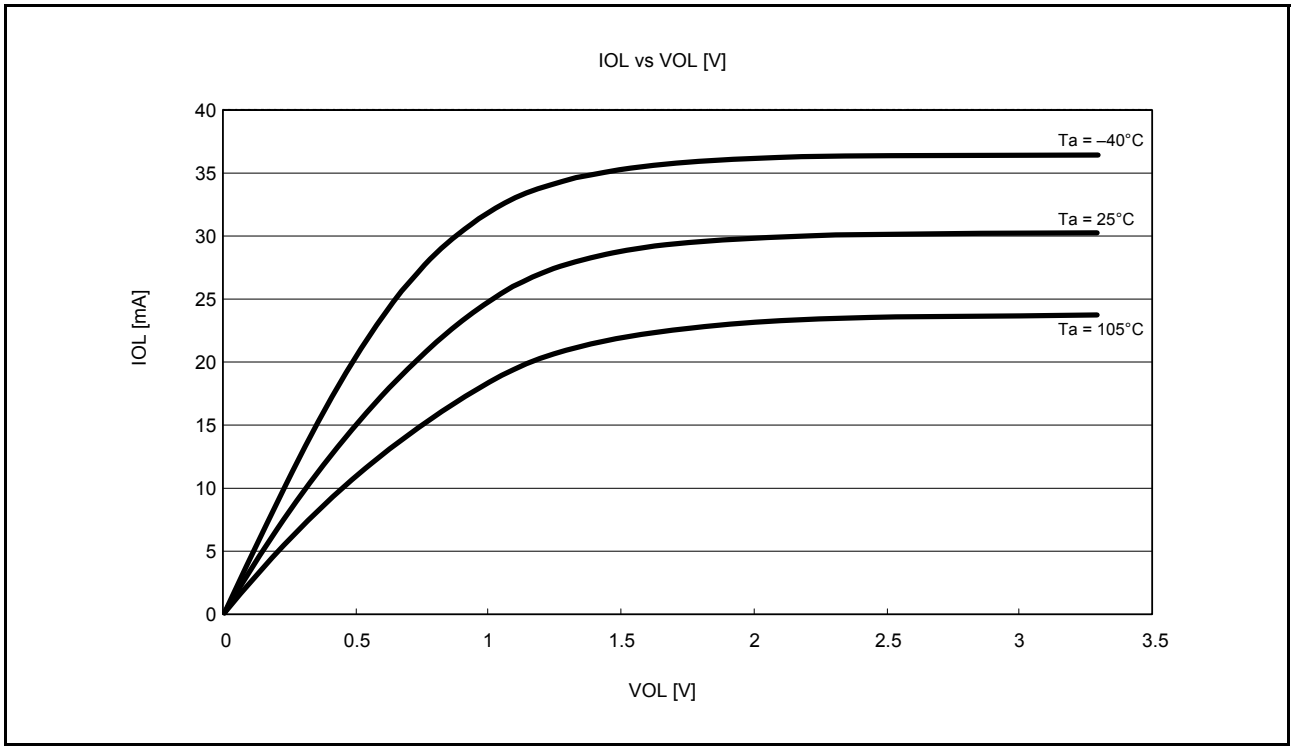


Figure 5.23 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

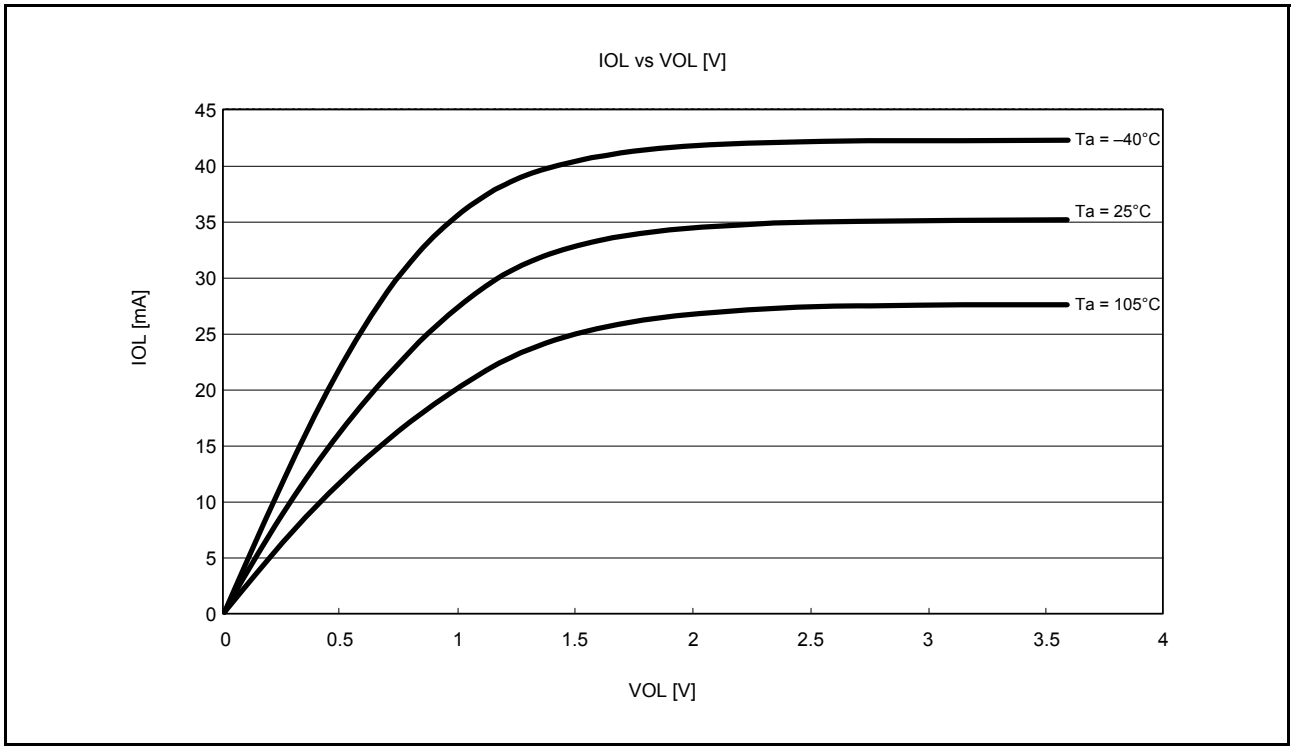


Figure 5.24 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.6 V (Reference Data)

5.3 AC Characteristics

Table 5.19 Operation Frequency Value (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC	Unit
			2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	50	MHz
	FlashIF clock (FCLK)*1		25	
	Peripheral module clock (PCLKA)		50	
	Peripheral module clock (PCLKB)		25	
	Peripheral module clock (PCLKC)*2		25	
	Peripheral module clock (PCLKD)*3		25	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.20 Operation Frequency Value (Medium-Speed Operating Mode 1A)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	25	25	MHz
	FlashIF clock (FCLK)*1		25	25	
	Peripheral module clock (PCLKA)		25	25	
	Peripheral module clock (PCLKB)		25	25	
	Peripheral module clock (PCLKC)*2		25	25	
	Peripheral module clock (PCLKD)*3		25	25	

Note 1. The VCC is 2.7 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.21 Operation Frequency Value (Medium-Speed Operating Mode 1B)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	25	25	MHz
	FlashIF clock (FCLK)*1		25	25	
	Peripheral module clock (PCLKA)		25	25	
	Peripheral module clock (PCLKB)		25	25	
	Peripheral module clock (PCLKC)*2		25	25	
	Peripheral module clock (PCLKD)*3		25	25	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.22 Operation Frequency Value (Medium-Speed Operating Mode 2A)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	12.5	25	MHz
	FlashIF clock (FCLK)*1		12.5	25	
	Peripheral module clock (PCLKA)		12.5	25	
	Peripheral module clock (PCLKB)		12.5	25	
	Peripheral module clock (PCLKC)*2		12.5	25	
	Peripheral module clock (PCLKD)*3		12.5	25	

Note 1. The VCC is 2.7 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.23 Operation Frequency Value (Medium-Speed Operating Mode 2B)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	12.5	25	MHz
	FlashIF clock (FCLK)*1		12.5	25	
	Peripheral module clock (PCLKA)		12.5	25	
	Peripheral module clock (PCLKB)		12.5	25	
	Peripheral module clock (PCLKC)*2		12.5	25	
	Peripheral module clock (PCLKD)*3		12.5	25	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.24 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	4	8	MHz
	FlashIF clock (FCLK)*1		4	8	
	Peripheral module clock (PCLKA)		4	8	
	Peripheral module clock (PCLKB)		4	8	
	Peripheral module clock (PCLKC)*2		4	8	
	Peripheral module clock (PCLKD)*3		4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.25 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	
	Peripheral module clock (PCLKA)		32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	
	Peripheral module clock (PCLKC)*2		32.768	32.768	
	Peripheral module clock (PCLKD)*3		32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The A/D converter cannot be used.

5.4 Clock Timing

Table 5.26 Clock Timing

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.25
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2		f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.26
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		µs	
Main clock oscillation stabilization wait time (crystal)*2		$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2		$t_{MAINOSCWT}$	—	100		µs	
LOCO, IWDTCLK clock cycle time		t_{cyc}	7.27	8	8.89	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	112.5	125	137.5	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.27
HOCO clock oscillation frequency		f_{HOCO}	31.680	32	32.320	MHz	Ta = 0 to 50°C
			36.495	36.864	37.233		
			39.600	40	40.400		
			49.500	50	50.500		
			31.520	32	32.480		Ta = -40 to 105°C
			36.311	36.864	37.417		
			39.400	40	40.600		
			49.250	50	50.750		
HOCO clock oscillation stabilization time 1		t_{HOCO1}	—	—	300	µs	Figure 5.28
HOCO clock oscillation stabilization time 2		t_{HOCO2}	—	—	175	µs	Figure 5.29
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	—	—	350	µs	Figure 5.29
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	350	µs	Figure 5.30
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.31
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time*4	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	3.5*3	—	ms	Figure 5.32
PLL clock oscillation stabilization wait time*4		t_{PLLWT2}	—	7	—	ms	
PLL clock power supply stabilization time		t_{PLLPW}	—	—	30	µs	Figure 5.33
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	2	—	—	s	Figure 5.34
Sub-clock oscillation stabilization wait time*5		$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

Note 2. When specifying the main clock oscillator stabilization time, load MOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the main lock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the main clock oscillation stabilization time.
Start using the main clock in the main clock oscillation stabilization wait time (tMAINOSCWT) after setting up the main clock oscillator for operation with the MOSCCR.MOSTP bit.
The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 3. Sum of the main clock oscillation stabilization time and the PLL oscillation stabilization time.
Note 4. The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 5. When specifying the sub-clock oscillation stabilization time, load SOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the sub-clock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the sub-clock oscillation stabilization time. Start using the sub-clock in the sub-clock oscillation stabilization wait time (tSUBOSCWT) after setting up the sub-clock oscillator for operation with the SOSCCR.SOSTP or RCR3.RTCEN bit.

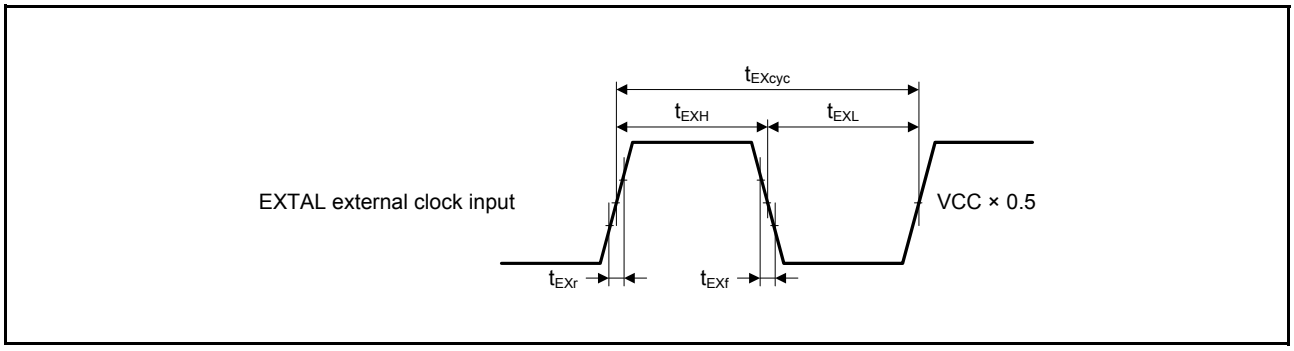


Figure 5.25 EXTAL External Clock Input Timing

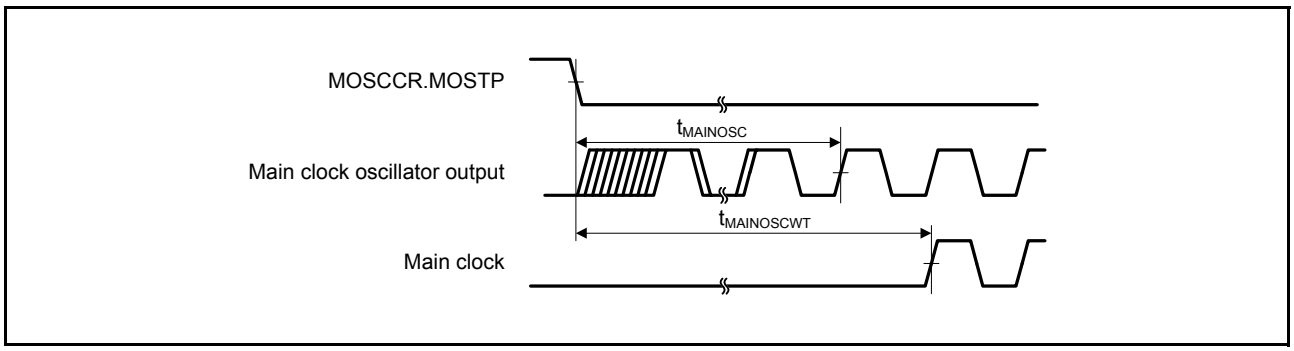


Figure 5.26 Main Clock Oscillation Start Timing

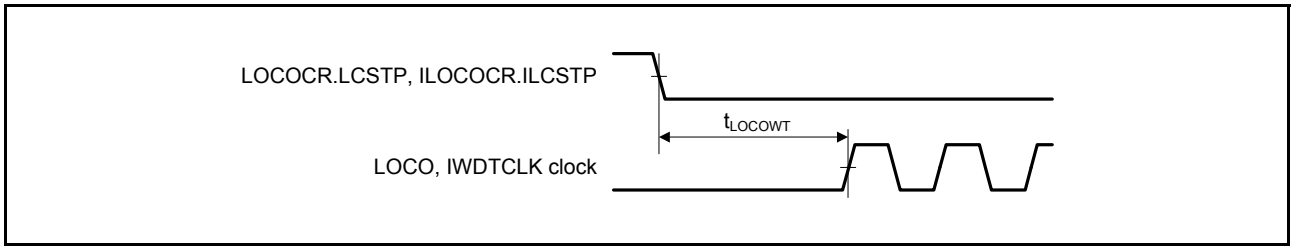


Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing

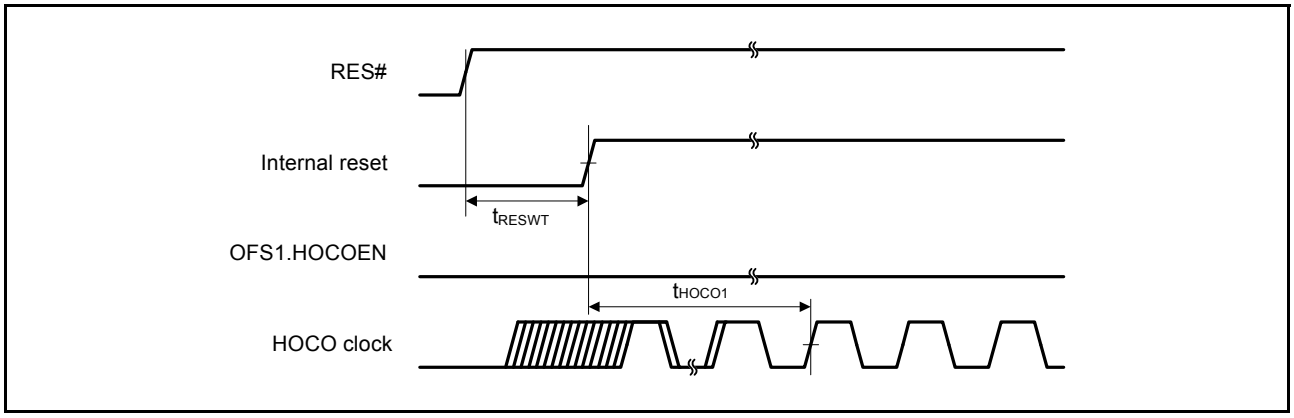


Figure 5.28 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

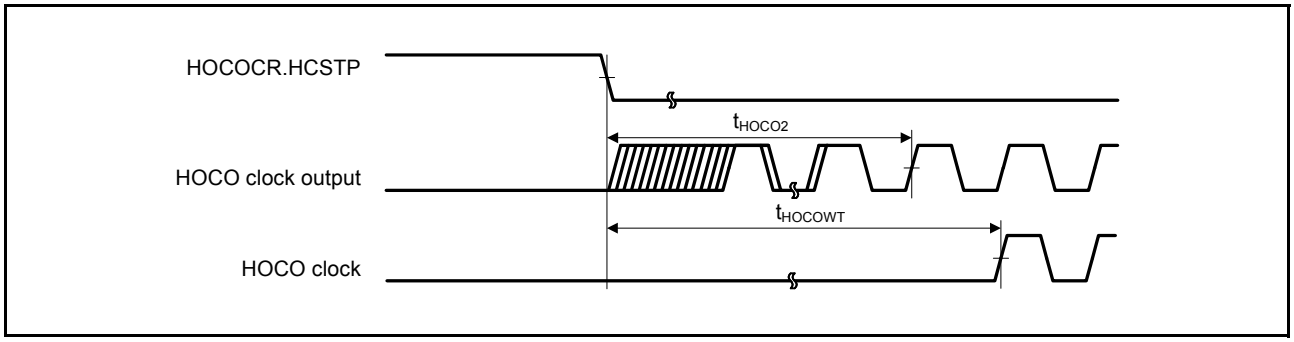


Figure 5.29 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

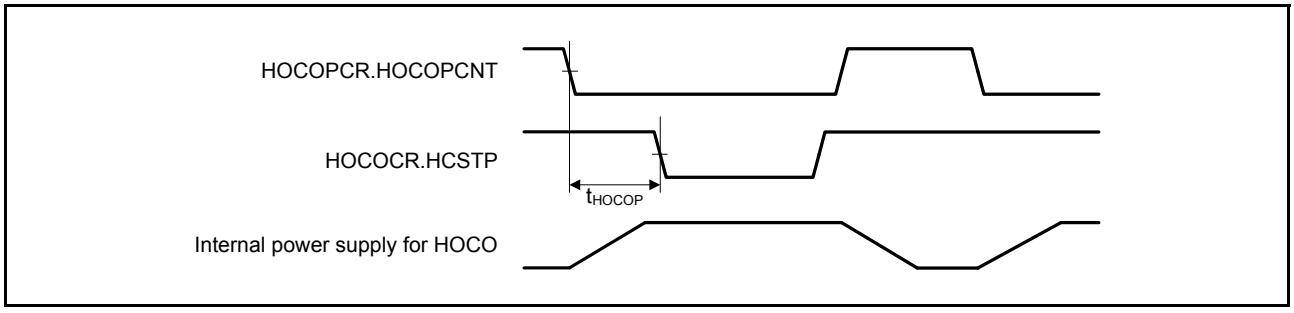


Figure 5.30 HOCO Power Control Timing

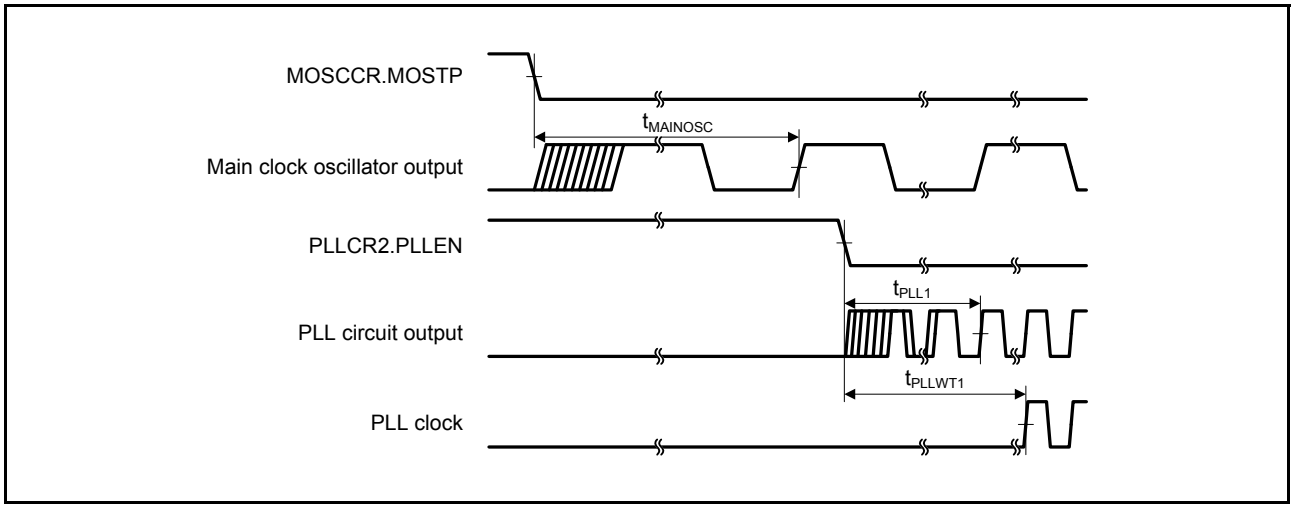


Figure 5.31 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

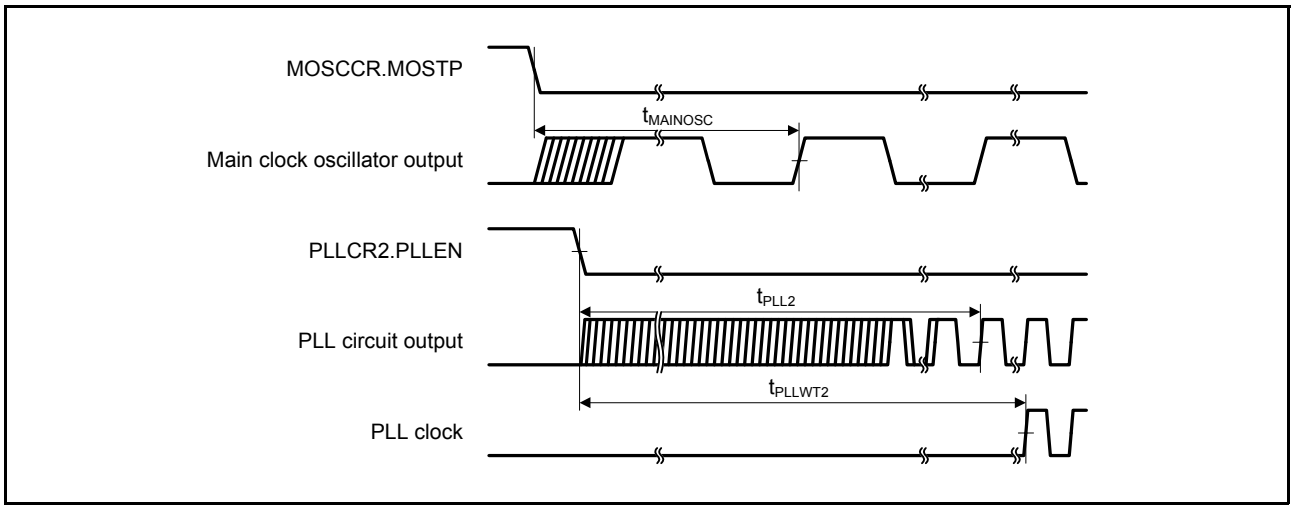


Figure 5.32 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

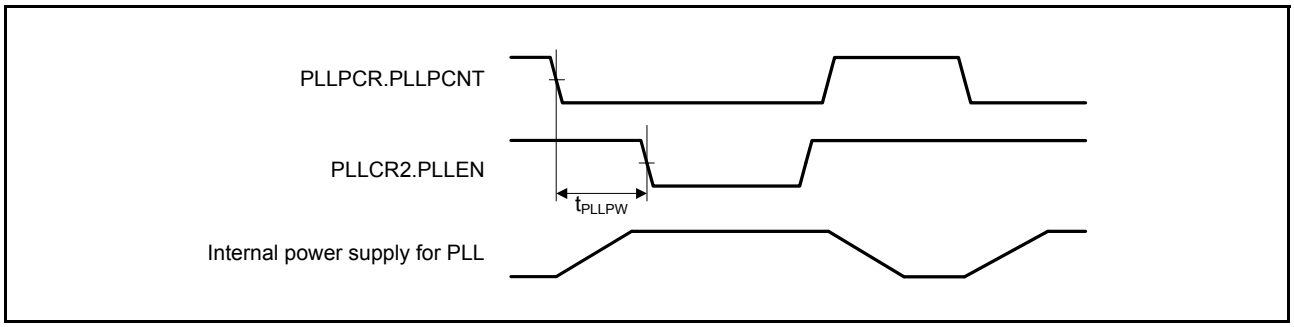


Figure 5.33 PLL Power Control Timing

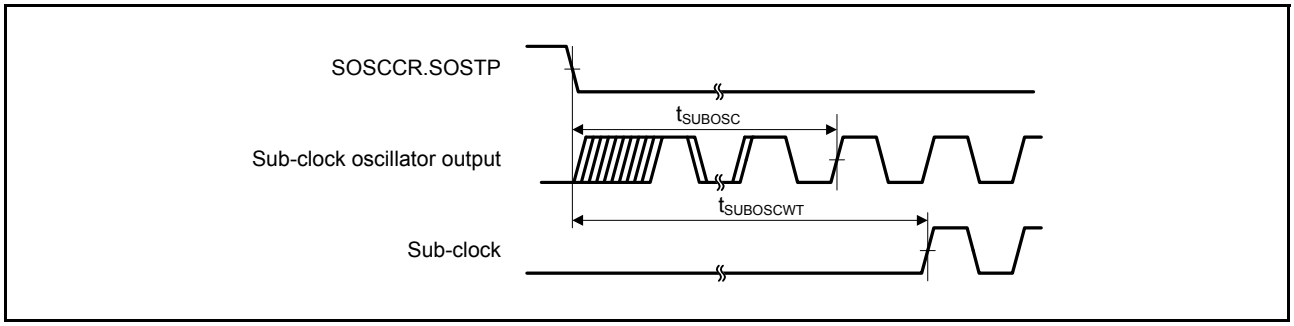


Figure 5.34 Sub-clock Oscillation Start Timing

5.4.1 Reset Timing

Table 5.27 Reset Timing

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	8	—	—	ms	Figure 5.35
	Deep software standby mode	t_{RESWD}	8	—	—	ms	Figure 5.36
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	—	—	912	µs	Figure 5.35
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	—	—	1.4	ms	

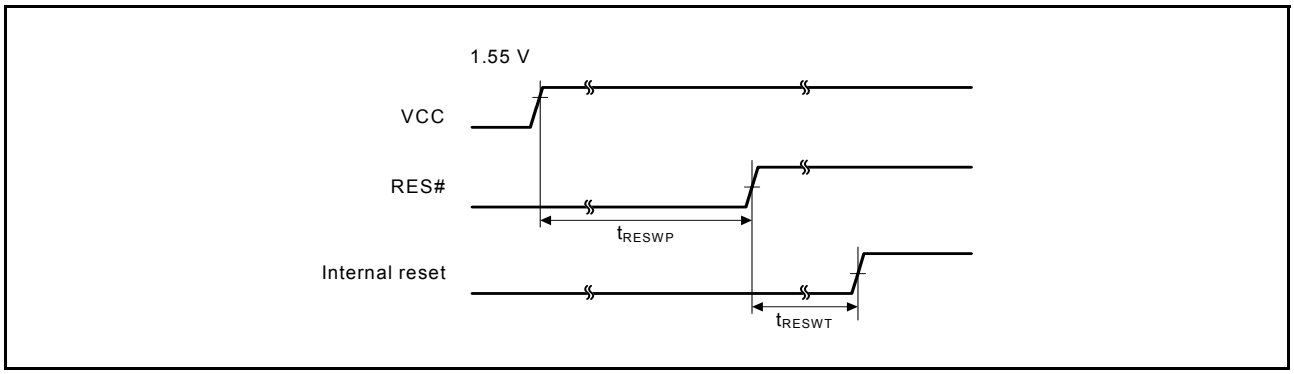


Figure 5.35 Reset Input Timing at Power-On

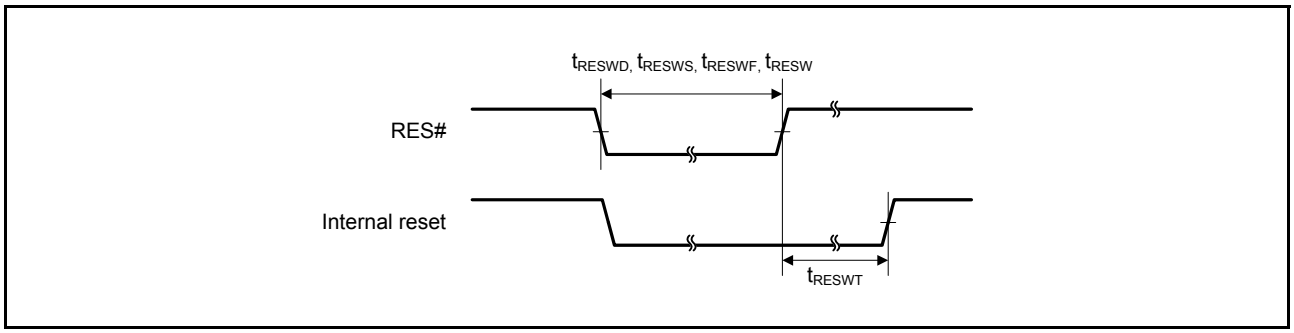


Figure 5.36 Reset Input Timing

5.4.2 Timing of Recovery from Low Power Consumption Modes

Table 5.28 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.37
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	10	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	500	µs	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.37
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	8	ms	Figure 5.38
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	—	—	0.8	ms	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.

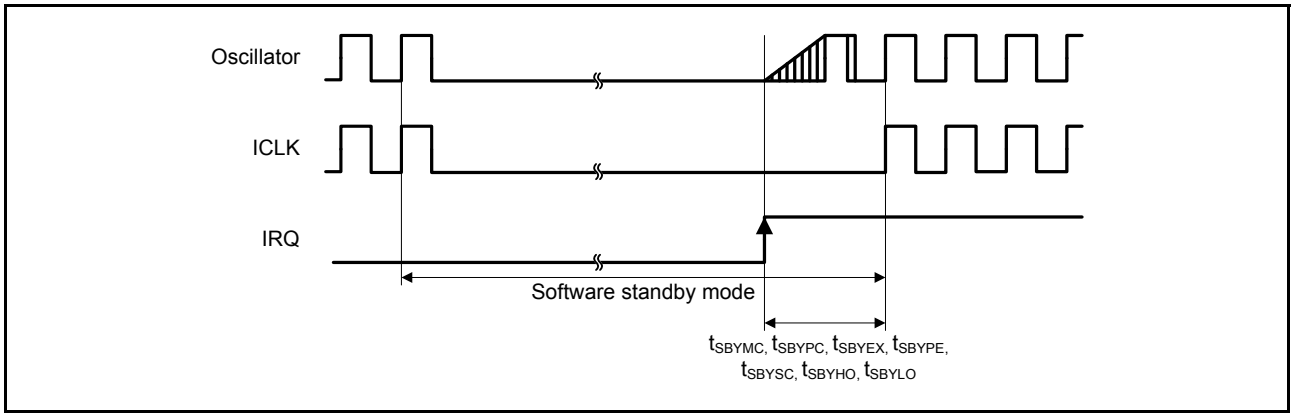


Figure 5.37 Software Standby Mode Cancellation Timing

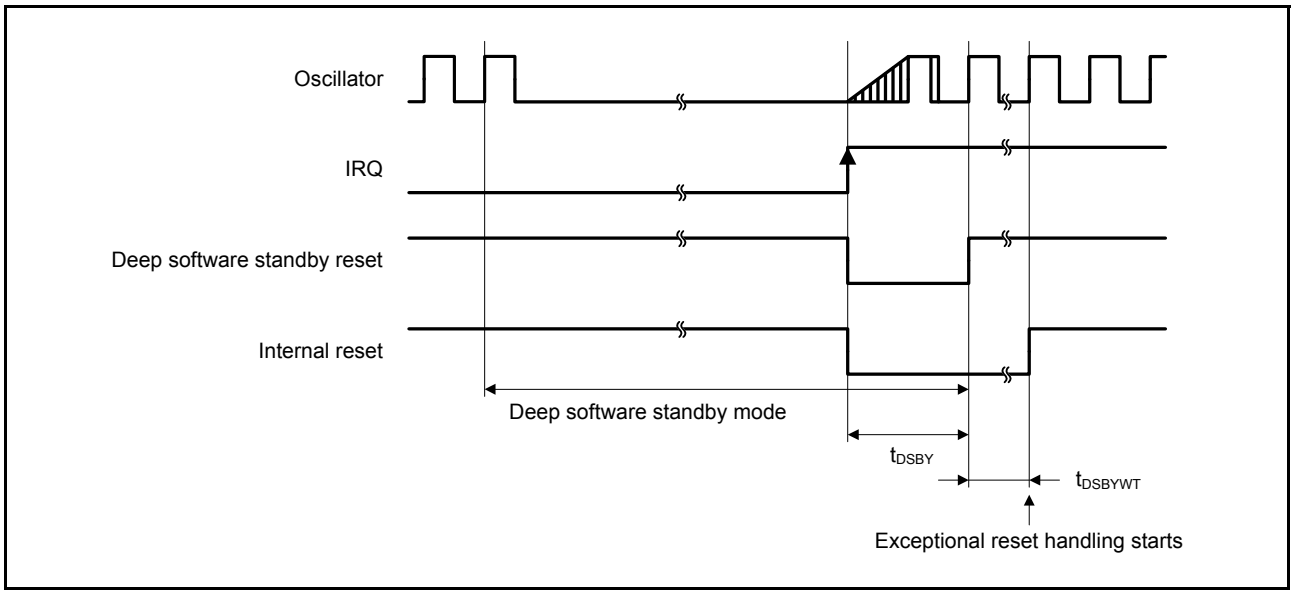


Figure 5.38 Deep Software Standby Mode Cancellation Timing

5.4.3 Control Signal Timing

Table 5.29 Control Signal Timing

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.39
		$t_{c(PCLKB)}$ × 2	—	—	ns	$t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.39
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.40
		$t_{c(PCLKB)}$ × 2	—	—	ns	$t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.40

Note: • 200 ns minimum in deep software standby and software standby modes.

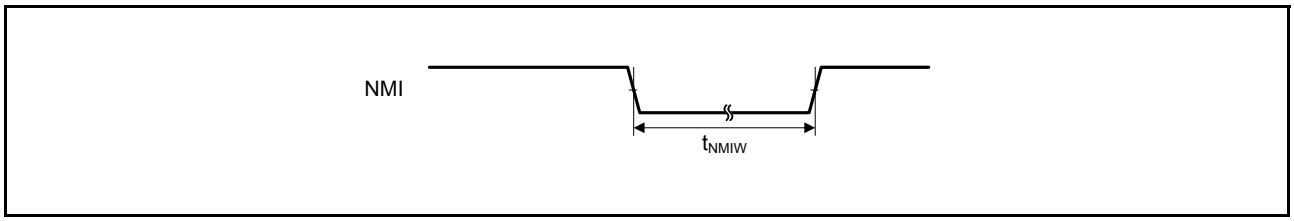


Figure 5.39 NMI Interrupt Input Timing

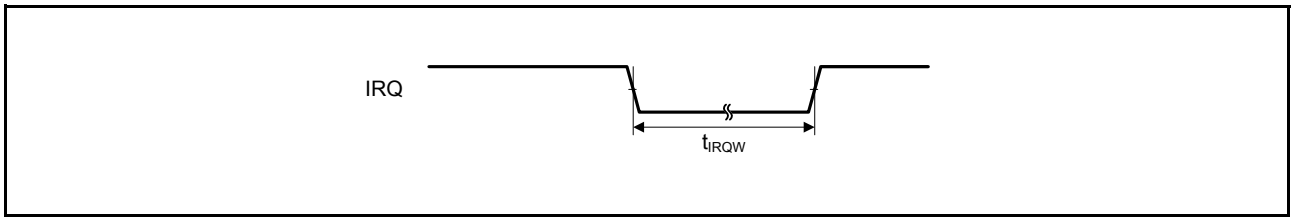


Figure 5.40 IRQ Interrupt Input Timing

5.4.4 Timing of On-Chip Peripheral Modules

Table 5.30 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.41
MTU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.42
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.43
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.44
8-bit timer	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.45
		Both-edge setting		2.5	—		
A/D converter	Trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.48
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle

Table 5.31 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register while 1.8 V ≤ VCC < 2.7 V

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	C = 30 pF Figure 5.46
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	C = 30 pF Figure 5.47
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous (master)	t_{TXD}	—	40	ns	
	Transmit data delay time	Clock synchronous (slave) 2.7 V ≤ VCC ≤ 3.6 V		—	65		
		Clock synchronous (slave) 1.8 V ≤ VCC < 2.7 V		—	85		
	Receive data setup time	Clock synchronous (master) 2.7 V ≤ VCC ≤ 3.6 V	t_{RXS}	65	—	ns	
		Clock synchronous (master) 1.8 V ≤ VCC < 2.7 V		75	—		
		Clock synchronous (slave)		40	—		
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.32 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master 2.7 V ≤ VCC ≤ 3.6 V	t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF Figure 5.49
		Master 1.8 V ≤ VCC < 2.7 V		4	4096		
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	10	ns	
		Input		—	1	µs	
	Data input setup time	Master 2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	4	—	ns	C = 30 pF Figure 5.50 to Figure 5.53
		Master 1.8 V ≤ VCC < 2.7 V		16	—		
		Slave		$20 - t_{Pcyc}$	—		
	Data input hold time	Master	t_H	t_{Pcyc}	—	ns	
		Slave		$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	—	10	ns	
		Slave 2.7 V ≤ VCC ≤ 3.6 V		—	$3 \times t_{Pcyc} + 55$		
		Slave 1.8 V ≤ VCC < 2.7 V		—	$3 \times t_{Pcyc} + 72$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	10	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	20	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	5	t_{Pcyc}	C = 30 pF Figure 5.52 and Figure 5.53
	Slave output release time	2.7 V ≤ VCC ≤ 3.6 V	t_{REL}	—	4	t_{Pcyc}	
		1.8 V ≤ VCC < 2.7 V		—	5		

Note 1. t_{Pcyc}: PCLK cycle

Table 5.33 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register while 1.8 V ≤ VCC < 2.7 V

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF Figure 5.49
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (Master)	2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	65	—	ns	C = 30 pF Figure 5.50 to Figure 5.53
		1.8 V ≤ VCC < 2.7 V		75	—		
	Data input setup time (Slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time		t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time (Master)		t_{OD}	—	40	ns	
	Data output delay time (Slave)	2.7 V ≤ VCC ≤ 3.6 V		—	65		
		1.8 V ≤ VCC < 2.7 V		—	85		
	Data output hold time		t_{OH}	–10	—	ns	
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	5	t_{Pcyc}	C = 30 pF Figure 5.52 and Figure 5.53
	Slave output release time	2.7 V ≤ VCC ≤ 3.6 V	t_{REL}	—	5	t_{Pcyc}	
		1.8 V ≤ VCC < 2.7 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle

Table 5.34 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.54
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.54
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b indicates the total capacity of the bus line.

Table 5.35 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.54
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*2	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	Figure 5.54
	SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*2	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{Pcyc}: PCLK cycle
Note 1. C_b indicates the total capacity of the bus line.
Note 2. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

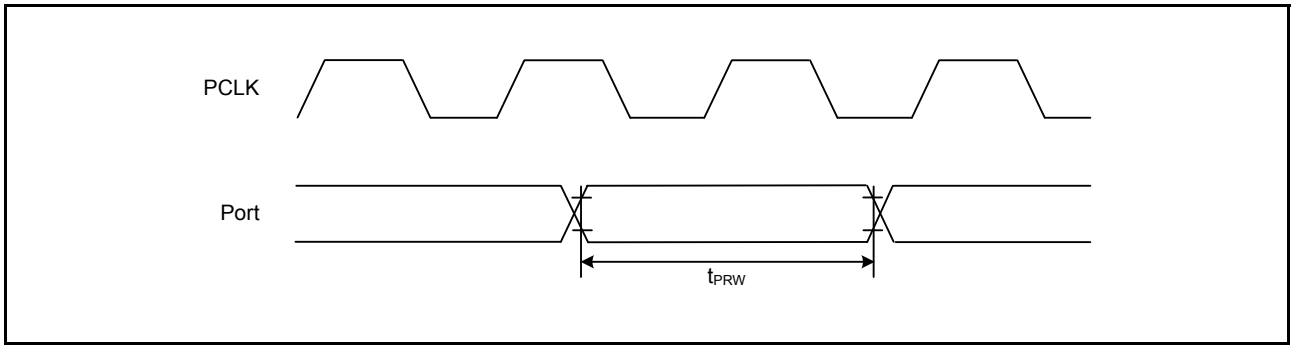


Figure 5.41 I/O Port Input Timing

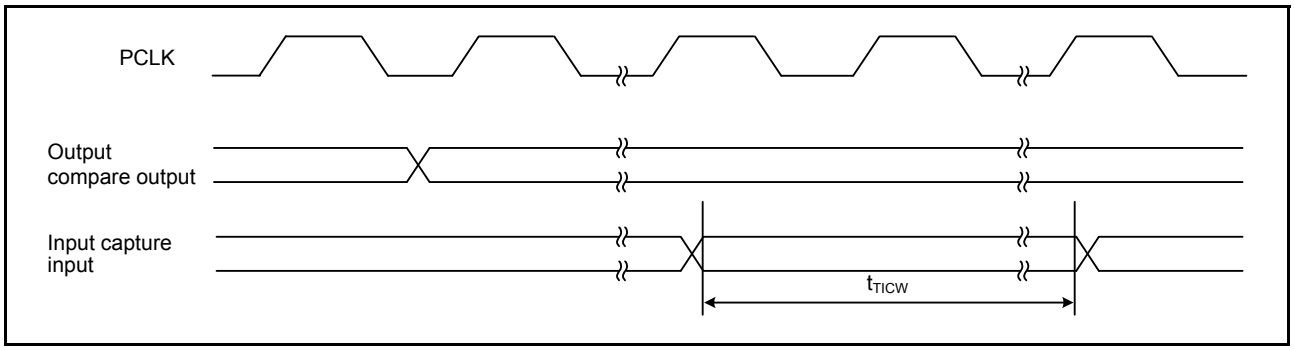


Figure 5.42 MTU Input/Output Timing

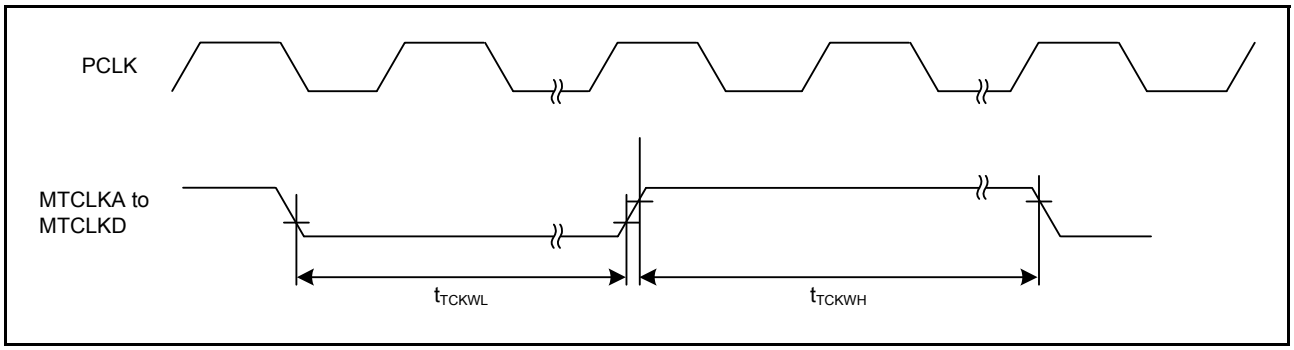


Figure 5.43 MTU Clock Input Timing

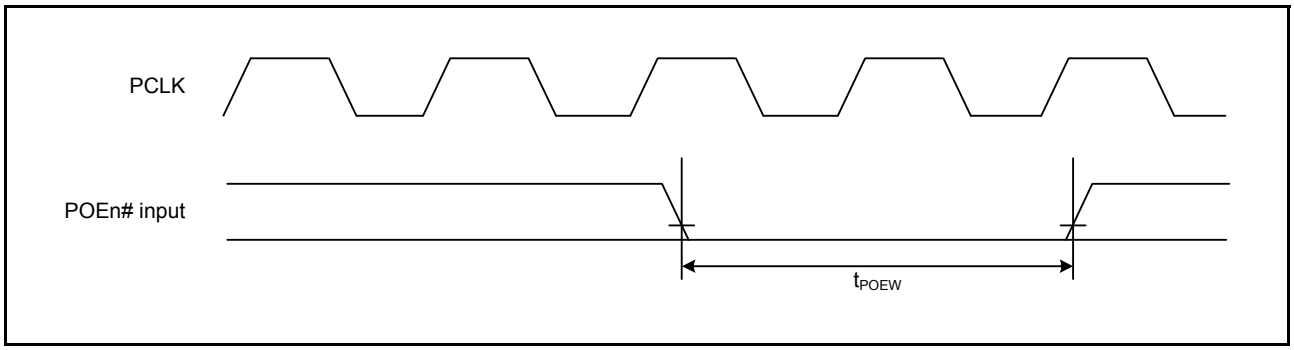


Figure 5.44 POE# Input Timing

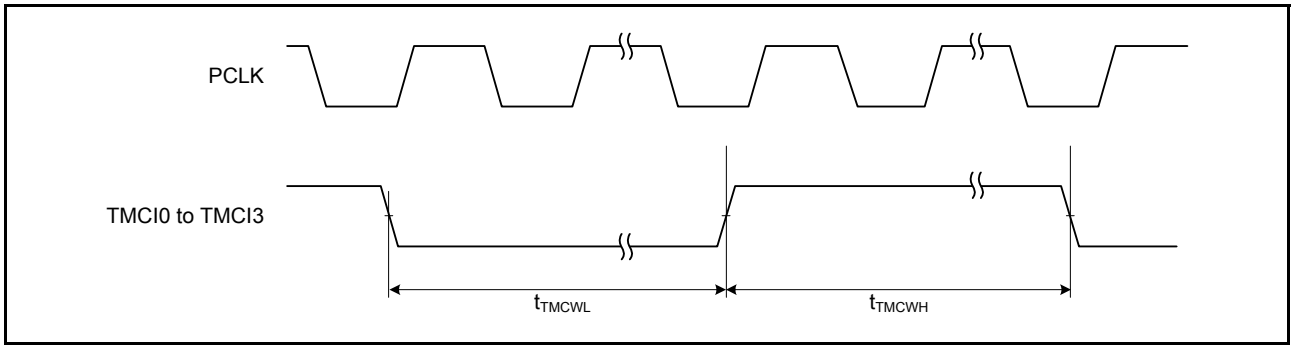


Figure 5.45 8-Bit Timer Clock Input Timing

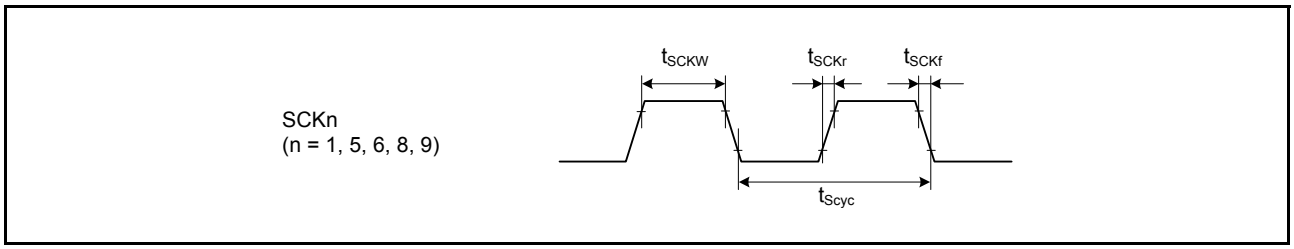


Figure 5.46 SCK Clock Input Timing

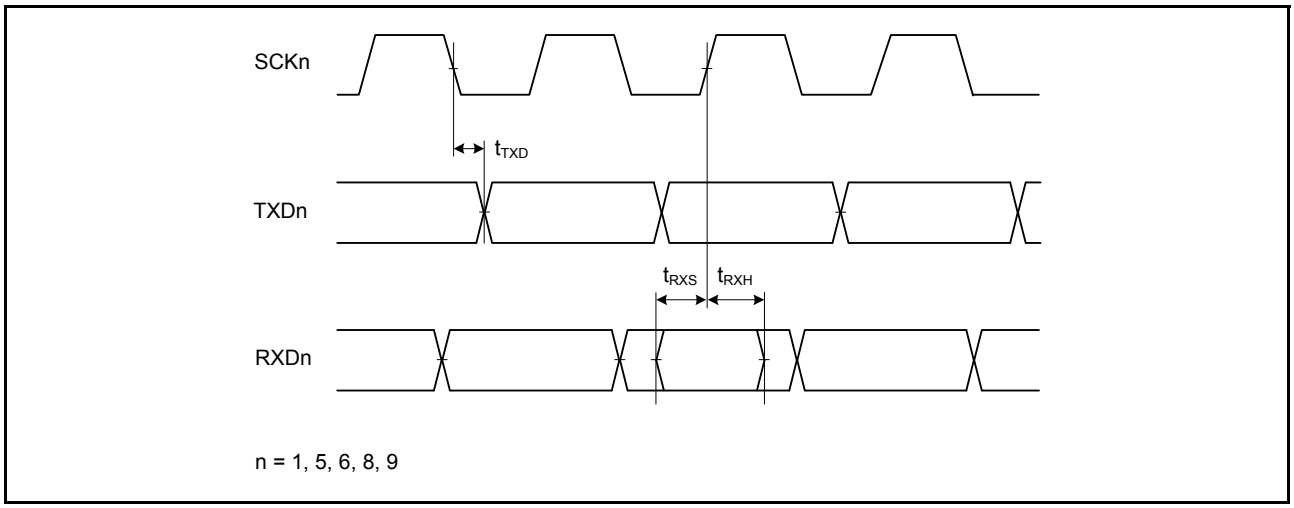


Figure 5.47 SCI Input/Output Timing: Clock Synchronous Mode

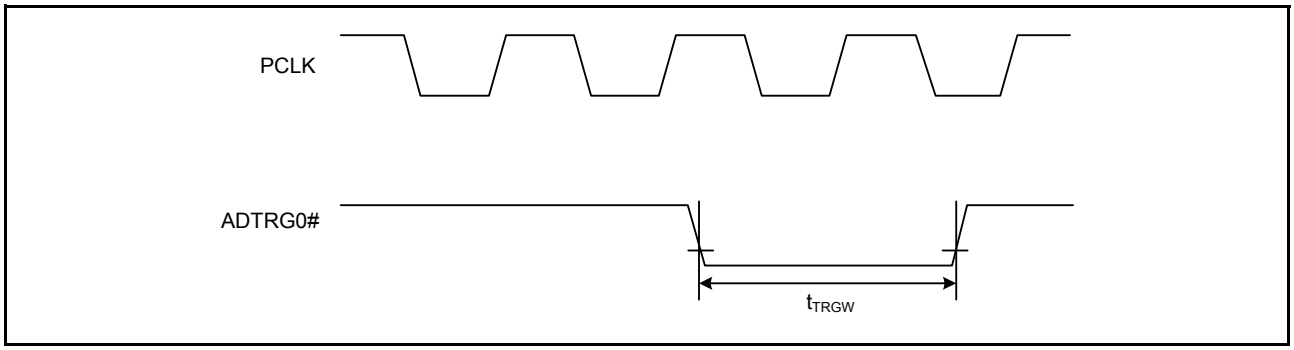


Figure 5.48 A/D Converter External Trigger Input Timing

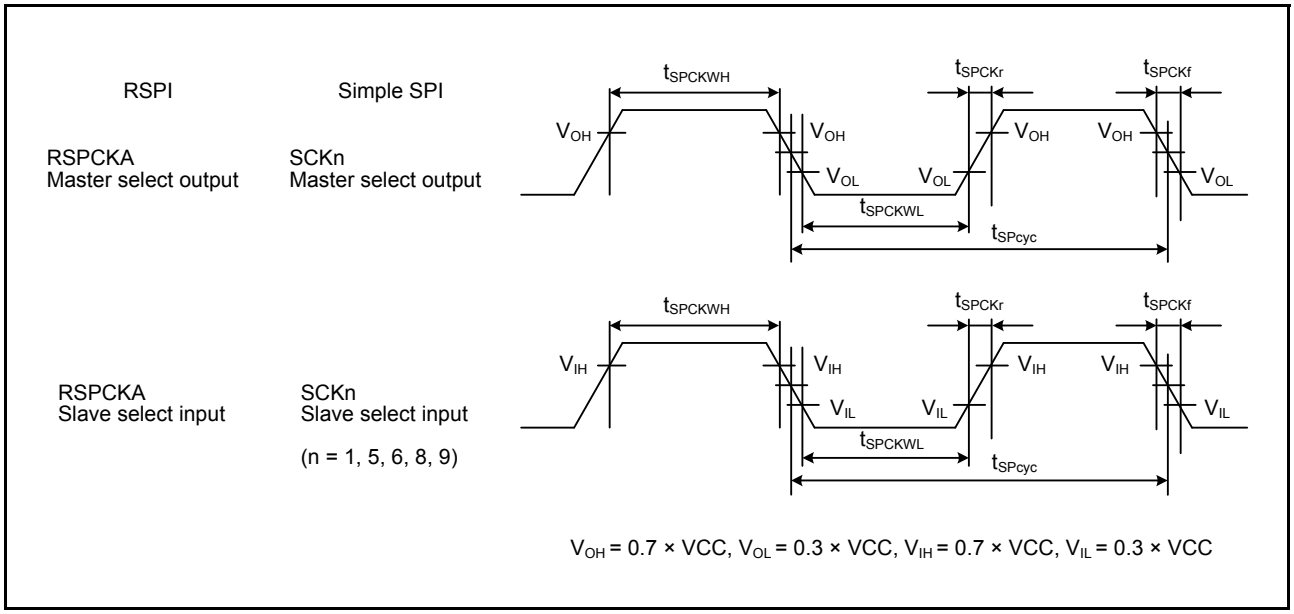


Figure 5.49 RSPI Clock Timing and Simple SPI Clock Timing

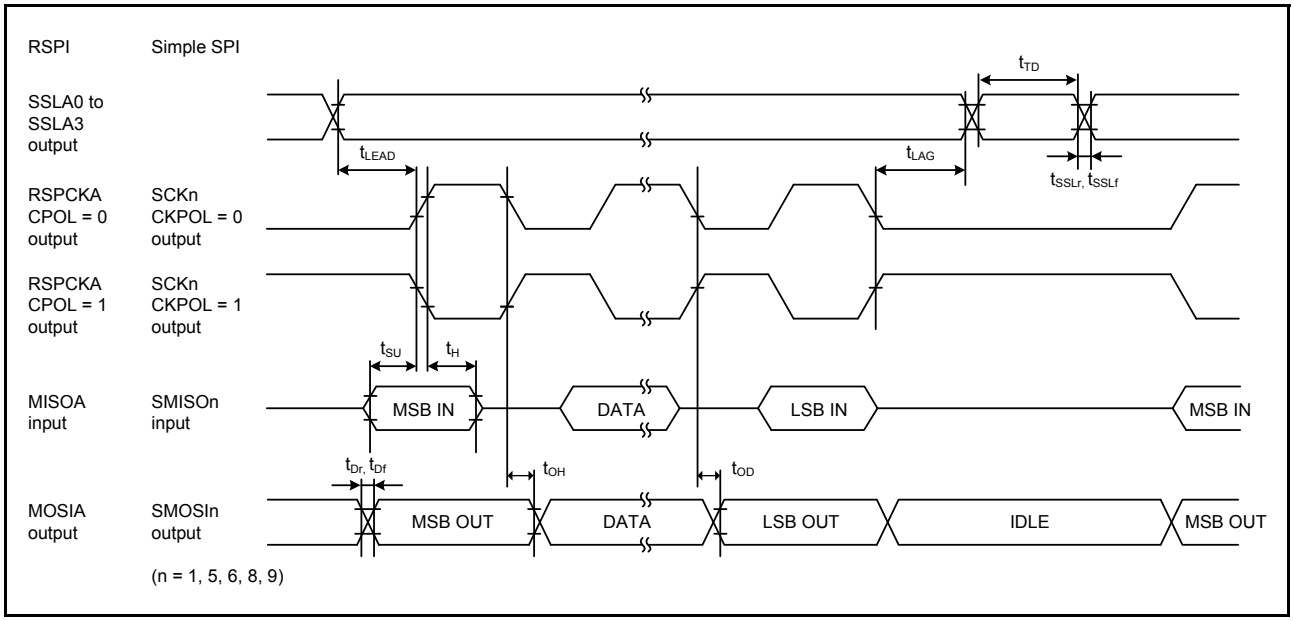


Figure 5.50 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

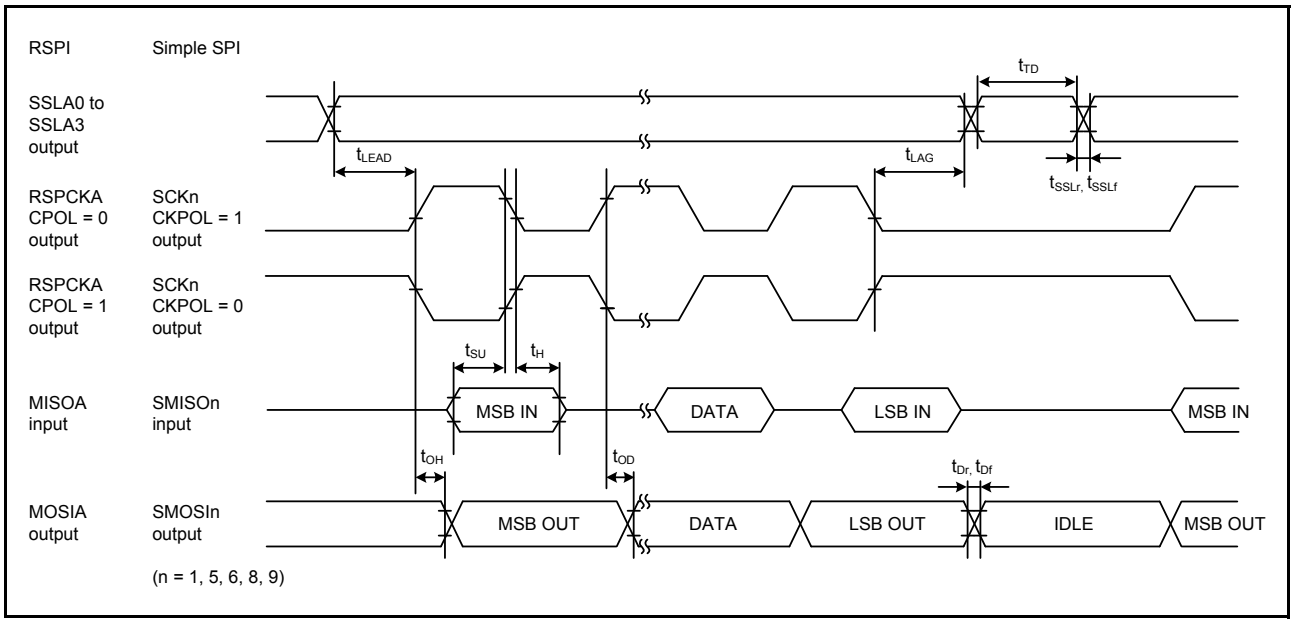


Figure 5.51 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

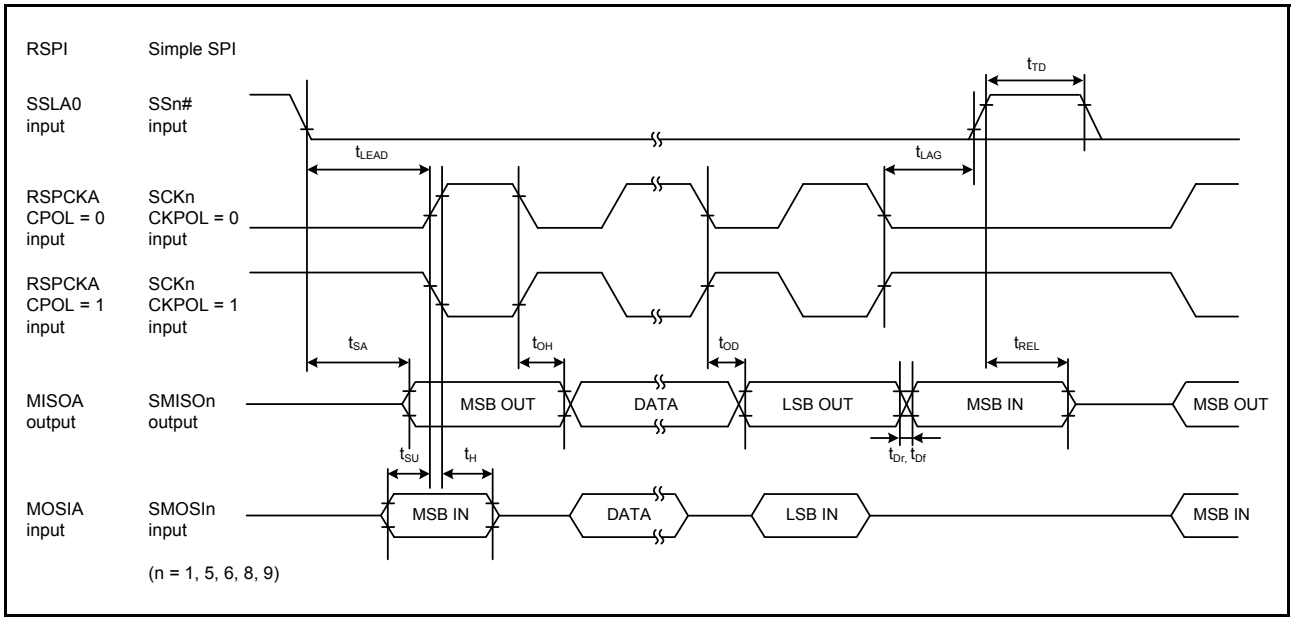


Figure 5.52 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

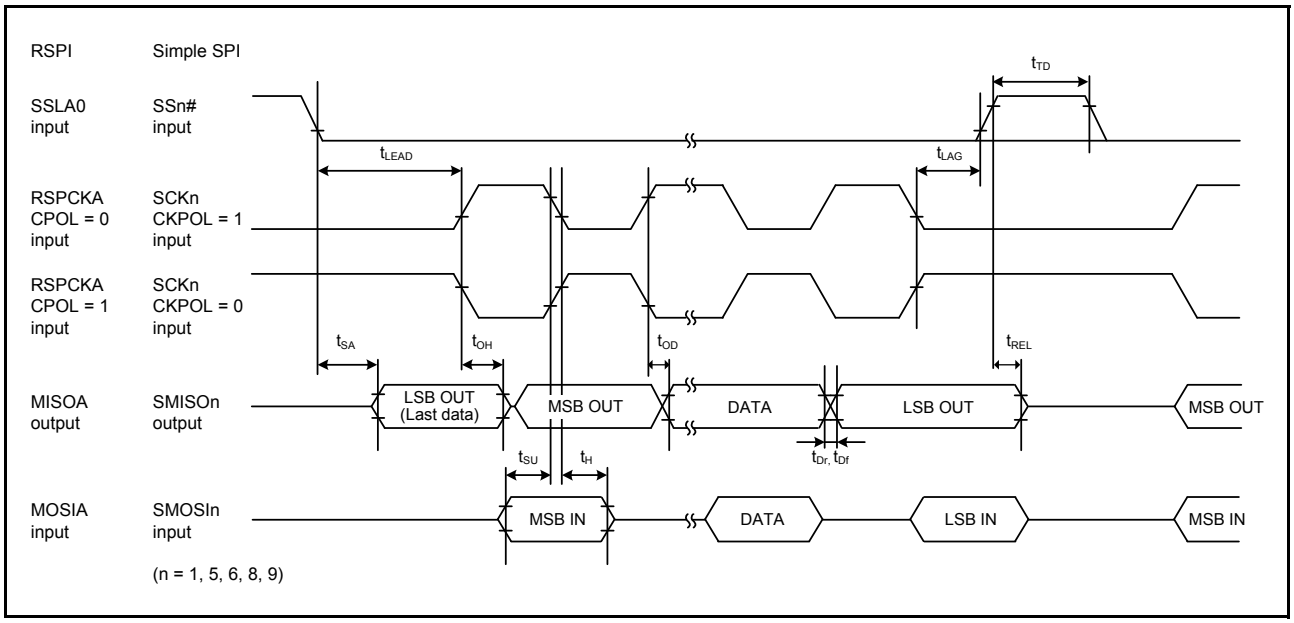


Figure 5.53 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

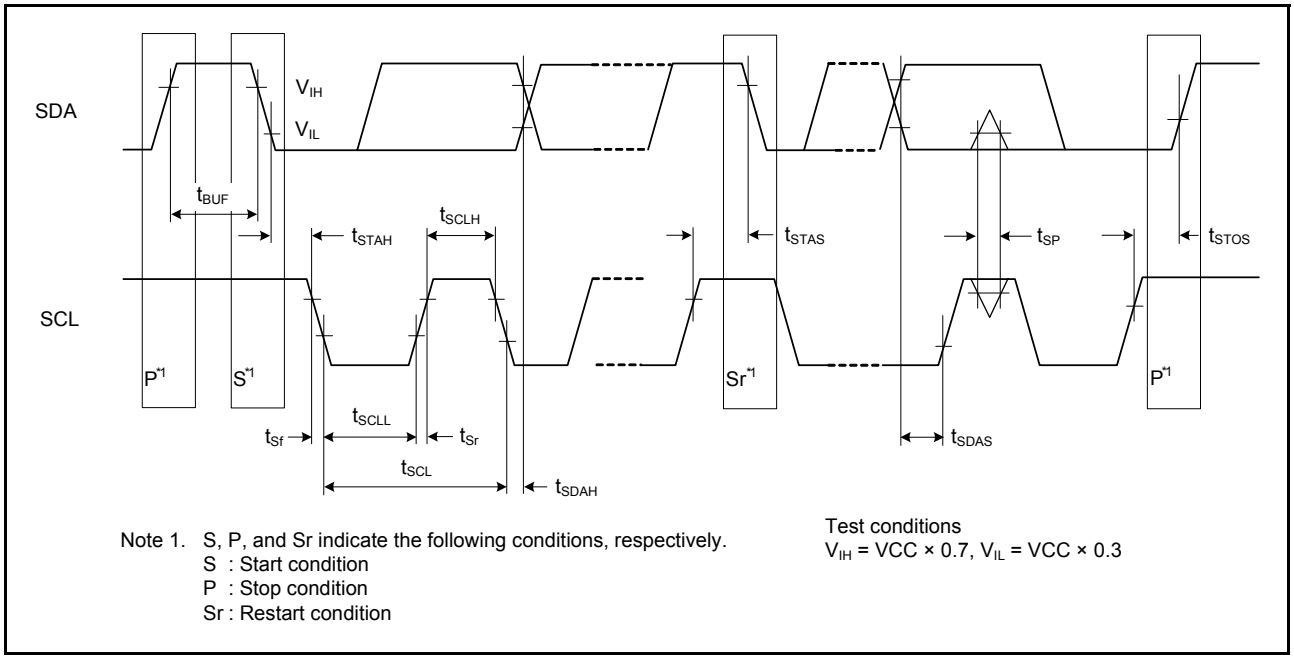


Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

5.5 ΔΣ A/D Conversion Characteristics

Table 5.36 ΔΣ A/D Conversion Characteristics

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, fPCLKC = 25 MHz, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	24	24	24	Bit	
Reference voltage (VREFDSH)	590	600	610	mV	EXREF = 0
BGR_BO pin applied voltage	—	1220	—	mV	EXREF = 1
BGR_BO pin voltage to reference voltage conversion coefficient	—	0.492	—	—	EXREF = 1
BGR_BO pin impedance	135	—	—	kΩ	EXREF = 1
Reference voltage temperature coefficient	—	—	30	ppm/°C	
Gain (×1)	—	1.00	—	—	
Gain (×2)	—	2.00	—	—	
Gain (×4)	—	4.00	—	—	
Gain (×8)	—	8.00	—	—	
Gain (×16)	—	16.00	—	—	
Gain (×32)	—	32.00	—	—	
Gain (×64)	—	64.00	—	—	
Differential input voltage (ANDSiP - ANDSiN) (i = 0 to 3)	–500.0	—	500.0	mV	GAIN = 000b, Figure 5.55
	–250.0	—	250.0	mV	GAIN = 001b
	–125.0	—	125.0	mV	GAIN = 010b
	–62.5	—	62.5	mV	GAIN = 011b
	–31.2	—	31.2	mV	GAIN = 100b
	–14.4	—	14.4	mV	GAIN = 101b
	–5.0	—	5.0	mV	GAIN = 110b
Differential input Common mode voltage	—	700.0	—	mV	
Single-ended input voltage	–500.0	—	500.0	mV	GAIN = 00b, Figure 5.56
	–250.0	—	250.0	mV	GAIN = 01b
	–125.0	—	125.0	mV	GAIN = 10b
Conversion with the ΔΣ modulator only Differential input voltage	–500.0	—	500.0	mV	GAIN = 000b, 001b, 010b, 011b, 100b (DSADGSR0 to 3) GAIN = 00b, 01b, 10b (DSADGSR4 to 6)
	–250.0	—	250.0	mV	GAIN = 101b (DSADGSR0 to 3)
	–125.0	—	125.0	mV	GAIN = 110b (DSADGSR0 to 3)
Conversion with the ΔΣ modulator only Common mode input voltage	—	700.0	—	mV	
PGA input pin bias voltage	—	700.0	—	mV	
PGA output common mode voltage	—	700.0	—	mV	
Reference voltage startup time	—	1	5	ms	
PGA and ΔΣ modulator startup time	—	—	0.1	ms	
Input pull-up resistor	120	200	—	kΩ	
Input impedance for differential input (×1, ×2, ×4, ×8)	40	66	—	kΩ	
Input impedance for differential input (×16, ×32, ×64)	30	50	—	kΩ	
Input impedance for single-ended input (×1)	48	80	—	kΩ	
Input impedance for single-ended input (×2)	51	86	—	kΩ	

Item	Min.	Typ.	Max.	Unit	Test Conditions	
Input impedance for single-ended input (×4)	54	91	—	kΩ		
Oversampling frequency	3.125	3.125	3.125	MHz		
Oversampling period	0.32	0.32	0.32	µs		
Conversion time	81.92	—	245.76	µs		
Sampling frequency	4.07	—	12.21	kHz		
SNDR (Gain: ×1 Input amplitude: 500.0 mV)	—	80	—	dB		Sampling frequency = 12.21 kHz Clock source: Resonator
	—	85	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×2 Input amplitude: 250.0 mV)	—	80	—	dB		
	—	85	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×4 Input amplitude: 125.0 mV)	—	78	—	dB		
	—	83	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×8 Input amplitude: 62.5 mV)	—	75	—	dB		
	—	80	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×16 Input amplitude: 31.2 mV)	—	71	—	dB		
	—	76	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×32 Input amplitude: 14.4 mV)	—	64	—	dB		
	—	69	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×64 Input amplitude: 5 mV)	—	54	—	dB		
	—	59	—	dB	Bandwidth = up to 1.7 kHz	

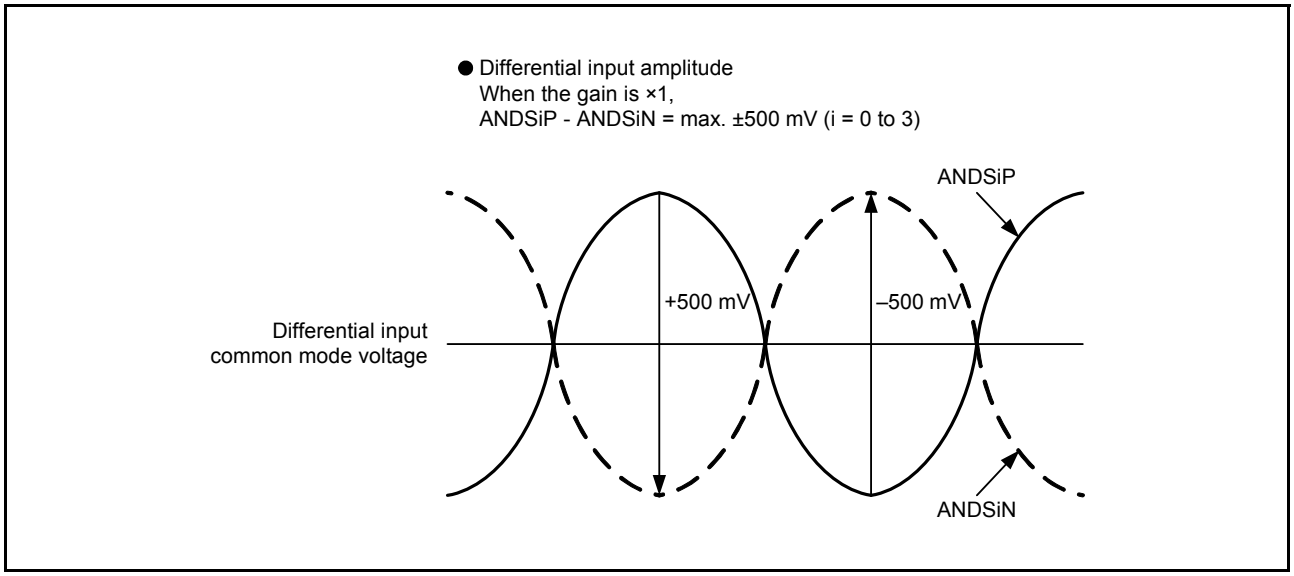


Figure 5.55 Differential Input Amplitude

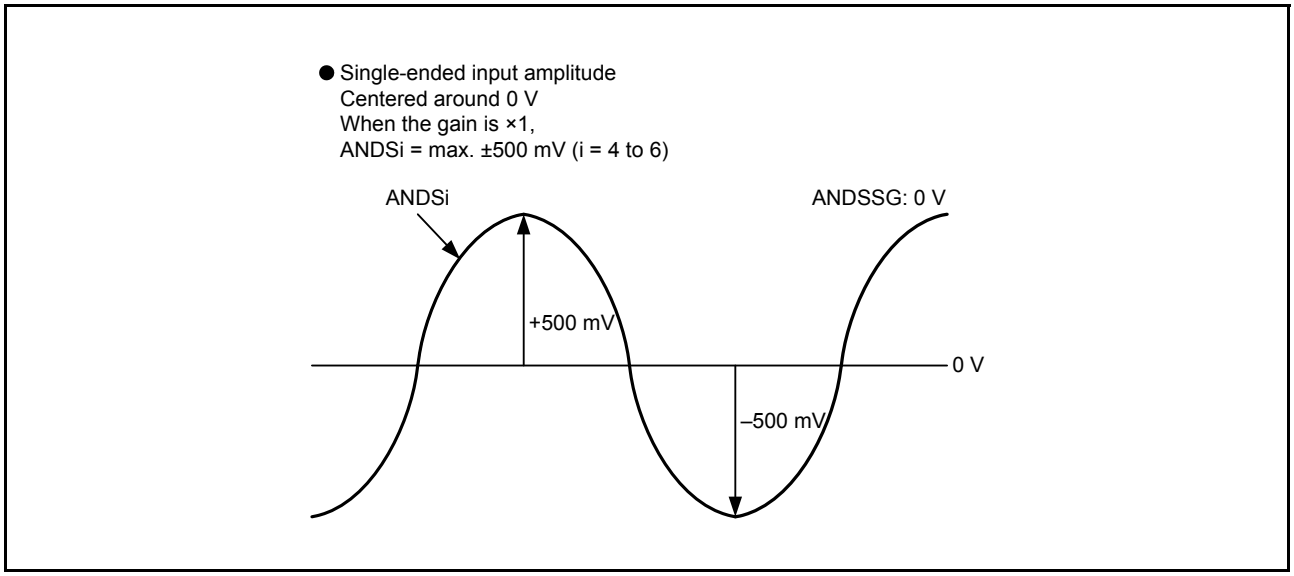


Figure 5.56 Single-ended Input Amplitude

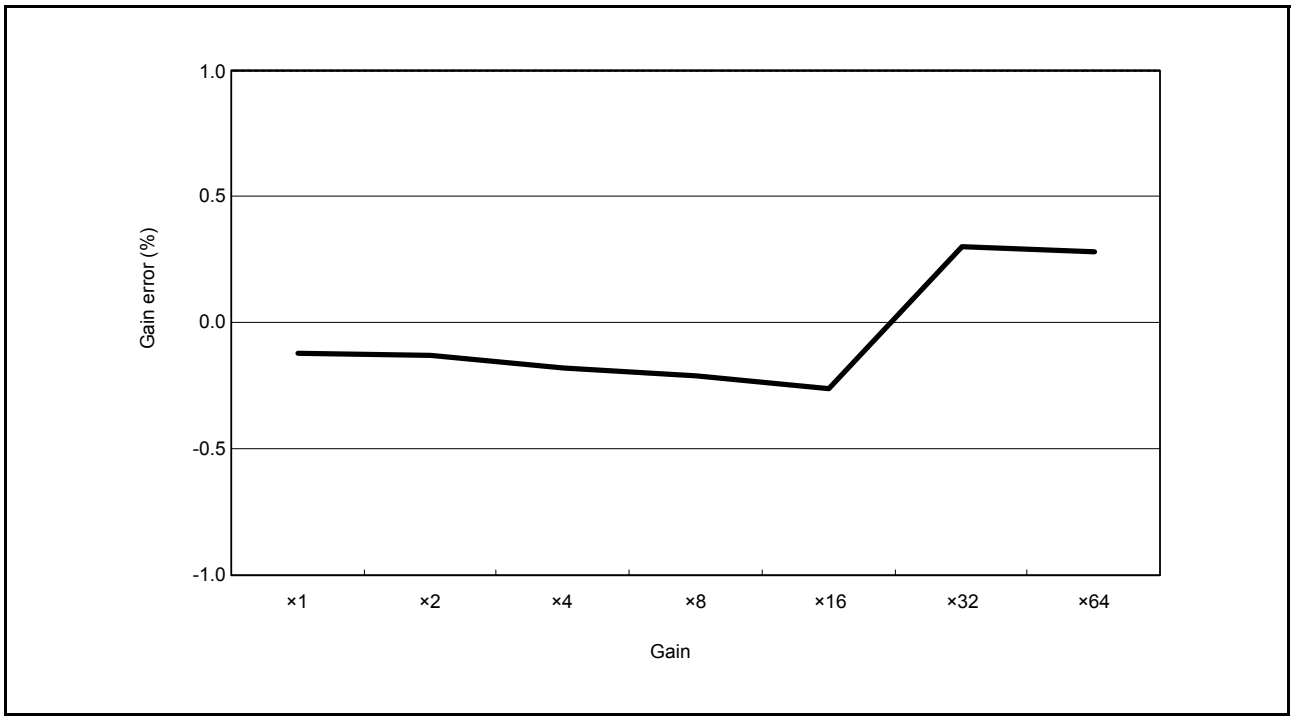
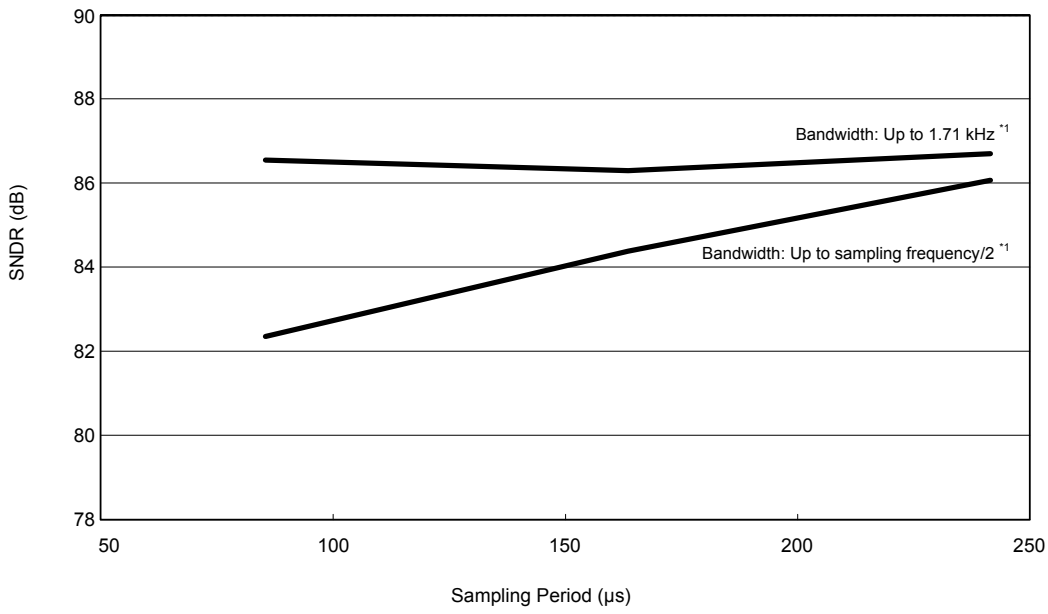
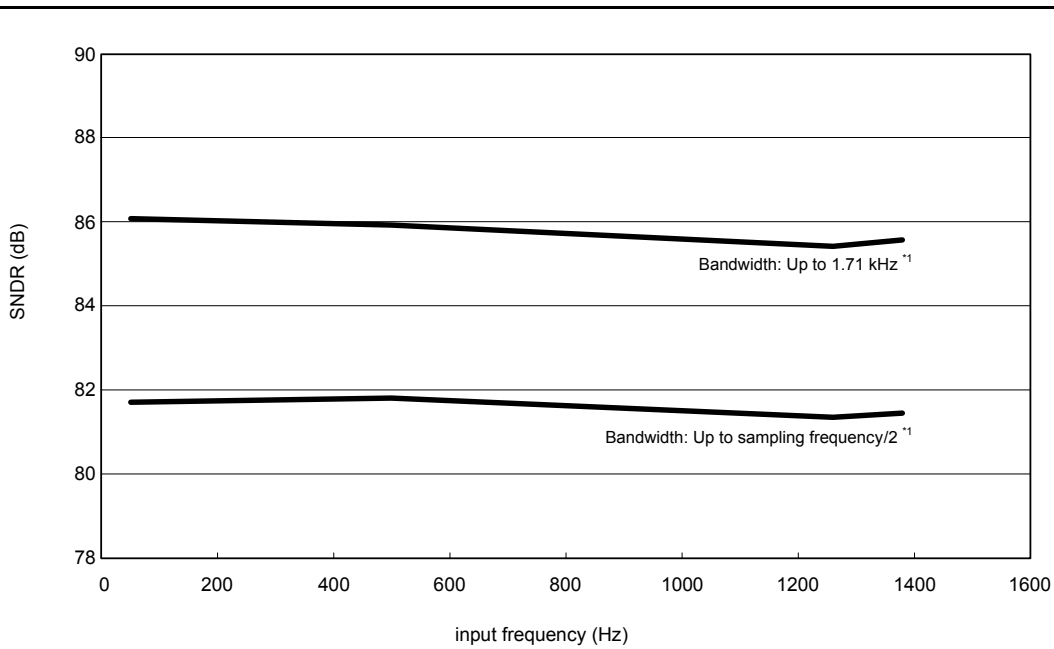


Figure 5.57 Gain Error (Reference Data)



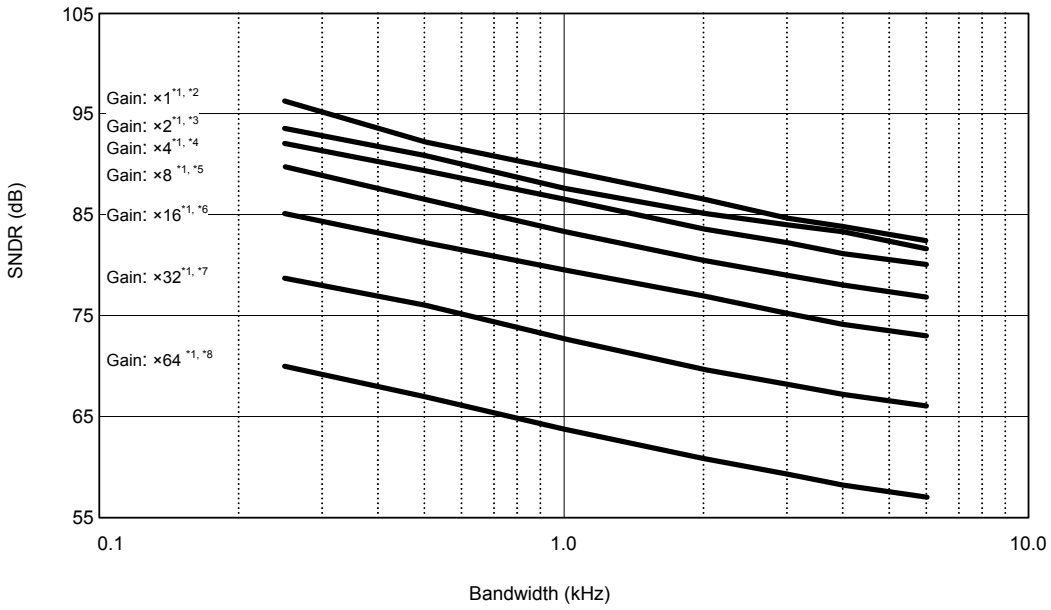
Note 1. Gain: ×1, input frequency: 50 Hz, input amplitude: 500 mV

Figure 5.58 Sampling Period Dependency of SNDR (Reference Data)



Note 1. Gain: ×1, sampling period: 81.92 µs, input amplitude: 500 mV

Figure 5.59 Input Frequency Dependency of SNDR (Reference Data)



Note 1. Input frequency: 50 Hz, sampling period: 81.92 µs
Note 2. Input amplitude: 500.0 mV
Note 3. Input amplitude: 250.0 mV
Note 4. Input amplitude: 125.0 mV
Note 5. Input amplitude: 62.5 mV
Note 6. Input amplitude: 31.2 mV
Note 7. Input amplitude: 14.4 mV
Note 8. Input amplitude: 5.0 mV

Figure 5.60 Bandwidth Dependency of SNDR (Reference Data)

5.6 A/D Conversion Characteristics

Table 5.37 A/D Conversion Characteristics (1)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0*3,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, fT_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	25	MHz	
Resolution		—	—	10	Bit	
Conversion time*1 (Operation at fPCLKD = 25 MHz)	Permissible signal source impedance (Max.) = 1.5 kΩ	2.0 (1.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.0	±2.0	LSB	
Full-scale error		—	±1.0	±2.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy*4		—	±1.0	±3.0	LSB	
DNL differential nonlinearity error*4		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.0	±2.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, fullscale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

Note 4. The characteristics of the channel AN4 on a 64-pin LQFP may inferior to the values on this table; ±1.5 LSB in Absolute accuracy, ±0.5 LSB in DNL differential nonlinearity error.

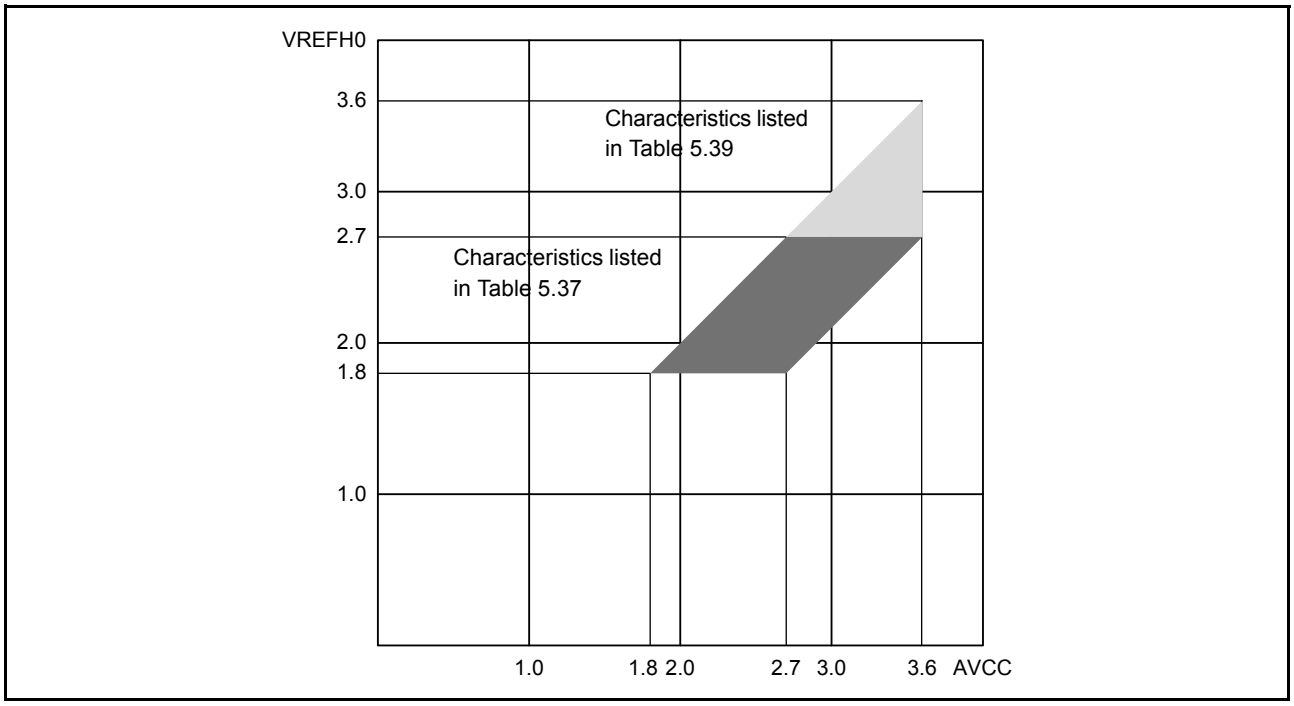


Figure 5.61 AVCC to VREFH0 Voltage Range

Table 5.38 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
Ta = –40 to +105

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.35	1.50	1.65	V	

Table 5.39 A/D Conversion Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, 1.8 V ≤ VREFH0 ≤ 2.7 V, AVCC0 –0.9 V ≤ VREFH0 ≤ AVCC0*3,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	12.5	MHz	
Resolution		—	—	10	Bit	
Conversion time*1 (Operation at fPCLKD = 12.5 MHz)	Permissible signal source impedance (Max.) = 1.5 kΩ	4.0 (2.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.5	±3.0	LSB	
Full-scale error		—	±1.5	±3.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy*4		—	±2.0	±4.0	LSB	
DNL differential nonlinearity error*4		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, fullscale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

Note 4. The characteristics of the channel AN4 on a 64-pin LQFP may inferior to the values on this table; ±1.5 LSB in Absolute accuracy, ±0.5 LSB in DNL differential nonlinearity error.

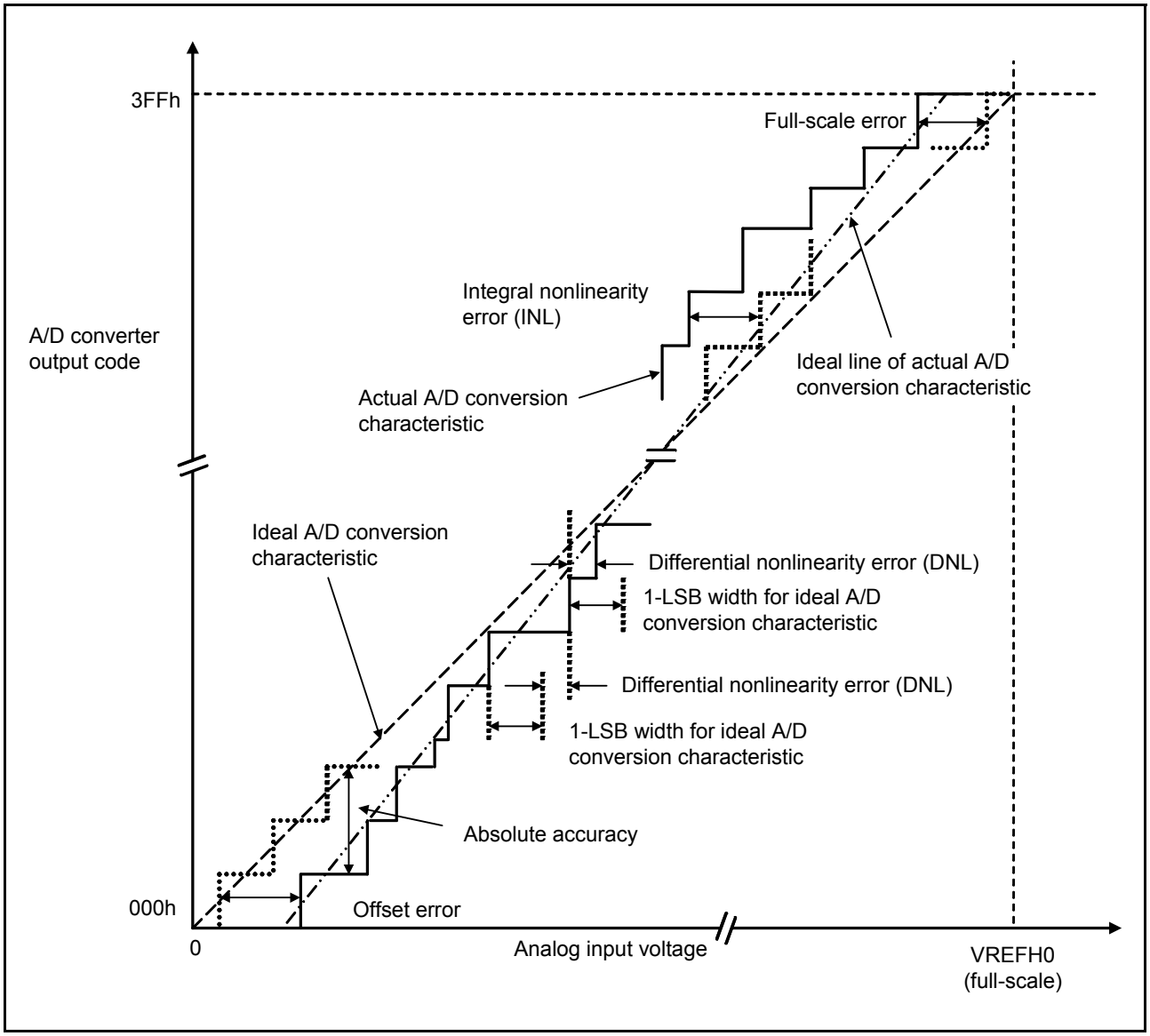


Figure 5.62 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 10-bit resolution is used and if reference voltage VREFH0 = 2.56 V, then 1-LSB width becomes 2.5 mV, and 0 mV, 2.5 mV, 5.0 mV, ... are used as analog input voltages.

If analog input voltage is 20 mV, absolute accuracy = ±4 LSB means that the actual A/D conversion result is in the range of 004h to 00Ch though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.7 D/A Conversion Characteristics

Table 5.40 D/A Conversion Characteristics (1)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±3.0	±5.0	LSB	4-MΩ resistive load
	—	—	±4.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

Table 5.41 D/A Conversion Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH =1.8 V to AVCC0,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	10.0	µs	20-pF capacitive load
Absolute accuracy	—	±5.0	±6.0	LSB	4-MΩ resistive load
	—	—	±5.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

5.8 Temperature Sensor Characteristics

Table 5.42 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCCA = VREFH0 = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy		—	—	±1.0	—	°C	
Temperature slope	1.8 ≤ AVCC0 < 2.7	—	—	7.27	—	mV/°C	PGAGAIN = 00b
	2.7 ≤ AVCC0 < 3.6		—	10.46	—		PGAGAIN = 01b
	AVCC0 = 3.6		—	13.98	—		PGAGAIN = 10b
Output voltage (@25°C)		—	—	1.375	—	V	VCC = 3.6 V
Temperature sensor start time		t_{START}	—	—	80	µs	Figure 5.63
Sampling time		—	30	72	300	µs	
PGA restart time		t_{RST_PGA}	—	—	40	µs	

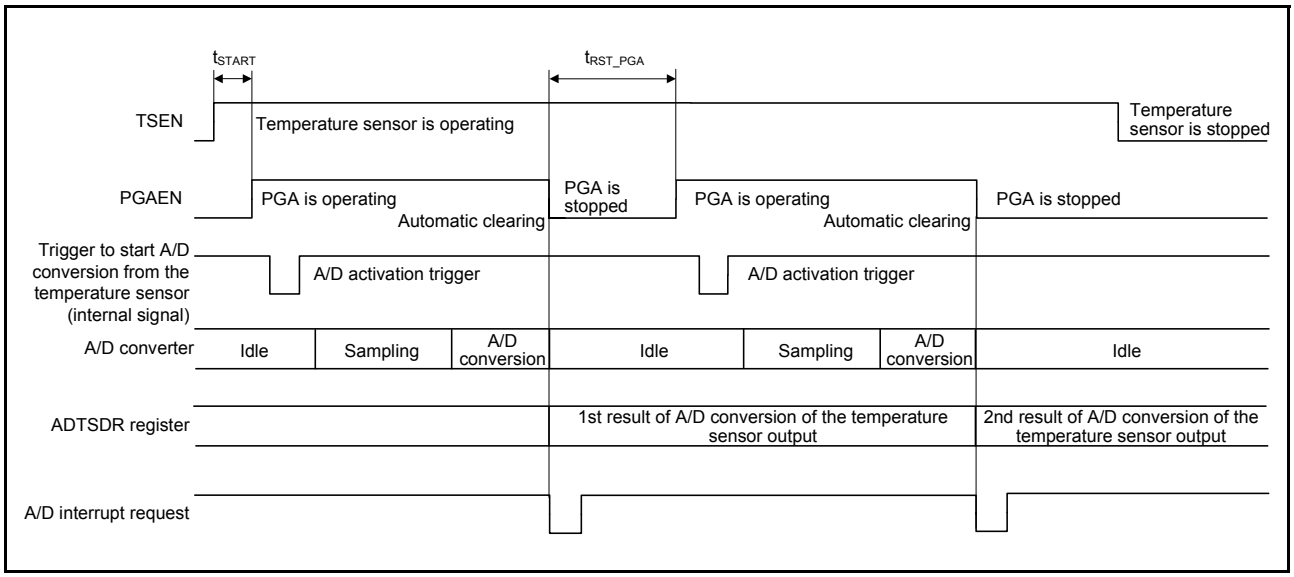


Figure 5.63 A/D Conversion Timing Example of the Temperature Sensor (Two Conversions Performed)

5.9 Comparator Characteristics

Table 5.43 Comparator Characteristics

Conditions: VCC = AVCC0 = AVCCA =1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Comparator A	External reference voltage input range	LVREF	1.4	—	VCC	V	
	External comparison voltage (CMPA1, CMPA2) input range	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±50	±150	mV	
	Comparator output delay time*1	—	—	3	—	µs	At falling edge VI = LVREF – 110 mV
			—	2	—	µs	At falling edge VI < LVREF – 1 V
			—	3	—	µs	At rising edge VI = LVREF + 160 mV
			—	1.5	—	µs	At rising edge VI > LVREF + 1 V
	Comparator operating current	ICMPA	—	0.5	—	µA	VCC = 3.3 V
Comparator B	Input reference voltage for CVREFB0, CVREFB1	VREF	0	—	VCC – 1.4	V	
	Input voltage for CMPB0, CMPB1	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±10	±100	mV	
	Comparator output delay time	t_d	—	—	1	µs	VI = VREF + 100 mV
	Comparator operating current	ICMPB	—	75	150	µA	VCC = 3.3 V For total two channels

Note 1. When the digital filter is disabled.

5.10 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.44 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = AVCC0 = AVCCA, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V_{POR}	1.30	1.40	1.55	V	Figure 5.64 and Figure 5.65
		Low power consumption function enabled*2		1.00	1.20	1.45		
	Voltage detection circuit (LVD0)*3		V_{det0_1}	2.70	2.80	2.90	V	Figure 5.66
			V_{det0_2}	1.80	1.90	2.00		
	Voltage detection circuit (LVD1)*4		V_{det1_7}	2.95	3.10	3.25	V	Figure 5.67
			V_{det1_8}	2.85	2.95	3.05		
			V_{det1_9}	2.70	2.80	2.90		At falling edge VCC
			V_{det1_A}	2.55	2.65	2.75		
			V_{det1_B}	2.40	2.50	2.60		
			V_{det1_C}	2.25	2.35	2.45		
			V_{det1_D}	2.10	2.20	2.30		
			V_{det1_E}	1.95	2.05	2.15		
			V_{det1_F}	1.80	1.90	2.00		

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. When the CPU is in a mode other than software standby and deep software standby modes, when the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 0, or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 0.

Note 2. When the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 1 or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 1.

Note 3. # in the symbol Vdet0_# denotes the value of the LDSEL[1:0] bits.

Note 4. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Table 5.45 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_7}	2.95	3.10	3.25	V	Figure 5.68
		V_{det2_8}	2.85	2.95	3.05		At falling edge VCC
		V_{det2_9}	2.70	2.80	2.90		
		V_{det2_A}	2.55	2.65	2.75		
		V_{det2_B}	2.40	2.50	2.60		
		V_{det2_C}	2.25	2.35	2.45		
		V_{det2_D}	2.10	2.20	2.30		
		V_{det2_E}	1.95	2.05	2.15		
		V_{det2_F}	1.80	1.90	2.00		
		V_{CMPA2}	1.18	1.33	1.48		EXVCCINP2 = 1
Internal reset time	Power-on reset time	t_{POR}	—	9	—	ms	Figure 5.65
	Voltage monitoring 0 reset time	t_{LVD0}	—	9	—		Figure 5.66
	Voltage monitoring 1 reset time	t_{LVD1}	—	1.4	—		Figure 5.67
	Voltage monitoring 2 reset time	t_{LVD2}	—	1.4	—		Figure 5.68
Minimum VCC down time*2		t_{VOFF}	200	—	—	µs	Figure 5.65
Response delay time		t_{det}	—	—	200	µs	Figure 5.65
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	15	µs	Figure 5.67 and Figure 5.68
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.65 VCC = 0.9 V or lower
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	100	—	mV	When selection is from among VdetX_7.
			—	50	—		When selection is from among VdetX_8 to F.

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/ LVD.

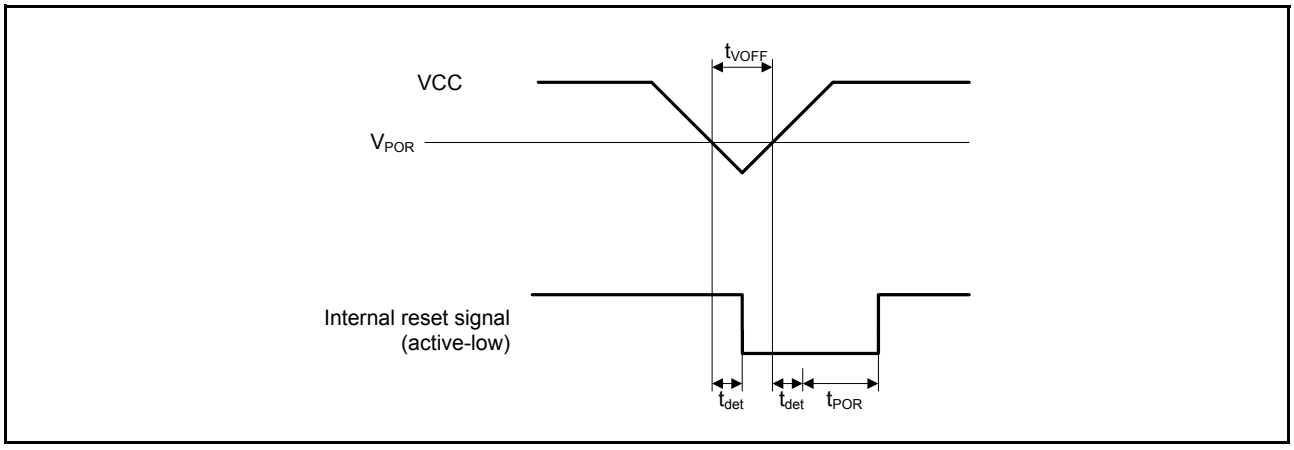
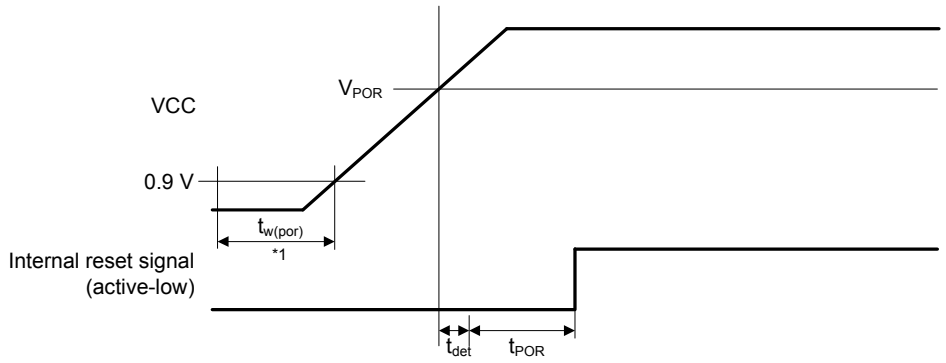


Figure 5.64 Voltage Detection Reset Timing



Note 1. $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (0.9 V).
When VCC turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.65 Power-on Reset Timing

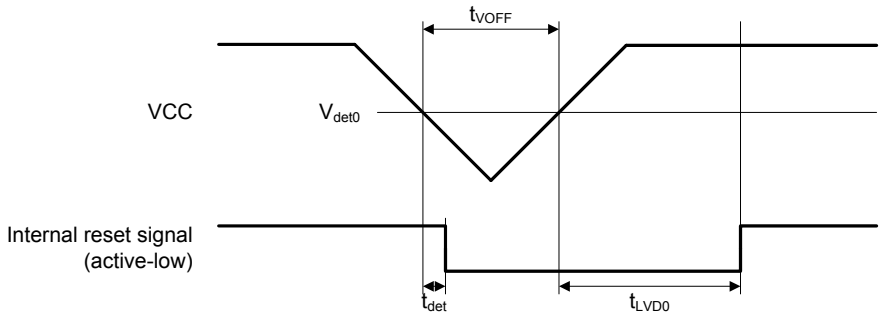


Figure 5.66 Voltage Detection Circuit Timing (V_{det0})

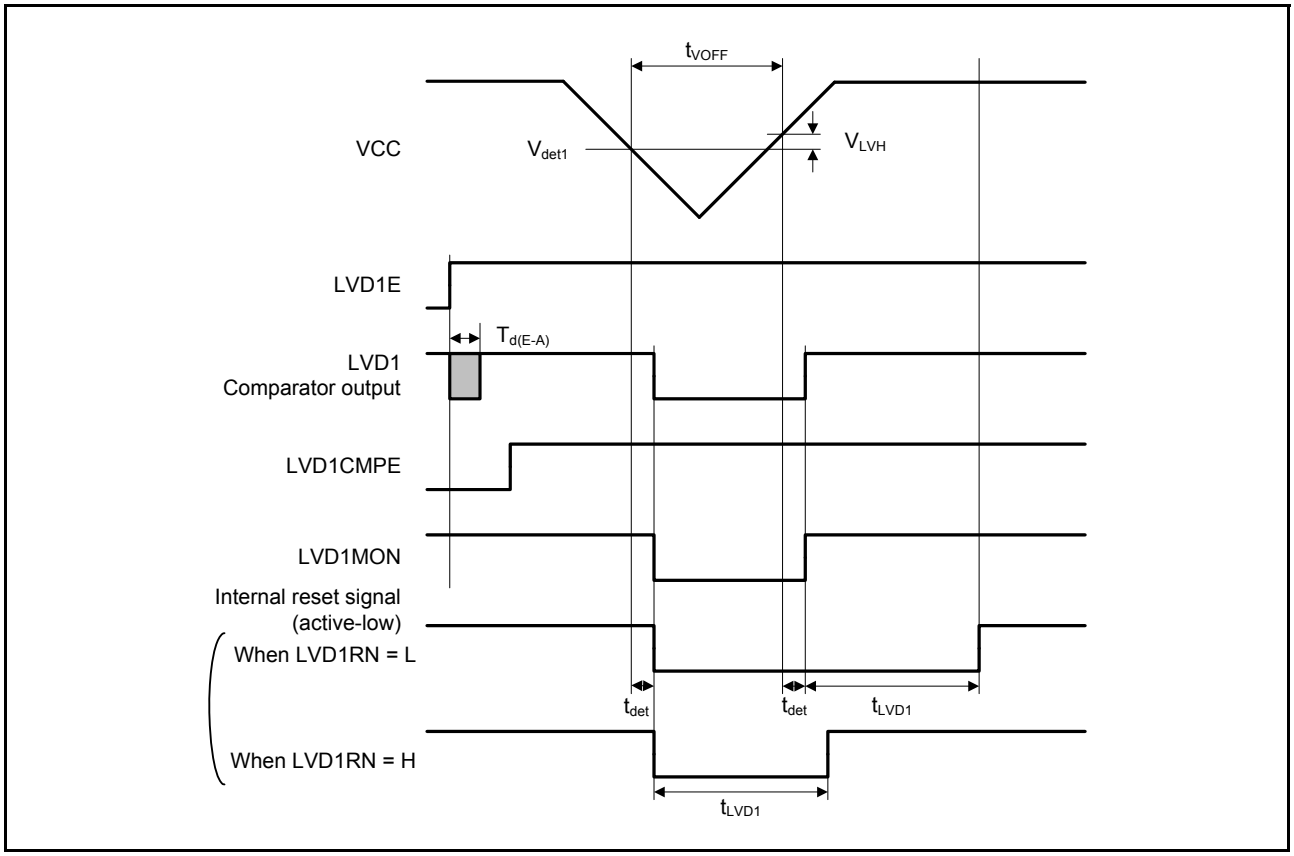


Figure 5.67 Voltage Detection Circuit Timing (V_{det1})

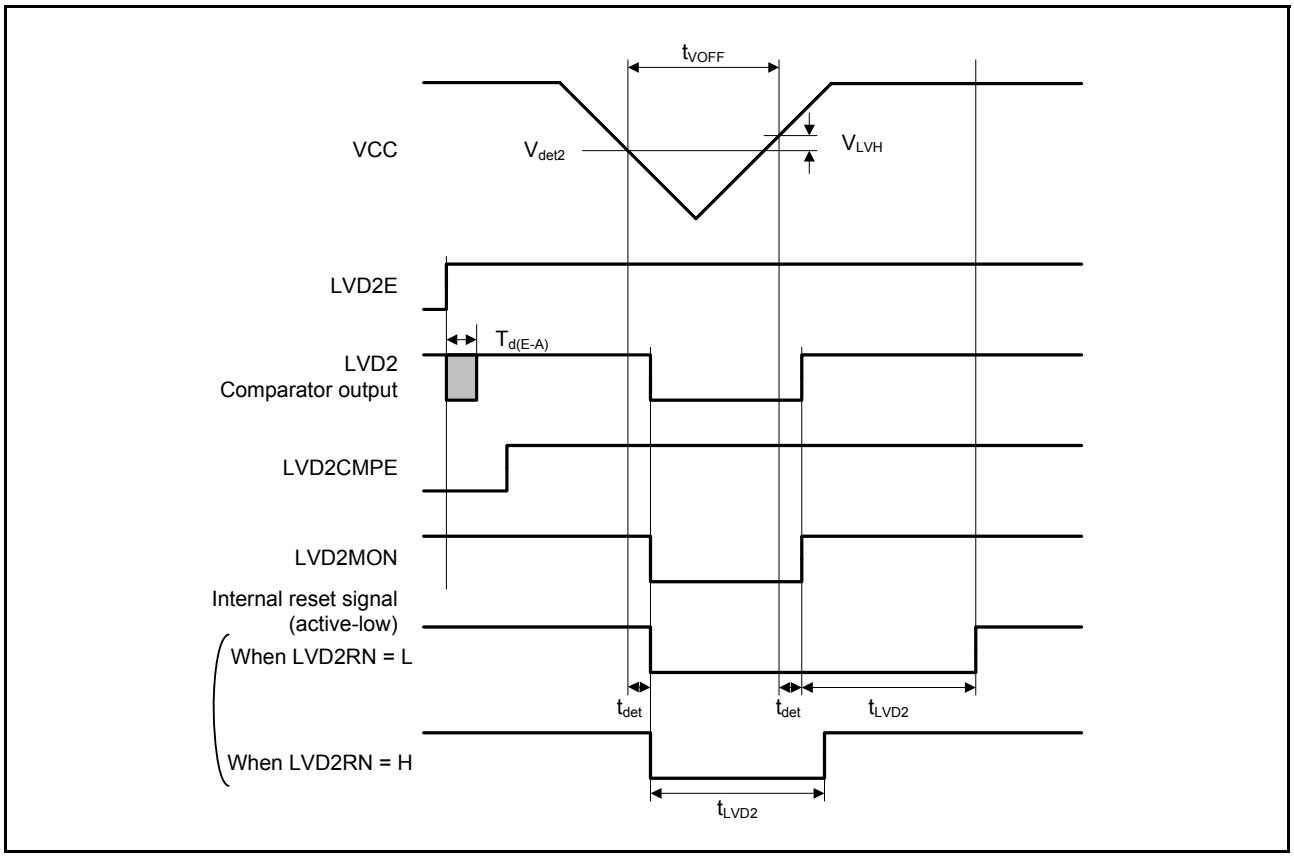


Figure 5.68 Voltage Detection Circuit Timing (V_{det2})

5.11 Oscillation Stop Detection Timing

Table 5.46 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.69

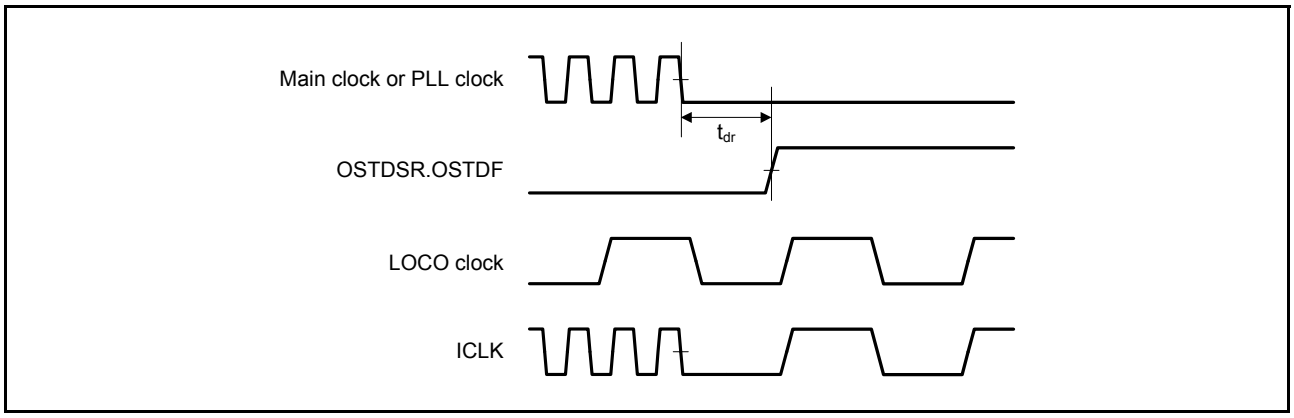


Figure 5.69 Oscillation Stop Detection Timing

5.12 ROM (Flash Memory for Code Storage) Characteristics

Table 5.47 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N_{PEC}	10000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C
	After 10000 times of N_{PEC}		1*2	—	—		

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

Table 5.48 ROM (Flash Memory for Code Storage) Characteristics (2) : high-speed operating mode, medium-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.19	4.3	—	0.12	2.1	ms
	8 bytes	t_{P8}	—	0.19	4.4	—	0.12	2.1	
	128 bytes	t_{P128}	—	0.67	10.7	—	0.42	5.0	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.23	5.3	—	0.15	2.6	ms
	8 bytes	t_{P8}	—	0.23	5.4	—	0.15	2.6	
	128 bytes	t_{P128}	—	0.80	13.2	—	0.50	6.3	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	13.0	92.8	—	10.6	31.6	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	15.9	176.9	—	13.0	64.7	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.9	—	—	0.804	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.9	—	—	0.804	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.9	—	—	0.804	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.9	—	—	0.804	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (3) : medium-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.25	5.0	—	0.21	2.9	ms
	8 bytes	t_{P8}	—	0.25	5.3	—	0.21	3.1	
	128 bytes	t_{P128}	—	0.92	14.0	—	0.66	8.5	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.31	6.2	—	0.26	3.6	ms
	8 bytes	t_{P8}	—	0.31	6.6	—	0.26	3.8	
	128 bytes	t_{P128}	—	1.09	17.5	—	0.78	10.3	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	21.0	113.6	—	18.6	48.7	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	25.6	220.6	—	22.7	94.5 (1000 times ≥ N_{PEC} > 100 times), 102.9 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.604	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.604	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.604	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.604	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The FCLK operating frequency is 12.5 MHz (max.) when the voltage is in the range from 1.8 V to less than 2.7 V in mid-speed operating mode 2B.

5.13 E2 DataFlash Characteristics

Table 5.50 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	—	—	Times	
Data hold time	After 100000 times of N_{DPEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This result is obtained from reliability testing.

Table 5.51 E2 DataFlash Characteristics (2)
: high-speed operating mode, medium-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.19	4.4	—	0.13	2.1	ms
	8 bytes	t_{DP8}	—	0.24	5.1	—	0.14	2.3	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.25	6.4	—	0.17	3.1	ms
	8 bytes	t_{DP8}	—	0.32	7.5	—	0.18	3.4	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	3.3	27.1	—	2.5	8.8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	4.0	45.1	—	3.1	13.3	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	38	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	3.0	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.804	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.804	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.804	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.804	ms

Table 5.52 E2 DataFlash Characteristics (3)
: medium-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.28	5.1	—	0.20	2.9	ms
	8 bytes	t_{DP8}	—	0.32	5.9	—	0.23	3.3	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.36	7.6	—	0.26	4.3	ms
	8 bytes	t_{DP8}	—	0.40	8.8	—	0.28	4.7	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	4.8	32.3	—	4.1	12.8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	5.8	51.4	—	5.0	18.4	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	43	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	3.1	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.604	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.604	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.604	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.604	ms

Note 1. The FCLK operating frequency is 12.5 MHz (max.) when the voltage is in the range from 1.8 V to less than 2.7 V in mid-speed operating mode 2B.

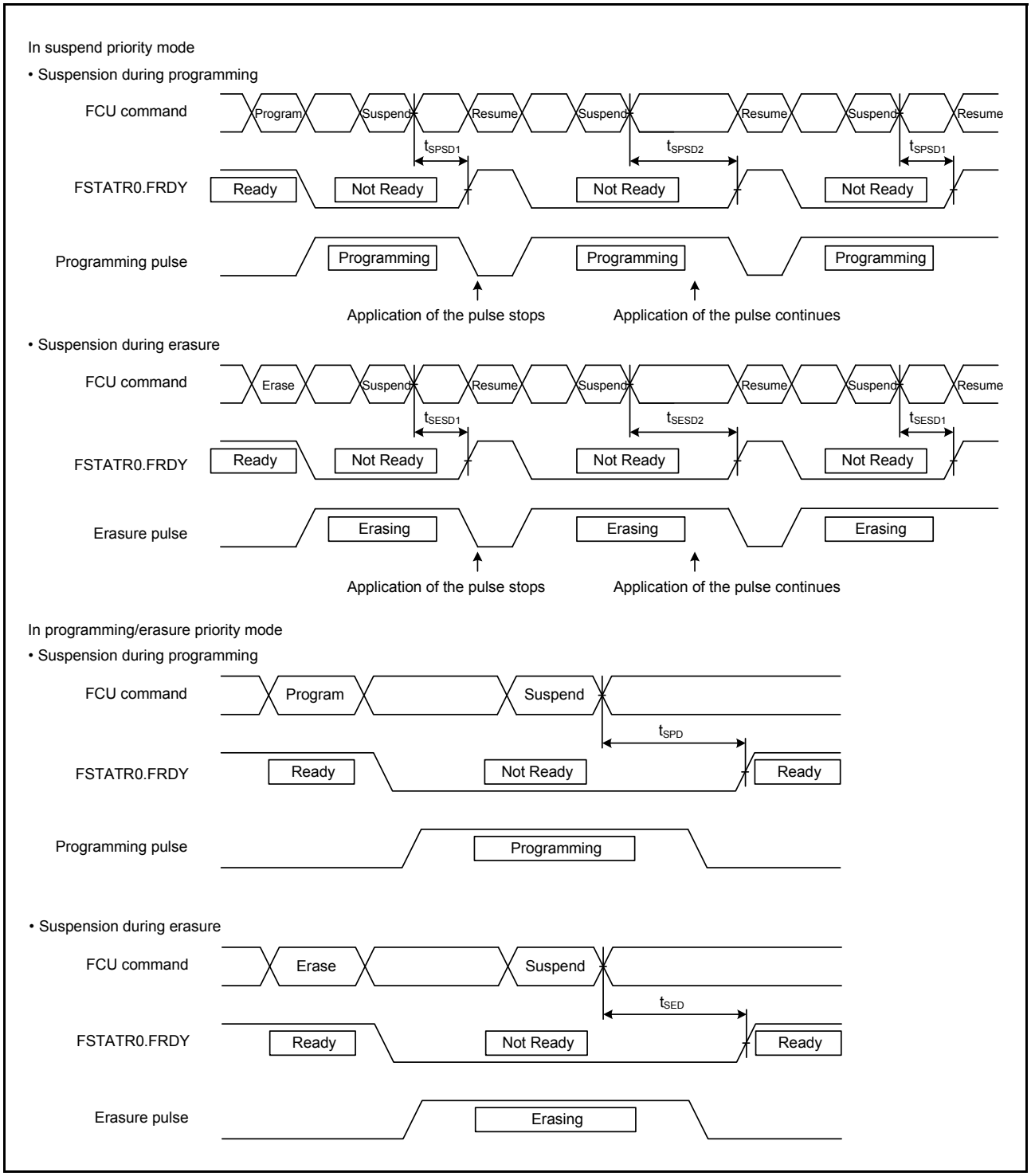
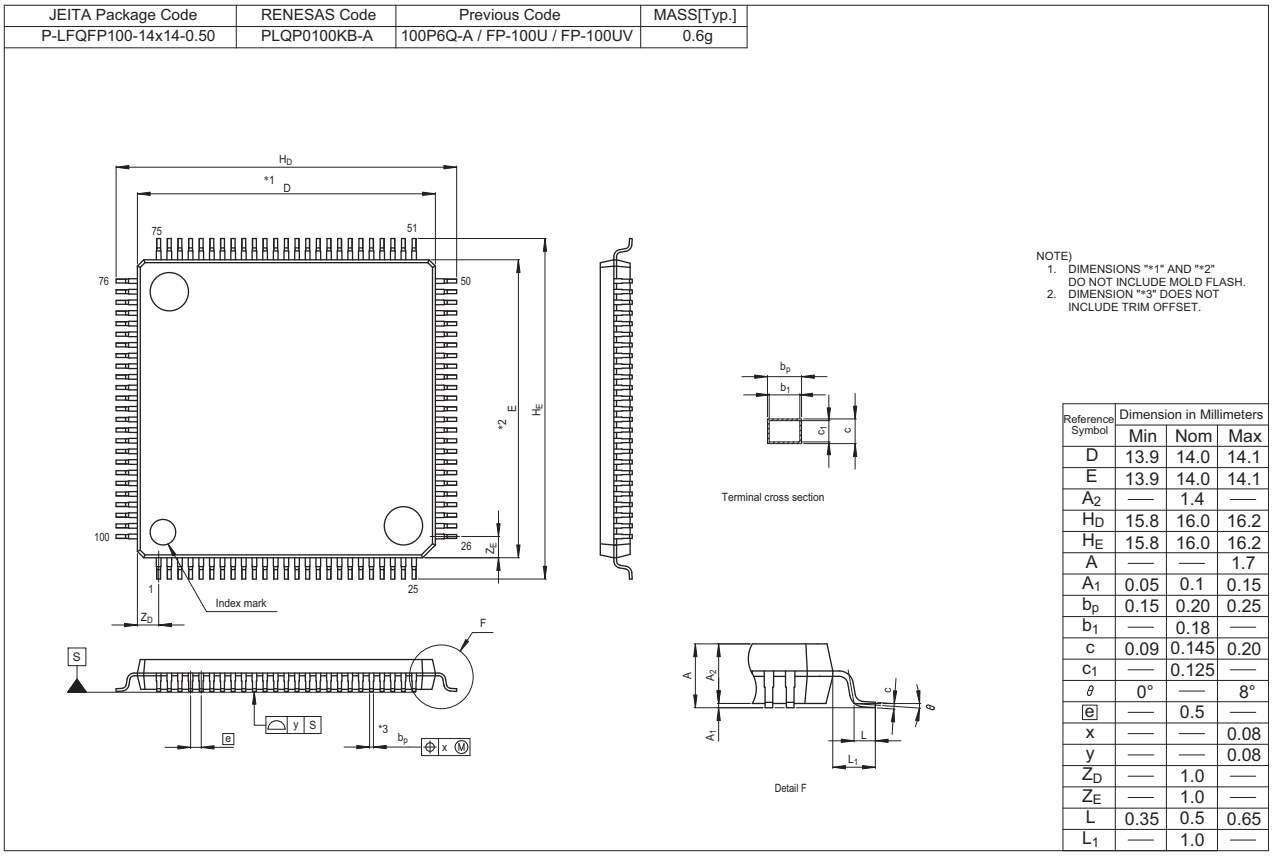


Figure 5.70 Flash Memory Program/Erase Suspend Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

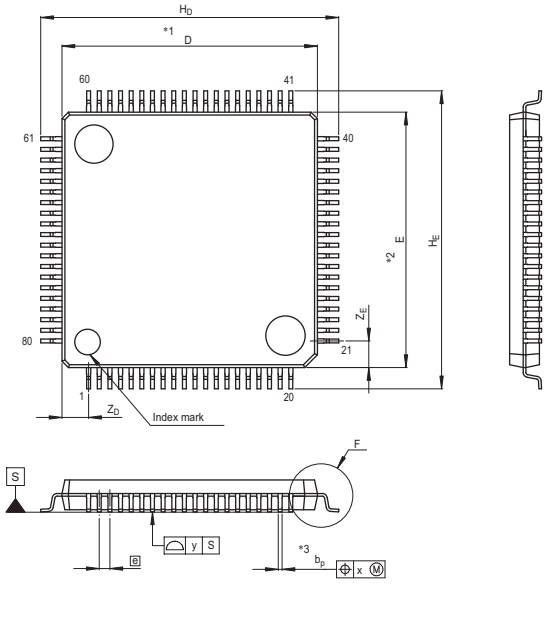
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 100-Pin LQFP (PLQP0100KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g

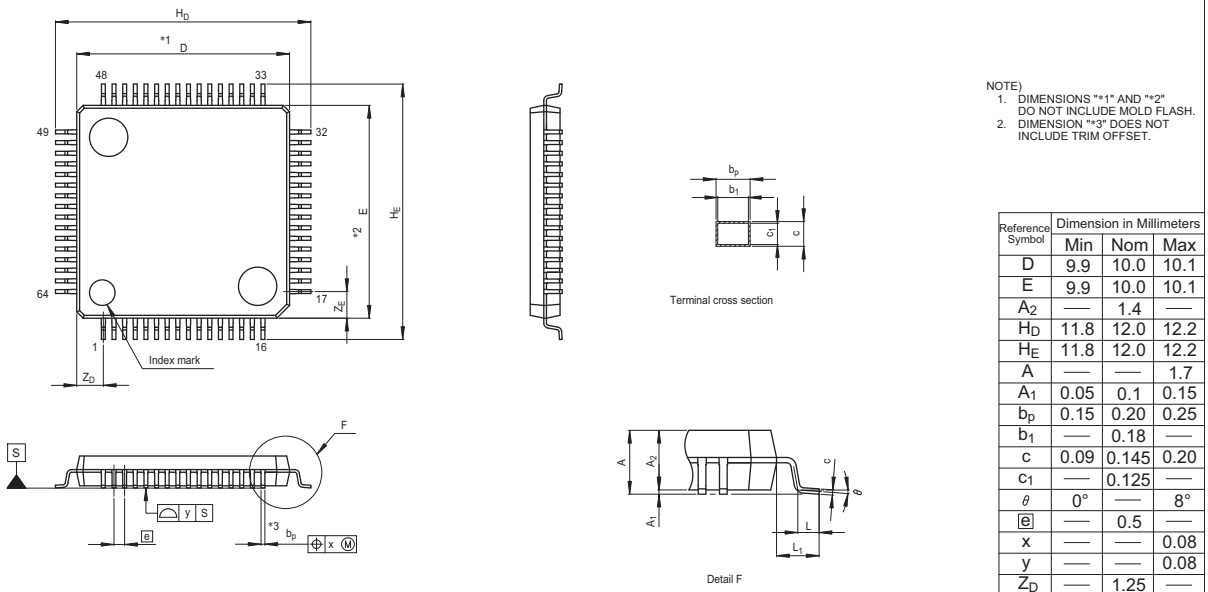


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure B 80-Pin LQFP (PLQP0080KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

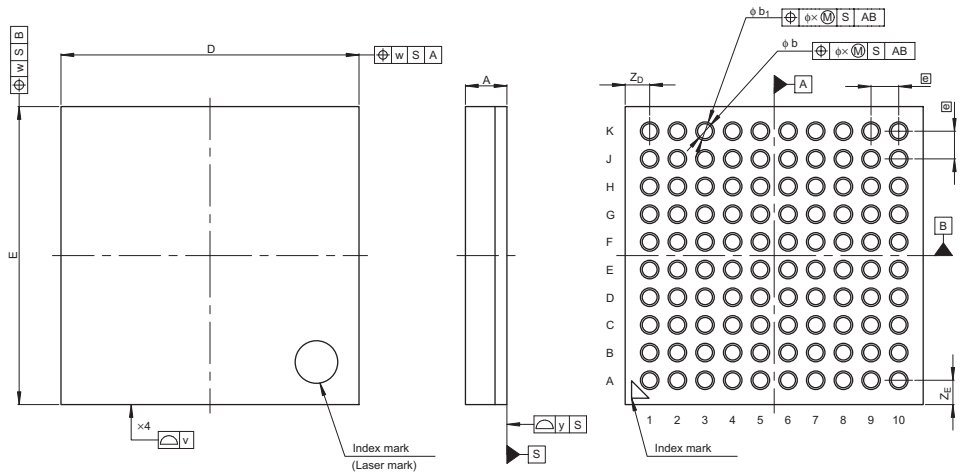


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 64-Pin LQFP (PLQP0064KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure D 100-Pin TFLGA (PTLG0100JA-A)

REVISION HISTORY	RX21A Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 24, 2012	—	First edition, issued

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.10	2014.08.28	Features		
		1	LGA package, added	TN-RX*-A072A/E
		1. Overview		
		5	Table 1.1 Outline of Specifications: Package added	TN-RX*-A072A/E
		5	Table 1.1 Outline of Specifications: Note 2 added	TN-RX*-A073A/E
		5	Table 1.1 Outline of Specifications: Note 3 added	
		5	Table 1.2 Comparison of Functions for Different Packages, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note 1 added	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note, Note 2 added	
		7	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed	TN-RX*-A072A/E
		9	Table 1.4 Pin Functions: Realtime clock changed	
		15	Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View), added	TN-RX*-A072A/E
		23 to 25	Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA), added	TN-RX*-A072A/E
		3. Address Space		
		29	Figure 3.1 Memory Map, changed	
		4. I/O Registers		
		54 to 55	Table 4.1 List of I/O Registers (Address Order): FEFF FAC0h to FEFF FBD3h added	
		5. Electrical Characteristics		
		57	Table 5.3 DC Characteristics (2)	TN-RX*-A074A/E
		58	Table 5.4 DC Characteristics (3), changed	TN-RX*-A074A/E
		59	Table 5.6 DC Characteristics (5), changed	TN-RX*-A074A/E
		60	Table 5.7 DC Characteristics (6), changed	TN-RX*-A074A/E
		68	Table 5.9 DC Characteristics (8), added	TN-RX*-A074A/E
		68	Table 5.10 DC Characteristics (9), changed	
		68	Table 5.11 DC Characteristics (10), changed	
		69	Table 5.14 DC Characteristics (13), changed	TN-RX*-A074A/E
		69	Table 5.15 Permissible Output Currents (1), changed Table 5.16 Permissible Output Currents (2), added	TN-RX*-A074A/E
		70	Table 5.18 Output Values of Voltage (2), changed	TN-RX*-A074A/E
		82	Table 5.26 Clock Timing, changed	TN-RX*-A097A/E
		83	Table 5.26 Clock Timing: Note 5 changed	TN-RX*-A105A/E
		83	Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		87	Figure 5.35 Reset Input Timing at Power-On, changed	TN-RX*-A074A/E
		94	Table 5.33 Timing of On-Chip Peripheral Modules (4), changed	TN-RX*-A074A/E
		103	Table 5.36 ΔΣ A/D Conversion Characteristics, changed	TN-RX*-A105A/E
		104	Figure 5.55 Differential Input Amplitude, changed	
		108	Table 5.37 A/D Conversion Characteristics (1), changed	TN-RX*-A074A/E
		108	Figure 5.61 AVCC to VREFH0 Voltage Range, added	TN-RX*-A074A/E
		109	Table 5.39 A/D Conversion Characteristics (2), changed	TN-RX*-A074A/E
		111	Differential nonlinearity error (DNL), description changed	TN-RX*-A073A/E
		115	Table 5.44 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1): Note1, Note2 changed	TN-RX*-A074A/E
		Appendix 1. Package Dimensions		
		128	Figure D. 100-Pin TFLGA (PTLG0100JA-A), added	TN-RX*-A072A/E

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

R5F521A6BDFM#V0 R5F521A8BDFM#30 R5F521A8BDFP#30 R5F521A8BDFN#V0 R5F521A6BDLJ#U0
R5F521A6BDFP#30 R5F521A8BDLJ#U0 R5F521A7BDFP#30 R5F521A8BDFM#V0 R5F521A8BDFP#V0
R5F521A7BDFM#V0 R5F521A6BDFP#V0 R5F521A6BDFN#30 R5F521A6BDFN#V0 R5F521A7BDFN#30
R5F521A7BDFM#30 R5F521A6BDFM#30 R5F521A8BDFN#30 R5F521A7BDFN#V0 R5F521A7BDLJ#U0