

MOS FIELD EFFECT TRANSISTOR

2SK2462

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2462 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Low On-Resistance
 $R_{DS(on)1} = 0.14 \Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 8.0 \text{ A)}$
 $R_{DS(on)2} = 0.17 \Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 8.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 790 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

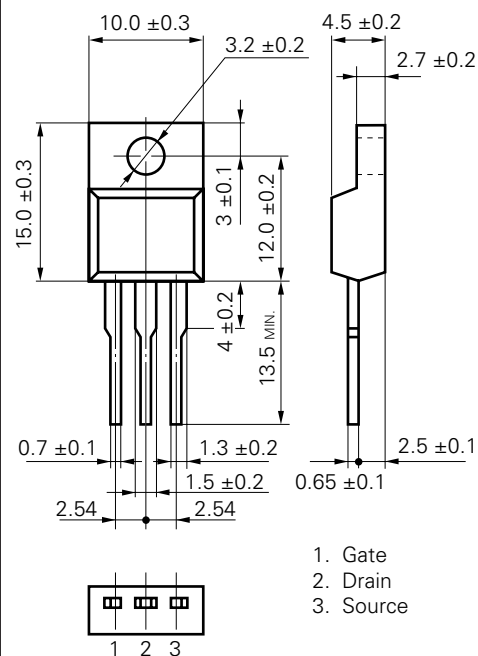
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 15	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 60	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	30	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current**	I_{AS}	15	A
Single Avalanche Energy**	E_{AS}	22.5	mJ

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

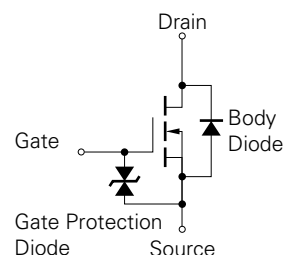
** Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

PACKAGE DIMENSIONS

(in millimeters)



MP-45F(ISOLATED TO-220)

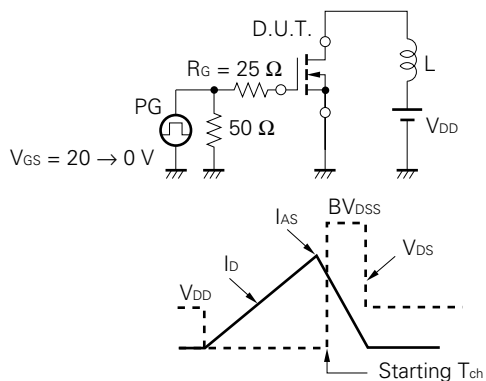


The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding rated voltage may be applied to this device.

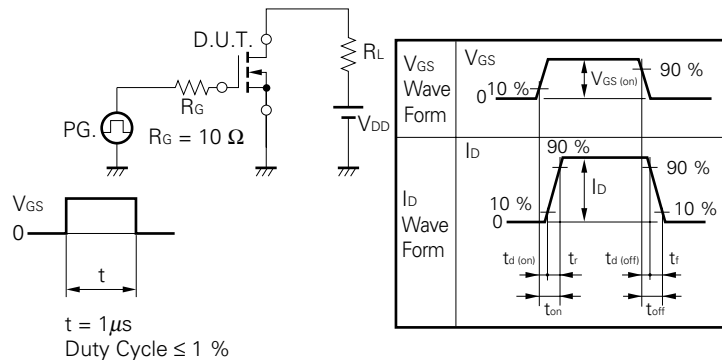
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R _{DS(on)1}		0.10	0.14	Ω	V _{GS} = 10 V, I _D = 8.0 A
Drain to Source On-Resistance	R _{DS(on)2}		0.12	0.17	Ω	V _{GS} = 4 V, I _D = 8.0 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0	1.6	2.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	7.0	14		S	V _{DS} = 10 V, I _D = 8.0 A
Drain Leakage Current	I _{BSS}			10	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		790		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		280		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		88		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		16		ns	I _D = 8.0 A
Rise Time	t _r		110		ns	V _{GS(on)} = 10 V
Turn-Off Delay Time	t _{d(off)}		88		ns	V _{DD} = 50 V
Fall Time	t _f		62		ns	R _G = 10 Ω
Total Gate Charge	Q _G		33		nC	I _D = 15 A
Gate to Source Charge	Q _{GS}		5.4		nC	V _{DD} = 80 V
Gate to Drain Charge	Q _{GD}		25		nC	V _{GS} = 10 V
Body Diode Forward Voltage	V _{F(S-D)}		1.1		V	I _F = 15 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		160		ns	I _F = 15 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		670		nC	di/dt = 100 A/μs

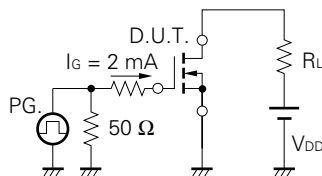
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

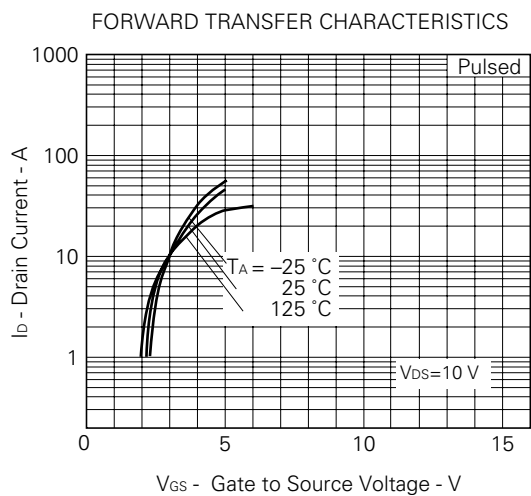
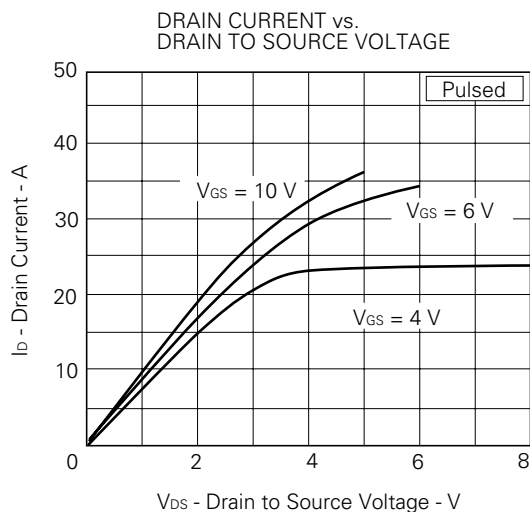
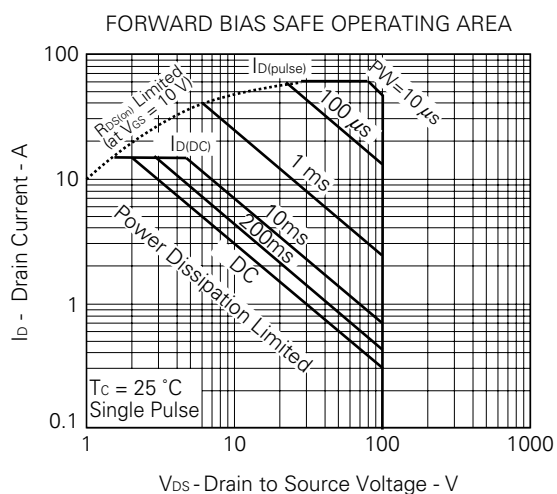
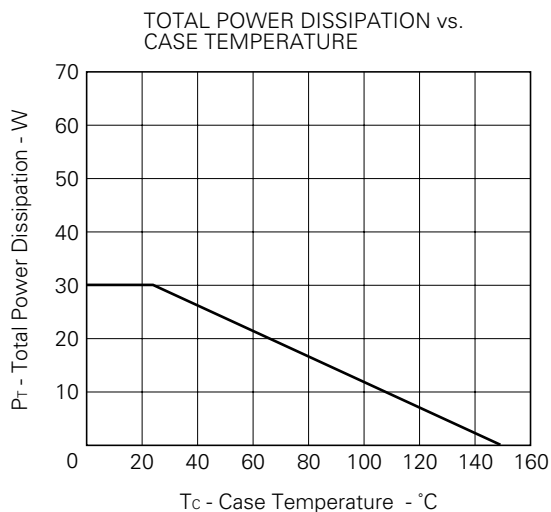
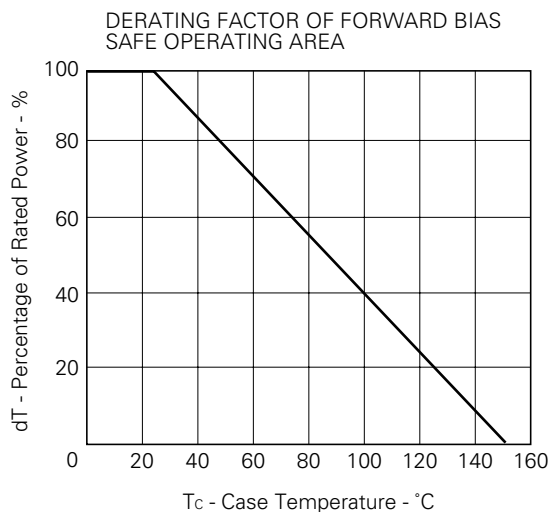


Test Circuit 3 Gate Charge

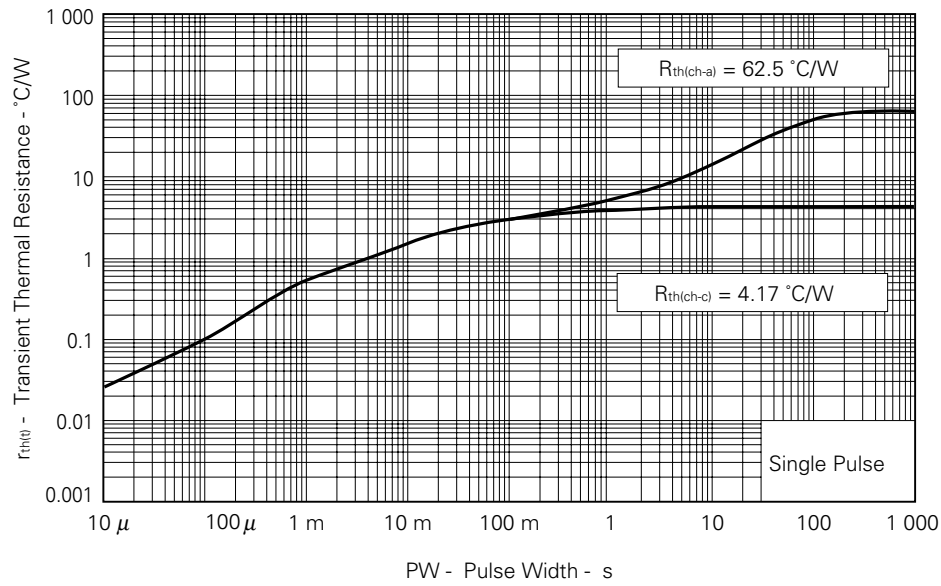


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

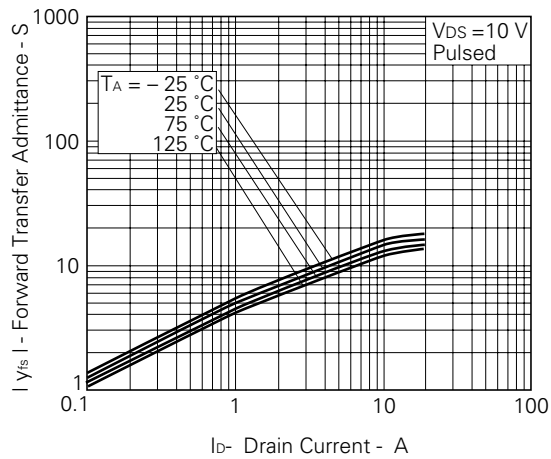
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$)



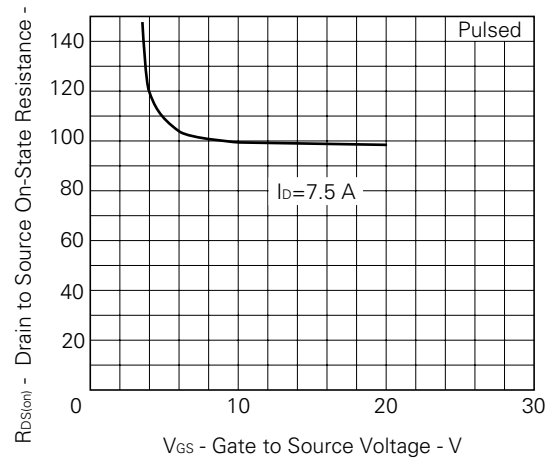
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



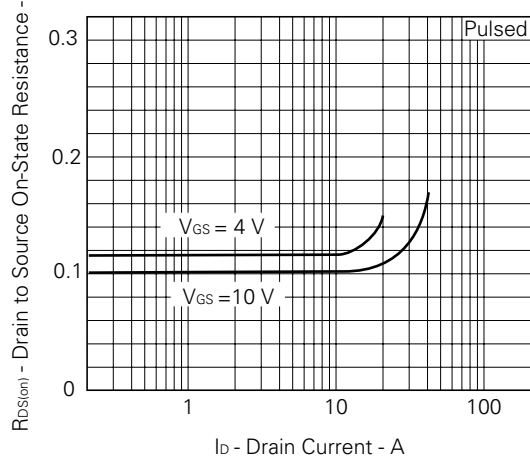
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



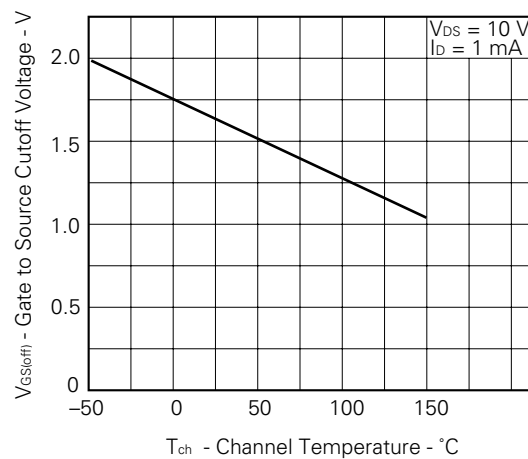
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



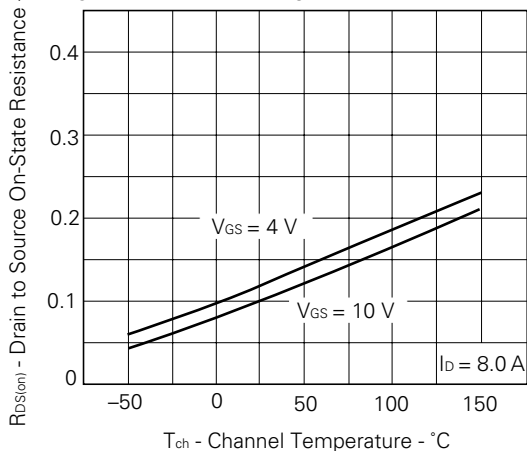
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



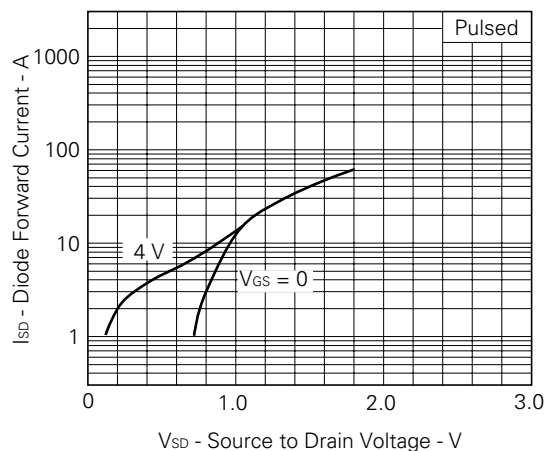
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



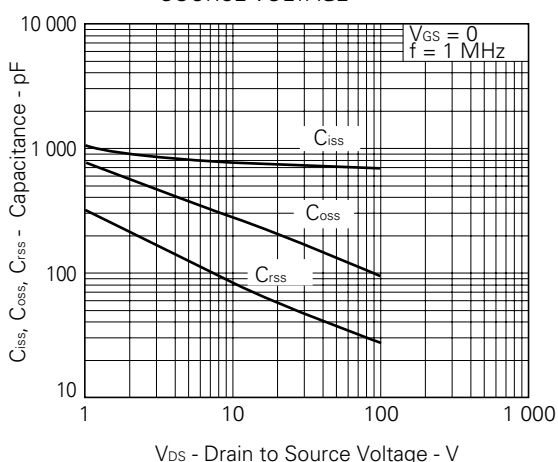
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



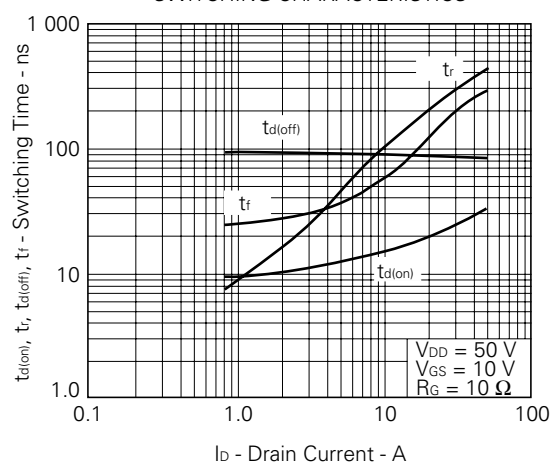
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



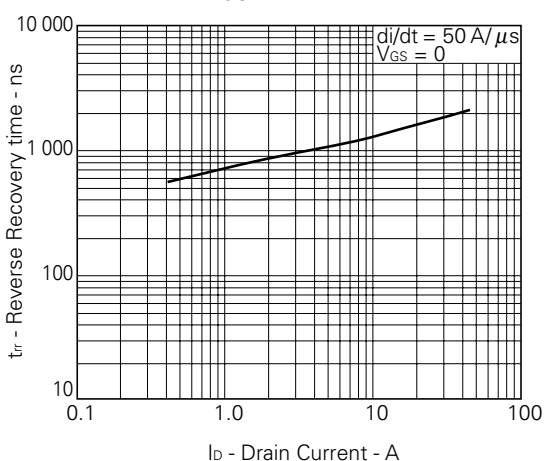
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



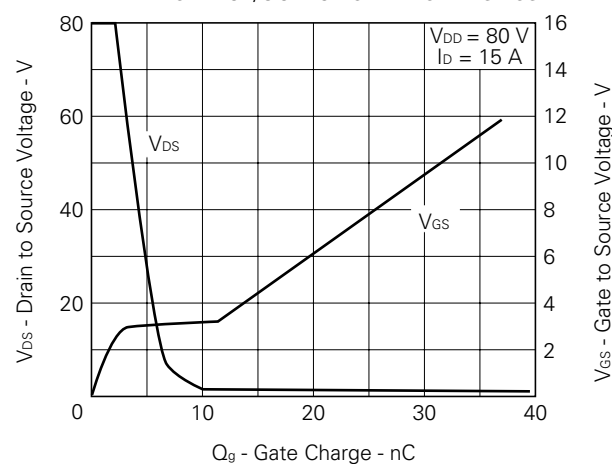
SWITCHING CHARACTERISTICS



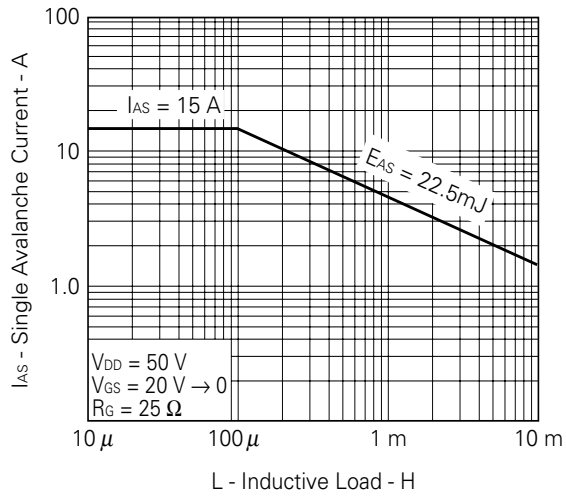
REVERSE RECOVERY TIME vs. DRAIN CURRENT



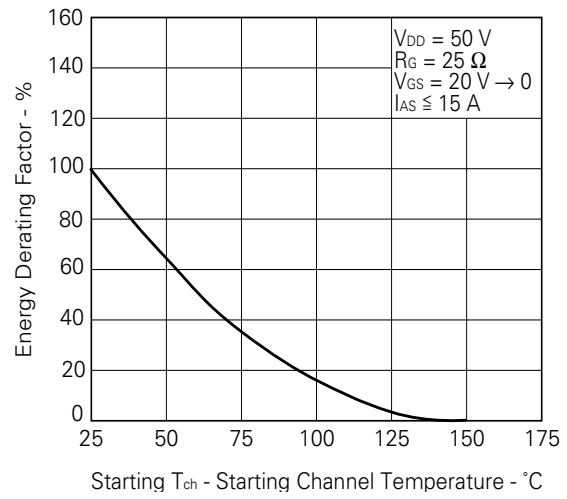
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.