MC1405, MC1505

Dual Ramp A/D Converter Subsystem

The MC1405/MC1505 is intended to perform the dual ramp function for either a 3-1/2 or 4-1/2 digit DVM or use as a general-purpose analog-to-digital (A/D) converter. It can be combined with the CMOS MC14435 logic system to produce the complete 3-1/2 digit DVM function.

The MC1505 uses the proven dual ramp A/D conversion technique. The subsystem consists of an on-chip voltage reference, a pair of voltage/current converters, an integrator, a comparator, a current switch and associated control and calibration circuitry. Only one capacitor and two calibration potentiometers are required for normal operation.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

MOTOROLA

MC1405
MC1505

DUAL RAMP A/D CONVERTER SUBSYSTEM

The MC1505/MC1405 is intended to perform the dual ramp function for either a 3-1/2 or 4-1/2 digit DVM or use as a general-purpose analog-to-digital (A/D) converter. It can be combined with the CMOS MC14435 logic system to produce the complete 3-1/2 digit DVM function.

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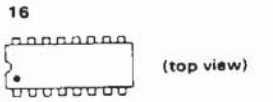
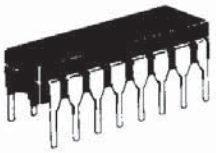
- Accuracies to 13 Bits
- Low Power Consumption: 42 mW @ +5.0 V
- Single Power Supply Operation – +5.0 V to +15 V
- Low Power Supply and Temperature Sensitivity
- Digital Inputs and Outputs Compatible with Both MTTL and CMOS
- Accepts Either Positive or Negative Input Voltages
- Combines with MC14435 to Produce 3-1/2 Digit A/D Converter

ANALOG-TO-DIGITAL CONVERTER SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT





L SUFFIX
CASE 620
CERAMIC PACKAGE

FIGURE 1 – COMPLETE A/D CONVERTER SYSTEM

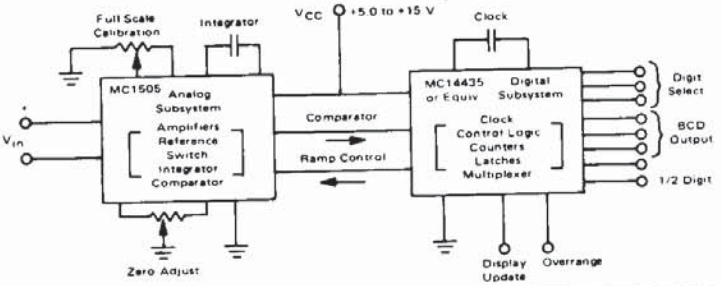
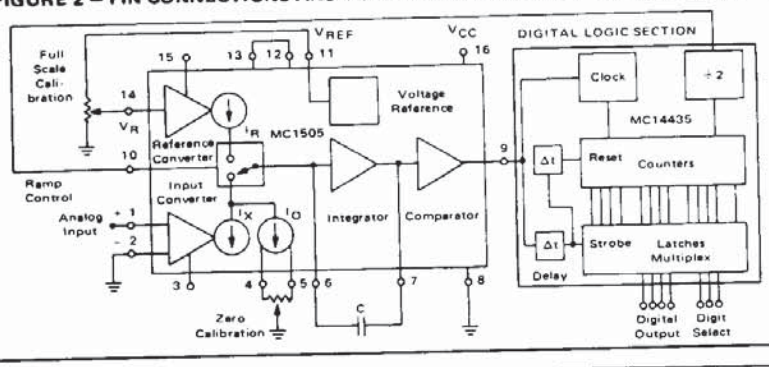


FIGURE 2 – PIN CONNECTIONS AND FUNCTIONAL DIAGRAM (as used in Figure 1)



TYPICAL APPLICATIONS

BCD A/D Converter: 2-1/2 to 4-1/2 Digits (LSI or MSI Logic)
- Panel Meters
- Digital Voltmeters
- Portable Instruments
- Industrial Measurement and Control

Binary A/D Converter: 8-to-13 Bits (LSI or MSI Logic)
- Industrial Measurement and Control
- High Noise Environments (Integrating Converter with MTTL, MHTL, and CMOS Compatibility)

Other Uses:
- Data Acquisition Systems with Remote MC1505
- Voltage to Frequency Conversion
- Delta Modulation and Signal Generation

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MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16.5	Vdc
Digital Input Voltage	V_{10}	+16.5	Volts
Reference Input Voltage	V_R	2.0	Volts
Unknown Input Voltage Range	V1 V2	±5.0 ±5.0	Volts
Zero Calibration Control Pin Voltage	V4	5.0	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	1000 6.0	mW mW/°C
Operating Ambient Temperature Range MC1505L MC1405L	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_R = 1.000 Vdc, V1 = 2.000 Vdc, V2 = 0.000 Vdc, V10 ≥ 2.0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Figure	MC1505 Min	MC1505 Typ	MC1505 Max	MC1405 Min	MC1405 Typ	MC1405 Max	Unit
A/D CONVERSION SYSTEM (1)									
Linearity: Deviation from Straight Line through Zero and Full Scale (2)	E_r	9, 11	–	±0.01	±0.05	–	±0.01	±0.05	%F.S.
Mid-Scale Power Supply Sensitivity (PSS of I_R-(I_X + I_O), V1 = 1.0 V)	PSSF	3	–	0.002	±0.02	–	0.002	±0.02	%/%
Zero Calibration Power Supply Sensitivity (V1 = V2 = 0 V)	PSSZ	9	–	0.001	–	–	0.001	–	%F.S./%
Input Common Mode Sensitivity (V_X = 2.0 V, V_{CM} = V2 is varied)	$\|CMSI_X\|$	3	–	0.0006	0.0012	–	0.0006	0.0018	%/mV
Full Scale Temperature Drift (3)	$\|TCF\|$	9	–	0.004	–	–	0.004	–	%/°C
Zero Calibration Temperature Drift (3)	$\|TCZ\|$	9	–	0.001	–	–	0.001	–	%F.S./°C
VOLTAGE REFERENCE									
Reference Voltage, Pin 11	V_{REF}	3	1.15	1.25	1.35	1.1	1.25	1.4	Vdc
Reference Voltage Power Supply Sensitivity	$PSSV_{REF}$	3	–	0.003	±0.01	–	0.003	±0.02	%/%
Reference Voltage Temperature Drift	$\|TCV_{REF}\|$	3	–	0.015	–	–	0.015	–	%/°C
REFERENCE CURRENT CONVERTER									
Reference Current	I_R	3	–	250	–	–	250	–	μA
Input Bias Current	I14	3	–	10	40	–	10	40	nA
Input Range of V_R	V14	3	0.8	–	1.2	0.8	–	1.2	Vdc
Input Offset Voltage (V14–V15)	$\|V_{RR}\|$	3	–	1.0	2.5	–	2.0	5.5	mV
INPUT CURRENT CONVERTER									
Unknown Current	I_X	3	–	500	–	–	500	–	μA
Input Resistance	R_I	3	–	4.0	–	–	4.0	–	kΩ
Input Differential Range	V_X	3,10	0	2.0	–	0	2.0	–	Volts
Input Common Mode Range	CMR	3,10,12	-1.5	–	+1.5	-1.5	–	+1.5	Volts
Input Bias Currents	11 12	3,9	– –	200 -300	– –	– –	200 -300	– –	μA
Input Offset Voltage (V13–V3)	$\|V_{XX}\|$	3	–	1.0	2.5	–	2.0	5.5	mV
RAMP OFFSET SOURCE									
Ramp Offset Current	I_O	4	–	25	–	–	25	–	μA

(1) System parameters measured using external voltage reference, independent of V11 = V_{REF}.
Integrator Capacitor = 2.0 μF
Clock Frequency = 30 kHz
V_{CC} = 15 V

(2) Does not include quanitizing error. See Figure 10 for calibration.

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ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_R = 1.000 Vdc, V1 = 2.000 Vdc, V2 = 0.000 Vdc, V10 ≥ 2.0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Figure	MC1505 Min	MC1505 Typ	MC1505 Max	MC1405 Min	MC1405 Typ	MC1405 Max	Unit
CURRENT SWITCH									
Digital Input Logic Levels, Pin 10									
High Level, Logic "1"	V_{IH}	3,18	2.0	–	–	2.0	–	–	Vdc
Low Level, Logic "0"	V_{IL}	3,18	–	–	0.8	–	–	0.8	Vdc
Digital Input Current									
High Level, Logic "1"	I_{IH}	3	–	0	1.0	–	0	1.0	μA
Low Level, Logic "0"	I_{IL}	3	–	-5.0	-50	–	-5.0	-50	μA
INTEGRATOR									
Input Bias Current	I6	5	–	10	30	–	10	50	nA
Output Voltage Swing	V7	–							Volts
High			12.8	13.0	–	12.8	13.0	–	
Low			–	0.2	0.35	–	0.2	0.35	
COMPARATOR									
Output Logic Levels, Pin 9									Volts
High Level, Logic "1"	V_{OH}	3	13.5	14.0	–	13.5	14.0	–	
Low Leve, Logic "0" $T_A = T_{low}$ to T_{high}	V_{OL}	3	–	0.35	0.5	–	0.35	0.5	
(Sink Current = 1.6 mA)									
Input Threshold	$V_{TH(7)}$	–	0.9	1.0	1.1	0.9	1.0	1.1	Volts
POWER SUPPLY									
Power Supply Current	I_{CC}								mA
(V_{CC} = +5.0 Vdc)		3	–	8.4	12.0	–	8.4	12.0	
(V_{CC} = +15.0 Vdc)		3	–	9.0	13.0	–	9.0	13.0	
Power Supply Voltage Range	V_{CC}	–	4.75	–	16.5	4.75	–	16.5	Vdc
Power Consumption	P_C								mW
(V_{CC} = +5.0 Vdc)		–	–	42	60	–	42	60	
(V_{CC} = +15.0 Vdc)		–	–	135	195	–	135	195	

T_{low} = -55°C for MC1505L, 0°C for MC1405L
T_{high} = +125°C for MC1505L, +70°C for MC1405L

FIGURE 3 – STANDARD TEST CONFIGURATION

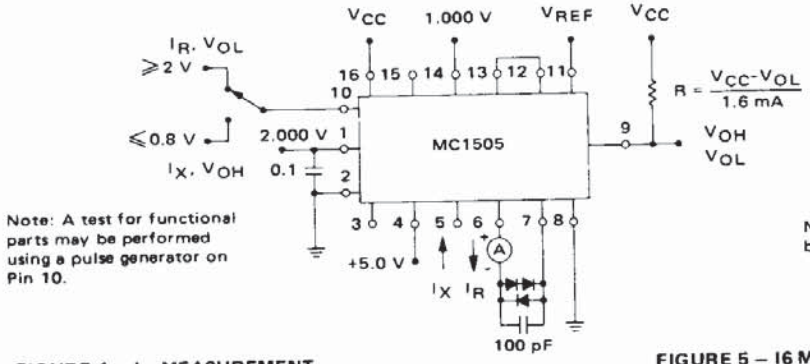


FIGURE 4 – I_O MEASUREMENT

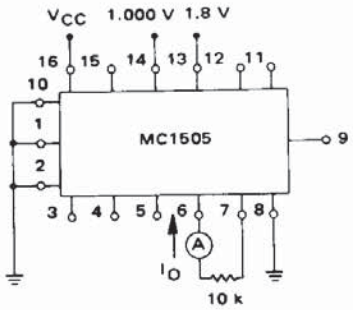
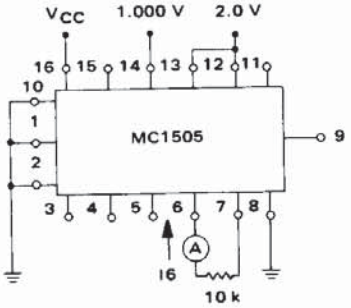


FIGURE 5 – I6 MEASUREMENT



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GENERAL INFORMATION

Dual Ramp Analog-to-Digital Conversion

The dual ramp method of A/D conversion is a proven system which is capable of very high accuracy. The conversion is an integrating process which offers high noise rejection and immunity to changes in the clock rate and integrator capacitor value. The particular method used in the MC1505 is a noniterating dual slope technique which produces an accurate result after one conversion period.

Dual ramp conversion is accomplished with the system of Figure 2. The conversion begins at time t1, when current I_X causes the integrator output, or ramp, to cross the comparator threshold, as shown in Figure 6. The clock is activated and the counters begin counting from zero. The system counts for a fixed period T, with a ramp slope which depends on the input voltage, i.e., a steep slope is caused by a high input voltage. When the counters have reached full scale, the overflow count triggers a ÷ 2 flip-flop which changes the ramp control polarity current. I_R now controls the integrator and the down ramp begins at t2. This ramp continues at a fixed slope for a time period which depends on the amplitude achieved by the up ramp. Thus T2 is determined by the input voltage. When the ramp crosses the comparator threshold at t3, the clock stops and the counter holds a digital value which is proportional to the unknown input voltage.

After the down ramp crosses the comparator threshold, a timing sequence in the digital section strobes the latches to store the data, resets the counters, and reverses the ramp at t4 to begin a new conversion.

Since the voltage change across the capacitor is equal on the up and down ramps, an equal amount of charge is exchanged. The equations of Figure 6 show that the system output is the ratio of the unknown and reference currents, and long term changes in the clock rate and integrator capacitor do not effect the reading.

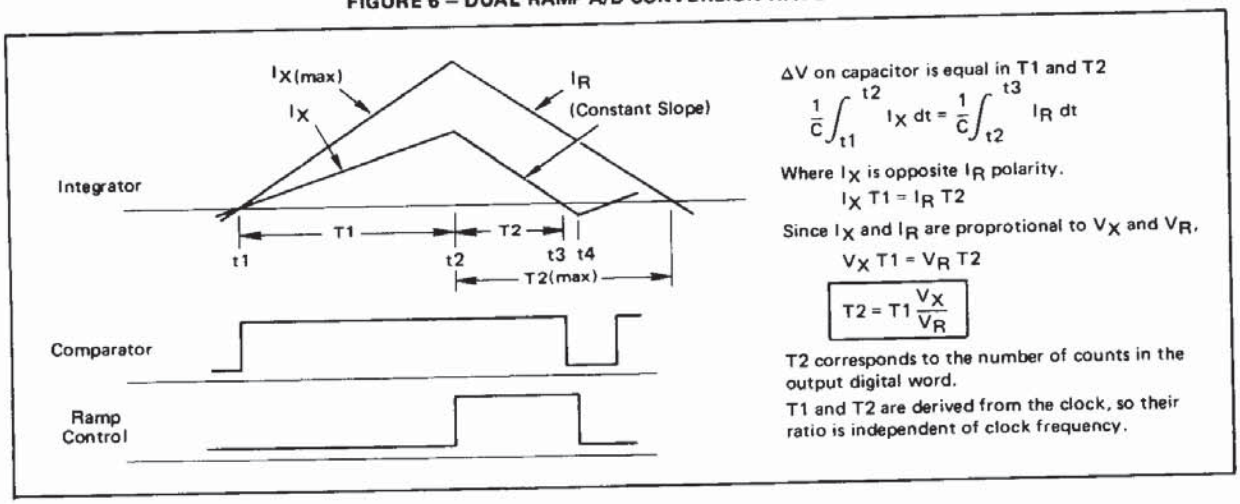
A/D Subsystem Circuit Description

The MC1505 incorporates special circuit features which allow all the analog functions of the dual ramp system to be performed on a single monolithic chip using standard bipolar processing.

Voltage-to-current conversion for both the input and reference voltages allows the use of a high-speed current switch and single supply operation. The unbuffered differential inputs have sufficiently high input impedance for power supply monitoring applications, and provide flexibility for other input formats since they will accept either positive or negative voltages.

The voltage reference, shown in Figure 7, is one of the six basic circuits in the subsystem. It provides a low impedance output which has excellent temperature stability, and high power supply rejection. Biasing for the other circuits in the MC1505 is derived from the voltage reference circuitry.

FIGURE 6 – DUAL RAMP A/D CONVERSION WAVEFORMS



The same basic amplifier circuit is used in both the reference and input voltage-to-current converters. It is an extremely well balanced amplifier with low input offset voltage temperature drift. The reference converter uses a pair of PNP transistors to derive current I_R, in conjunction with a reference resistor which has the same temperature coefficient as those used in the input converter. The value of the reference current is $V_R/R5$. The collectors of transistors Q1, Q2 and Q3 in Figure 7 all track with a two diode temperature coefficient, which assures constant current ratios.

The reference resistor value can vary by 30% of 4.0 kΩ due to process variations. Moreover, these variations will also affect the input bridge resistors. Thus, the ratio of reference to unknown current has a close tolerance for a wide range of resistor values.

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The input voltage-to-current converter is a bridge or bilateral current source whose output current is $V_X/R1$. If the bridge is perfectly balanced, its output impedance and common mode rejection are infinite. However, the design has the ability to tolerate bridge mismatches of approximately 0.5%. In order to tolerate this mismatch, the output of the bridge current source is connected to the current switch which is a low temperature coefficient, low impedance source of 1.25 volts. This technique effectively eliminates output current changes due to finite output impedance which is caused by resistor mismatch. This input current converter makes possible the use of a single supply voltage and differential inputs which can be used at or below ground potential.

An important feature of the MC1505 is the ramp offset current source which is added to the unknown current and does not allow the ramp to reach zero slope when the input voltage is zero. The ramp range is shown in Figure 8. The ramp offset current has a value of $I_R/10$, so that the minimum ramp slope is 5% of the full scale slope. This allows reliable conversion at low input voltages by assuring a nearly constant comparator propagation delay and a good ramp signal-to-noise ratio. It also prevents turn-off of the diode in the current switch at low levels, restricting the voltage change at the output of the resistor bridge. Still another feature is that it provides a convenient temperature compensated zero adjust which can correct errors in the resistor bridge and input buffer amplifiers when they are used. The ramp offset current is compensated by 100 extra counts in the digital logic during ramp down, so it does not appear in the digital output (see Figure 8).

The current switch uses current steering for very high speed operation. A smooth transition occurs as one current is turned on while the other is turned off. This minimizes error during the ramp reversal at its peak, especially since the reference current source has a very high output impedance and does not change value when switched. The settling time of the input current converter is not a factor in system accuracy. At the ramp peak, I_X is turned off, so the amplifier settles after the unknown current is decoupled from the integrator. When the ramp is below the comparator threshold, the unknown current is switched on and thus the current can settle before the ramp enters the active conversion range. The switch operates into a voltage of 1.95 volts and is translated by a follower so its input

FIGURE 7 – A/D CONVERTER ANALOG SUBSYSTEM

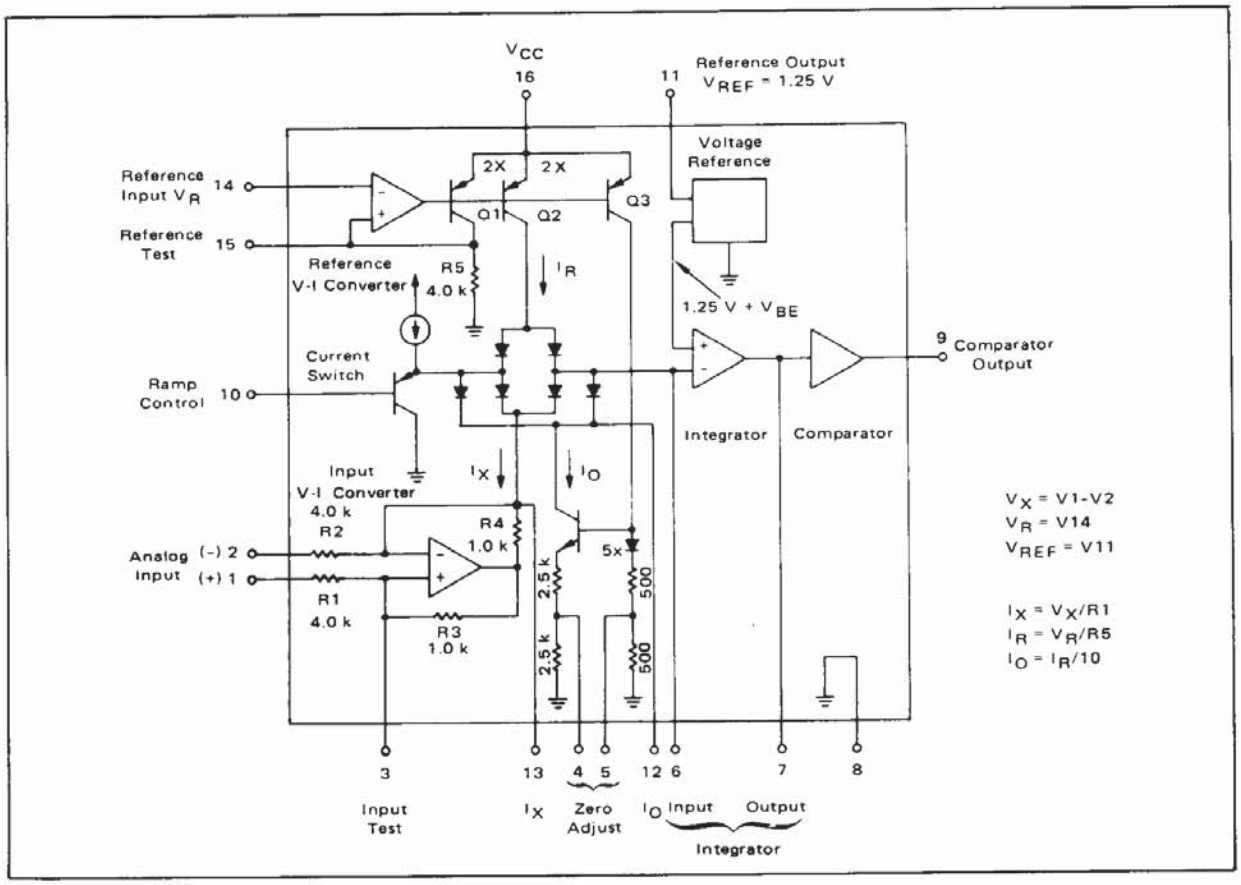
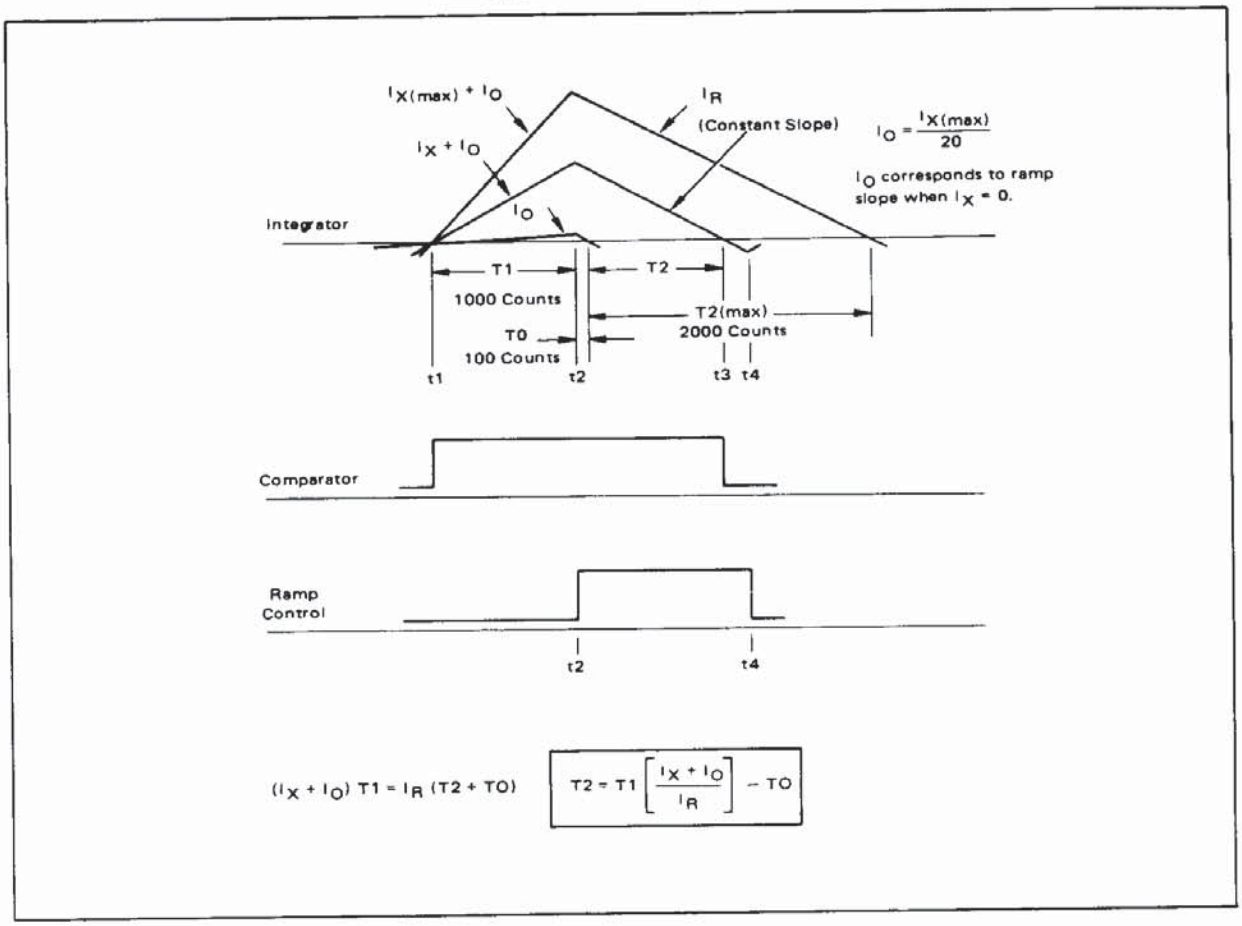


FIGURE 8 – MC1505 SYSTEM TIMING DIAGRAM
(2.0 Volt Full Scale Input)



threshold is 1.25 volts.

The integrator is a single stage, wide bandwidth amplifier. Its low propagation delay and low output impedance minimize ramp spikes due to output current reversal during ramp turn-around. The input bias current is typically one part in 50,000 of the full scale current, so that its temperature change contributes negligible error. Gain and input offset voltage are not critical since the integrator is driven from current sources.

The comparator is designed for low hysteresis by maintaining a constant power dissipation regardless of output state. This hysteresis is typically 0.1 mV and remains constant with temperature variations, so that no measurable system error is contributed. Temperature variations in the value of the comparator threshold are not an error factor, since the only requirement is that the threshold remain constant during a given conversion cycle. Voltage gain of the comparator is 2,000,000 when driving CMOS, and 40,000 with one TTL load. The comparator output is slew rate controlled to provide output rise and fall times of approximately 80 ns. This minimizes noise generation which could affect system stability.

The system is zeroed and full scale calibrated by potentiometers which provide temperature compensation. All the other resistors are diffused in close proximity, yielding reference and unknown currents which have a closely tracking resistive temperature coefficient.

APPLICATIONS INFORMATION

The input configurations for the MC1505 are shown in Figure 11. Note that the differential input voltage must always remain the same polarity with Pin 1 positive with respect to Pin 2. Figures 11 and 13 will aid in the understanding of the input circuitry.

The input common mode rejection of the MC1505 is high enough to maintain rated accuracy with small changes in common mode voltage, such as would be seen with ground errors and noise. The system must be recalibrated, however, for larger changes in common mode input voltage.

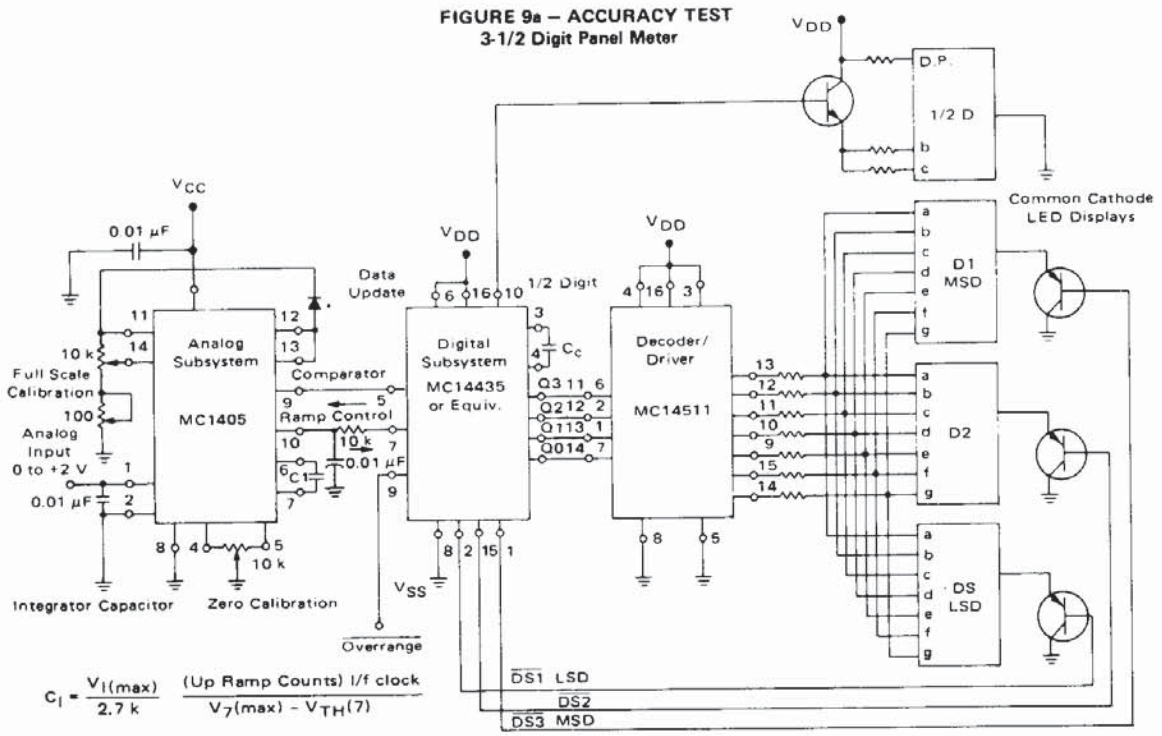
The MC1505 is arranged so that $I_X = I_R$ when $V_X = V_R$, or so that the ramp slopes are equal for input and reference voltages of 1 volt. As shown in Figure 8, a system with a 2 volt full-scale input requires twice as many digital counts during T2 as for T1. A system with a 1 volt full scale would require an equal number of counts in T1 and T2. Figure 9 illustrates a 3-1/2 digit system, but typical accuracies of the MC1505 allow its use in 4 digit applications. It can also be used in systems which require 4-1/2 digit resolution.

The ramp offset current and 100 count delay are shown in Figure 8. In certain applications, a different number of counts may be used. The system will not always operate properly, however, with a 10 count delay since the ramp offset current is used to zero the system and compensate for error in the input resistor bridge. This error, known as I_{XO}, is current which flows to or from the input converter with zero volts applied to the input. It is typically between ±5.0 μA, which is 1% of full scale in a 2 volt system. A 10 count delay would need a 0.5% ramp offset current, which would not always be able to cancel this error. Also, a 10 count delay does not provide enough signal-to-noise margin for consistently accurate low-level conversion.

The integrating capacitor is chosen with the equations shown in Figure 9. The maximum ramp voltage should be used for best signal-to-noise ratio, but temperature changes in I_X, I_R and the capacitor should be anticipated to prevent integrator saturation. Variations in clock frequency should also be considered. A polar capacitor with Pin 7 at the + terminal may be used. However, settling time will be increased when electrolytics are used, Tantalum electrolytics are preferred.

The lower half of the diode current switch is split with separate diodes for I_X and I_O. In most applications Pins 12 and 13 will be connected so that the two device emitters are effectively one, since the main purpose of these pins is for testing. Connecting these pins allows proper system zero adjustment and prevents turn-off of the switch diode with low unknown current levels. This yields better conversion accuracy.

FIGURE 9a – ACCURACY TEST
3-1/2 Digit Panel Meter



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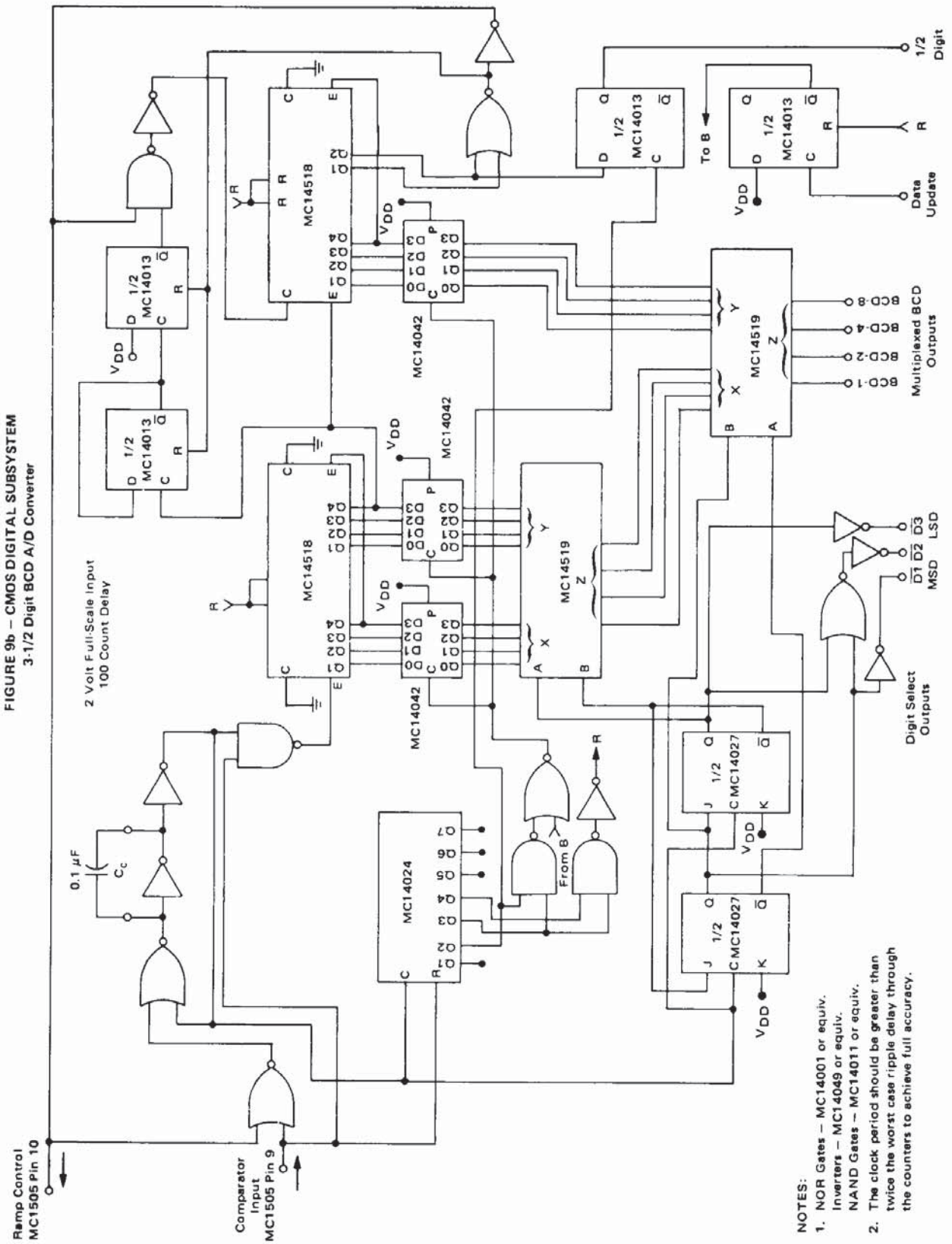

FIGURE 9b – CMOS DIGITAL SUBSYSTEM
3-1/2 Digit BCD A/D Converter

NOTES:
1. NOR Gates – MC14001 or equiv.
   Inverters – MC14049 or equiv.
   NAND Gates – MC14011 or equiv.
2. The clock period should be greater than twice the worst case ripple delay through the counters to achieve full accuracy.

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FIGURE 9c – FUNCTIONAL DIAGRAM OF MC14435 CMOS DIGITAL SUBSYSTEM

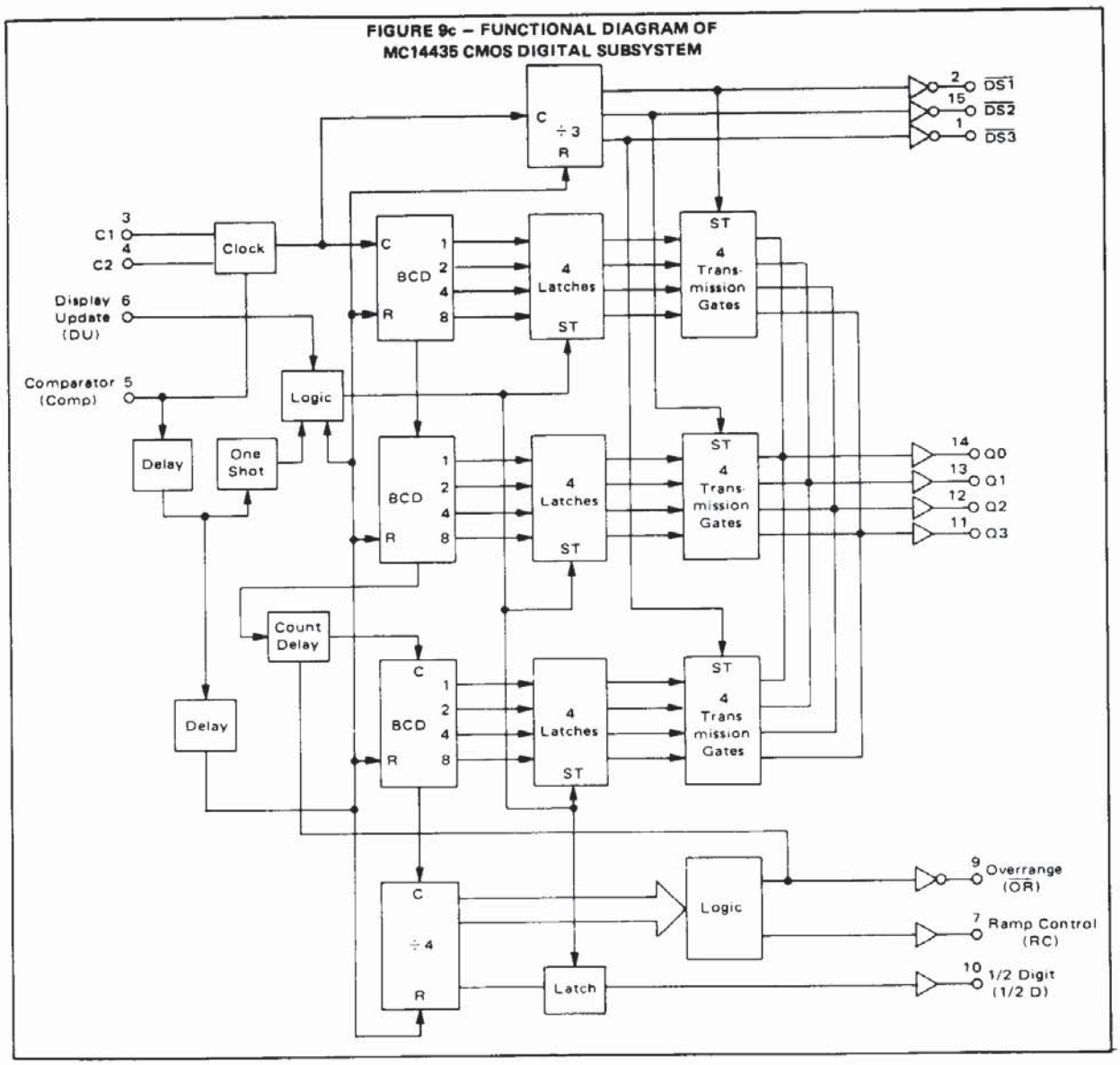
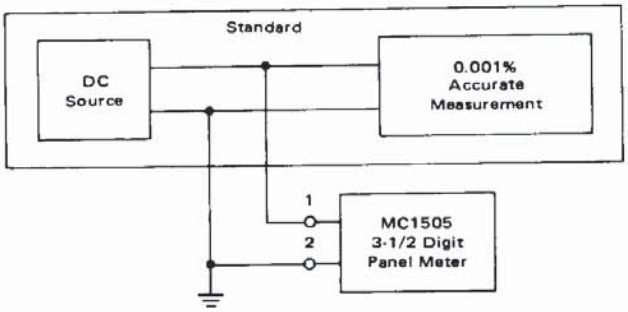


FIGURE 10 – CALIBRATION SET-UP



Zero Calibration:

Set standard at 0.0005 V.

Adjust zero potentiometer for panel meter display transition between 0.000 and 0.001 V. Note: An analog input of -1 mV yields a reading of 0.099.

Repeat zero and full scale calibration until meter is calibrated at both ends of the scale.

Full Scale Calibration:

Set standard at 1.9995 V.

Adjust full scale potentiometer for panel meter display transition between 1.999 and 1.000 V. (overrange)

Linearity Test:

Adjust standard for the desired panel meter transition and record the value of the standard.

At initial turn-on, set Pin 14 to ≈1.0 Volt with full scale potentiometer.

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FIGURE 11 – ANALOG INPUT RANGE

The input circuit for the MC1505 has a unipolar differential input range of +2 volts and a bipolar common mode input range of ±1.5 volts.

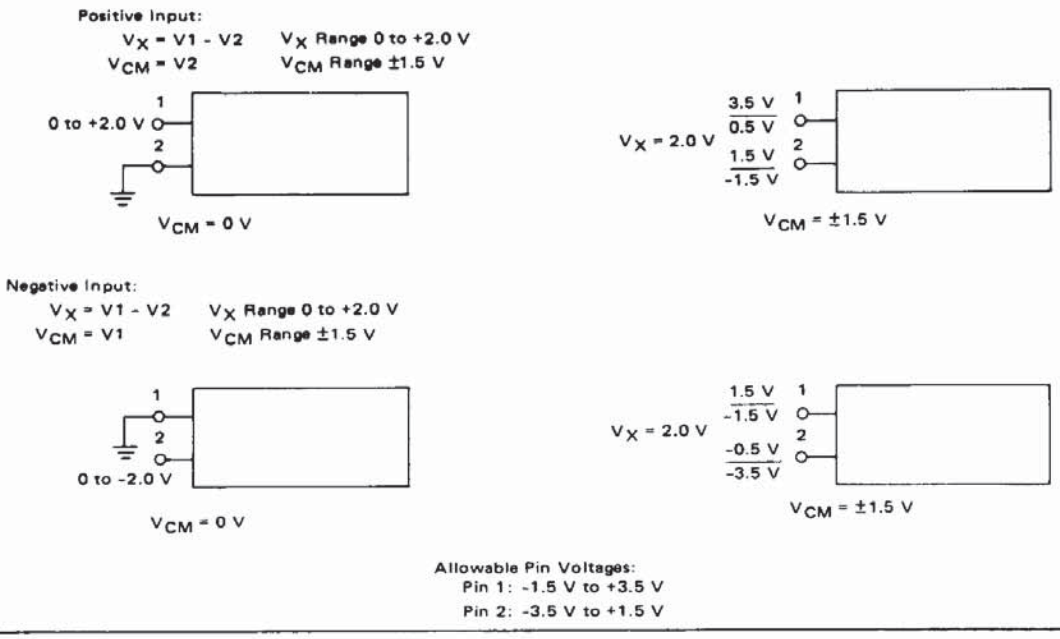

FIGURE 12 – CIRCUIT TO PREVENT POSSIBLE LATCHUP WITH APPLICATION OF NEGATIVE INPUT VOLTAGES

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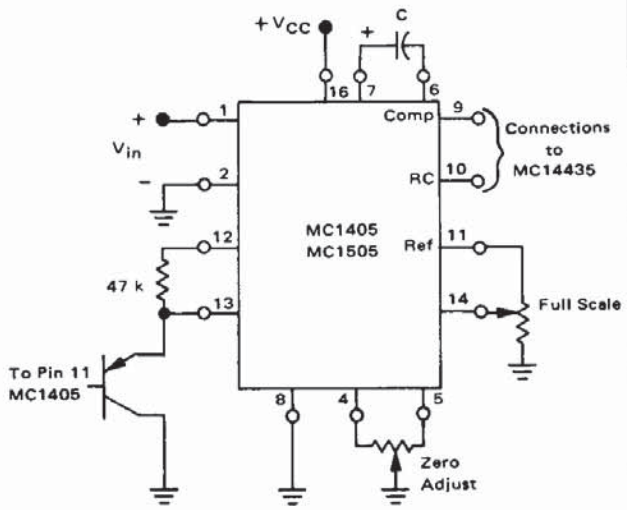
The MC1405/1505 A/D analog subsystem is intended for positive input voltages only (i.e., pin 1 positive with respect to pin 2). However, should pin 2 become more than 100 mV positive with respect to pin 1, the internal input amplifier may go into a latchup mode which will require that the system power be turned off and then reapplied to reset the system. To prevent this problem a PNP transistor can be used as shown in the accompanying figure. The base-emitter junction of the transistor clamps pin 13 at one diode drop above the reference voltage (pin 11) to prevent the latchup. The gain of the transistor insures that the reference need not sink more than 500 μA of current.

The 47 kΩ resistor is required only if the A/D system is to continue to convert under reverse polarity conditions such as for autopolarity schemes.



*47 kΩ resistor required if conversions are to continue during input polarity reversal, otherwise tie pins 12 and 13 together.

TYPICAL PERFORMANCE CURVES

FIGURE 13 – MAXIMUM COMMON-MODE INPUT VOLTAGE versus TEMPERATURE

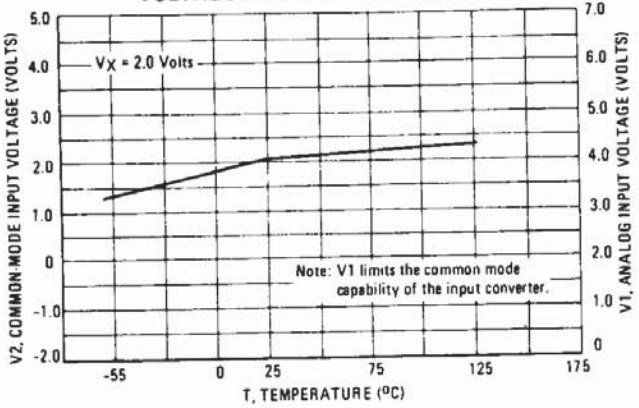


FIGURE 14 – INPUT CURRENT versus INPUT VOLTAGE

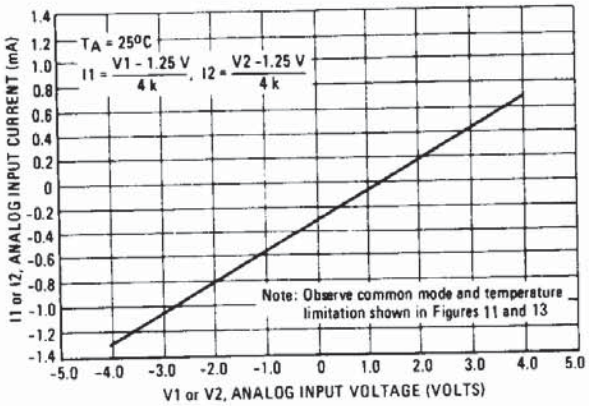


FIGURE 15 – UNKNOWN CURRENT versus ANALOG INPUT VOLTAGE

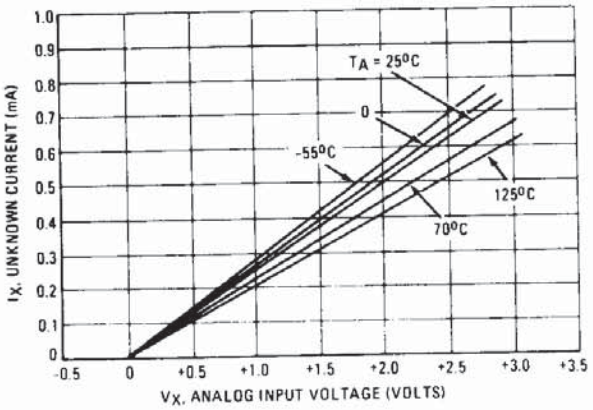


FIGURE 16 – REFERENCE CURRENT versus REFERENCE INPUT VOLTAGE

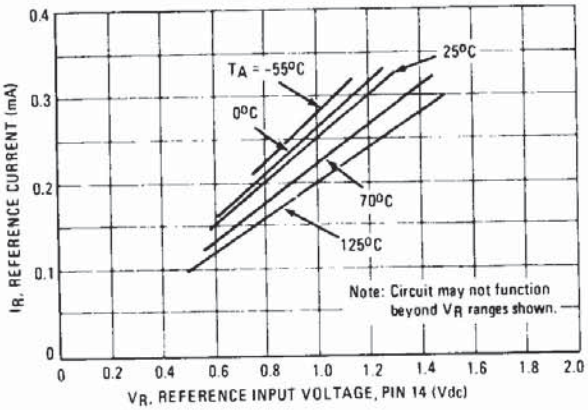


FIGURE 17 – TYPICAL POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

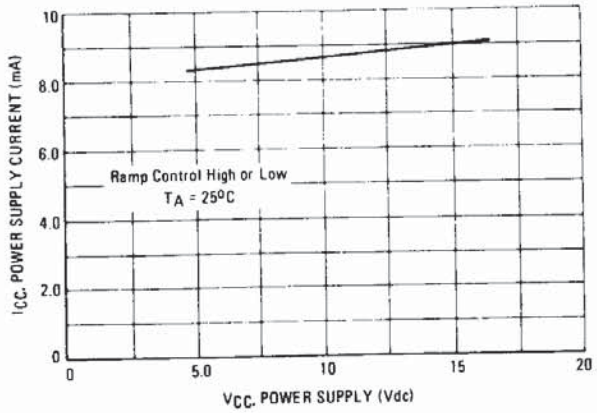


FIGURE 18 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

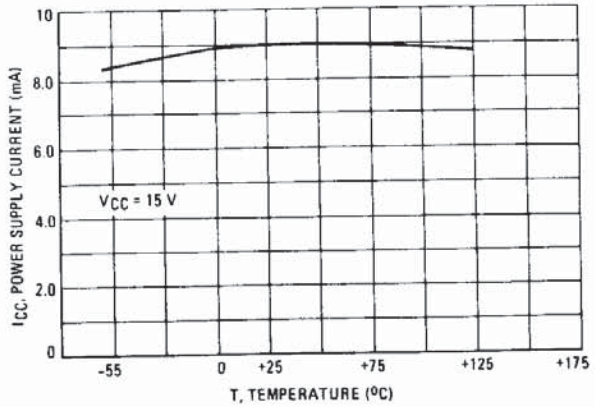


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FIGURE 19 – CURRENT SWITCH TRANSFER CHARACTERISTIC

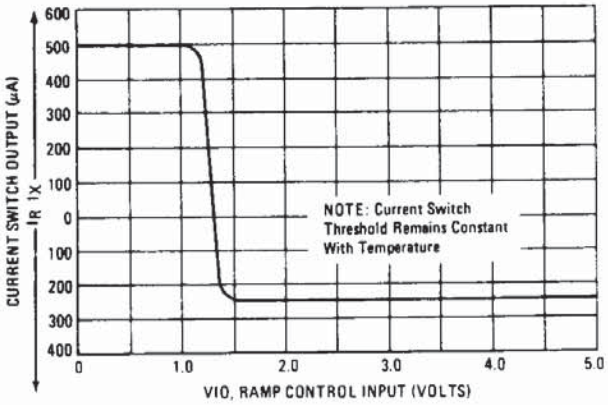


FIGURE 20 – INTEGRATOR OUTPUT SWING versus TEMPERATURE

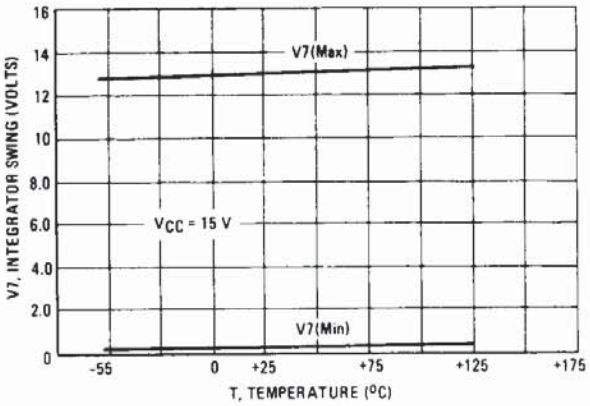


FIGURE 21 – COMPARATOR THRESHOLD versus TEMPERATURE

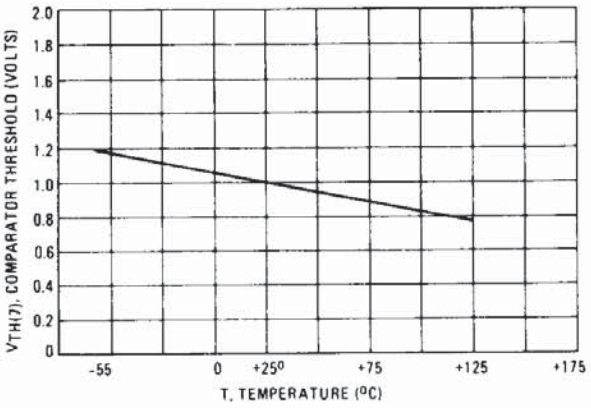


FIGURE 22 – RAMP CURRENT RATIO versus POWER SUPPLY

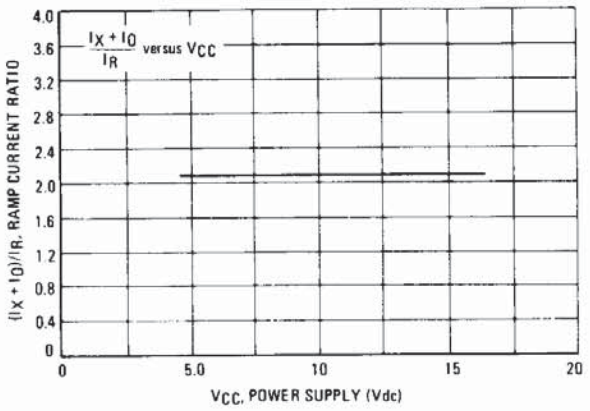
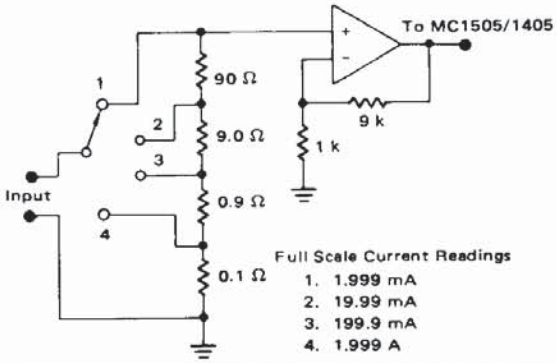
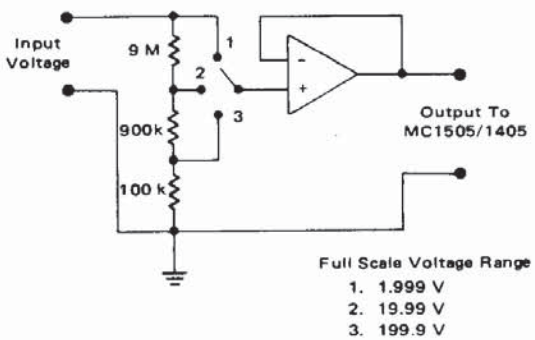


FIGURE 23 – CURRENT MEASUREMENT CIRCUITRY



If a voltage drop of 2.0 V full scale can be tolerated the resistors may be increased by a factor of ten and a unity gain buffer may be employed.

FIGURE 24 – DVM VOLTAGE RANGING



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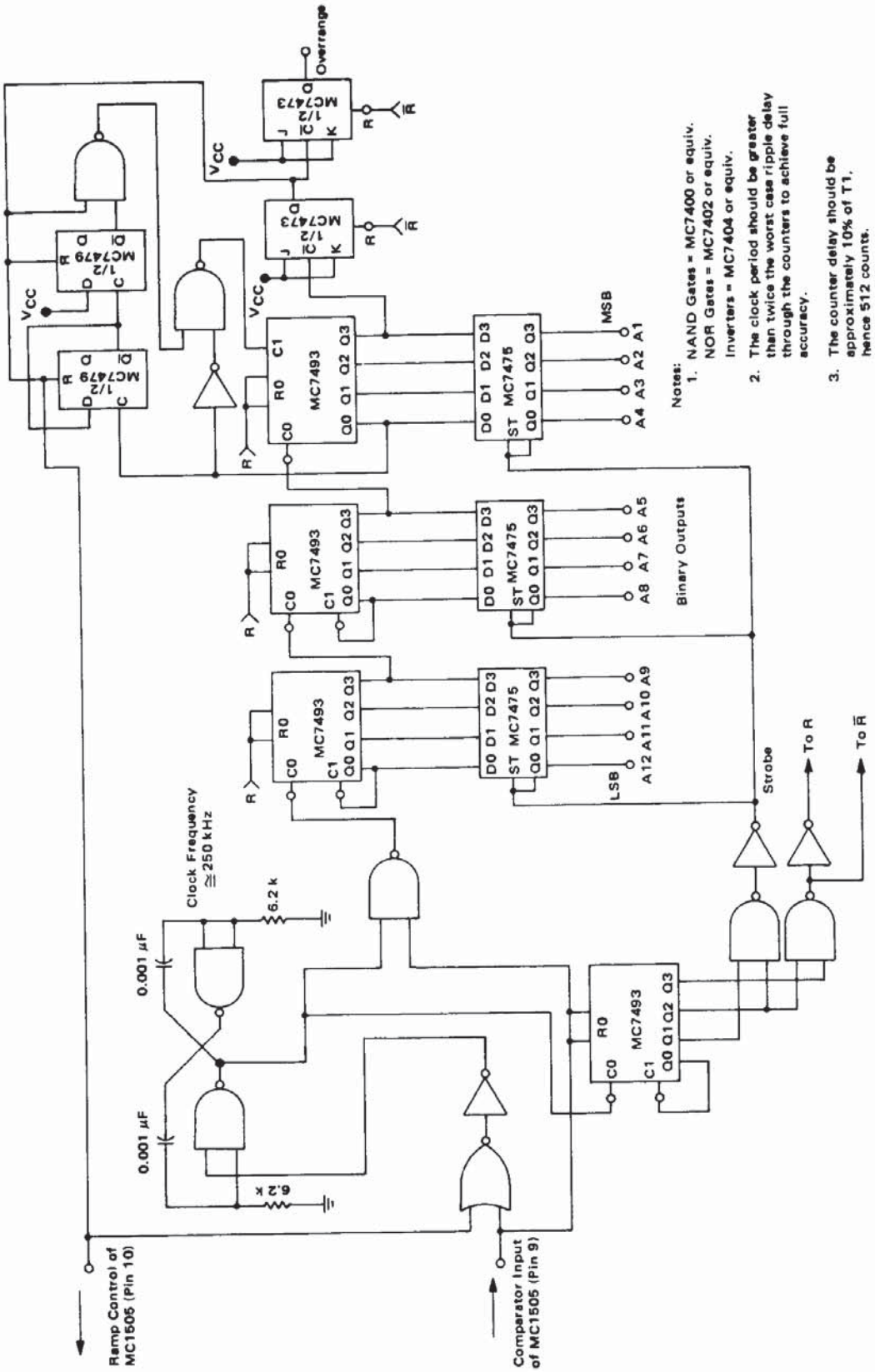

FIGURE 25 – MTTL DIGITAL SUBSYSTEM
12 Bit Binary A/D Converter
(1.0 Volt Full Scale, 512 Count Delay)

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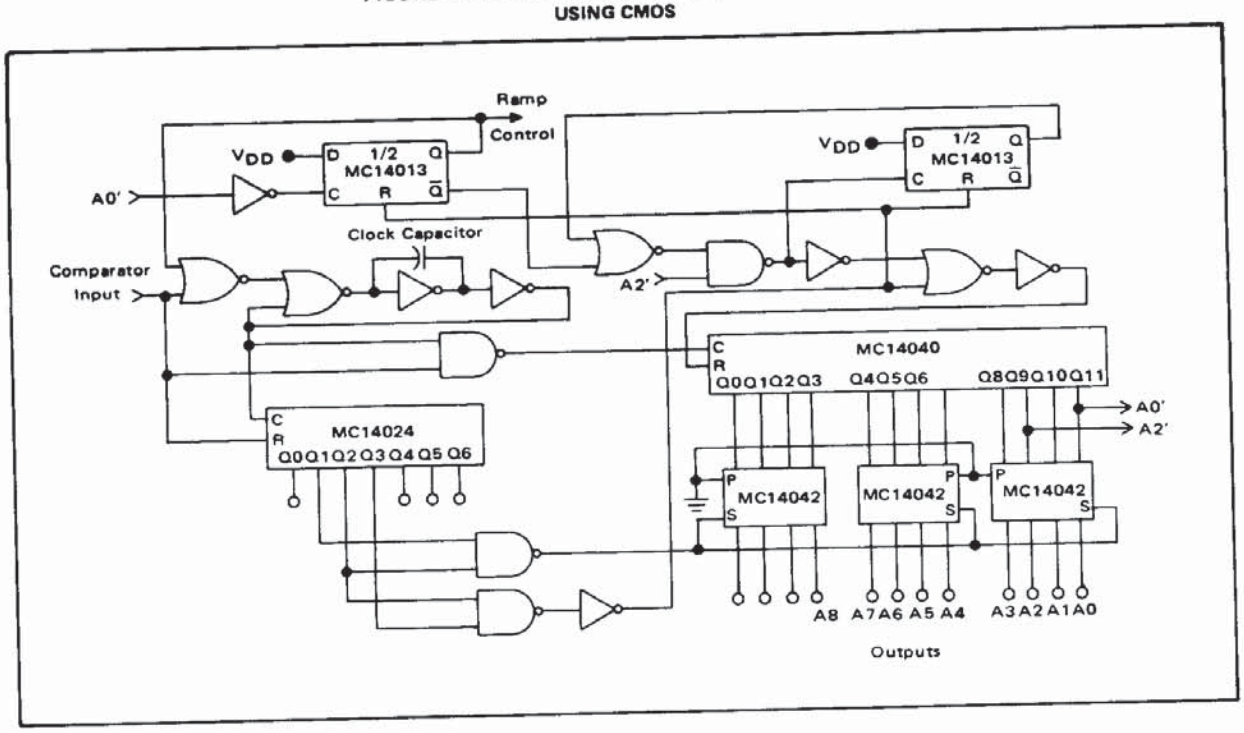
FIGURE 26 – 12-BIT BINARY A/D LOGIC SUBSYSTEM USING CMOS



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