PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD63711

COMPACT DISC DIGITAL SERVO/DATA PROCESSOR WITH ON-CHIP RF AMPLIFIER

The μPD63711 is an LSI that has all of the functions required to control a CD player, with a digital servo, data processor, RF amplifier, audio DAC, and post-processing filter incorporated on a single chip. CD-TEXT is also supported.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD63711 User's Manual: To be prepared

FEATURES

- Realization of set miniaturization by integrating a digital servo, data processor, 8-fs oversampling digital filter, D/A converter, and RF amplifier on a single chip.
- On-chip SCF (Switched Capacitor Filter) as audio DAC block post-processing filter
- Employment of digital loop filter for four servo systems. Since the filter coefficient is programmable, a variety of characteristics can be realized.
- On-chip automatic adjustment function. Automatic adjustments of focus offset, focus gain, focus balance, tracking offset, tracking gain, and tracking balance are possible.
- On-chip 16-Kbit SRAM needed for de-interleaving.
- Since a digital PLL circuit is employed, the external components of the bit clock regeneration circuit are not needed.
- CIRC error correction capability C1: Double correction C2: Quadruple correction (CD-ROM mode)
- On-chip fourth order ΔΣ type one-bit D/A converter and post-processing filter
- On-chip mirror circuit, DEFECT circuit, RFOK circuit, and EFM comparator.
- A de-emphasis circuit can be controlled via a microcontroller for supporting connection with shock-proof ICs.
- Crystal oscillation stop function
- Pickup of both current and voltage output can be supported.
- Single 5-V power supply

ORDERING INFORMATION

Part Number	Package
μPD63711GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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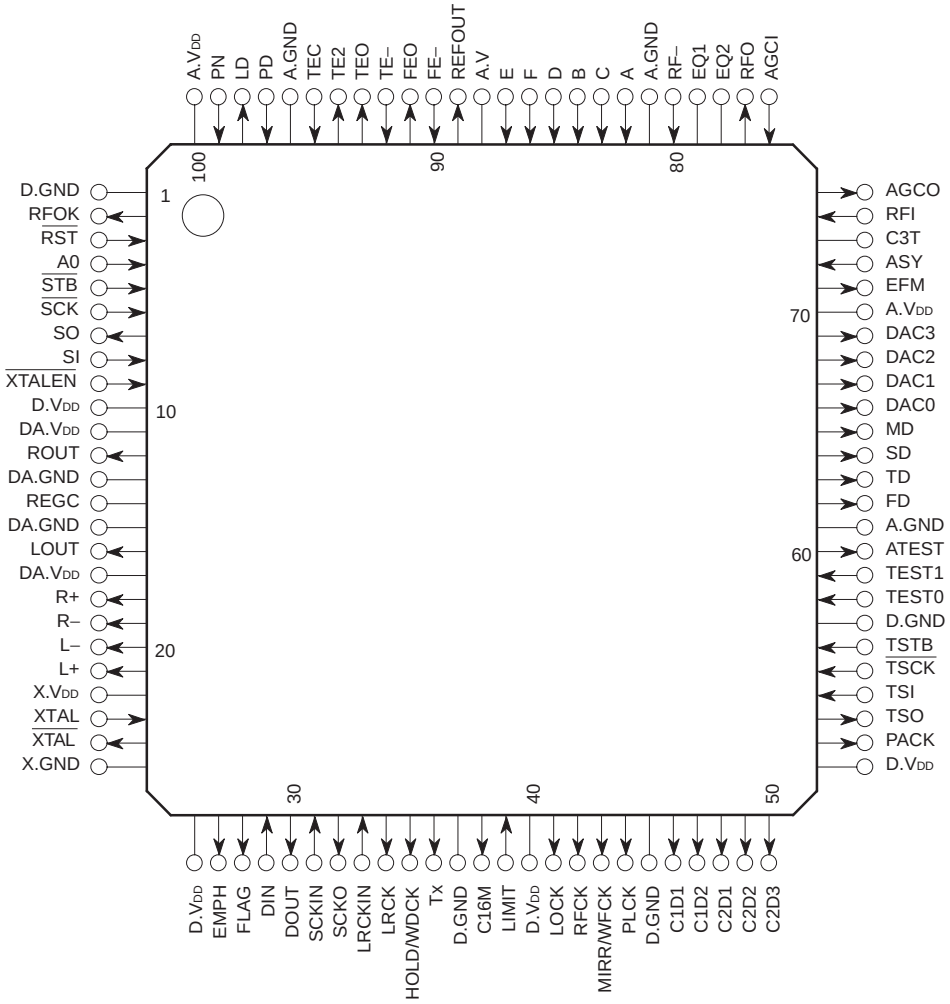
PIN CONFIGURATION (Top View)

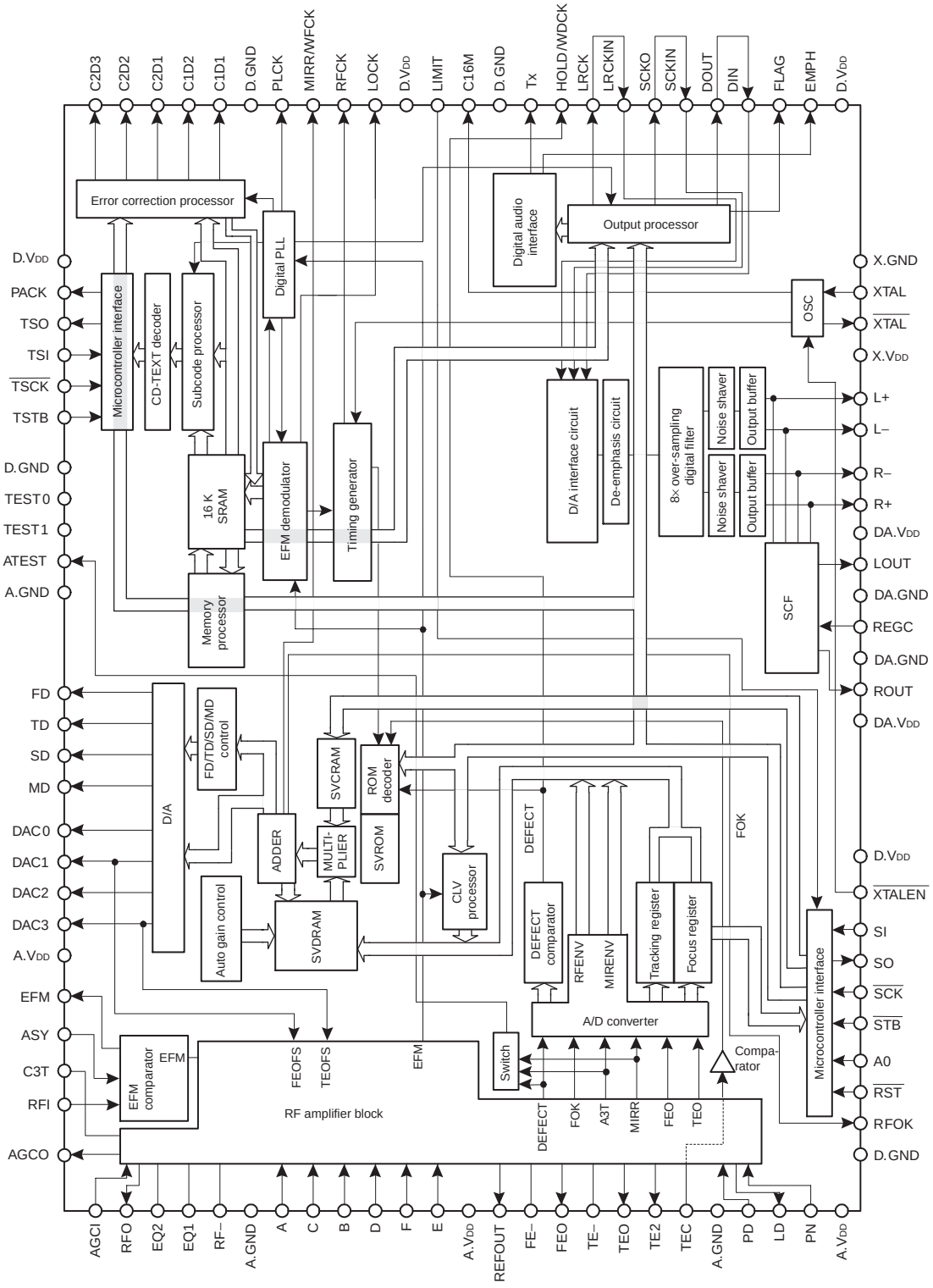
• 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

μPD63711GC-8EU

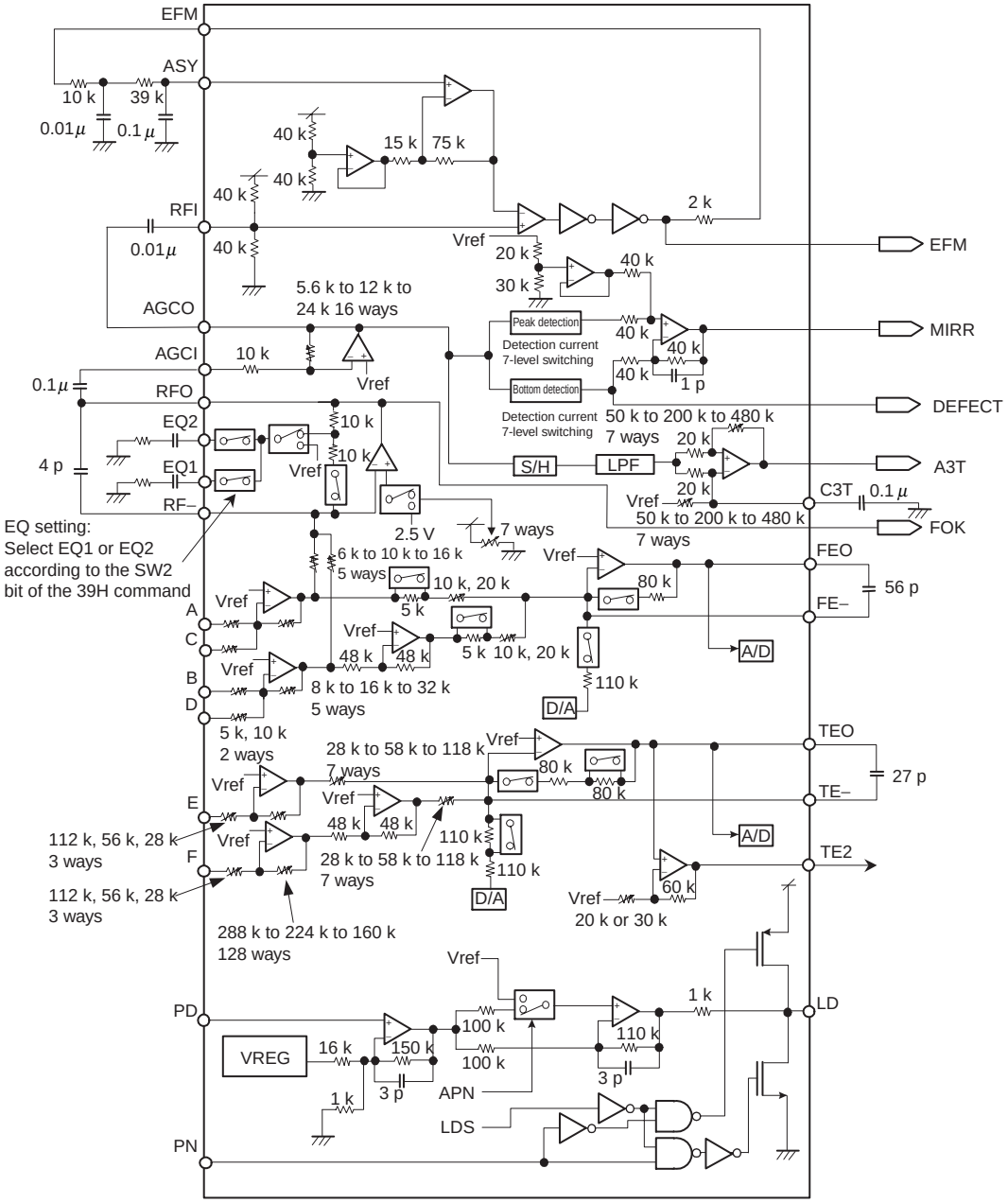


A, C, B, D, F, E:	Error Signal Input
A.GND:	Analog Ground
A.V_{DD}:	Analog Power Supply
A0:	Address 0
AGCI:	AGC Amp Input
AGCO:	AGC Amp Output
ASY:	Slice Level
ATEST:	Analog Test
C16M:	Clock 16 MHz
C1D1, C1D2,: C2D1 to C2D3	Correction Data
C3T:	Capacitance Connection for 3T Signal Detecting Circuit
D.GND:	Digital Ground
D.V_{DD}:	Digital Power Supply
DA.GND:	D/A Converter Ground
DA.V_{DD}:	D/A Converter Power Supply
DAC0 to DAC3:	D/A Converter Output
DIN:	Data Input
DOUT:	Data Output
EFM:	EFM Signal
EMPH:	Emphasis
EQ1, EQ2:	Equalizer Parts Connection for RF Amp
FD:	Focus Drive
FE:	Focus Error
FE–:	Impedance Connection to Focus Error Amp for Negative Feedback
FEO:	Focus Error Amp Output
FLAG:	Flag
HOLD/WDCK:	Hold Control/Word Clock
L+, L–:	L-channel Sound Data Output (PWM)
LD:	Laser Diode Control Current Output
LOCK:	Lock
LOUT:	L-channel Audio Signal Output
LRCK:	LR Clock
LRCKIN:	LR Clock Input
MD:	Motor Drive
MIRR/WFCK:	MIRR Signal/Write Frame Clock
PACK:	Pack Signal Sync
PD:	Photo Diode Signal (for Detecting Laser Power) Input
PLCK:	PLL Lock
PN:	APC Circuit Polarity Control
LIMIT:	Pick Inner Detect
R+, R–:	R-channel Sound Data Output (PWM)
REFOUT:	Reference Output
REGC:	Capacitor Connection for Regulator
RF–:	Impedance Connection to RF Amp for Negative Feedback
RFCK:	Read Frame Clock
RFI:	RF Signal Input
RFO:	RF Amp Output
RFOK:	RFOK Signal
ROUT:	R-channel Audio Signal Output
$\overline{RST}$:	Reset
$\overline{SCK}$:	Serial Clock
SCKIN:	Serial Clock Input
SCKO:	Serial Clock Output
SD:	Sled Drive
SI:	Serial Data Input
SO:	Serial Data Output
$\overline{STB}$:	Strobe
TD:	Tracking Drive
TE:	Tracking Error
TE–:	Impedance Connection to Tracking Error Amp for Negative Feedback
TE2:	Tracking Error Amp Output Multiplied by Two
TEC:	Tracking Error Comparator
TEO:	Tracking Error Amp Output
TEST0, TEST1:	Test
$\overline{TSCK}$:	Serial Clock for Text Data
TSI:	Parameter Input for Text Data
TSO:	Serial Text Data Output
TSTB:	Text Parameter Strobe
Tx:	Transmit Data
X.GND:	Crystal Oscillator Ground
X.V_{DD}:	Crystal Oscillator Power Supply
XTAL, $\overline{XTAL}$:	Crystal Connection
$\overline{XTALEN}$:	Crystal Oscillation Enable

BLOCK DIAGRAM



RF amplifier block



Remark The unit of resistance is Ω and capacitance is F.

CONTENTS

1. PIN FUNCTIONS

Pin No.	Pin Name	Description	I/O	Initial Value
1	D.GND	Logic circuit GND	–	–
2	RFOK	RFOK signal output pin	O	Undefined
3	$\overline{\text{RST}}$	Reset signal input pin (Active low)	I	–
4	A0	Command/parameter identifying signal input pin This is used in combination with $\overline{\text{STB}}$. A0 = L: With $\overline{\text{STB}}$ active, set to address register A0 = H: With $\overline{\text{STB}}$ active, parameter setting	I	–
5	$\overline{\text{STB}}$	Data strobe signal input pin This is the signal for latching serial data inside the LSI.	I	–
6	$\overline{\text{SCK}}$	Clock signal input pin for serial data input and output Input data from the SI pin is captured when this signal rises and serial data from the SO pin is output when it falls.	I	–
7	SO	Outputs serial data and status signal	O	Undefined
8	SI	Serial data input pin	I	–
9	$\overline{\text{XTALEN}}$	Crystal oscillation control pin. Be sure to input the reset signal before stopping crystal oscillation. When the status shifts from crystal oscillation stop mode to normal mode, input the reset signal after crystal oscillation has stabilized. $\overline{\text{XTALEN}}$ = L: Normal mode $\overline{\text{XTALEN}}$ = H: Crystal oscillation stop mode	I	–
10	$D.V_{DD}$	Positive power supply pin to logic circuit	–	–
11	$DA.V_{DD}$	Positive power supply pin to D/A converter block	–	–
12	ROUT	R-ch audio signal output pin	AO	Undefined
13	DA.GND	D/A converter block GND	–	–
14	REGC	SCF regulator external capacitor connection pin	A–	–
15	DA.GND	D/A converter block GND	–	–
16	LOUT	L-ch audio signal output pin	AO	Undefined
17	$DA.V_{DD}$	Positive power supply pin to D/A converter block	–	–
18	R+	Right channel sound data output pin. PWM output	O	L
19	R–			H
20	L–	Left channel sound data output pin. PWM output	O	H
21	L+			L
22	$X.V_{DD}$	Positive power supply pin to crystal oscillator	–	–
23	XTAL	Crystal oscillator connection pin (input)	I	–
24	$\overline{\text{XTAL}}$	Crystal oscillator connection pin (output)	O	–
25	X.GND	Crystal oscillator GND	–	–
26	$D.V_{DD}$	Positive power supply pin to logic circuit	–	–
27	EMPH	Subcode Q pre-emphasis information output pin When applying emphasis, a high level is output. Commands can be used to switch polarity. F6H LSB EP = 0: Normal output EP = 1: Inverted output	O	Undefined

Pin No.	Pin Name	Description	I/O	Initial Value
28	FLAG	Flag output pin indicating that the data currently being output was configured with uncorrectable data. (Active high)	O	Undefined
29	DIN	Serial data input pin to on-chip DAC If a DSP (etc.) is not connected, this must be shorted with the DOUT pin.	I	–
30	DOUT	Serial sound data output pin	O	L
31	SCKIN	Serial clock input pin to on-chip DAC	I	–
32	SCKO	Sound data output from DOUT changes with the falling of this clock. Ensure that the system connected in the next stage captures the data at the rising of this signal.	O	Undefined
33	LRCKIN	LRCK signal input pin to on-chip DAC	I	–
34	LRCK	Signal that distinguishes left channel and right channel of sound data output from DOUT	O	Undefined
35	HOLD/ WDCK	Defect detection output pin (HOLD) Pin that outputs a signal twice the frequency of LRCK (88.2 kHz) (WDCK) HOLD and WDCK can be switched by microcontroller.	O	Undefined
36	Tx	Data output pin of digital audio interface	O	L
37	D.GND	Logic circuit GND	–	–
38	C16M	Buffering output pin of oscillation clock	O	–
39	LIMIT	The state of this pin is output in Bit5 of the status output.	I	–
40	$D.V_{DD}$	Positive power supply pin to logic circuit	–	–
41	LOCK	EFM synchronization detection signal This is high level if the frame counter output matches the synchronization pattern detection signal in the EFM demodulation block, and low level if they do not match.	O	Undefined
42	RFCK	Frame synchronization signal of XTAL system This is the divided crystal resonator clock and indicates a period of one frame (7.35 kHz).	O	Undefined
43	MIRR/ WFCK	Mirror output pin (MIRR) Frame synchronization signal of PLL system. This signal is a signal with a frequency that is a division of the basic frequency (44.1 kHz) of the read signal acquired from the PLL system and is approximately equal to 1 frame cycle (7.35 kHz) (WFCK). MIRR and WFCK can be switched by microcontroller.	O	Undefined
44	PLCK	Pin for bit clock monitor When a PLL lock occurs, the falling edge of this signal locks to the EFM signal.	O	Undefined
45	D.GND	Logic circuit GND	–	–
46	C1D1	Output pins that indicate the results of C1 error correction These pins are defined until the falling edge of RFCK.	O	Undefined
47	C1D2			
48	C2D1	Output pins that indicate the results of C2 error correction These pins are defined until the falling edge of RFCK.	O	Undefined
49	C2D2			
50	C2D3			
51	$D.V_{DD}$	Positive power supply pin to logic circuit	–	–
52	PACK	PACK synchronization signal of CD-TEXT The fall of this signal indicates the beginning of the pack.	O	Undefined

Pin No.	Pin Name	Description	I/O	Initial Value
53	TSO	CD-TEXT data serial output pin	O	Undefined
54	TSI	CD-TEXT control parameter serial input pin	I	–
55	$\overline{\text{TSCK}}$	CD-TEXT serial clock input pin	I	–
56	TSTB	CD-TEXT parameter strobe signal input pin	I	–
57	D.GND	Logic circuit GND	–	–
58	TEST0	Test pins. Normally, connect to GND.	I	–
59	TEST1			
60	ATEST	Test pin. Normally, leave open.	AO	Undefined
61	A.GND	Analog circuit GND	–	–
62	FD	Focus drive output pin	AO	½ A.V_{DD}
63	TD	Tracking drive output pin	AO	½ A.V_{DD}
64	SD	Sled drive output pin	AO	½ A.V_{DD}
65	MD	Spindle drive output pin	AO	½ A.V_{DD}
66	DAC0	DAC output pin for adjustment. Outputs CRAM 7FH setting value.	AO	½ A.V_{DD}
67	DAC1	DAC output pin for adjustment. Outputs CRAM 7CH setting value. (On-chip RF FE amplifier offset)	AO	½ A.V_{DD}
68	DAC2	DAC output pin for adjustment. Outputs CRAM 7DH setting value.	AO	½ A.V_{DD}
69	DAC3	DAC output pin for adjustment. Outputs CRAM 7EH setting value. (On-chip RF TE amplifier offset)	AO	½ A.V_{DD}
70	A.V_{DD}	Positive power supply pin to analog circuit	–	–
71	EFM	EFM signal output pin	O	Undefined
72	ASY	EFM comparator reference voltage input pin	AI	–
73	C3T	Capacitor connection pin for 3T detection	A–	–
74	RFI	RF signal input pin for EFM data generation	AI	–
75	AGCO	RF signal output pin after gain adjustment	AO	½ A.V_{DD}
76	AGCI	RF-AGC amplifier input pin	AI	½ A.V_{DD}
77	RFO	RF summing amplifier output pin	AO	Undefined
78	EQ2	RF amplifier equalizer parts connection pin	A–	–
79	EQ1			
80	RF-	RF summing amplifier inverse input pin	AI	–
81	A.GND	Analog circuit GND	–	–
82	A	Photo-detector A input pin	AI	½ A.V_{DD}
83	C	Photo-detector C input pin	AI	½ A.V_{DD}
84	B	Photo-detector B input pin	AI	½ A.V_{DD}
85	D	Photo-detector D input pin	AI	½ A.V_{DD}
86	F	Photo-detector F input pin	AI	½ A.V_{DD}
87	E	Photo-detector E input pin	AI	½ A.V_{DD}
88	A.V_{DD}	Positive power supply pin to analog circuit	–	–
89	REFOUT	Reference potential output pin	AO	½ A.V_{DD}
90	FE-	Focus error amplifier inverse input pin	AI	½ A.V_{DD}

Pin No.	Pin Name	Description	I/O	Initial Value
91	FEO	Focus error amplifier output pin	AO	½ A.V_{DD}
92	TE-	Tracking error amplifier inverse input pin	AI	½ A.V_{DD}
93	TEO	Tracking error amplifier output pin	AO	½ A.V_{DD}
94	TE2	Pin from which tracking error is output after amplification	AO	½ A.V_{DD}
95	TEC	Tracking comparator input pin Inputs a tracking error signal whose DC component is cut. A tracking zero-cross is detected inside the LSI using this signal.	AI	–
96	A.GND	Analog circuit GND	–	–
97	PD	PD detection signal input pin for LD output monitor	AI	GND
98	LD	LD control current output pin	AO	Undefined
99	PN	APC circuit control polarity setting pin	I	–
100	A.V_{DD}	Positive power supply pin to analog circuit	–	–

Cautions 1. Do not allow any input pin to exceed the power supply voltage.

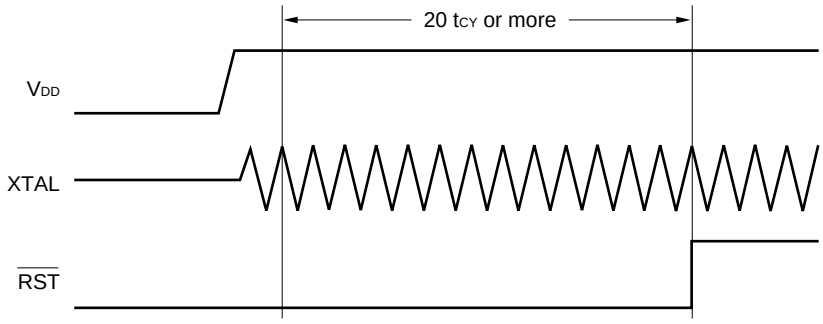
2. Make each power supply voltage (D.V_{DD}, A.V_{DD}, X.V_{DD}, DA.V_{DD}) the same potential.

Remark The meanings of symbols in the I/O column are as follows.

I: Logic level input pin
O: Logic level output pin
AI: Analog input pin
AO: Analog output pin
A–: Analog parts connection pin

Reset input

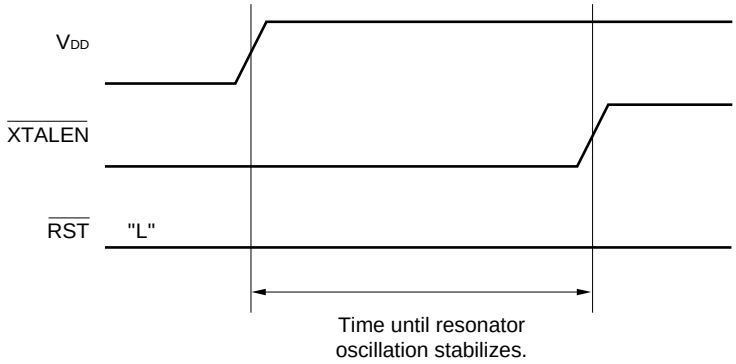
In the μPD63711, when the reset signal (active low) is input from the $\overline{RST}$ pin (pin 3) while the clock is being input from the XTAL pin (pin 23), it takes up to 20 clocks (about 1.2 μs) before the statuses of all the pins are defined. To allow for this, therefore, be sure to input the reset signal for a sufficient amount of time.



Cautions on using the $\overline{\text{XTALEN}}$ pin

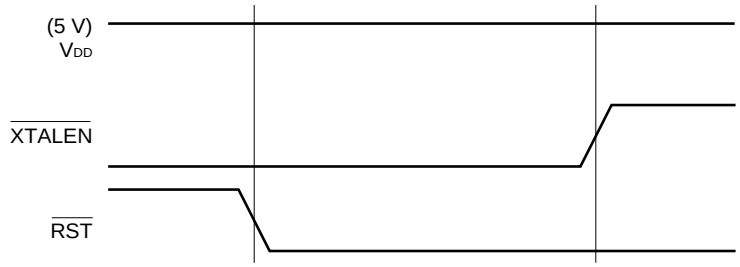
When stopping oscillation using the $\overline{\text{XTALEN}}$ pin, note the following.

1. When stopping oscillation immediately after the power supply is turned on.



The clock must be supplied while the reset signal is active, as in the above chart, even when stopping oscillation immediately after turning on the power supply.

2. When stopping oscillation in the normal use state



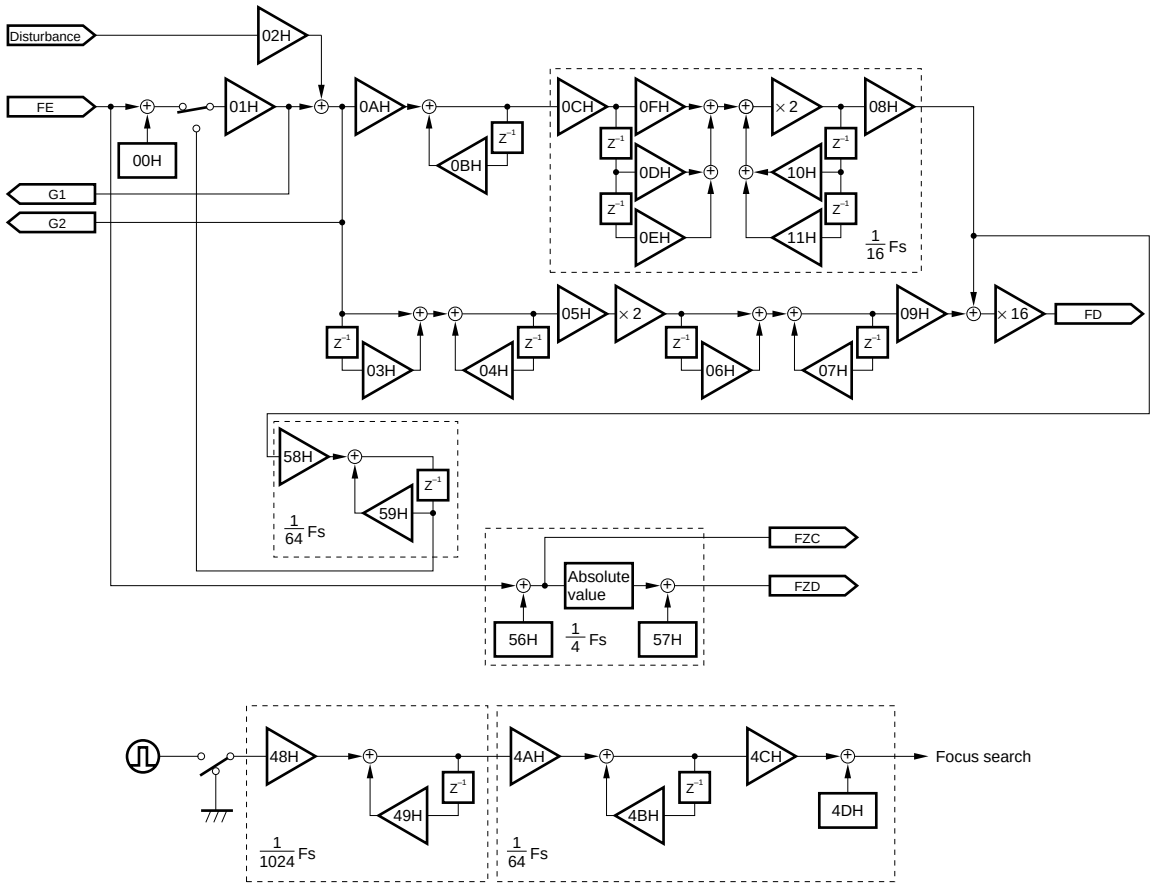
Be sure to set the reset signal to active before stopping oscillation.

If oscillation is stopped without setting the reset signal to active, output of the servo drive or sound will stop or become unstable, which may cause bugs in external devices.

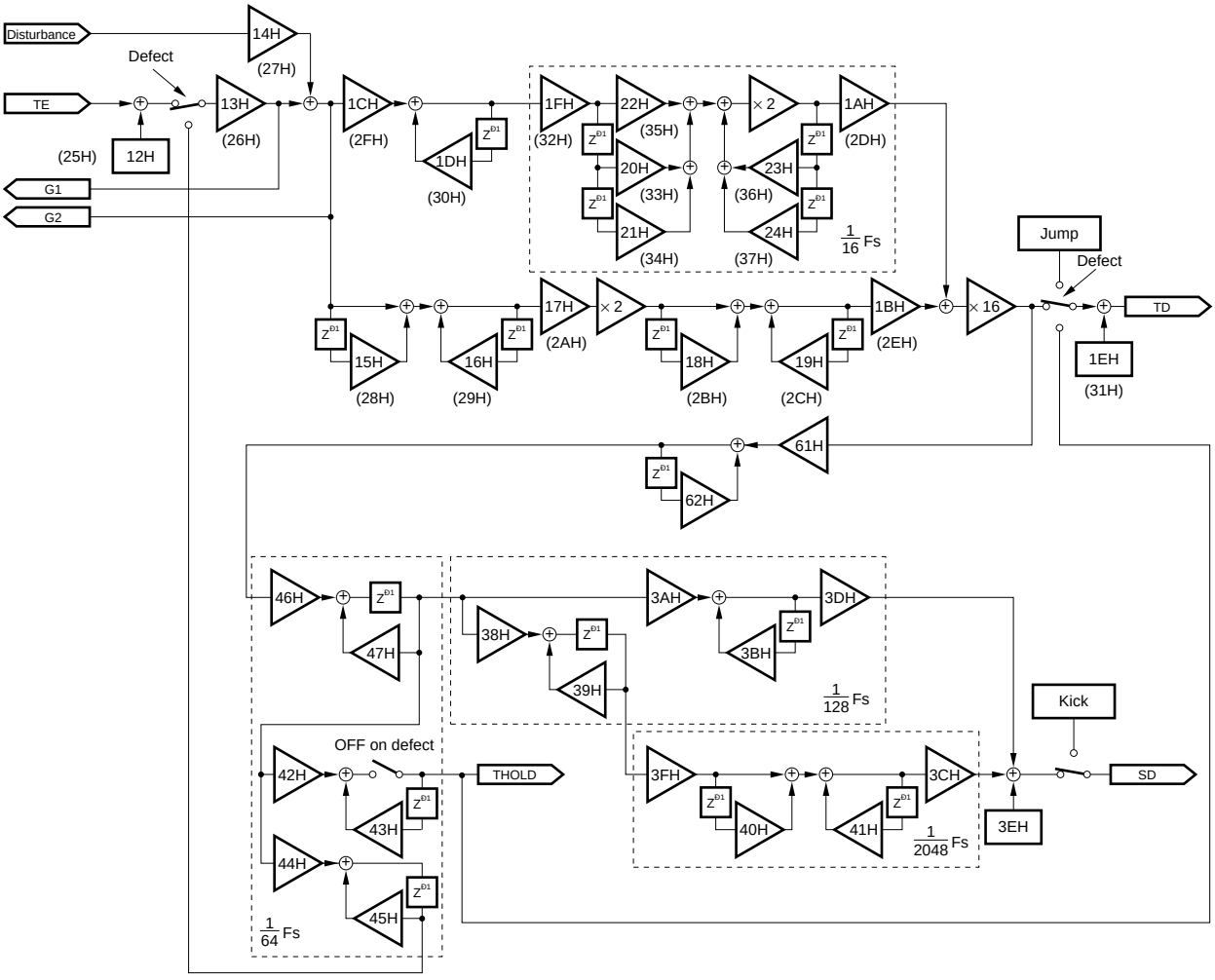
2. DIGITAL FILTER FLOWCHARTS

Flowcharts of the digital filters are shown below. Fs = 176.4 kHz.

(1) Focus filter

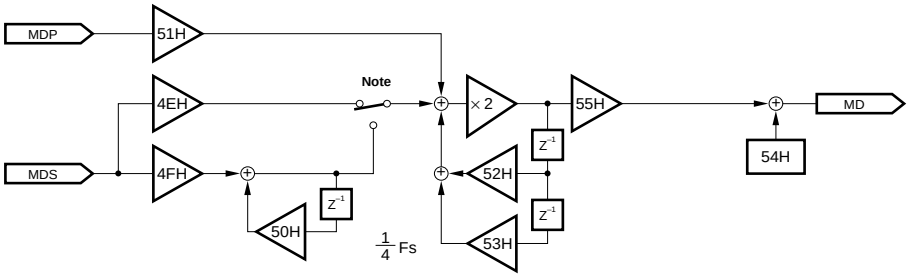


(2) Tracking and sled filters



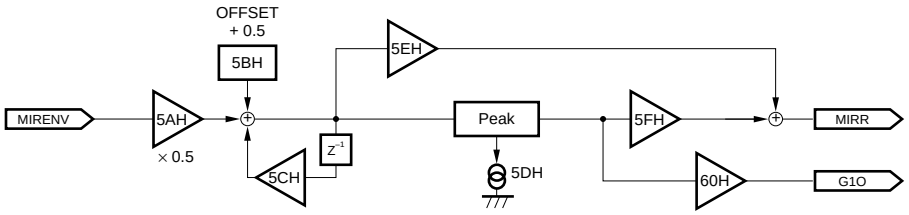
Remark Bank 1 addresses are shown in parentheses.

(3) Spindle system

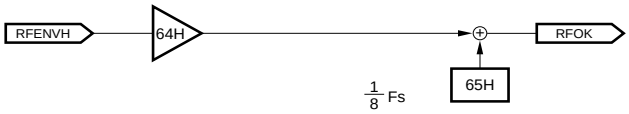


Note This switch is controlled according to the CLV lock decision signal (same signal as FR bit in status signal).
Asynchronous state: FR = 0 → Switch is down
Synchronous state: FR = 1 → Switch is up

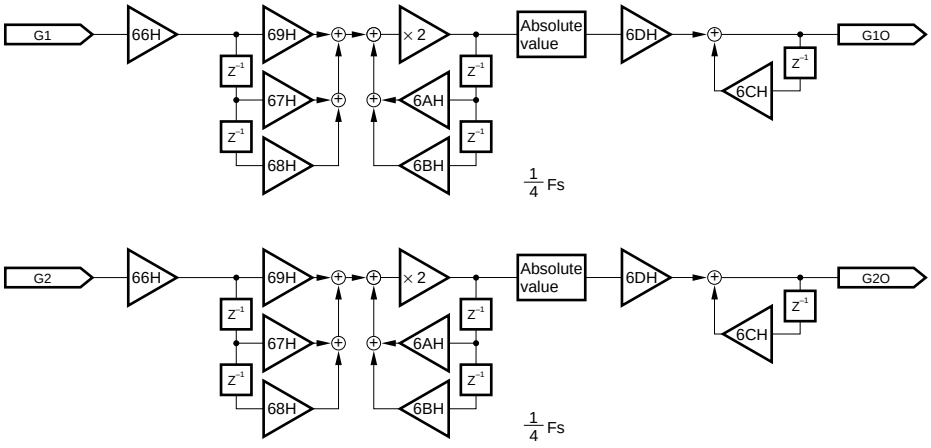
(4) MIRR signal



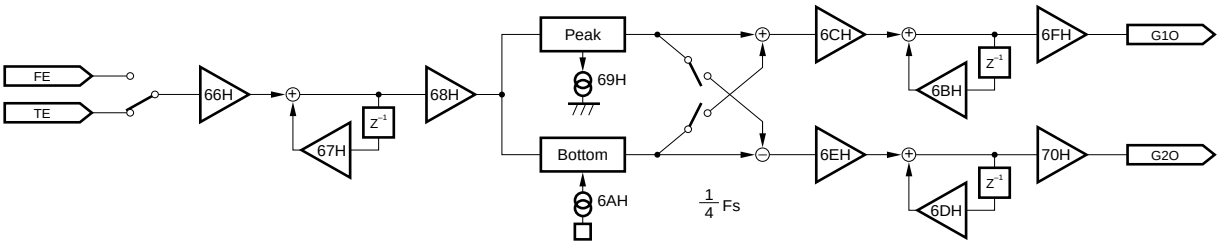
(5) RFOK signal



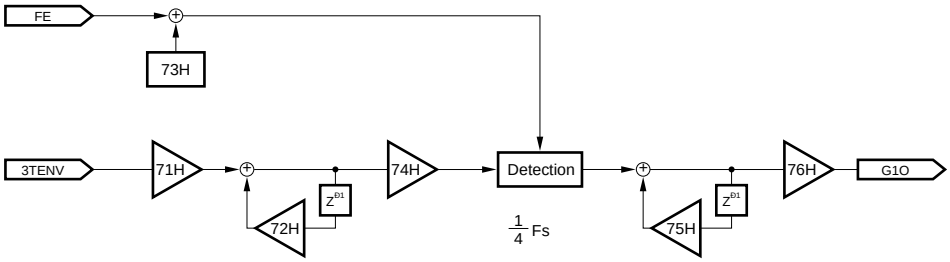
(6) Gain detection filter



(7) Balance adjustment filter



(8) 3T detection filter



3. MICROCONTROLLER INTERFACE COMMANDS

3.1 Servo System Commands

Table 3-1. Servo System Command Functions

Command	Function	Reference
00H	Writing data to CRAM	–
01H	CRAM address setting	–
10H	Servo control 0	p.18
11H	Servo control 1	p.20
12H	Servo control 2	p.22
13H	Focus search setting	p.23
14H	Disturbance generation and SO data output settings	p.24
15H	Half-wave brake control	p.26
17H	Disturbance frequency and level settings	p.27
18H	Defect comparator level setting	p.28
22H	Track jump kick time setting, traverse counter setting	p.29
23H		
24H		

Table 3-2. List of Servo System Commands (1/2)

Command (Command Code)	Parameter (Data)							
	MSB	6	5	4	3	2	1	LSB
00H	Writing data to CRAM							
01H	CRAM address							
10H	SK	TM	TEH	FR	TK	TB	T·CNT	BRK
11H	FON	TON	SON	MON	FST	DFCT	JSK	TAB
12H	BALON	SDMSK	SDL1	SDL0	DFCTT	SCV	0	TFP
13H	0	0	0	0	0	0	T1	T0
14H	GST	GON	GFT	T/3	G/B	SEL2	SEL1	SEL0
15H	BALSW	0	0	0	BKLMT	0	0	0
17H	FD2	FD1	FD0	FRQ4	FRQ3	FRQ2	FRQ1	FRQ0
18H	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
22H	0	TRACK KICK TIME A						
23H	0	TRACK KICK TIME B/TRAVERSE COUNTER N (H)						
24H	TRAVERSE COUNTER N (L)/TRACK JUMP COUNTER							

Table 3-2. List of Servo System Commands (2/2)

CRAM Address	CRAM Data
77H	TRACK KICK LEVEL A (kick level)
78H	TRACK KICK LEVEL B (brake level)
79H	SLED KICK LEVEL
7AH	Sled dead zone level setting (–)
7BH	Sled dead zone level setting (+)
7CH	DAC level setting for adjustment (DAC1 pin output) (On-chip RF FE amplifier offset)
7DH	DAC level setting for adjustment (DAC2 pin output)
7EH	DAC level setting for adjustment (DAC3 pin output) (On-chip RF TE amplifier offset)
7FH	DAC level setting for adjustment (DAC0 output)

Caution Do not send an undefined command.

(1) 10H command (Servo control 0)

MSB			Command				LSB
0	0	0	1	0	0	0	0
MSB			Parameter				LSB
SK	TM	TEH	FR	TK	TB	T·CNT	BRK

BRK	Half-Wave Brake Circuit
0	–
1	ON

T·CNT	Function of TK Bit
0	Start of track jump sequencer
1	Load value in traverse counter

TB	Tracking Filter Coefficient Bank
0	Bank 0
1	Bank 1

TK	Track Jump/Load Trigger
0	–
1	Execute operation specified by T·CNT bit

FR	Output Polarity Switching
0	Output level × –1
1	Leave output level unchanged

TEH	Error Hold Function on Track Jump
0	Hold reference (data 00)
1	Hold previous value

TM	Tracking Mute
0	Output results of tracking filter (normal operation)
1	Output value specified by TEH bit

SK	Sled Kick
0	–
1	Execute sled kick

[Functional description]

BRK: Controls the half-wave brake circuit.
- "1" Half-wave brake circuit is ON

T·CNT: Used in combination with the TK bit.
- "0" If TK = 1 is set, start a track jump sequencer
- "1" If TK = 1 is set, load the values of registers 23H and 24H in the traverse counter

TB: Switches the tracking filter coefficient bank.
- "0" Tracking filter bank 0
- "1" Tracking filter bank 1

TK: This is the track jump trigger and traverse counter load control.
It has two meanings depending on the T.CNT bit. An operation using the TK bit is a one-shot operation that operates only in the instant this is set to "1".

FR: Controls the output level polarity when tracking and sled kicking.
- "0" Output the value in the output level register (CRAM 77H to 79H) multiplied by –1
- "1" Output the value in the output level register unchanged

TEH: Controls the error hold function when track jumping.
Selects tracking output when SK = TM = 1.
- "0" Hold reference
- "1" Hold previous value

TM: Controls tracking mute.
- "0" Output the arithmetic result of the tracking filter (normal operation)
- "1" Either hold the previous value or hold a reference (data value 00) depending on the TEH bit specification

SK: Controls sled kick.
- "1" Perform sled kick using the value set in CRAM 79H

(2) 11H command (Servo control 1)

MSB			Command				LSB
0	0	0	1	0	0	0	1
MSB			Parameter				LSB
FON	TON	SON	MON	FST	DFCT	JSK	TAB

TAB	Track Jump Sequencer
0	–
1	Halt operation

JSK	Sled Kick
0	–
1	Execute sled kick

DFCT	Error Hold Output Upon Defect Detection
0	No
1	Yes

FST	Focus Search
0	–
1	Start focus search

MON	Spindle Servo Output
0	OFF (D/A output stopped, 1/2 A.V_{DD})
1	ON

SON	Sled Servo Output
0	OFF (D/A output stopped, 1/2 A.V_{DD})
1	ON

TON	Tracking Servo Output
0	OFF (D/A output stopped, 1/2 A.V_{DD})
1	ON

FON	Focus Servo Output
0	OFF (D/A output stopped, 1/2 A.V_{DD})
1	ON

[Functional description]

TAB: Controls close of track jump sequencer operation.

"1" Halt track jump sequencer operation

An operation using the TAB bit is a one-shot operation that operates only on the instant this is set to "1".

JSK: Controls sled kick when track jumping.

"1" Perform sled kick in the track jump period using the level set in CRAM 79H

DFCT: Controls error hold output on defect detection.

"0" No hold output

All switches controlled by a DEFECT signal in the focus filter and tracking filter are fixed in the up position (normal position).

"1" Hold output

Switch the above switches according to the DEFECT signal state.

FST: Focus search control.

"1" Start focus search

FON must be "1" at this time.

MON: Controls whether spindle servo output (D/A output) is ON or OFF.

"0" D/A output is OFF, output $\frac{1}{2}$A.V_{DD}

"1" D/A output is ON

SON: Controls whether sled servo output (D/A output) is ON or OFF.

"0" D/A output is OFF, output $\frac{1}{2}$A.V_{DD}

"1" D/A output is ON

TON: Controls whether tracking servo output (D/A output) is ON or OFF.

"0" D/A output is OFF, output $\frac{1}{2}$A.V_{DD}

"1" D/A output is ON

FON: Controls whether focus servo output (D/A output) is ON or OFF.

"0" D/A output is OFF, output $\frac{1}{2}$A.V_{DD}

"1" D/A output is ON

(3) 12H command (Servo control 2)

MSB			Command				LSB
0	0	0	1	0	0	1	0
MSB			Parameter				LSB
BALON	SDMSK	SDL1	SDL0	DFCTT	SCV	0	TFP

TFP	Output Polarity of TEC Pin
0	Normal
1	Inverted

SCV	Sled Servo Control by CLV Lock
0	Sled servo OFF when CLV is unlocked
1	Sled servo always ON

DFCTT	Input Hold Time Limit
0	Approximately 2.8 ms
1	Approximately 1.4 ms

SDMSK	SDL1	SDL0	Sled Kick Time after Track Jump
1	0	0	1.4 ms
1	0	1	2.9 ms
1	1	0	5.8 ms
1	1	1	11.6 ms
0	×	×	0 (none)

(Resolution = 180 μs)

BALON	DAC Pin Output
0	1/2 A.V_{DD}
1	DC voltage based on setting

[Functional description]

TFP: TEC signal (tracking error zero-cross signal) polarity control.
- "0" Normal output
- "1" Inverted output

SCV: Sled servo control by CLV lock.
- "0" Sled servo is OFF (D/A output halted) when CLV is unlocked (when FR bit in status signal is 0)
- "1" Sled servo is always ON regardless of CLV lock

At the time of a sled kick, D/A output is performed regardless of a CLV lock.

DFCTT: Sets the tracking or focus input hold time limit when the absence of an RF signal is detected.
- "0" Approximately 2.8 ms
- "1" Approximately 1.4 ms

SDMSK, SDL[1:0]: Sets the sled kick time after a track jump.

BALON: Sets DAC0 to DAC3 pin outputs.

This bit is set to "0" on a reset.
- "0" Output $\frac{1}{2}$ A.V_{DD}
- "1" Output DC voltage set using CRAM 7FH, 7CH, 7DH, and 7EH from DAC0 to DAC3 pins respectively

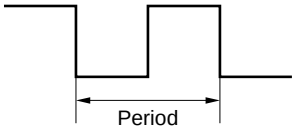
(4) 13H command (Focus search setting)

MSB			Command				LSB
0	0	0	1	0	0	1	1
MSB			Parameter				LSB
0	0	0	0	0	0	T1	T0

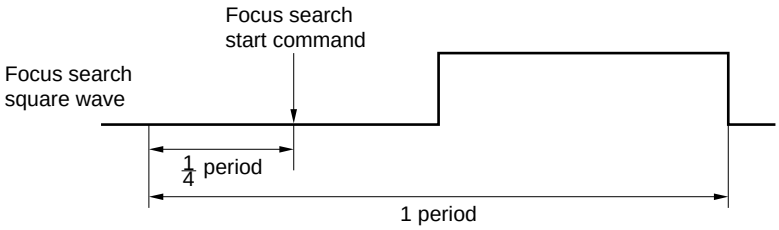
T1	T0	Square Wave Period on Focus Search
0	0	Approximately 0.37 s
0	1	Approximately 0.74 s
1	0	Approximately 1.49 s
1	1	Approximately 2.97 s

[Functional description]

T[1:0]: Sets the period of the square wave for focus search.



As shown below, square wave output on focus search is begun from the time one quarter of the period has gone by.



(5) 14H command (Disturbance generation and SO data output setting)

MSB			Command				LSB
0	0	0	1	0	1	0	0
MSB			Parameter				LSB
GST	GON	GFT	T/3	G/B	SEL2	SEL1	SEL0

SEL2	SEL1	SEL0	SO Data Output
0	1	0	FE
0	1	1	TE
1	0	0	G1
1	0	1	G2

T/3	G/B	Output Data to G1 and G2
0	0	Gain detection results
0	1	Data of filter for tracking balance adjustment (TE·PEAK, TE·BOTTOM)
1	0	RF amplitude detection results
1	1	3T detection results

GFT	Disturbance Feed Destination Selection (Selects Signal Input to Balance Detection Filter)
0	Focus equalizer (FE signal)
1	Tracking equalizer (TE signal)

GON	Feed of Disturbance to TE or FE Filter ON/OFF
0	Disturbance OFF
1	Disturbance ON

GST	Fetch Arithmetic Result of Filter for Gain Detection
0	–
1	Fetch

[Functional description]

SEL[2:0]: Sets SO data output.

G/B, T/3: Sets data to latch to G1 and G2 registers inside the LSI.

GFT: Selects the disturbance feed destination.

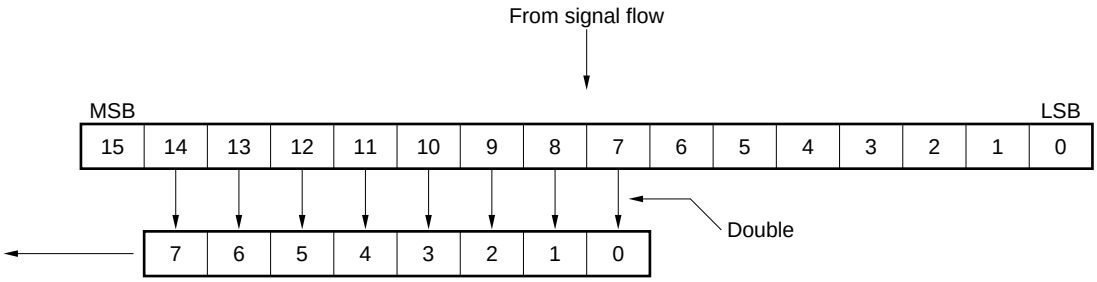
GON: Controls whether disturbance feed to the TE or FE filters is ON or OFF.

GST: Controls fetching of arithmetic result of filter for gain detection.

"1" Arithmetic result of filter for gain detection (G1O, G2O) is latched to G1 and G2 registers inside LSI (during which time SO pin outputs high level and is in BUSY state)

On data readout from the serial interface using the 14H command, the following one-bit shift processing toward the MSB is executed for G1 and G2 data read from the serial interface by means of the settings of T/3 and G/B bits.

Figure 3-1. Data Readout Block



The aim of one-bit shift processing toward the MSB is to improve the bit precision of values that are read. For filters such as the gain detection filter, which always output positive values, the sign bit has no meaning. By performing one-bit shift processing toward the MSB on values read from the serial interface in the μPD63711, the precision of a value that is read is improved by one bit from reading the LSB bit instead of the sign bit.

When reading sign output (positive and negative values) as in the case of balance detection, as a procedure for avoiding losing a sign due to one-bit shift processing toward the MSB, multiply (shift one bit to the right) a value less than 0.5 in the final output stage multiplier in advance. By doing so, the correct sign value is read.

(6) 15H command (Half-wave brake control)

MSB			Command				LSB
0	0	0	1	0	1	0	1
MSB			Parameter				LSB
BALSW	0	0	0	BKLMT	0	0	0

BKLMT	Half-Wave Brake Control
0	–
1	Half-wave brake OFF at or above approximately 1.4 ms

BALSW	TBAL or FBAL Detection Filter Internal SW
0	OFF
1	ON

[Functional description]

BKLMT: Controls half-wave brake circuit

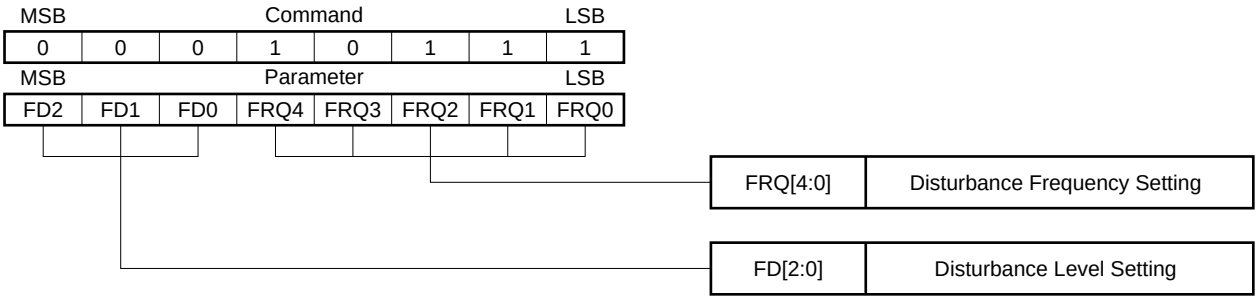
"1" Half-wave brake is OFF at or above approximately 1.4 ms

BALSW: Controls addition/subtraction switch inside tracking or focus balance detection filter.

"0" OFF

"1" ON

(7) 17H command (Disturbance frequency and level setting)



[Functional description]

FRQ[4:0]: Sets the disturbance frequency (5-bit absolute value).
FD[2:0]: Sets the disturbance level (3-bit absolute value).

The disturbance frequency and disturbance level are calculated using the following expressions.

Frequency $(F) = \frac{fs}{(FQ + 1) \times 4}$

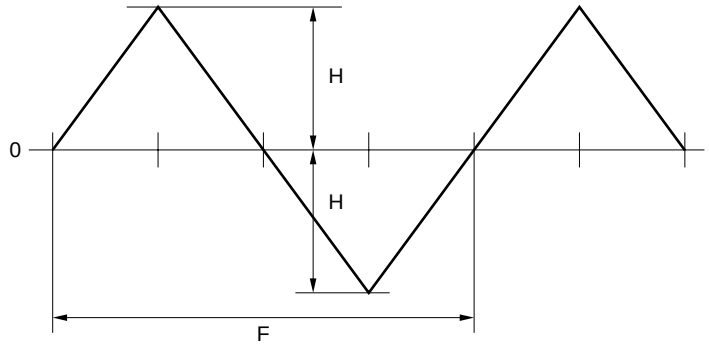
Level $(H) = FD \times (FQ + 1)$

fs: $\frac{176.4\ kHz}{2} = 88.2\ kHz$

FQ: Value set in FRQ[4:0]

FD: Value set in FD[2:0]

Caution Set FD to the greatest value that satisfies H ≤ 127.



Example When 17H register = B5H

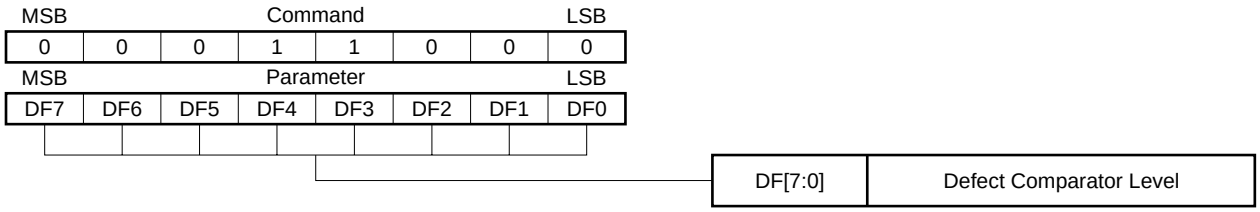
B5H = 10110101B → FD = 101B, FQ = 10101B

Since FQ = 21, $F = \frac{88.2\ kHz}{(21 + 1) \times 4} \fallingdotseq 1.0\ kHz$

Since FD = 5, $H = 5 \times (21 + 1) = 110 = 6EH$

17H register = D5H is not possible because FD = 6, $H = 6 \times (21+1) = 132$, and H then exceeds 127.

(8) 18H command (Defect comparator level setting)



[Functional description]

DF[7:0] : Set the defect signal comparator level.

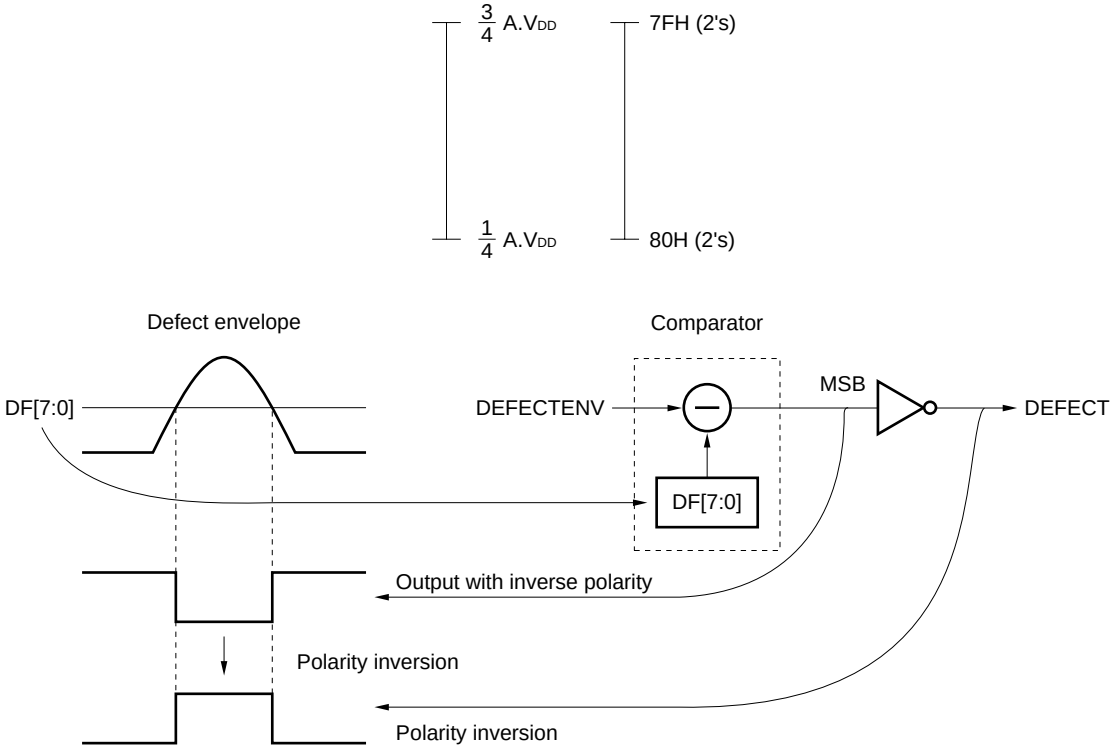
The range of $\frac{1}{2}$A.$V_{DD} \pm \frac{1}{4}$ A.V_{DD} can be set in 256 8-bit levels.

The setting value becomes the comparison threshold value.

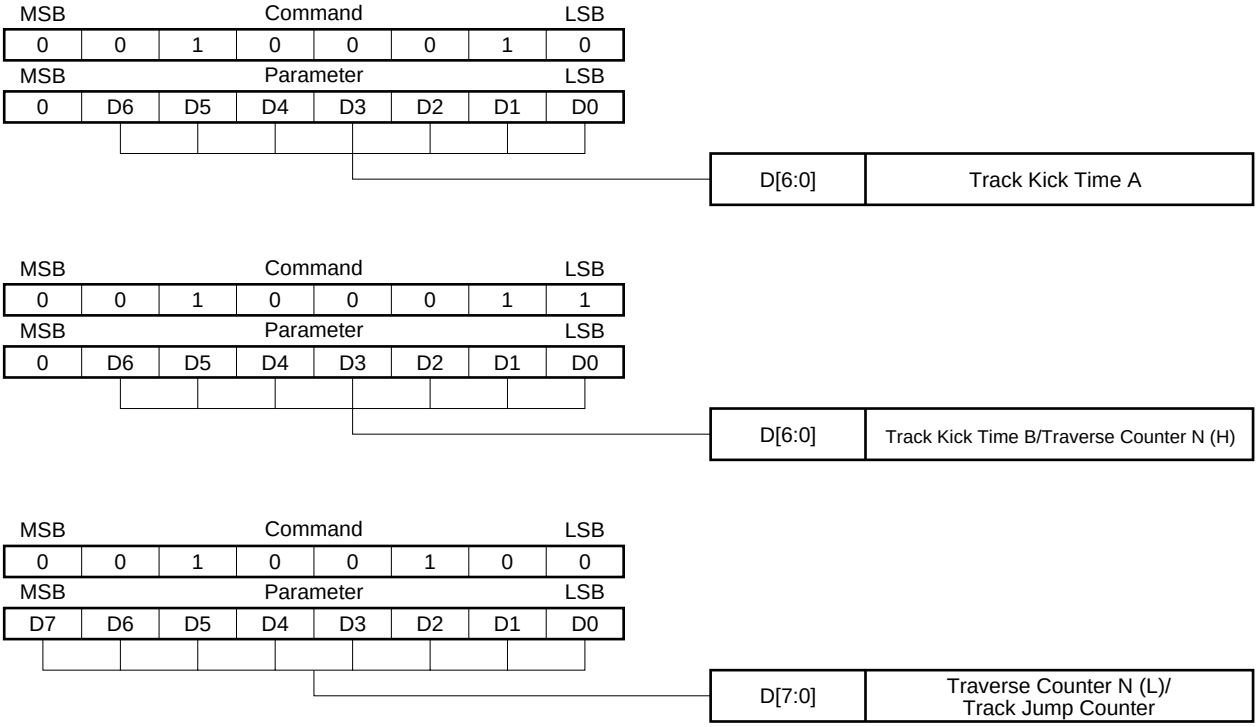
The comparison result has the inverse polarity of the input (because the MSB after subtracting is used).

Output is inverted (because the signal after comparator output handled as a signal absence detection by DEFECT = H).

The relationship between comparator level setting values and defect envelope signal voltages is shown below.



(9) 22H, 23H, and 24H commands (Track jump control)



[Functional description]

- **Track jump**

22H: The kick time setting

7 bits wide. Always set the MSB to 0.

The kick time is calculated using the following expression.

$$\text{Kick time} = \frac{(\text{Setting value} + 1) \times 1}{\text{fs}} \quad (\text{fs} = \frac{176.4\ \text{kHz}}{2} = 88.2\ \text{kHz})$$

23H: Brake time setting

7 bits wide. Always set the MSB to 0.

The brake time is calculated using the following expression.

$$\text{Brake time} = \frac{(\text{Setting value} + 1) \times 1}{\text{fs}} \quad (\text{fs} = \frac{176.4\ \text{kHz}}{2} = 88.2\ \text{kHz})$$

24H: Track counter setting

7 bits wide. Always set the MSB to 0.

The value set in 24H is used as a counter value.

- **Traverse count**

23H: Traverse counter setting (higher 7 bits, always set MSB to 0)

24H: Traverse counter setting (lower 8 bits)

The values set in 23H and 24H (15 bits wide) are used as counter values.

23H and 24H are used both when track jumping and when counting traverses, and are switched according to the setting of the T·CNT bit of the 10H command.

3.2 RF System Commands

Table 3-3. Functions of RF System Commands

Command	Function	Reference
30H	AGC amplifier gain setting, RF amplifier offset setting	p.31
31H	3T component detection gain setting, 3T detection circuit LPF setting, TE amplifier gain setting	p.32
32H	FE, RF, and TE amplifier gain settings	p.33
33H	TE amplifier balance setting	p.34
34H	MIRR detection block peak and bottom time constant settings, TE2 signal gain setting	p.35
35H	3T component extraction from RF signal timing setting	p.37
36H	EFM output block buffer setting, RF amplifier external load resistor setting	p.38
37H	Setting of output to ATEST pin, FE and TE amplifier load resistors setting	p.39
39H	Playback speed setting, EQ speed selection (×1 or ×2), APC amplifier polarity selection, Current input type setting	p.40

Table 3-4. List of RF System Commands

Command (Command Code)	Parameter (Data)							
	MSB	6	5	4	3	2	1	LSB
30H	DRF3	DRF2	DRF1	DRF0	GA3	GA2	GA1	GA0
31H	GTU1	GTU0	F31	F30	GF5	G32	G31	G30
32H	GT2	GT1	GT0	GF4	GF3	GF2	GF1	GF0
33H	TB6	TB5	TB4	TB3	TB2	TB1	TB0	IVS2
34H	TM3	TM2	TM1	GTEC	SOST	TM5	TM4	TMC
35H	0	3TS6	3TS5	3TS4	3TS3	3TS2	3TS1	3TS0
36H	DEQO	GR2	GR1	GR0	SEQ	0	0	EFMO
37H	TFO	TTO	0	0	0	TS3	TSD	TSM
39H	LDS	0	IVS	SW2	APN	0	0	CV2

Caution Do not send an undefined command.

(1) 30H command (Settings of AGC amplifier gain and RF amplifier offset)

MSB			Command				LSB
0	0	1	1	0	0	0	0
MSB			Parameter				LSB
DRF3	DRF2	DRF1	DRF0	GA3	GA2	GA1	GA0

GA3	GA2	GA1	GA0	AGC Amplifier Gain
1	0	0	0	–5.0 dB
1	0	0	1	–4.0 dB
1	0	1	0	–3.0 dB
1	0	1	1	–2.1 dB
1	1	0	0	–1.5 dB
1	1	0	1	–1.0 dB
1	1	1	0	–0.4 dB
1	1	1	1	+0.2 dB
0	0	0	0	* +1.0 dB
0	0	0	1	+1.7 dB
0	0	1	0	+2.4 dB
0	0	1	1	+3.1 dB
0	1	0	0	+4.2 dB
0	1	0	1	+5.3 dB
0	1	1	0	+6.4 dB
0	1	1	1	+7.5 dB

DRF3	DRF2	DRF1	DRF0	RF Amplifier Output DC Voltage[Note]
1	1	0	0	2.25 V
1	0	0	0	2.00 V
0	1	0	0	1.75 V
0	0	0	0	* 1.50 V
0	0	1	0	1.25 V
0	0	0	1	1.00 V
0	0	1	1	0.75 V

Note Values shown here are standard values, not rated values.

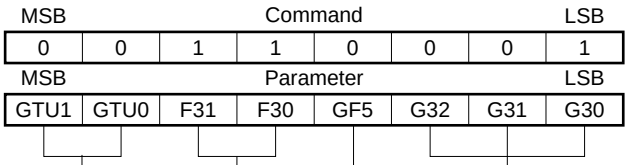
Remark The mark * indicates the contents set after a reset.

[Functional description]

GA[3:0]: Used in setting the AGC amplifier gain.
Perform gain setting while monitoring the MIRR signal's (peak) - (bottom) signal. The 37H command can be used to output the value of a MIRR signal from the ATEST pin before A/D conversion. In addition, in order to monitor amplitude stably, make adjustments by using the 34H command to maximize the time constant.

DRF[3:0]: Used in setting the RF amplifier output DC voltage.
Can be cancelled using DEQO in the 36H command.

(2) 31H command (Settings of 3T component detection gain, 3T detection circuit LPF, and TE amplifier gain)



G32	G31	G30	3T Detection Circuit Gain
1	0	1	+8.0 dB
1	1	0	+14.0 dB
1	1	1	+16.5 dB
0	0	0	* +20.0 dB
0	0	1	+23.5 dB
0	1	0	+26.0 dB
0	1	1	+28.0 dB

GF5	GF4	FE Amplifier Gain Adjustment
1	1	+2.5 dB
1	0	–2.0 dB
0	1	+6.0 dB
0	0	* 0 dB

F31	F30	3T Circuit LPF after S/H
1	0	fc = 50 kHz
0	0	* fc = 100 kHz
0	1	fc = 200 kHz

GTU1	GTU0	TE Amplifier Gain Adjustment
0	0	* +14 dB (On gain TYP setting of 32H command)
0	1	+6 dB up
1	0	+12 dB up

Remark The mark * indicates the contents set after a reset.

[Functional description]

G3[2:0]: Used in setting the 3T detection circuit sensitivity.
When disturbance is injected into the FE system, an amplitude of approximately 2.0 V_{p-p} is obtained in the default state when the RF signal fluctuates 20%.

F3[1:0]: The LPF for eliminating noise after S/H in the 3T detection circuit.
Since S/H samples using an EFM high frequency signal, LPF is set for stability.

GF5: Adjusts the FE amplifier gain.
Changes the input resistor value of the FE amplifier second stage.
Used with the GF4 bit of the 32H command.

GTU[1:0]: Used to raise the TE amplifier gain.
Switches the gain by changing the input resistor value. Note that GTU0 and GTU1 cannot be used together.

(3) 32H command (FE, RF, and TE amplifier gain settings)

MSB			Command				LSB
0	0	1	1	0	0	1	0
MSB			Parameter				LSB
GT2	GT1	GT0	GF4	GF3	GF2	GF1	GF0

GF2	GF1	GF0	FE/RF Amplifier Gain
0	1	0	+22.0 dB/+28.0 dB
1	1	0	+19.0 dB/+25.0 dB
0	0	0	* +16.0 dB/+22.0 dB
1	0	1	+13.0 dB/+19.0 dB
0	0	1	+10.0 dB/+16.0 dB

GF3	FE/RF Amplifier Gain Adjustment
1	+6 dB up
0	* +16 dB/+22 dB (On gain TYP setting with GF[2:0])

GF4	FE Amplifier Gain Adjustment
	Refer to GF5 bit of 31H command

GT2	GT1	GT0	TE Amplifier Gain
1	0	1	+8.0 dB
1	1	0	+10.5 dB
1	1	1	+12.5 dB
0	0	0	* +14.0 dB
0	0	1	+15.5 dB
0	1	0	+17.5 dB
0	1	1	+20.0 dB

Remark The mark * indicates the contents set after a reset.

[Functional description]

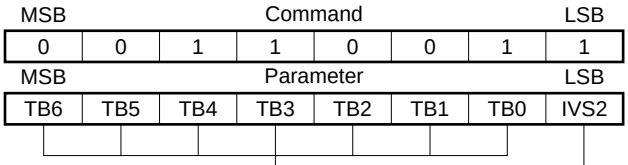
GF[2:0]: Sets the FE amplifier and RF amplifier gain.
Raising/decreasing the gain can be performed in 6-dB units and can be set in variations of five stages.

GF3: Raises the FE amplifier and RF amplifier gain +6 dB.
Changes the resistor value of first-stage amplifier input.

GF4: Adjusts the FE amplifier gain.
Used with the GF5 bit of the 31H command.

GT[2:0]: Sets the TE amplifier gain.
Raising/decreasing the gain can be performed in 6-dB units and can be set in variations of seven stages.

(4) 33H command (TE amplifier balance setting)



IVS2	TE Amplifier Current Input Mode
1	Only E and F pins are in the current input mode
0	* All A to F pins are in the current input mode[Note]

Note Selected with IVS bit of 39H command.

TB[6:0]	E/F Gain[Note]
1000000	11.42 dB/16.50 dB
1000001	11.48 dB/16.47 dB
1000010	11.53 dB/16.44 dB
	~
1111111	13.96 dB/14.04 dB
0000000	* 14.00 dB/14.00 dB
0000001	14.04 dB/13.96 dB
	~
0111101	16.44 dB/11.53 dB
0111110	16.47 dB/11.48 dB
0111111	16.50 dB/11.42 dB

(128 divisions)

Note Values shown above are standard values, not rated values.

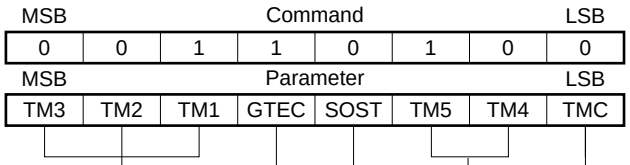
Remark The mark * indicates the contents set after a reset.

[Functional description]

IVS2: Sets E and F pins to the current input mode.
When using this mode, be sure to set the IVS bit of the 39H command to 1.

TB[6:0]: Prior stage to the TE amplifier. Sets the photo-detector E and F signal gains.
Switching is possible in 128 ways over an adjustment range of ±5 dB.

(5) 34H command (Settings of MIRR detection block peak and bottom time constants and TE2 signal gain)



TMC	MIRR/DEFECT Time Constants
1	Set to μPC2572 ratio
0	* Follow TM[3:1] settings

TM5	TM4	DEFECT Time Constant Ratio
1	0	Change the DEFECT time constant to 1/4
0	1	Change the DEFECT time constant to 1/2
0	0	* Follow TM[3:1] and TMC settings

SOST	FE Output Offset Control SW
1	Offset injection using CRAM 7CH
0	* No offset injection

GTEC	TE2 Signal Gain
1	+24.0 dB (TE × 3)
0	* +26.0 dB (TE × 4)

TM3	TM2	TM1	MIRR Peak/Bottom/DEFECT Bottom Time Constants
1	0	1	8 μs/V/40 μs/V/40 μs/V
1	1	0	10 μs/V/50 μs/V/50 μs/V
1	1	1	14 μs/V/70 μs/V/70 μs/V
0	0	0	* 20 μs/V/100 μs/V/100 μs/V
0	0	1	27 μs/V/140 μs/V/140 μs/V
0	1	0	40 μs/V/200 μs/V/200 μs/V
0	1	1	50 μs/V/250 μs/V/250 μs/V

Remark The mark * indicates the contents set after a reset.

[Functional description]

TMC: Changes MIRR/DEFECT time constants to the μPC2572 ratio.
Example MIRR peak/bottom/DEFECT bottom = 20 μs/V/400 μs/V/100 μs/V
(When TM[5:4] = [0:0], TMC = 1, TM[3:1] time constants is TYP)

TM[5:4]: Of the MIRR/DEFECT time constants set using TM[3:1], changes only the DEFECT detection time constant. Valid only when TMC is set to "1".
Example MIRR peak/bottom/DEFECT bottom = 20 μs/V/400 μs/V/50 μs/V
(When TM[5:4] = [0,1], TMC = 1, and TM[3:1] time constant is TYP)

SOST: Controls the offset level of the on-chip FE amplifier using CRAM 7CH.

GTEC: Used in setting the TE2 signal gain. This setting can be used to set the TE2 signal gain to 3 times or 4 times that of the TE signal.

TM[3:1]: Used in setting the MIRR/DEFECT circuit peak and bottom time constants.

MIRR signal generation.....A MIRR signal is generated by superimposing RF (peak) – (bottom) detection waveform on DC 1.5 V and comparing them to a fixed value after A/D conversion. Set an arbitrary comparator level in CRAM 5FH.

DEFECT signal generation .....A DEFECT signal is generated by superimposing RF bottom detection signals centered around DC 2.5 V and comparing them to a fixed value after A/D conversion. Set an arbitrary comparator level using the 18H command.

AGC amplifier adjustment .....AGC amplifier control can be adjusted using the MIRR signal generation filter after A/D conversion. To monitor RF amplitude (G1O) stably, adjust with the MIRR time constant (CRAM 5DH) in its the longest state.

The MIRR and DEFECT signals before A/D conversion can be monitored at the ATEST pin using the 37H command.

(6) 35H command (Setting of timing for 3T component extraction from RF signal)

MSB			Command				LSB
0	0	1	1	0	1	0	1

MSB			Parameter				LSB
0	3TS6	3TS5	3TS4	3TS3	3TS2	3TS1	3TS0

3TS2	3TS1	3TS0	3T Extraction Pulse Width
0	0	0	* 7.46 ns
0	0	1	14.9 ns (7.46 × 2)
0	1	0	22.4 ns (7.46 × 3)
0	1	1	29.8 ns (7.46 × 4)
1	0	0	37.3 ns (7.46 × 5)
1	0	1	44.8 ns (7.46 × 6)
1	1	0	52.2 ns (7.46 × 7)
1	1	1	59.7 ns (7.46 × 8)

3TS6	3TS5	3TS4	3TS3	3T Extraction Pulse Delay
0	0	0	0	* 29.8 ns
0	0	0	1	59.6 ns (29.8 × 2)
0	0	1	0	89.4 ns (29.8 × 3)
0	0	1	1	119.2 ns (29.8 × 4)
0	1	0	0	149.0 ns (29.8 × 5)
0	1	0	1	178.8 ns (29.8 × 6)
0	1	1	0	208.6 ns (29.8 × 7)
0	1	1	1	238.4 ns (29.8 × 8)
1	0	0	0	59.6 ns
1	0	0	1	119.2 ns (59.6 × 2)
1	0	1	0	178.8 ns (59.6 × 3)
1	0	1	1	238.4 ns (59.6 × 4)
1	1	0	0	298.0 ns (59.6 × 5)
1	1	0	1	357.6 ns (59.6 × 6)
1	1	1	0	417.2 ns (59.6 × 7)
1	1	1	1	476.8 ns (59.6 × 8)

Remark The mark * indicates the contents set after a reset.

[Functional description]

3TS[6:0]: Sets the timing for extracting 3T components from RF signals.
Note that if this value is not set accurately, 11T and not 3T detection sensitivity will be high.

(7) 36H command (Settings of EFM output block buffer and RF amplifier external load resistor)

MSB			Command				LSB
0	0	1	1	0	1	1	0
MSB			Parameter				LSB
DEQO	GR2	GR1	GR0	SEQ	0	0	EFMO

EFMO	EFM Output Buffer
1	Output buffer ON
0	* Output buffer OFF

SEQ	RF Output Load
1	External RF load
0	* On-chip RF load

GR2	GR1	GR0	RF Gain Fine Adjustment
1	0	1	+18.0 dB
1	1	0	+20.0 dB
0	0	0	* +22.0 dB (When FE/RF gain is TYP)
0	0	1	+24.0 dB
0	1	0	+26.0 dB

DEQO	RFEQ Output DC Offset Switching
1	2.5 V (Offset injection by external resistor)
0	* RFEQ output 1.5 V

Remark The mark * indicates the contents set after a reset.

[Functional description]

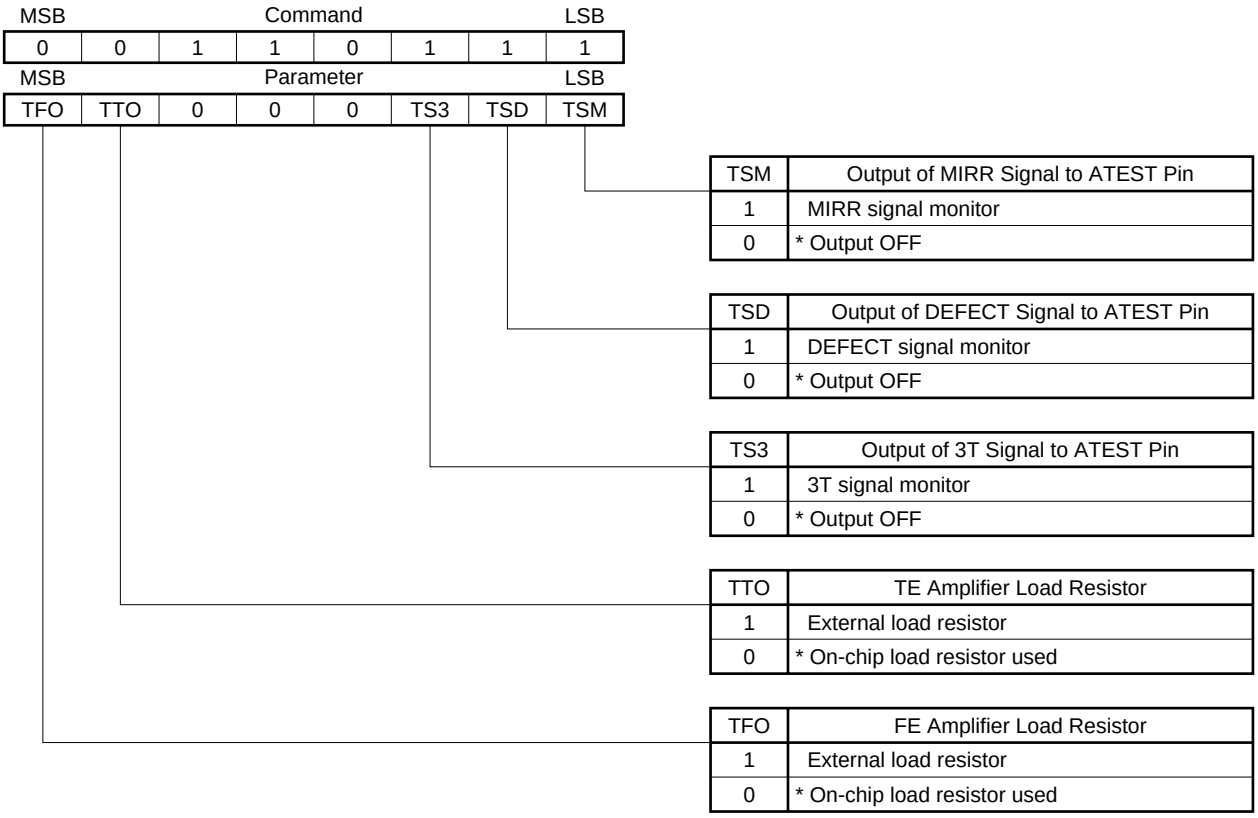
EFMO: Sets EFM comparator output buffer ON or OFF.
Normally, chattering is avoided by using a 2-kΩ resistor on output.

SEQ: Used when there is an externally attached RF amplifier load.

GR[2:0]: Used in fine tuning of RF gain when an RF amplifier load is externally attached.
Performed by dividing the variation of ±4 dB into five stages.

DEQO: Switches the RF amplifier output voltage.
When an RFEQ load resistor is externally attached, by setting this register to 2.5 V, the offset can be adjusted using the external resistor.

(8) 37H command (Settings of output to ATEST pin and FE and TE amplifier load resistors)



TSM	Output of MIRR Signal to ATEST Pin
1	MIRR signal monitor
0	* Output OFF

TSD	Output of DEFECT Signal to ATEST Pin
1	DEFECT signal monitor
0	* Output OFF

TS3	Output of 3T Signal to ATEST Pin
1	3T signal monitor
0	* Output OFF

TTO	TE Amplifier Load Resistor
1	External load resistor
0	* On-chip load resistor used

TFO	FE Amplifier Load Resistor
1	External load resistor
0	* On-chip load resistor used

Remark The mark * indicates the contents set after a reset.

[Functional description]

TSM: When TSM = 1, the MIRR signal is output from the ATEST pin.

TSD: When TSD = 1, the DEFECT signal is output from the ATEST pin.

TS3: When TS3 = 1, the 3T signal is output from the ATEST pin.

TTO: Selects whether the TE amplifier load resistor is on-chip or external.
The TE amplifier on-chip load resistor is 80 kΩ when a current input type is selected, and 160 kΩ when a voltage input type is selected.

TFO: Selects whether the FE amplifier load resistor is on-chip or external.
The FE amplifier on-chip load resistor is 80 kΩ.

Cautions 1. The ATEST pin is for monitoring. Since its output drivability is not high, use it only for monitoring and normally leave it open. At the present stage, operation of the ATEST pin is not guaranteed.

2. Do not set two or more of the bits TSM, TSD, and TS3 to 1 at one time. Be sure to set only one of the bits to 1.

(9) 39H command (Settings of playback speed, EQ speed, APC amplifier polarity, and current input type)

MSB			Command				LSB
0	0	1	1	1	0	0	1
MSB			**Parameter**				**LSB**
LDS	0	IVS	SW2	APN	0	0	CV2

CV2	Double-Speed Setting
1	Set double-speed
0	* Set single-speed

APN	APC Circuit N-Sub or P-Sub Selection
1	* APC circuit, N-Sub supported
0	APC circuit, P-Sub supported

SW2	RFEQ Single or Double SW Selection
1	Use circuit on pin 79 EQ1 side
0	* Use circuit on pin 78 EQ2 side

IVS	Selection of Signal Input Method from Pickup
1	Current input type
0	* Voltage input type

LDS	APC Circuit ON or OFF Selection
1	APC circuit operation (LD control current output)
0	* Stop APC circuit operation (LD control current output stopped)

Remark The mark * indicates the contents set after a reset.

[Functional description]

CV2: Selects the playback speed (double-speed).
APN: Selects whether the APC circuit supports N-Sub or P-Sub.
SW2: Selects the RFEQ circuit to use.
IVS: Set the appropriate value for the form of input from the pickup.
LDS: Selects whether the APC circuit (LD drive current controller) is ON or OFF.

3.3 Signal Processing System Commands

Table 3-5. Functions of Signal Processing System Commands

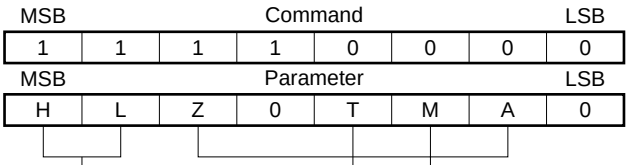
Command	Function	Reference
F0H	ON or OFF selection for muting and attenuation, ON or OFF selection for interpolate processing of uncorrectable data medium values, setting of number of interpolated frames for synchronization guard	p.43
F1H	CLV servo control	p.44
F2H	Readout-start Q code address specification, peak level data readout	p.45
F5H	Q code consecutive readout	p.47
F6H	LRCK pin polarity switching EMPH pin polarity switching	p.49
F7H	Attenuation ON or OFF	p.50
F8H	NOP (no target)	p.50
FAH	Attenuation amount setting (L-ch)	p.51
FBH	Attenuation amount setting (R-ch)	p.51
FCH	Error correcting capability selection, ON or OFF selection for subcode synchronization guard, forcible muting selection, bilingual mode selection, ON or OFF selection for digital out	p.52
FDH	C bit setting	p.53
FEH	Digital attenuation amount setting	p.53

Table 3-6. List of Signal Processing System Commands

Command (Command Code)	Parameter (Data)							
	MSB	6	5	4	3	2	1	LSB
F0H	H	L	Z	0	T	M	A	0
F1H	D	I	0	G	T	D2	D1	D0
F2H	PR	0	0	0	A3	A2	A1	A0
F5H	None							
F6H	0	0	0	0	PSEL	0	LP	EP
F7H	PWM	0	0	0	WD2	WD1	MON	AT2
F8H	None							
FAH	L7	L6	L5	L4	L3	L2	L1	L0
FBH	R7	R6	R5	R4	R3	R2	R1	R0
FCH	TX	BR	BL	T1	T0	S	E1	E0
FDH	S3	S2	S1	S0	0	0	C1	C0
FEH	0	0	0	0	0	0	A1	A0

Caution Do not send an undefined command.

(1) F0H command (EFM signal input and audio/CD-ROM data output related parameter setting)



Z	M	A	Sound Output
0	0	0	Muting OFF
0	0	1	Attenuation 1 ON
0	1	0	* Muting ON
0	1	1	Setting prohibited
1	0	0	Zero-cross muting OFF
1	0	1	Setting prohibited
1	1	0	Zero-cross muting ON
1	1	1	Setting prohibited

T	Interpolate Processing of Uncorrectable Data Medium Values
0	* Yes (CD mode)
1	No (CD-ROM mode)

H	L	Synchronization Guard
0	0	2-frame interpolation
0	1	* 4-frame interpolation
1	0	8-frame interpolation
1	1	16-frame interpolation

Remark The mark * indicates the contents set after a reset.

[Functional description]

Z, M, A: Selects ON or OFF for muting and attenuation.

T: Selects CD mode or CD-ROM mode.

"0" CD mode

When an uncorrectable error is detected in the upper or lower 8 bits of audio data (16 bits), it is output after performing interpolation. High level is output from the FLAG pin at the same time.

"1" CD-ROM mode

Even if an uncorrectable error is detected in the upper or lower 8 bits of CD-ROM data (16 bits), it is output without performing interpolation. However, the FLAG pin outputs whether an error was detected in either the upper or the lower 8 bits. This makes highly accurate erasure correction possible in a CD-ROM system connected to the μPD63711.

H, L: Interpolates the signal based on 588 counter when the frame synchronization signal is not in the window. This specifies the number of frames.

(2) F1H command (CLV servo control)

MSB			Command				LSB
1	1	1	1	0	0	0	1
MSB			Parameter				LSB
D	I	0	G	T	D2	D1	D0

D2	D1	D0	Control State
0	0	0	* Stop
0	0	1	Kick
0	1	0	Brake
0	1	1	Setting prohibited
1	0	0	Lead-in servo
1	0	1	Rough servo
1	1	0	Steady servo
1	1	1	Adaptive servo

T	Peak Hold Period
0	* RFCK/2
1	RFCK/4

G	Lead-in Servo Gain
0	–12 dB
1	* 0 dB

I	Bottom Hold Period
0	* RFCK/16
1	RFCK/32

D	Steady Servo Phase Comparison
0	* RFCK/4 and WFCK/4
1	RFCK/8 and WFCK/8

Remark The mark * indicates the contents set after a reset.

[Functional description]

D[2:0]: Controls the CLV servo.

T: Selects whether to make the peak hold period of the lead-in servo RFCK/2 or RFCK/4.

G: Selects whether to make the gain of the lead-in servo –12 dB or 0 dB.

I: Selects whether to make the bottom hold period of the lead-in servo RFCK/16 or RFCK/32.

D: Selects whether to make the phase comparison signals of the steady servo RFCK/4 and WFCK/4 or RFCK/8 and WFCK/8.

(3) F2H command (Readout-start Q code address specification and peak level data readout)

MSB			Command				LSB
1	1	1	1	0	0	1	0
MSB			Parameter				LSB
PR	0	0	0	A3	A2	A1	A0

A3	A2	A1	A0	Q Code Data
0	0	0	0	CONTROL, ADR
0	0	0	1	TNO
0	0	1	0	POINT or X
0	0	1	1	MIN
0	1	0	0	SEC
0	1	0	1	FRAME
0	1	1	0	ZERO
0	1	1	1	PMIN or AMIN
1	0	0	0	PSEC or ASEC
1	0	0	1	PFRAME or AFRAME
1	0	1	0	* ECT
1	0	1	1	PKLU[Note]
1	1	0	0	PKLD[Note]
1	1	0	1	PKRU[Note]
1	1	1	0	PKRD[Note]

Note The CC flag must be checked when reading peak level data.

PR	Peak Register Clear
0	* –
1	Peak register clear

Remark The mark * indicates the contents set after a reset.

[Functional description]

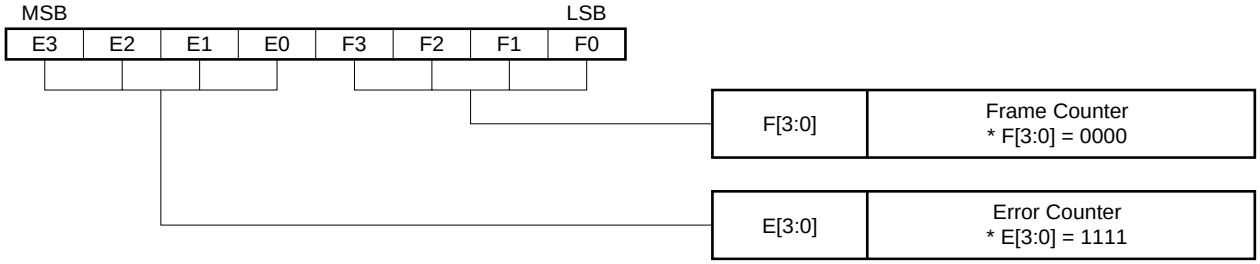
This command reads out the Q code data and peak level data indicated by parameters. Q code data consists of 8-bit units, and arbitrary data (80 bits excluding the CRC word) can be read by specifying a pointer address using parameters. The pointer addresses that can be specified using parameters are 00H through 0EH. Do not specify addresses other than these.

After data has been read out, the pointer address is incremented ($\rightarrow 0 \rightarrow 1 \rightarrow 2 \rightarrow$).

Q code data also can be read out using the F5H command. Refer to the F5H command for details of the reading method.

The Q code data that can be read out using this command and the F5H command is frame data for which CRC checking was OK. Therefore, CRC checking need not be performed on the microcontroller.

The contents of the internal register ECT of the LSI, which were read by AH parameter input following F2H command input, are described below. As shown below, the ECT register consists of an error counter in the upper 4 bits and a frame counter in the lower 4 bits.



Remark The mark * indicates the contents set after a reset.

[Functional description]

F[3:0]: Whenever the Q code is updated, the value of this counter is incremented (0 → 1 → ... → F → 0...). If a CRC error occurs, the Q code is not updated and the value of the counter does not change.

E[3:0]: This counter indicates the CRC error state. If a CRC error occurs, the counter value is incremented (with a limit of FH). If an error does not occur, the value of the counter is reset (0H).

Peak level data is described below.

PKLU: L channel peak level data (upper 8 bits)
PKLD: L channel peak level data (lower 8 bits)
PKRU: R channel peak level data (upper 8 bits)
PKRD: R channel peak level data (lower 8 bits)

The maximum value of both the L channel and R channel in the a subcode 1 frame can be read.
Data is output as 16 bits divided into 8 upper bits and 8 lower bits.
The CC flag must be checked when reading peak level data.

(4) F5H command (Q code consecutive readout (excluding peak level data))

MSB			Command				LSB
1	1	1	1	0	1	0	1

[Functional description]

Use this command to read out consecutive Q code data starting from the address specified in the F2H command (incrementing the pointer). Refer to the F2H command for the relationship between the address pointer and Q code data.

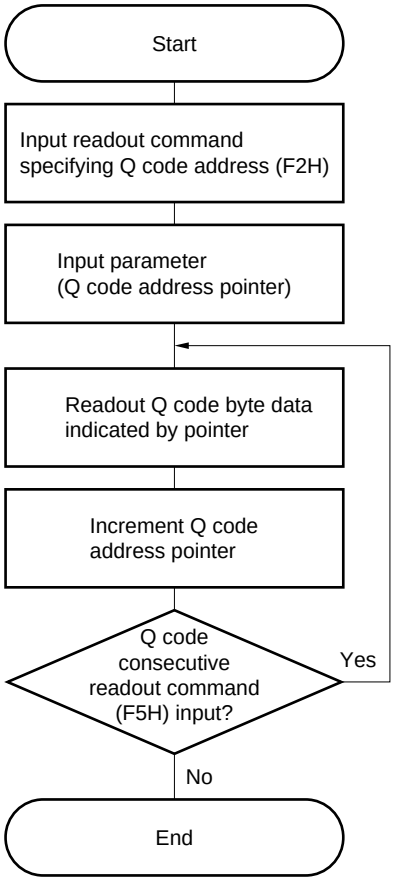
When a command other than the F2H, F5H, or F8H commands is input to the μPD63711, the address pointer is initialized (put in the same state as after a reset) automatically to AH (refer to the F2H command).

After reading data, the pointer address is incremented ($\rightarrow 9 \rightarrow A \rightarrow 0 \rightarrow 1 \rightarrow 2 \rightarrow ...$).

The basic reading method is described first. This actually is used in combination with the method of reading n bytes of Q code data (described later).

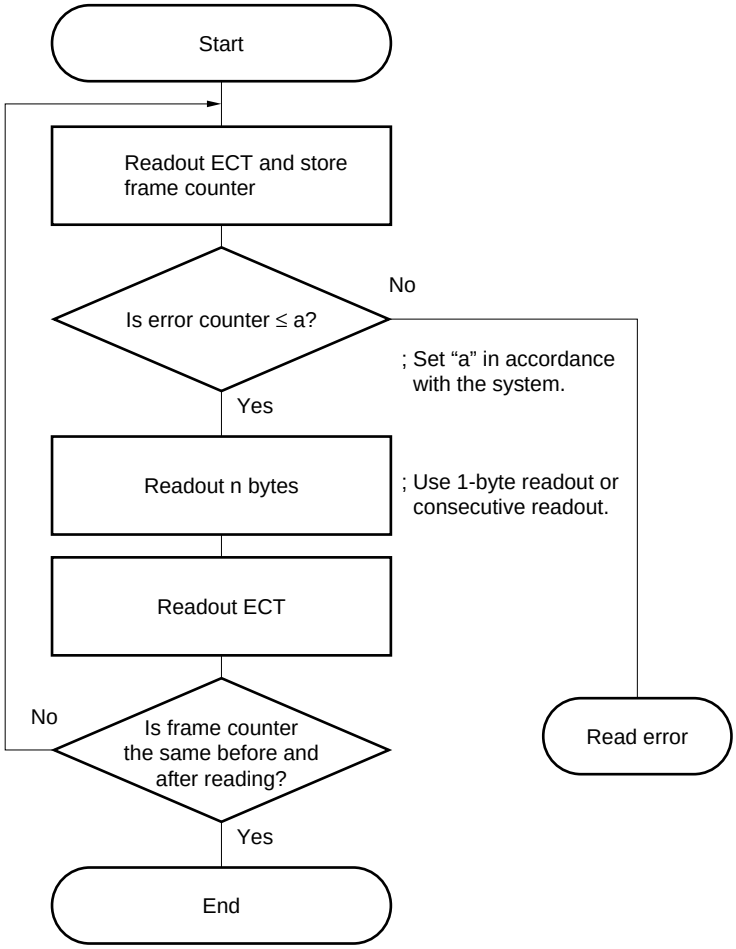
- To read out 1 byte of Q code data, use the F2H command.
- To read out multiple bytes of Q code data consecutively, read out according to the flowchart shown below.

Figure 3-2. Q Code Consecutive Readout Method



A flowchart for actually reading out n bytes of Q code data (read out n bytes starting from arbitrary position in a frame) is shown below.

Figure 3-3. Readout Method of n Bytes of Q Code Data



(5) F6H command (LRCK pin and EMPH pin polarity switching)

MSB			Command				LSB
1	1	1	1	0	1	1	0
MSB			Parameter				LSB
0	0	0	0	PSEL	0	LP	EP

EP	EMPH Pin Polarity
0	* Normal output
1	Inverted output

LP	LRCK Pin Polarity
0	* Normal output
1	Inverted output

PSEL	HOLD/MIRR Pin Output
1	WDCK/WFCK signal output
0	* Normal output (HOLD/MIRR output)

Remark The mark * indicates the contents set after a reset.

[Functional description]

EP: Selects whether EMPH pin output is normal or inverted.

LP: Selects whether LRCK pin output is normal or inverted.

PSEL: Controls WDCK/WFCK signal output from HOLD/MIRR pin.

Caution When using the on-chip D/A converter, be sure to set LP = EP = 0.

(6) F7H command (Sound output mode and sync window width setting)

MSB			Command				LSB
1	1	1	1	0	1	1	1

MSB			Parameter				LSB
PWM	0	0	0	WD2	WD1	MON	AT2

AT2	Attenuation (Set the Attenuation Value Independently for L and R)
0	* Attenuation OFF
1	Attenuation ON

MON	Audio Output Signal Switching
0	* Normal (stereo)
1	Monaural

WD2	WD1	Sync Window Block
0	0	* ±7 PLCK
0	1	±30 PLCK
1	0	±60 PLCK
1	1	±80 PLCK

PWM	Sound DAC PWM OFF
0	PWM ON
1	* PWM OFF

Remark The mark * indicates the contents set after a reset.

[Functional description]

AT2: Selects ON or OFF for attenuation. This is μPD63703 equivalent attenuation. Set the amount of L-ch and R-ch attenuation using the FAH and FBH commands, respectively.

MON: Selects stereo or monaural for the audio output signal.

WD[2:1]: Sets the width of the PLL synchronization detection window.

PWM: Selects ON or OFF for sound DAC PWM output.
In the default state (PWM OFF), PWM output (L+, L–, R+, R–) is fixed (+pin: H, –pin: L).

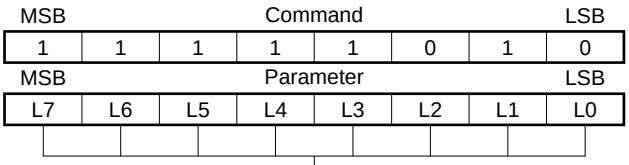
(7) F8H command (NOP command)

MSB			Command				LSB
1	1	1	1	1	0	0	0

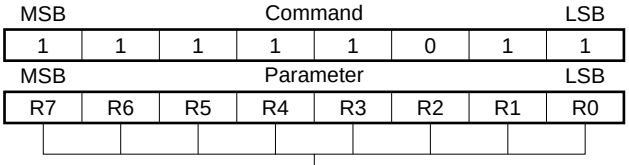
[Functional description]

This command has no object.

(8) FAH and FBH commands (L-ch and R-ch attenuation amount setting)



L[7:0]	L-ch Attenuation Amount
00000000	–∞
00000001	–48 dB
00000010	–42.1 dB
	~
11111111	–0.03 dB



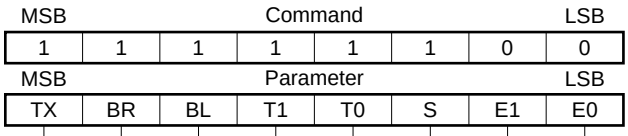
R[7:0]	R-ch Attenuation Amount
00000000	–∞
00000001	–48 dB
00000010	–42.1 dB
	~
11111111	–0.03 dB

[Functional description]

L[7:0]: Sets the L-ch attenuation amount.
R[7:0]: Sets the R-ch attenuation amount.

This is μPD63703 equivalent attenuation. As in the case of the μPD63703, this is undefined just after a reset. Therefore, after setting the attenuation amount using the FAH and FBH commands, execute attenuation with the F7H command.

(9) FCH command (Parameter setting)



E1	E0	Error Correction
0	0	* 2-symbol correction
1	0	2-symbol correction (If uncorrectable, set C2 flag)
0	1	Triple correction[Note]
1	1	Quadruple correction[Note]

Note Can be used only in CD-ROM mode.

S	Subcode Synchronization Guard
0	* OFF
1	ON

T1	T0	Forcible Muting Time
0	0	* Tn × 2
0	1	Tn × 4
1	0	Tn × 8
1	1	Tn × 16

Tn = 5 ms

BR	BL	Bilingual Mode
0	0	* Normal output
0	1	L channel
1	0	R channel
1	1	L and R reversed

TX	Digital Audio Interface
0	ON
1	* OFF

Remark The mark * indicates the contents set after a reset.

[Functional description]

E[1:0]: Selects the error correcting capability.
S: Selects ON or OFF for subcode synchronization guard.
T[1:0]: Selects the forcible muting time.
BR, BL: Selects the bilingual mode.
TX: Selects ON or OFF for digital audio interface data output.

(10) FDH command (C bit setting)

MSB							LSB
Command							
1	1	1	1	1	1	0	1
MSB							LSB
Parameter							
S3	S2	S1	S0	0	0	C1	C0

C1	C0	Clock Precision
0	0	* Standard mode Level II
0	1	Variable pitch mode Level III
1	0	High precision mode Level I
1	1	Setting prohibited

S3	S2	S1	S0	Source Number
0	0	0	0	Setting prohibited
1	0	0	0	* 1
0	1	0	0	2
1	1	0	0	3
				~
1	1	1	1	15

Remark The mark * indicates the contents set after a reset.

[Functional description]

C[1:0]: Sets the clock precision of the C bit of the digital audio interface.
S[3:0]: Sets the source number of the C bit of the digital audio interface.

This command is only used to output values set for digital audio interface output and is unrelated to other operations of the LSI.

(11) FEH command (Digital attenuation amount setting)

MSB							LSB
Command							
1	1	1	1	1	1	1	0
MSB							LSB
Parameter							
0	0	0	0	0	0	A1	A0

A1	A0	Attenuation Amount
0	0	–6 dB
0	1	* –12 dB
1	0	–18 dB
1	1	–24 dB

Remark The mark * indicates the contents set after a reset.

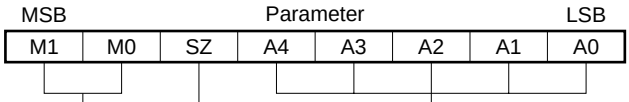
[Functional description]

A[1:0]: Sets the digital attenuation amount.

3.4 CD-TEXT Function

(1) Parameter format

Inputs the parameters at the TSI pin in the format shown below. Command input is not necessary.



A[4:0]	Readout Data Address

SZ	Readout Data Output Format Selection
0	6/8 conversion
1	None (output 6-bit data justified on the LSB side)

M1	M0	CD-TEXT Data Processing Method	MODE
0	0	Interleave autocheck decode mode	2
0	1	Specifies MODE = 4 (Lead in Area)	4
1	0	No interleave decoding	2
1	1	Interleave decoding command	2

Remark The mark * indicates the contents set after a reset.

[Functional description]

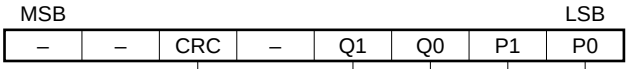
A[4:0]: Specifies the readout data address within Pack.
If SZ = 0, specify an address from 0H to 11H.
If SZ = 1, specify an address from 0H to 17H.
If A[4:0] = 18H, output correction results information.

SZ: Selects 6/8 conversion of readout data.
"0" There is 6/8 conversion.
"1" There is no 6/8 conversion.
Use SZ = 0 as needed to read a MODE = 2 (program area) data area. In other cases, use SZ = 1.

M[1:0]: Sets the decoding mode.
If M1 = 1, specify the interleave mode in the M0 bit.
"00" Determines the presence of interleaving in a program area using Item of 3 bits and performs automatic de-interleaving.
"01" Specifies MODE = 4 (Lead in Area). Only CRC checking is performed and not correction.
"10" No de-interleaving
"11" Has de-interleaving

(2) Correction result information

When A[4:0] = 18H, the following correction result information is output.



P1	P0	Error Correction State in MODE = 2
0	0	No errors
0	1	1 error
1	0	2 errors
1	1	Uncorrectable error

Q1	Q0	Error Correction State in MODE = 2
0	0	No errors
0	1	1 error
1	0	2 errors
1	1	Uncorrectable error

CRC	Result of CRC Checking in MODE = 4
0	CRC error
1	CRC OK

[Functional description]

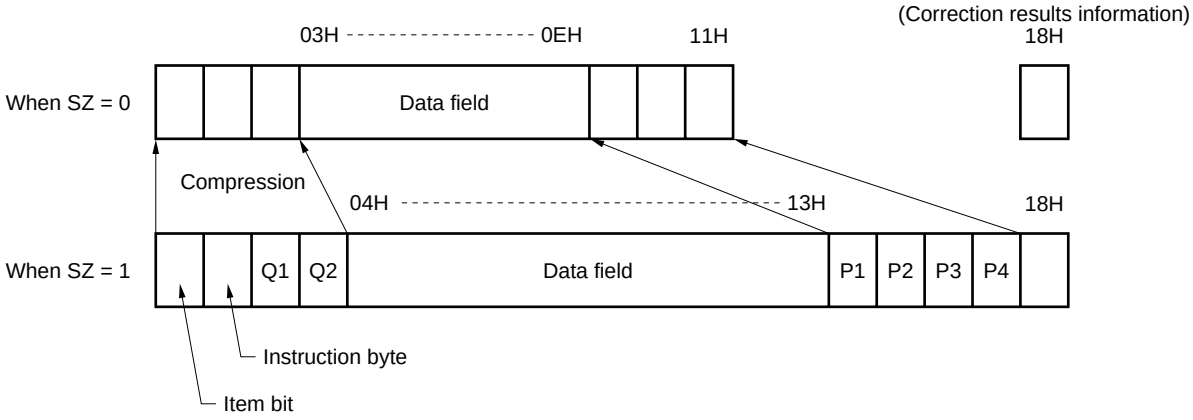
P[1:0]: Shows the P series error correction state for MODE = 2.

Q[1:0]: Shows the Q series error correction state for MODE = 2.

CRC: Shows the results of CRC checking for MODE = 4.
CRC = 1 means CRC checking was OK.

Refer to the CRC bit for MODE = 4 and the Q[1:0] and P[1:0] bits for MODE = 2 as needed.

Figure 3-4. Data Storage RAM Address Map Image (MODE = 2)

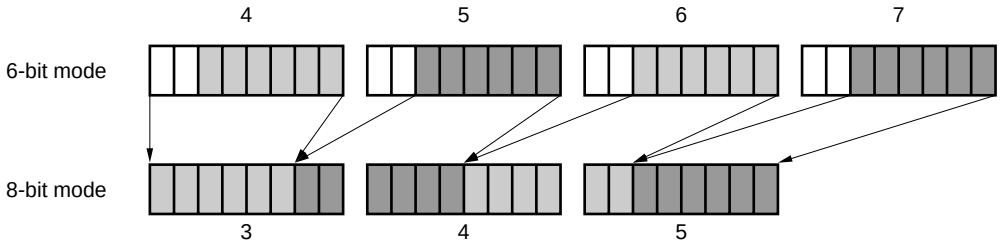


(3) 6/8 conversion

In MODE = 2 (Program Area), a constituent unit of data is 6 bits. If 8-bit mode is specified at this time, data output from the TSO pin is 6-bit data justified on the LSB side (the upper section of Figure 3-5).

If 6/8 conversion is specified, the 6-bit units of data are compressed and output (the lower section of Figure 3-5). Therefore, the time needed to read the data is shortened.

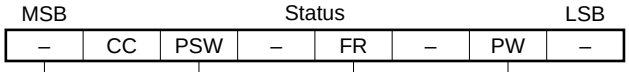
Figure 3-5. Data Compression in 6/8 Conversion



In 6/8 conversion based on SZ = 0, all data except 18H in the RAM is compressed. If you wish to read out the Item bit using a microcontroller and judge the possession of interleaving, specifying SZ = 1 is recommended.

3.5 Status

The status flags can be used to find out the internal state of the LSI.



PW	Detection of Maximum Interval between EFM Signal Transition Points
0	Maximum interval between EFM signal transition points < 188T
1	Maximum interval between EFM signal transition points ≥ 188T

T = bit rate = approximately 231.4 ns

FR	Synchronization Detection State
0	Asynchronized state
1	Synchronized state

PSW	Pick Inner Detection

CC	Command Execution State
0	Command execution finished
1	Command execution in progress

[Functional description]

PW: This is the maximum value of the inversion interval of the EFM signal detected during the RFCK period (peak hold) compared to 188T (approximately 43.5 μs). This flag is used to check whether or not rotation stopped when a brake was applied to the spindle for stopping the rotation of a disc. To avoid detection of errors due to defect (etc.), judge rotation to have stopped as long as PW = 1 multiple times in succession. Depending on the state of the EFM signal, PW may remain equal to 0 if the focus servo is out of position, so in addition to checking the PW flag, also check the focus servo state.

FR: In the EFM demodulation block, whether the output of the internal frame counter matches with the frame synchronization signal is sampled every WFCK/16 and a signal indicating a match or a non-match is output. If this signal indicates non-match 8 times in succession, this is regarded as an asynchronized state (FR = 0). At times other than this, it is regarded as a synchronized state (FR = 1).

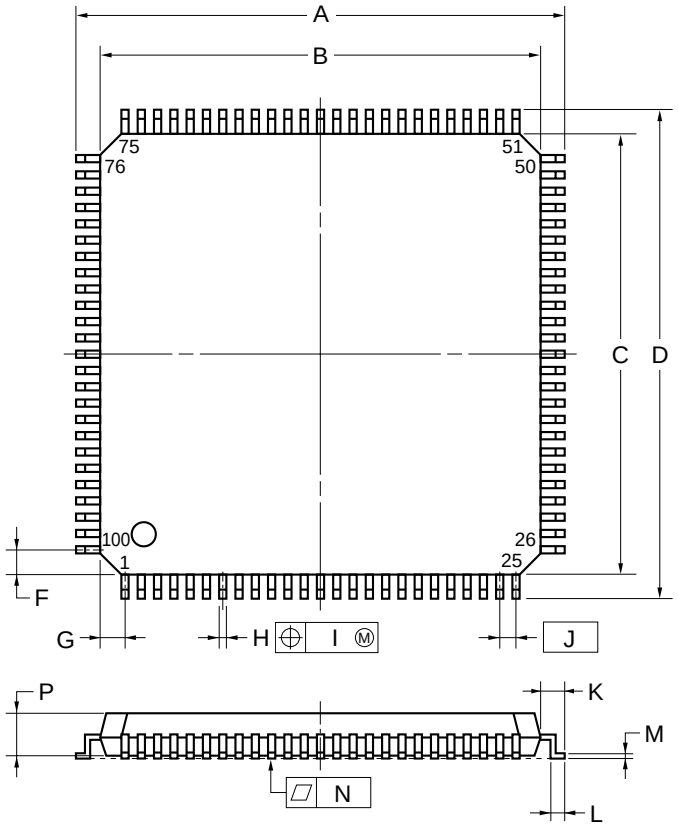
This flag is used to detect the mirror state of a disc and can be used in a sled servo or spindle servo guard. In addition, CLV adaptive servo mode switches the lead-in servo and normal servo according to this flag.

PSW: Outputs the state of the LIMIT pin (pin 39).

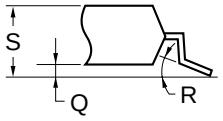
CC: When CC = 1, the processing of a command input from a microcontroller is being performed. The period in which CC = 1 is at most 12 μs (peak level data readout time).

4. PACKAGE DRAWING

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

5. RECOMMENDED SOLDERING CONDITIONS

The μPD63711 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 5-1. Surface Mounting Type Soldering Conditions

μPD63711GC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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