QUAD SPST BIFET ANALOG SWITCHES — SW-01/02, SW-03/04

(TEMPERATURE COMPENSATED R_{ON} AND DISABLE FUNCTION)

FEATURES

- **Low R_{ON} vs Temperature ..... 0.03%/°C**
- **Low Absolute R_{ON} 85Ω**
- **Low R_{ON} Variation vs Analog Signal 7%**
- **High Speed 300ns**
- **Low Leakage Current 0.2nA**
- **Overvoltage and Supply Loss Protected**
- **SW-01 is Improved Pin Compatible Device for DG201, ADG201, LF11201**
- **SW-02 is Improved Pin Compatible Device for DG202, LF11202, IH202**
- **SW-03 — Normally-Closed, with Disable. Functional Equivalent to LF11332.**
- **SW-04 — Normally-Open, with Disable. Functional Equivalent to LF11331.**

GENERAL DESCRIPTION

The SW-01 through SW-04 are four-channel single-pole, single-throw analog switches which offer operating characteristics unavailable in other JFET or CMOS devices. A unique circuit design provides a nearly constatn R_{ON} over the full operating temperature span. R_{ON} drift typically runs under 300ppm/°C.

The SW-01/02 are pin compatible with the DG201/202, while the SW-03/04 incorporate a chip disable pin which allows switch cascading for multiple switch systems. An Ion Implanted FET switch inherently exhibits low R_{ON} variations vs analog input signals. The junction FET construction also reduces static discharge destruction prevalent in CMOS devices.

Low R_{ON} sensitivity to temperature and voltage is complemented by guaranteed high-speed operation and low-leakage currents. Logic inputs may operate directly from either CMOS or TTL logic levels and are supply voltage independent. The SW-01 through SW-04 are protected during supply voltage power loss and against input signal overvoltages.

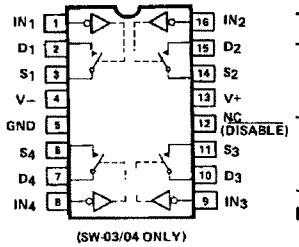
ORDERING INFORMATION†

FUNCTION	16-PIN HERMETIC DUAL-IN-LINE PACKAGE	
	MILITARY*	INDUSTRIAL
N.C.	SW01BQ	SW01FQ
N.C. (Disable)	SW03BQ	SW03FQ
N.O.	SW02BQ	SW02FQ
N.O. (Disable)	SW04BQ	SW04FQ

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS



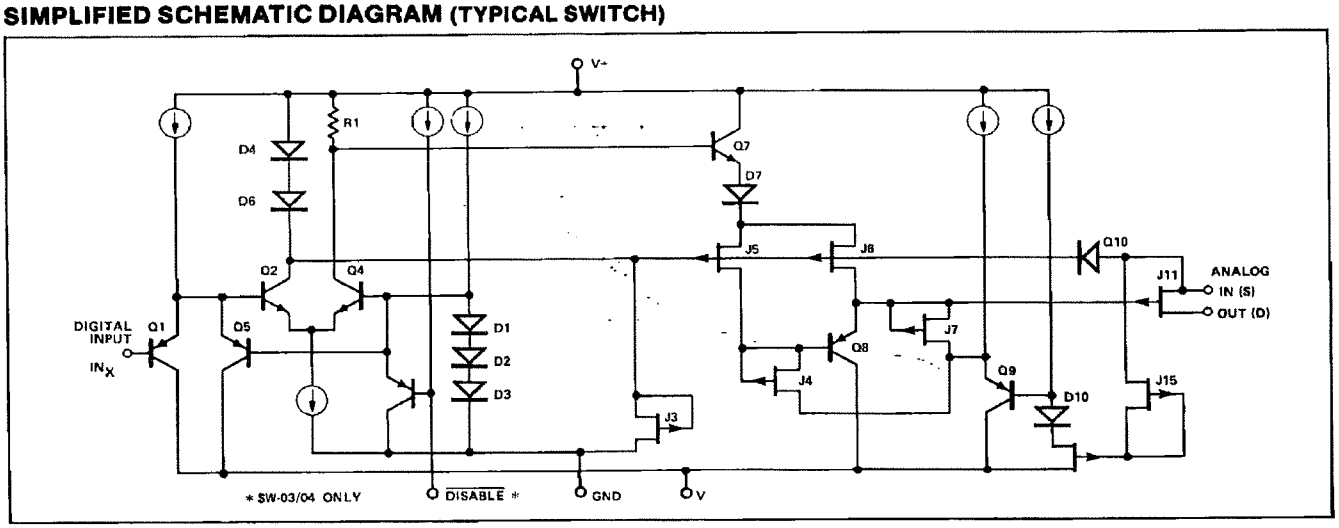
(SW-03/04 ONLY)

16-PIN DUAL-IN-LINE PACKAGE (Q-Package)

CONTROL LOGIC					
LOGIC		SWITCH STATE			
$\overline{DIS}$	IN_y	SW 01	SW 02	SW 03	SW 04
0	X	NA	NA	OFF	OFF
1	0	ON	OFF	ON	OFF
1	1	OFF	ON	OFF	ON

NOTES: $\overline{DIS}$ = DISABLE 1-4
INy = INPUT 1-4
X = DON'T CARE
NA = NOT APPLICABLE

SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted).

Operating Temperature Range
- SW-01-04BQ ..... −55°C to +125°C
- SW-01-04FQ ..... −25°C to +85°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Q-Package) 900mW
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
V+ Supply to Ground 36V

Logic Input Voltage ..... (V− or −4V) to V+ Supply
Analog Input Voltage
- Continuous ..... V− Supply −25V to V+ Supply +25V
- For V+ = V− = 0 ..... ±15V

Maximum Current Through Any Pin 30mA
Peak Current,
(Pulsed at 1ms, 10% Duty Cycle) 70mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04B MIN	SW-01-04B TYP	SW-01-04B MAX	SW-01-04F MIN	SW-01-04F TYP	SW-01-04F MAX	UNITS
"ON" Resistance	R_{ON}	−10V ≤ V_A ≤ 10V, I_D ≤ 1mA	—	85	100	—	85	120	Ω
R_{ON} Match		(Note 1)	—	4	10	—	4	10	%
Analog Voltage Range	V_A	R_L ≥ 2kΩ	+10	+11	—	+10	+11	—	V
		Full Temperature Range	−10	−15	—	−10	−15	—	
ΔR_{ON} vs V_A	ΔR_{ON}	V_A ≤ 10V, I_D ≤ 1mA	—	7	10	—	7	10	%
Analog Current Range	I_A	V_A ≤ 10V	—	5	—	—	5	—	mA
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = −10V	—	0.2	1	—	0.2	2	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V	—	0.2	1	—	0.2	2	nA
Leakage Current in "ON" Condition	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = ±10V, (Note 2)	—	—	1	—	—	2	nA
"OFF" Isolation	ISO_{OFF}	Test Figure 2	—	58	—	—	58	—	dB
Crosstalk	C_T	Test Figure 3	—	70	—	—	70	—	dB
Turn-On-Time	T_{ON}	Test Figure, (Note 3)	—	300	400	—	300	400	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	200	300	—	200	300	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Notes 3, 7)	—	100	—	—	100	—	ns
Source Capacitance	$C_{S(OFF)}$	V_A ≤ 10V	—	7	—	—	7	—	pF
Drain Capacitance	$C_{D(OFF)}$	V_A ≤ 10V	—	5.5	—	—	5.5	—	pF
Logic "1" Input Voltage	V_{INH}	Full Temperature Range	2	—	—	2	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	2 ≤ V_{IN} ≤ 15V, (Note 3)	—	1	3	—	1	3	μA
Logical "0" Input Current	I_{INL}	0 ≤ V_{IN} ≤ 0.8V	—	1	3	—	1	3	μA
Positive Supply Current	I+	(Note 5)	—	6.3	8.0	—	6.3	9.0	mA
Negative Supply Current	I−	(Note 5)	—	3.2	4.5	—	3.2	5.5	mA
Ground Current	I_G	(Note 5)	—	3.0	4.0	—	3.0	4.5	mA

NOTES:

1. V_A = 0V, I_D = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3}\,R_{ON4}}{4}$$

2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
3. Guaranteed by design.
4. Parameter tested at T_A = 125°C for military temperature range device.
5. Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
6. $TC_R = \frac{R_{ON}@T_H - R_{ON}@25°C}{R_{ON}@25°C \times (T_H - 25°C)} \times 100$; where T_H = 125°C for B grade, T_H = 85°C for F grade
7. Switching is guaranteed to be break-before-make.

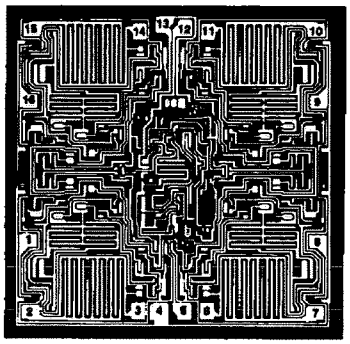
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $-55°C \le T_A \le +125°C$ for SW-01-04B and $-25°C \le T_A \le 85°C$ for SW-01-04F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04B MIN	SW-01-04B TYP	SW-01-04B MAX	SW-01-04F MIN	SW-01-04F TYP	SW-01-04F MAX	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_D \le 1mA$	—	—	120	—	—	140	Ω
R_{ON} Match		(Note 1)	—	10	15	—	10	15	%
R_{ON} Temperature Coefficient — Average	TC_R	$V_A = 0V$, $I_D = 100\mu A$, (Notes 3, 6)	—	0.03	0.20	—	0.03	0.15	%/°C
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 4)	—	—	10	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 4)	—	—	10	—	—	10	nA
Leakage Current in "ON" Condition	$I_{D(ON)}$+ $I_{S(ON)}$	$V_S = \pm 10V$, (Notes 2, 4)	—	—	10	—	—	10	nA
Turn-On-Time	T_{ON}	Test Figure 1, (Note 3)	—	500	600	—	500	600	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	400	500	—	400	500	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Notes 3, 7)	—	100	—	—	100	—	ns
Logical "1" Input Current	I_{INH}	$2 \le V_{IN} \le 15V$, (Note 3)	—	1	5	—	1	5	μA
Logical "0" Input Current	I_{INL}	$0 \le V_{IN} \le 0.8V$	—	—	5	—	—	5	μA
Positive Supply Current	I+	(Note 5)	—	—	11	—	—	12	mA
Negative Supply Current	I−	(Note 5)	—	—	6	—	—	7	mA
Ground Current	I_G	(Note 5)	—	—	5	—	—	6	mA

NOTES:

1. $V_A = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} R_{ON4}}{4}$$
2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
3. Guaranteed by design.
4. Parameter tested at $T_A = 125°C$ for military temperature range device.
5. Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
6. $TC_R = \frac{R_{ON}@T_H - R_{ON}@25°C}{R_{ON}@25°C \times (T_H - 25°C)} \times 100$; where $T_H = 125°C$ for B grade, $T_H = 85°C$ for F grade
7. Switching is guaranteed to be break-before-make.

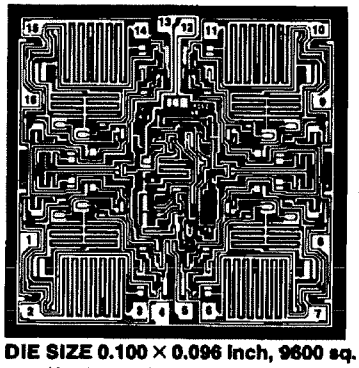
DICE CHARACTERISTICS



SW-01/03

DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils (2.540 × 2.438 mm, 6.193 sq. mm)

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY (SUBSTRATE)
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. DISABLE (NO CONNECTION SW-01)
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)



SW-02/04

DIE SIZE 0.100 × 0.096 inch, 9600 sq. mils (2.540 × 2.438 mm, 6.193 sq. mm)

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY (SUBSTRATE)
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. DISABLE (NO CONNECTION SW-02)
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)

For additional DICE information refer to Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01-04N LIMIT	SW-01-04G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_D \le 1mA$	100	120	Ω MAX
R_{ON} Match		$V_A = 0V$, $I_D \le 100\mu A$	10	10	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_A \le 10V$, $I_D \le 1mA$	10	10	% MAX
Positive Supply Current	I+	(Note 1)	8	9	mA MAX
Negative Supply Current	I−	(Note 1)	4.5	5.5	mA MAX
Ground Current	I_G		4.0	4.5	mA MAX
Analog Voltage Range	V_A	$R_L \ge 2k\Omega$	±10	±10	V MIN
Logical "1" Input Voltage	V_{INH}		2	2	V MIN
Logical "0" Input Voltage	V_{INL}		0.8	0.8	V MAX
Logical "0" Input Current	I_{INL}	$0 \le V_{IN} \le 0.8V$	3	3	μA MAX
Logical "1" Input Current	I_{INH}	$2 \le V_{IN} \le 15V$	3	3	μA MAX

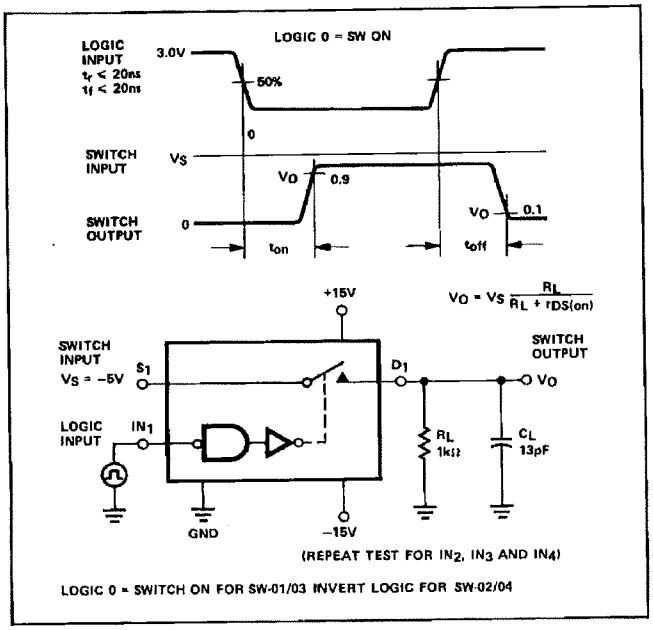
Note: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted..

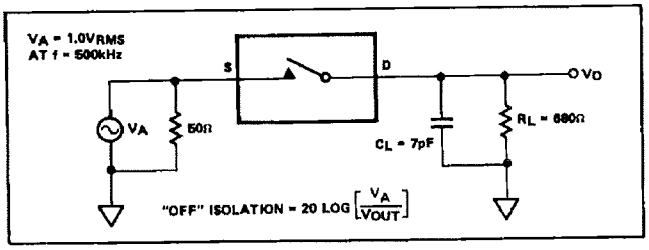
PARAMETER	SYMBOL	CONDITIONS	SW-01-04N TYPICAL	SW-01-04G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-55°C \le T_A \le 125°C$	90	90	Ω
R_{ON} Temperature Coefficient	TC_R	$V_A = 0$, $I_D = 100\mu A$	0.03	0.03	%/°C
Turn-On-Time	T_{ON}	$R_L = 1k$, $C_L = 13pF$	300	300	ns
Turn-Off-Time	T_{OFF}	$R_L = 1k$, $C_L = 13pF$	200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.2	0.2	nA
"OFF" Isolation	ISO_{OFF}	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTE:
1. Power supply and ground current specified for switch "ON" or "OFF".

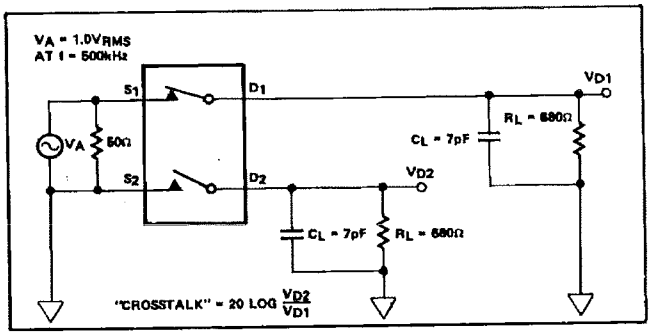
TEST CIRCUITS



TEST FIGURE 1



TEST FIGURE 2



TEST FIGURE 3

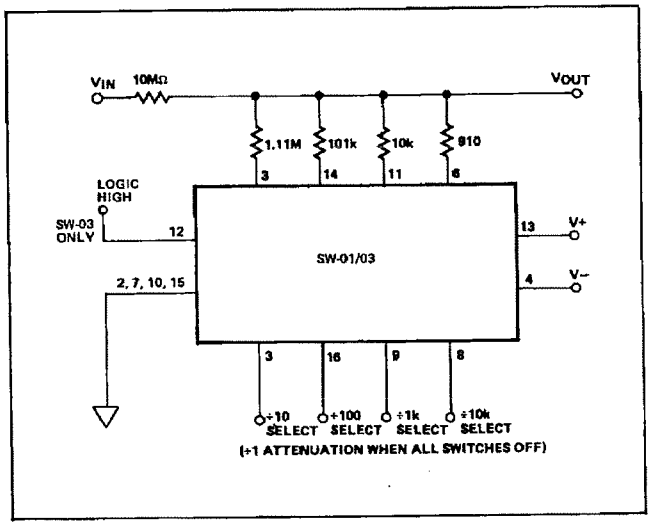
APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BIFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GSD} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

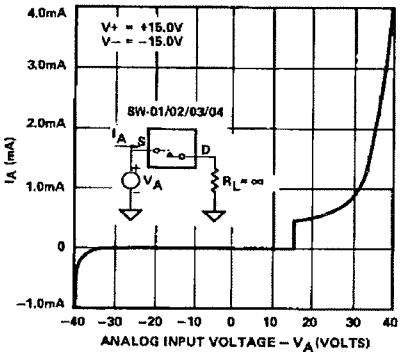
Proper switching requires the "Source" terminal to be connected to the input driving signal. If the DISABLE pin is left unconnected, the switches are controlled by the logic select pins.

PROGRAMMABLE ATTENUATOR (1 to 0.0001)

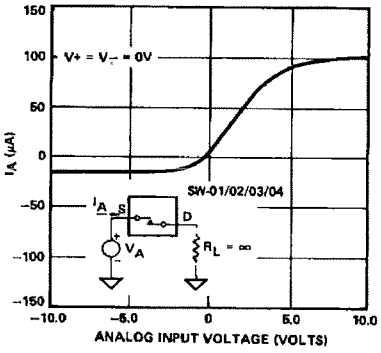


TYPICAL PERFORMANCE CHARACTERISTICS (SW-01/02/03/04)

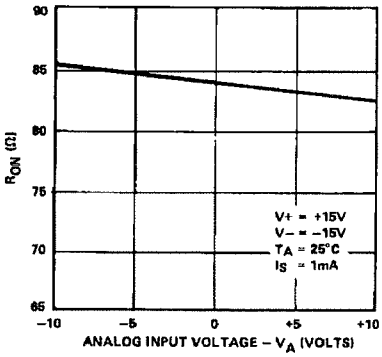
OVERVOLTAGE CHARACTERISTIC



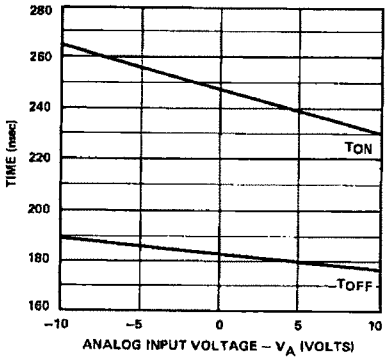
POWER SUPPLY LOSS CHARACTERISTIC



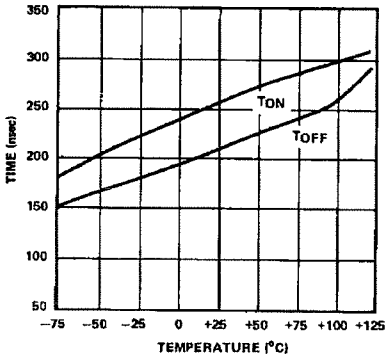
"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)



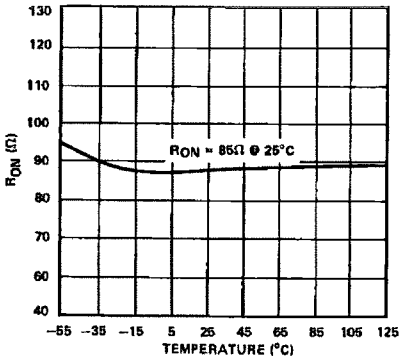
SWITCHING TIME vs ANALOG VOLTAGE



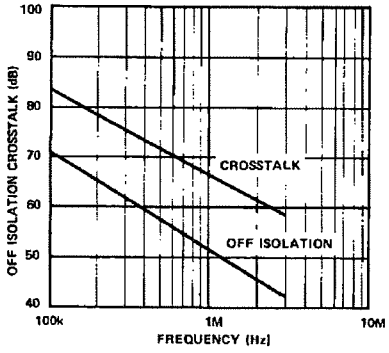
SWITCHING TIMES vs TEMPERATURE



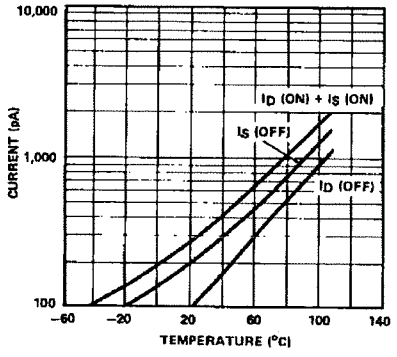
R_{ON} vs TEMPERATURE



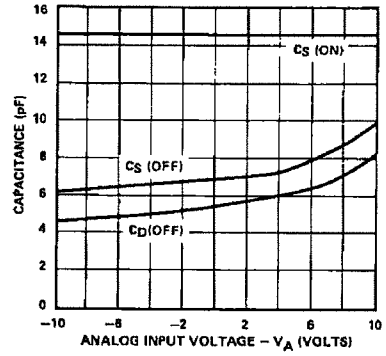
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



LEAKAGE CURRENT vs TEMPERATURE



SWITCH CAPACITANCE vs ANALOG VOLTAGE



The SW-01-SW-04 designs have been optimized for low "ON" resistance variation with temperature, signal voltage, and supply voltage changes. Fast switching response and low leakage currents at high temperature are also key performance improvements over older circuit designs.

The static electricity resistant BIFET switches and additional overvoltage protection circuitry make the precision switches extremely durable in most application environments.

The SW-01-SW-04 are well suited to applications requiring analog currents <5mA with driving source impedances <100Ω. Applications using op amps, buffers or voltage sources as input drive sources are typical of those fulfilling these conditions. Within the given range of source impedance and analog current near ideal signal transfer accuracy is obtainable.

Applications needing very high analog current capability (>5mA) or where the switch is driven from high source impedances (>100Ω) should use the SW-201 (Pin Compatible to SW-01) or the SW-202 (Pin Compatible to SW-02) high-current Quad Switches.

Although the SW-201/SW-202 do not offer the same "ON" resistance temperature coefficient, many other premium characteristics are similar. In addition, the SW-201/SW-202 offer exceptionally low signal distortion over a wide signal voltage and frequency range.

TYPICAL APPLICATIONS

DUAL SLOPE A/D CONVERSION