

Dual 4-input multiplexer (3-State)

74F353

FEATURES

- Inverting version of 74F253
- 3-State outputs for bus interface and multiplex expansion
- Common select inputs
- Separate Output Enable Inputs

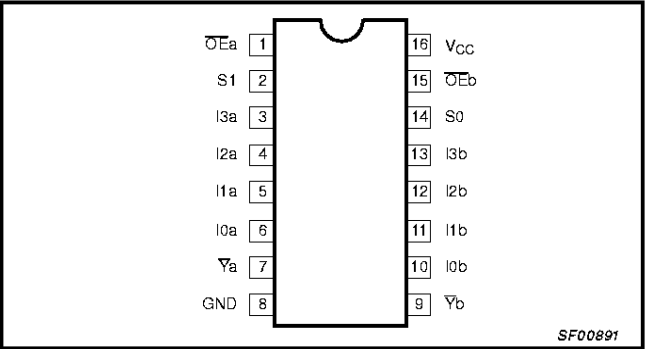
DESCRIPTION

The 74F353 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S0, S1). When the individual Output Enable ($\overline{OE}a$, $\overline{OE}b$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Hi-Z) state.

The 74F353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-State devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F353	6.0ns	11mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PACKAGE DRAWING NUMBER
16-pin plastic DIP	N74F353N	SOT38-4
16-pin plastic SO	N74F353D	SOT162-1

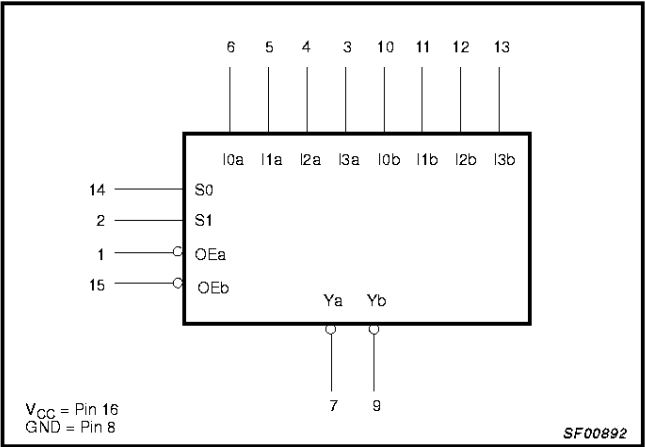
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a–I3a	Port A data inputs	1.0/1.0	20 μ A/0.6mA
I0b–I3b	Port B data inputs	1.0/1.0	20 μ A/0.6mA
S0, S1	Common Select inputs	1.0/1.0	20 μ A/0.6mA
$\overline{OE}a$	Port A Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
$\overline{OE}b$	Port B Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
Ya, Yb	3-State outputs	150/40	3mA/24mA

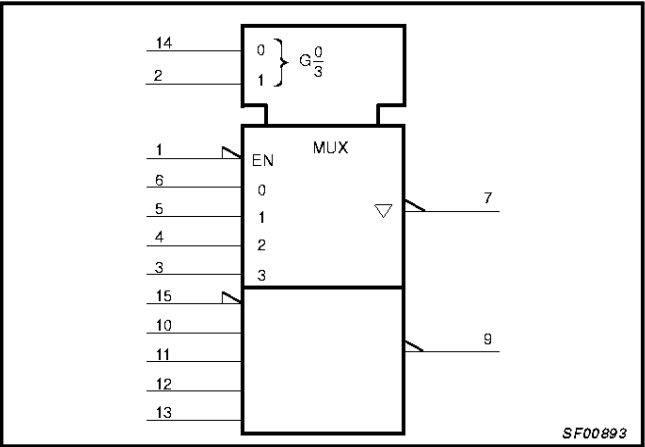
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



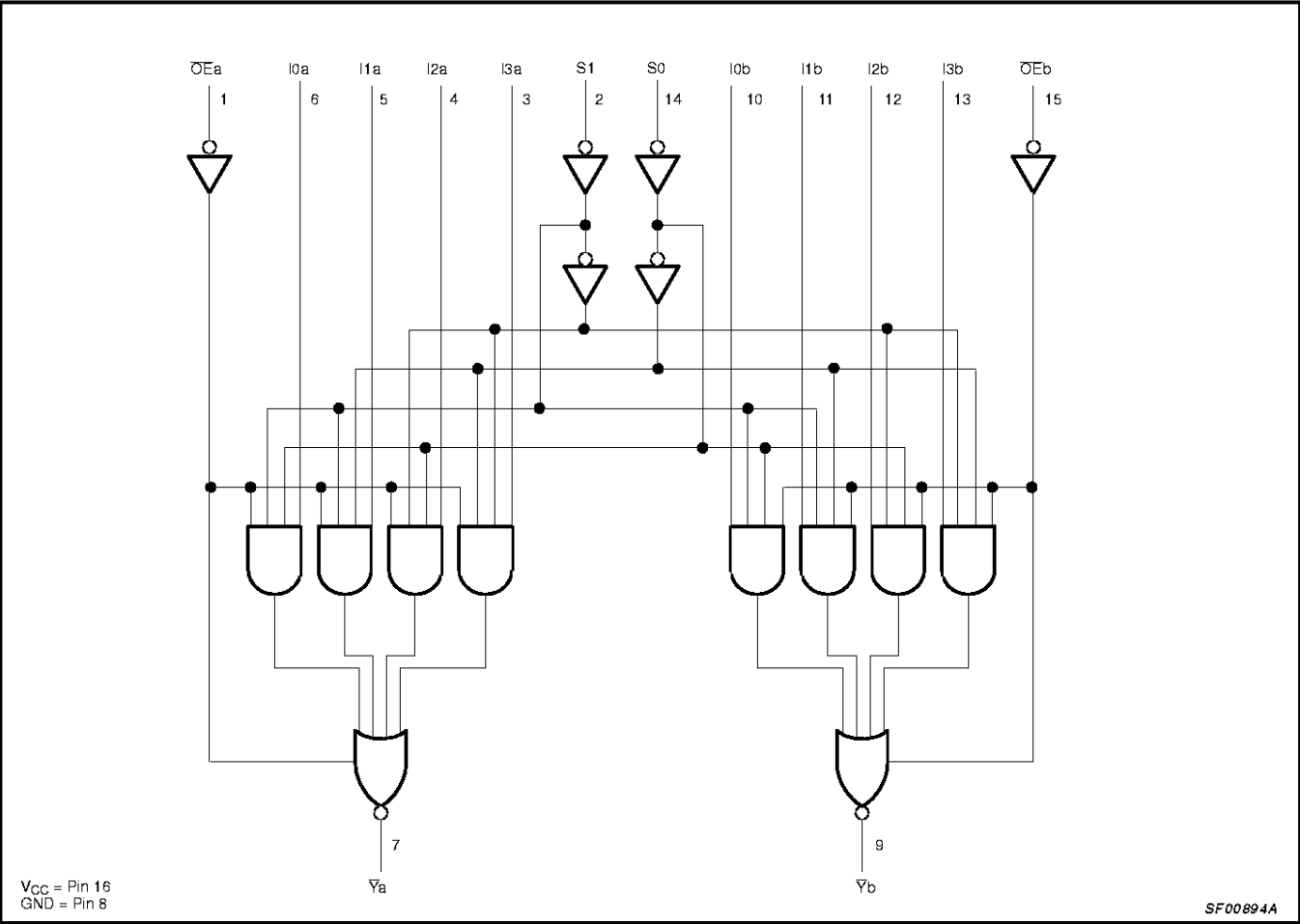
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S0	S1	I0	I1	I2	I3	$\bar{OE}$	$\bar{Y}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT
					MIN	TYP ²	MAX	
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.4			V
				±5%V _{CC}	2.7	3.3		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.35	0.50	V
				±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			−0.73	−1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V				−0.6	mA
I _{OZH}	Off-state output current High-level voltage applied		V _{CC} = MAX, V _O = 2.7V				50	μA
I _{OZL}	Off-state output current Low-level voltage applied		V _{CC} = MAX, V _O = 0.5V				−50	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX		−60		−150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX	$\overline{OE}$ =Sn=In=GND		9	14	mA
		I _{CCL}		$\overline{OE}$ =Sn=GND, In=4.5V		11	20	mA
		I _{CCZ}		$\overline{OE}$ =4.5V, Sn=In=GND		13	23	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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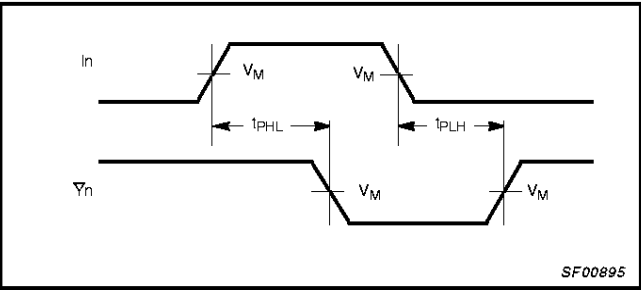
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AC ELECTRICAL CHARACTERISTICS

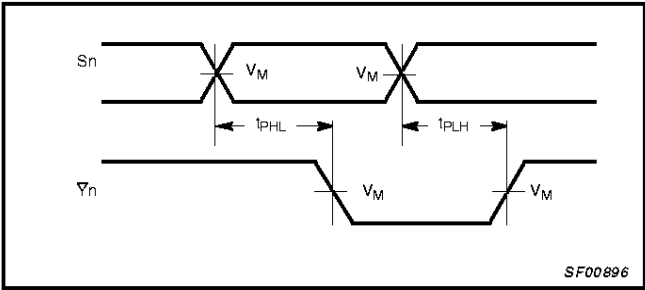
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = 5V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = 5V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay I _n to $\overline{Y}_n$	Waveform 1	3.0 1.5	5.0 3.0	7.0 5.0	3.0 1.0	8.0 5.5	ns
t _{PLH} t _{PHL}	Propagation delay S _n to $\overline{Y}_n$	Waveform 2	5.0 3.0	9.0 6.0	12.0 8.5	4.5 3.0	12.5 9.5	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 6.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.5 1.5	4.0 2.5	5.5 6.0	2.0 1.5	6.0 7.0	ns

AC WAVEFORMS

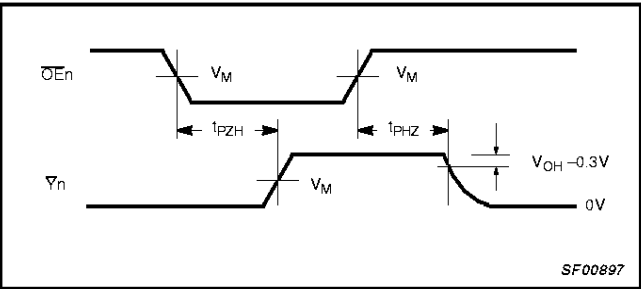
For all waveforms, $V_M = 1.5V$



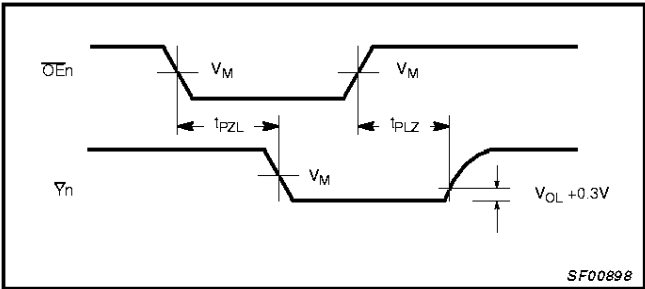
Waveform 1. Propagation Delay, Data to Output



Waveform 2. Propagation Delay, Select to Output



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

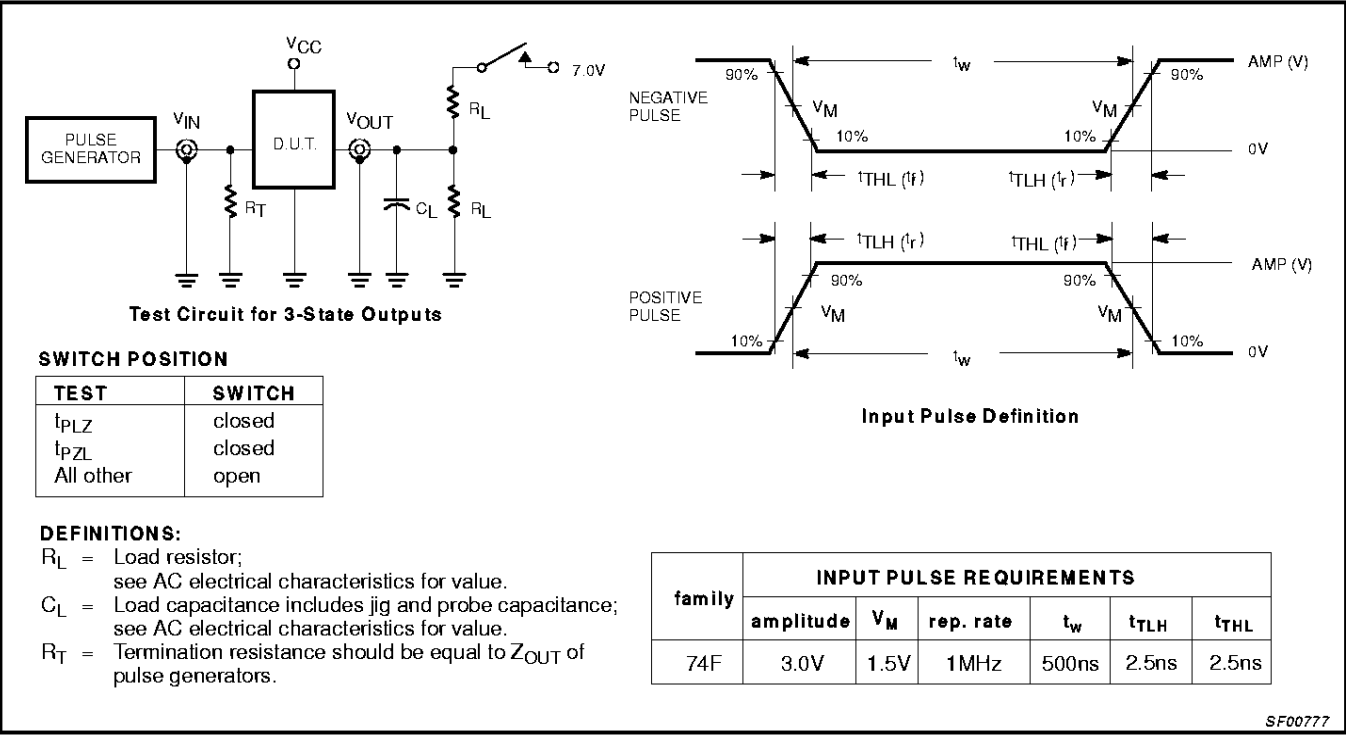


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORMS



SF00777