



Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTER (3-STATE)

IDT54/74FCT16374T/AT/CT/ET
IDT54/74FCT162374T/AT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
 - Extended commercial range of -40°C to $+85^{\circ}\text{C}$
 - $V_{CC} = 5V \pm 10\%$
- **Features for FCT16374T/AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$
- **Features for FCT162374T/AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$

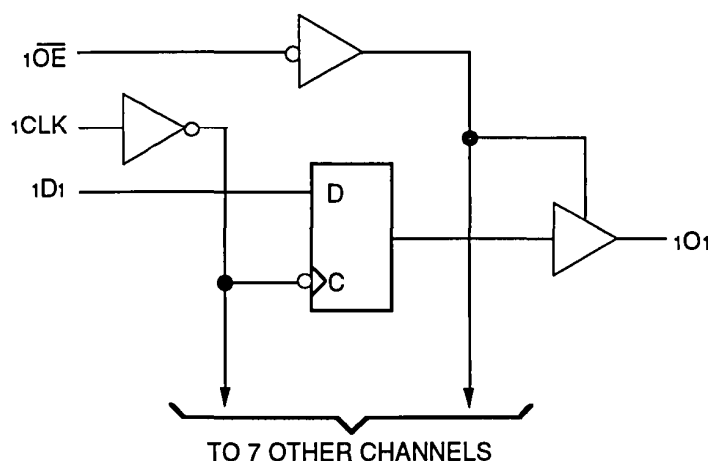
DESCRIPTION:

The IDT54/74FCT16374T/AT/CT/ET and IDT54/74FCT162374T/AT/CT/ET 16-bit edge-triggered D-type registers are built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable ($\overline{xOE}$) and clock ($\overline{xCLK}$) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

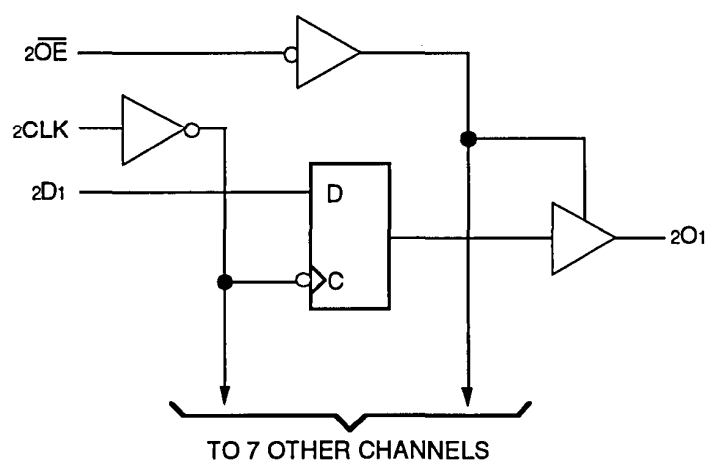
The IDT54/74FCT16374T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162374T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The IDT54/74FCT162374T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16374T/AT/CT/ET and 54/74ABT16374 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM

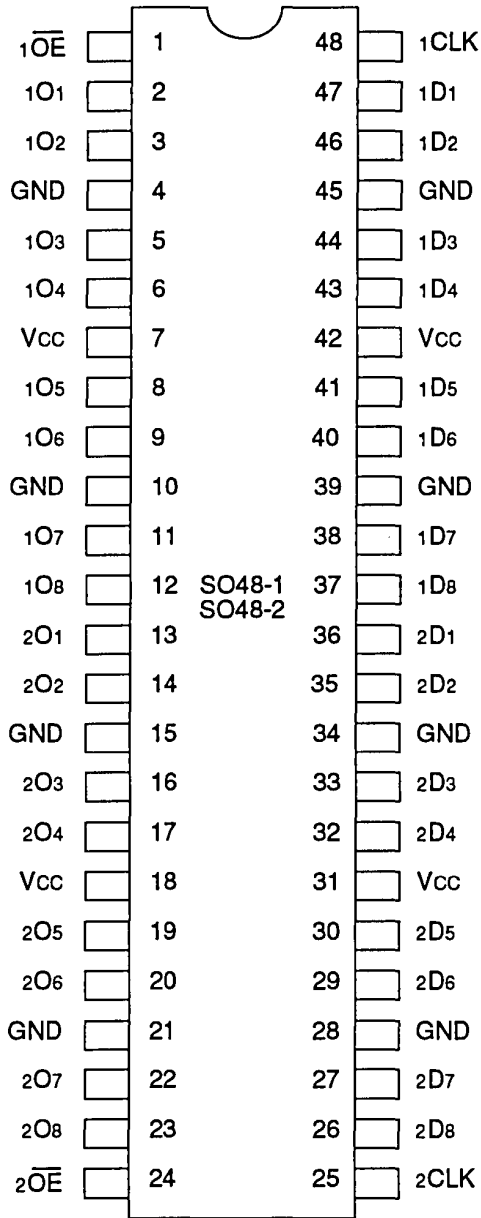


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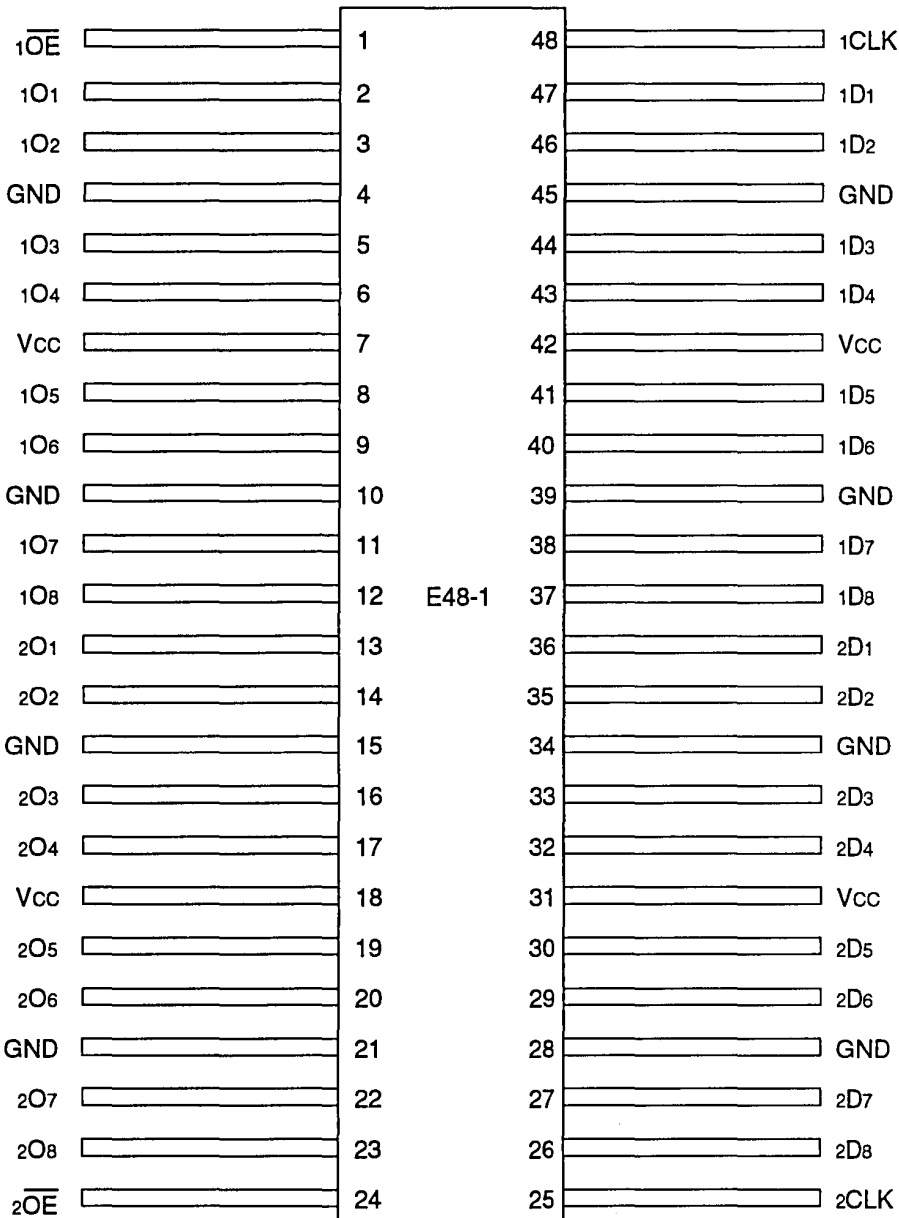
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PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2542 drw 03



CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs
x $\overline{OE}$	3-State Output Enable Input (Active LOW)

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FUNCTION TABLE⁽¹⁾

Function	Inputs			Outputs
	xDx	xCLK	x $\overline{OE}$	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

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- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC}	−0.5 to V _{CC}	V
T _A	Operating Temperature	−40 to +85	−55 to +125	°C
T _{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T _{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	−60 to +120	−60 to +120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

NOTE:

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- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, VCC = 5.0V ± 10%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	VCC = Max.	V _I = VCC	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{IL}	Input LOW Current (Input pins) ⁽⁵⁾		V _I = GND	—	—	±1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	VCC = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max., V _O = GND ⁽³⁾		-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _H	Input Hysteresis	—		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	VCC = Max., V _{IN} = GND or VCC		—	5	500	μA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT16374T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{OH}	Output HIGH Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA	2.5	3.5	—	V
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.4	3.5	—	V
			I _{OH} = -24mA MIL. I _{OH} = -32mA COM'L. ⁽⁴⁾	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA MIL. I _{OL} = 64mA COM'L.	—	0.2	0.55	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	VCC = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT162374T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL. I _{OH} = -24mA COM'L.	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16mA MIL. I _{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ± 5μA at TA = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	μA / MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.1	3.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ Sixteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.0	5.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	7.5	19.0 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL HIGH Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs HIGH}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16374T/162374T				FCT16374AT/162374AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
tpZH tpZL	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
tpHZ tPLZ	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
tsu	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition ⁽¹⁾	FCT16374CT/162374CT				FCT16374ET/162374ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2.0	5.2	2.0	6.2	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.5	1.5	6.2	1.5	4.4	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.7	1.5	3.6	—	—	ns
tsu	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	1.5	—	—	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	0.0	—	—	—	ns
tw	xCLK Pulse Width HIGH or LOW		5.0	—	6.0	—	3.0 ⁽⁴⁾	—	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

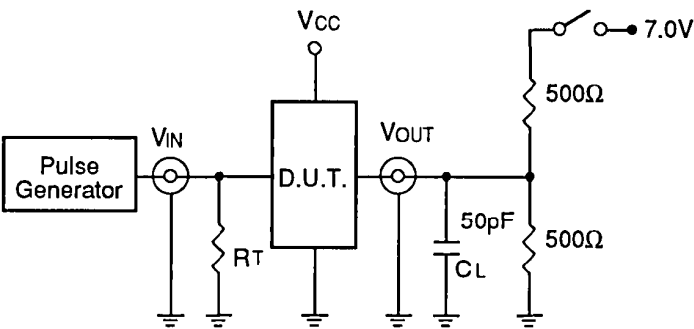
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- This limit is guaranteed but not tested.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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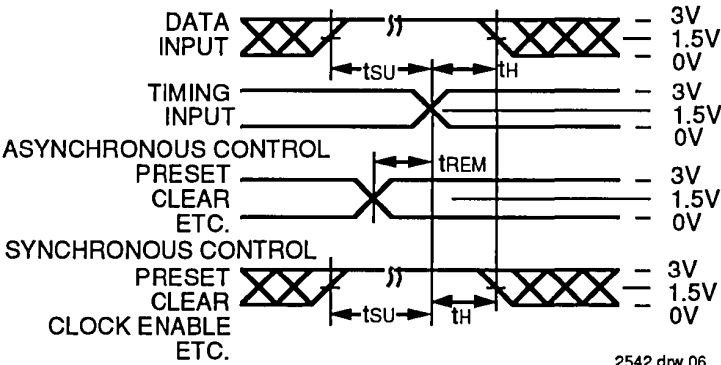
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:
CL= Load capacitance; includes jig and probe capacitance.
RT= Termination resistance; should be equal to ZOUT of the Pulse Generator.

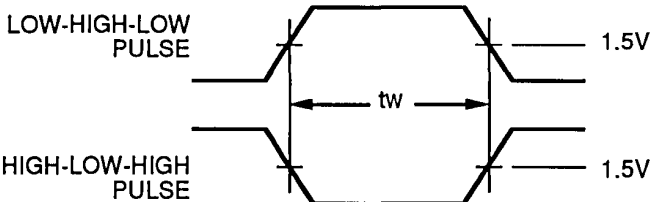
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SET-UP, HOLD AND RELEASE TIMES



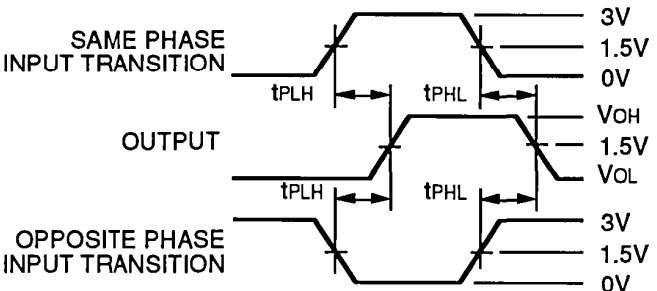
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PULSE WIDTH



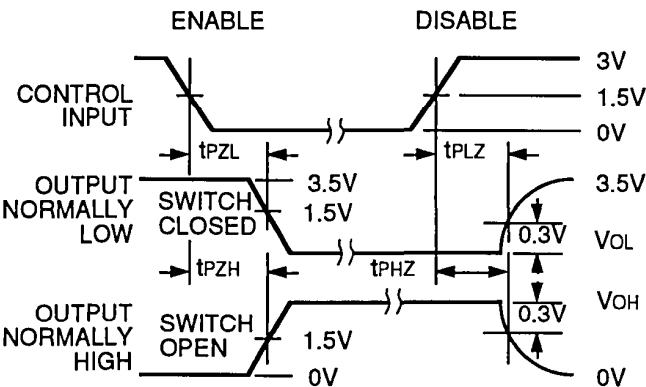
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES



- NOTES:**
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
 - Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

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ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X	
Temp. Range		Device Type		Package	Process	
					Blank B	Commercial MIL-STD-883, Class B
					PV PA E	Shrink Small Outline Package (SO48-1) Thin Shrink Small Outline Package (SO48-2) CERPACK (E48-1)
					16374T 16374AT 16374CT 16374ET 162374T 162374AT 162374CT 162374ET	Non-Inverting 16-Bit Register
				54		−55°C to +125°C
				74		−40°C to +85°C

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