QUALITY SEMICONDUCTOR, INC.

Low Skew Clock Driver/ Buffer for Desktop PC with 4 DIMMS

QS5818

ADVANCE INFORMATION

FEATURES/BENEFITS

- 1 to 18 output buffer/driver
- Tri-state pin for testing
- I^2C programming capability
- Power Supply Voltage 3.3V ±5%
- Low Skew outputs (<250ps)
- Multiple V_{DD} and GND for noise reduction
- 48 pin SSOP package

DESCRIPTION

The QS5818 is a high speed, low noise 1 - 18 non-inverting buffer designed for SDRAM clock buffer applications. Out of the 18 outputs 16 may be used to drive up to four SDRAM DIMMs, and the remaining two can be used for external feedback to a PLL. The QS5818 also includes an I^2C interface, which can enable or disable each output clock driver. Turning unused outputs off reduces EMI.

Figure 1. Functional Block Diagram

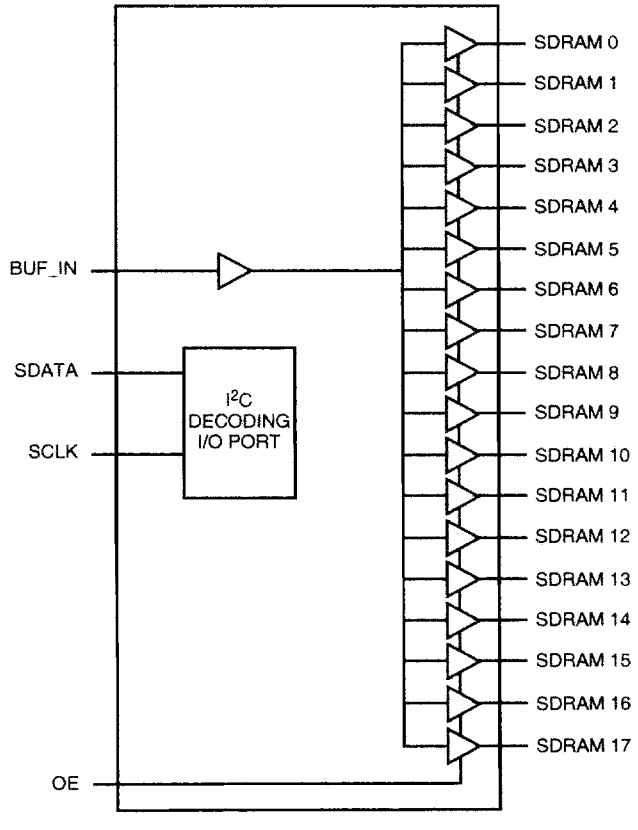


Figure 2. Pin Configuration
(All Pins Top View)

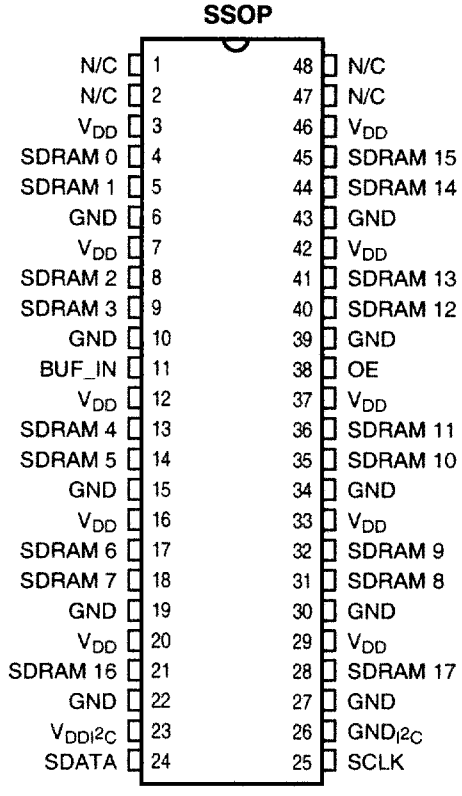


Table 1. Pin Description

Pin Name	Pin Number	Type	Functional Description
N/C	1,2,47,48	—	Pins are not internally connected.
SDRAM (0:3)	4,5,8,9	Out	SDRAM Byte 0 Clock outputs.
SDRAM (4:7)	13,14,17,18	Out	SDRAM Byte 1 Clock outputs.
SDRAM (8:11)	31,32,35,36	Out	SDRAM Byte 2 Clock outputs.
SDRAM (12:15)	40,41,44,45	Out	SDRAM Byte 3 Clock outputs.
SDRAM (16:17)	21,28	Out	SDRAM Clock Outputs useable for feedback.
BUF_IN	11	IN	Input for buffers.
OE	38	IN	Tri-state output enable. Includes internal pull up to V_{DD}. When asserted LOW, clock outputs are high impedance.
SDATA	24	I/O	I^2C Data Pin. Includes internal pull up to V_{DD}.
SCLK	25	I	I^2C Clock Pin. Includes internal pull up to V_{DD}.
V_{DD}	3,7,12,16,20, 29,33,37,42,46	PWR	3.3V power supply for output buffers.
GND	6,10,15,19,22, 27,30,34,39,43	PWR	Ground for output buffers
GND_{I2C}	26	PWR	Ground for I^2C circuitry.
V_{DDI2C}	23	PWR	3.3V power supply for I^2C circuitry.

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	−0.5V to 4.6V
DC Output Voltage V_{OUT}	−0.5V to 4.6V
DC Input Voltage V_{IN}	−0.5V to 4.6V
DC Input Diode Current with $V_I < 0$	−20mA
Maximum Power Dissipation At $T_A = 85°C$,	600mW
T_{STG} Storage Temperature	−65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power Supply Voltage	3.135	3.3	3.465	V
T_A	Operating Temperature	−40	25	85	°C
C_L	Load Capacitance	—	—	30	pF
C_{IN}	Input Capacitance[1]	—	—	7	pF

Table 4. DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	For all inputs	2.0	—	—	V
V_{IL}	Input Low Voltage	For all inputs except I^2C inputs	—	—	0.8	V
		I^2C inputs (SDATA and SCLK)	—	—	0.7	
I_{IH}	Input High Input Current	$V_{IN} = V_{DD}$	–5	—	5	µA
I_{IL}	Input Low Current	$V_{IN} = 0V$; BUF_IN	—	5	5	µA
		$V_{IN} = 0V$; OE, SDATA, SCLK	–100		0	
I_{DD}	Supply Current	$C_L = 0pF$; f_{IN} @ 66.66MHz(1)			150	mA
		$C_L = 0pF$; f_{IN} @ 100MHz(1)			200	
		$C_L = 30pF$; f_{IN} @ 66.66MHz(1)			230	
		$C_L = 30pF$; f_{IN} @ 100MHz(1)			360	mA
		BUF_IN = GND or V_{DD}, all other inputs at V_{DD}			500	µA
V_{OH}	Output High Voltage	SDRAM(0:17) $I_{OH} = -36mA$	2.4		—	V
V_{OL}	Output Low Voltage	SDRAM(0:17) $I_{OL} = 25mA$	—		0.4	V
V_{OLI^2C}	Output Low Voltage	SDATA $I_{OLI^2C} = 3mA$	—	—	0.4	V

Table 5. AC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_R	Rise Time(1)	0.4V to 2.4V; $C_L = 30pF$	—		2.2	ns
T_F	Fall Time(1)	2.4V to 0.4V; $C_L = 30pF$	—		2.2	ns
D_t	Duty Cycle(1)	$V_T = 1.5V$; $C_L = 30pF$; With 50% Input Clock	45	50	55	%
T_{SK}	Skew (output – output)(1)	$V_T = 1.5V$; $C_L = 30pF$ for all outputs see Figure 3	—		200	ps
T_{PHL} or T_{PLH}	Propagation Delay	$V_T = 1.5V$	—		4.0	ns
T_{PZL} or T_{PZH}	Enable Delay	$V_T = 1.5V$ see Figure 4	—		8.0	ns
T_{PLZ} or T_{PHZ}	Disable Delay	$V_T = 1.5V$ see Figure 4	—		8.0	ns

Note:
1. Applies to SDRAM(0:17) outputs. Guaranteed by design, not subject to 100% production testing.

I²C Serial Interface Control

The I²C interface permits individual enable/disable of each clock output: any unused outputs may be disabled to reduce the EMI. The QS5818 is a slave receiver device. It can read back the data stored in the latches for verification.

The data transfer rate supported by the I²C interface is 100K bits/sec. Data is transferred in bytes (with the addition of start, stop, acknowledge bits) in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The first two bytes transferred must be a Command Code followed by a Byte Count. Both of these bytes are ignored by the device.

The I²C address of the QS5818 is:

A7	A6	A5	A4	A3	A2	A1
1	1	0	1	0	0	1

Address A0 is the read/write bit and is set to 0 for writes and 1 for reads.

During read back, the first byte read is a Byte Count representing the number of bytes following (fixed at 3).

Table 6. Serial Configuration Command Bitmaps

Byte 0: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable, outputs held low),
Default = Enable

Bit	Pin #	Description
Bit 7	18	SDRAM 7 (Active/Inactive)
Bit 6	17	SDRAM 6 (Active/Inactive)
Bit 5	14	SDRAM 5 (Active/Inactive)
Bit 4	13	SDRAM 4 (Active/Inactive)
Bit 3	9	SDRAM 3 (Active/Inactive)
Bit 2	8	SDRAM 2 (Active/Inactive)
Bit 1	5	SDRAM 1 (Active/Inactive)
Bit 0	4	SDRAM 0 (Active/Inactive)

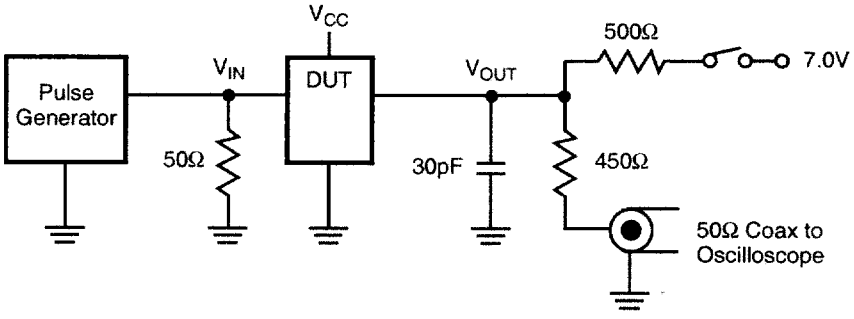
Byte 1: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable, outputs held low),
Default = Enable

Bit	Pin #	Description
Bit 7	45	SDRAM 15 (Active/Inactive)
Bit 6	44	SDRAM 14 (Active/Inactive)
Bit 5	41	SDRAM 13 (Active/Inactive)
Bit 4	40	SDRAM 12 (Active/Inactive)
Bit 3	36	SDRAM 11 (Active/Inactive)
Bit 2	35	SDRAM 10 (Active/Inactive)
Bit 1	32	SDRAM 9 (Active/Inactive)
Bit 0	31	SDRAM 8 (Active/Inactive)

Byte 2: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable, outputs held low),
Default = Enable

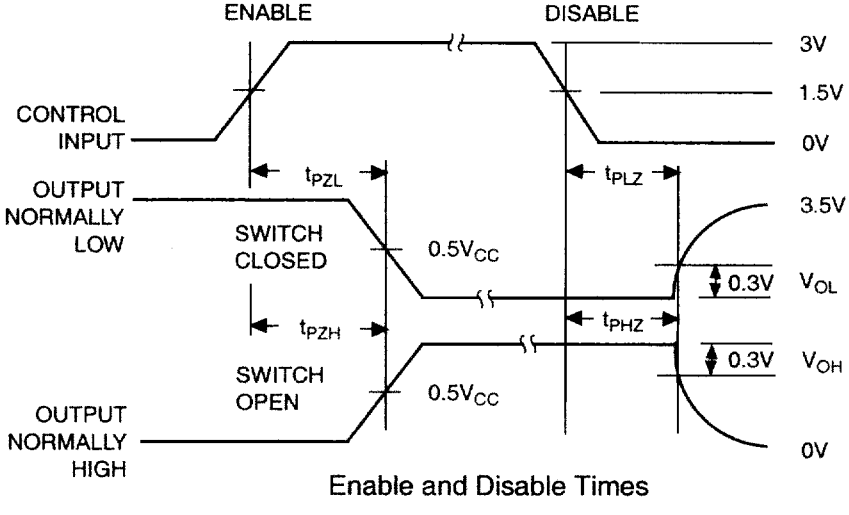
Bit	Pin #	Description
Bit 7	28	SDRAM 17 (Active/Inactive)
Bit 6	21	SDRAM 16 (Active/Inactive)
Bit 5	—	Reserved, 1 at power up, set to 0
Bit 4	—	Reserved, 1 at power up, set to 0
Bit 3	—	Reserved, 1 at power up, set to 0
Bit 2	—	Reserved, 1 at power up, set to 0
Bit 1	—	Reserved, 1 at power up, set to 0
Bit 0	—	Reserved, 1 at power up, set to 0

Figure 3. Test Circuit

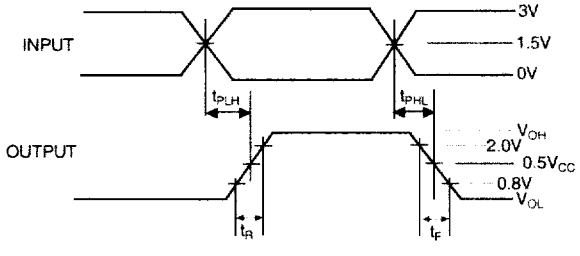


Parameter Tested	Switch Position
t_{PLZ}, t_{PZL}	Closed
All Others	Open

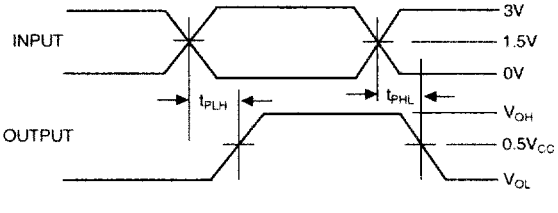
Figure 4. AC Timing Diagram



Enable and Disable Times



Propagation Delay



Pulse Skew - $t_{SK(p)}$

Figure 5. Ordering Information

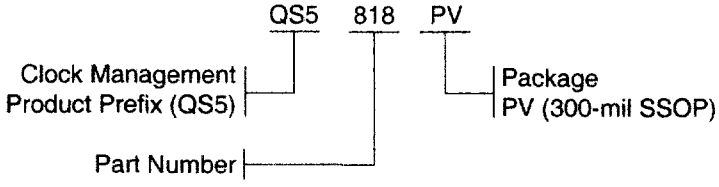
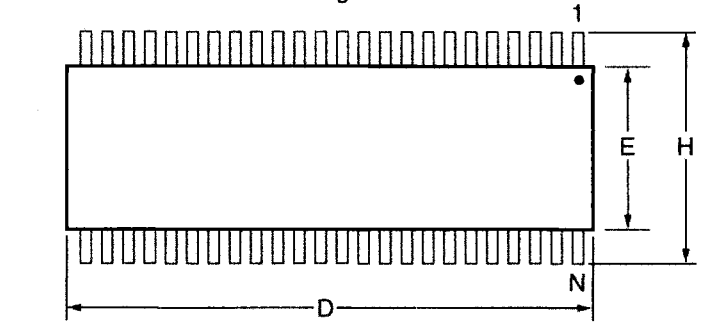
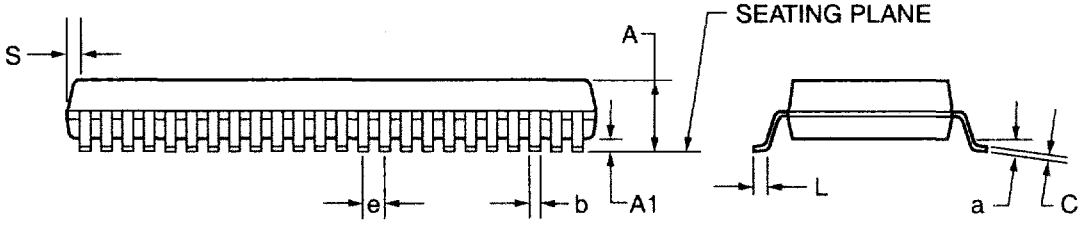


Figure 6. Packaging Information
300-mil SSOP - Package Code PV

Shrink Small Outline Package
Plastic Small Outline Gull-Wing



Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.



JEDEC#	MO-118AA			MO-118AB		
DWG#	PSS-48B			PSS-56B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.095	0.102	0.110	0.095	0.102	0.110
A1	0.008	0.012	0.116	0.008	0.012	0.016
b	0.008	0.010	0.0135	0.008	0.010	0.0135
C	0.005	0.008	0.010	0.005	0.008	0.010
D	0.620	0.625	0.630	0.720	0.725	0.730
E	0.291	0.295	0.299	0.291	0.295	0.299
e	0.025 BSC			0.025 BSC		
H	0.395	0.410	0.420	0.395	0.410	0.420
L	0.020	0.030	0.040	0.020	0.030	0.040
N		48			56	
a	0°	5°	8°	0°	5°	8°
S	0.022	0.025	0.028	0.022	0.025	0.028