

RJK0230DPA

Silicon N Channel Power MOS FET with Schottky Barrier Diode High Speed Power Switching

R07DS0541EJ0110

Rev.1.10

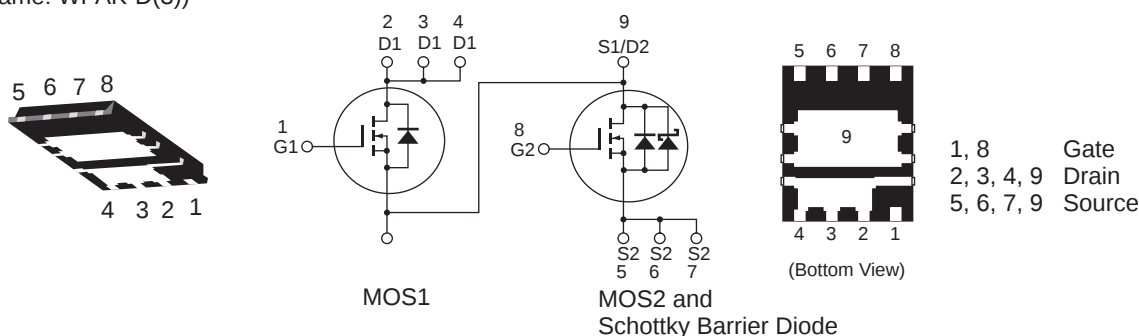
Sep 12, 2011

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PWSN0008DD-B
(Package name: WPAK-D(3))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2	
Drain to source voltage	V_{DSS}	25	25	V
Gate to source voltage	V_{GSS}	±20	±12	V
Drain current	I_D	20	50	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	80	200	A
Reverse drain current	I_{DR}	20	50	A
Avalanche current	I_{AP} ^{Note 2}	12	23	A
Avalanche energy	E_{AR} ^{Note 2}	18	66	mJ
Channel dissipation	P_{ch} ^{Note3}	15	35	W
Channel temperature	T_{ch}	150	150	°C
Storage temperature	T_{stg}	-55 to +150	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

3. $T_c = 25^\circ C$

Electrical Characteristics

• MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	5.8	7.0	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	8.4	10.9	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	35	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1180	1650	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	252	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	90	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.0	2.2	Ω	
Total gate charge	Q_g	—	7.7	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	3.3	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	2.0	—	nC	$I_D = 20 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	7.4	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$
Rise time	t_r	—	4.3	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	34	—	ns	$R_L = 1.0 \Omega$
Fall time	t_f	—	5.4	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 20 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	25	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

• MOS2

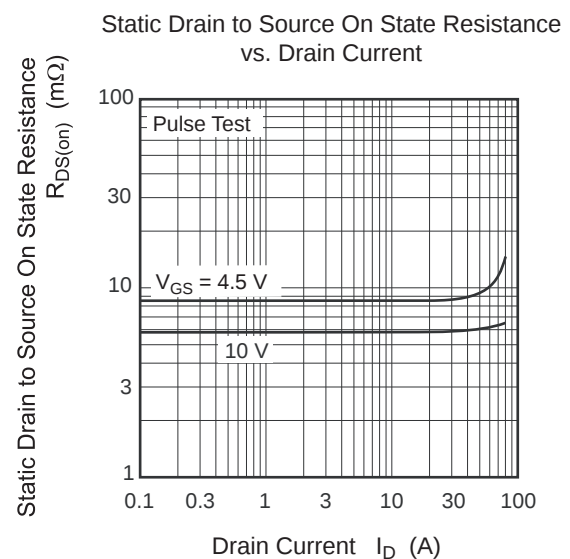
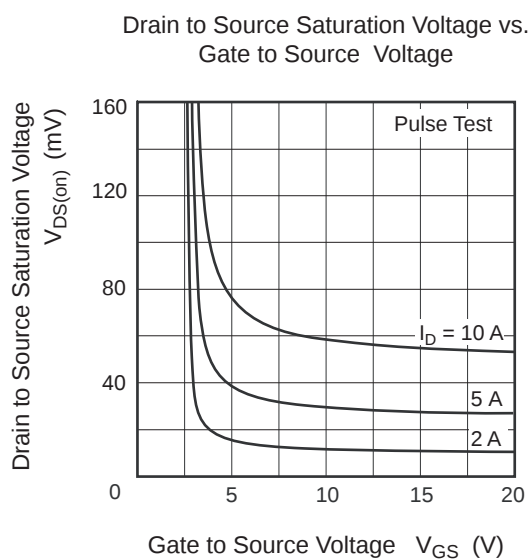
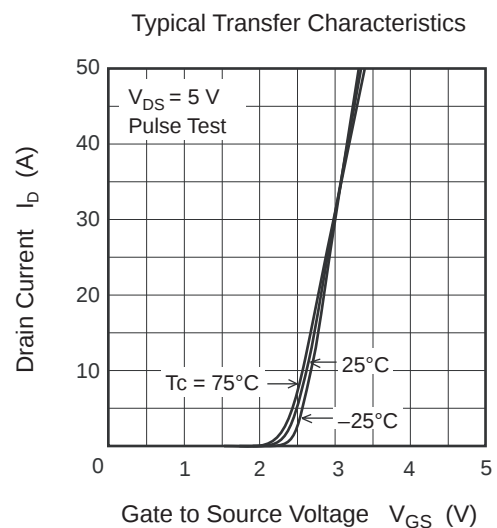
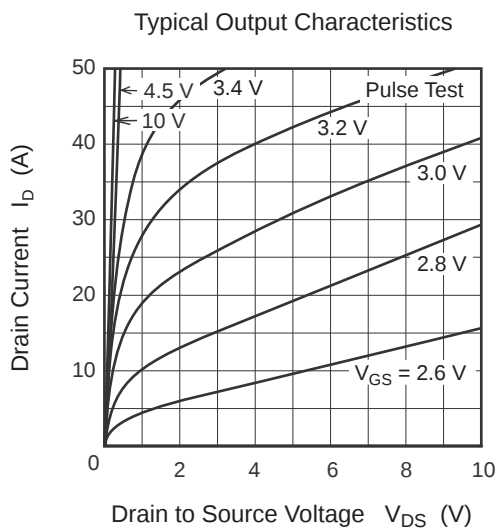
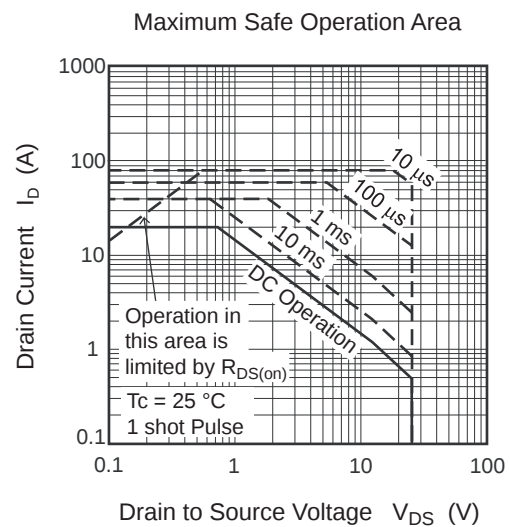
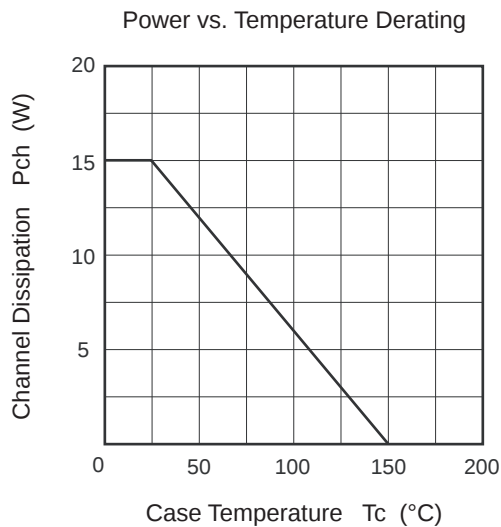
(Ta = 25°C)

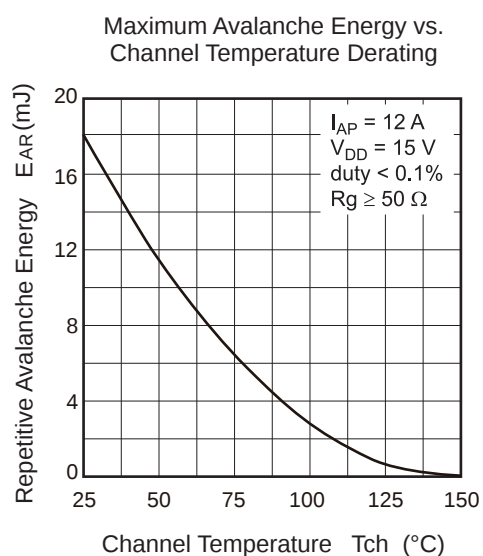
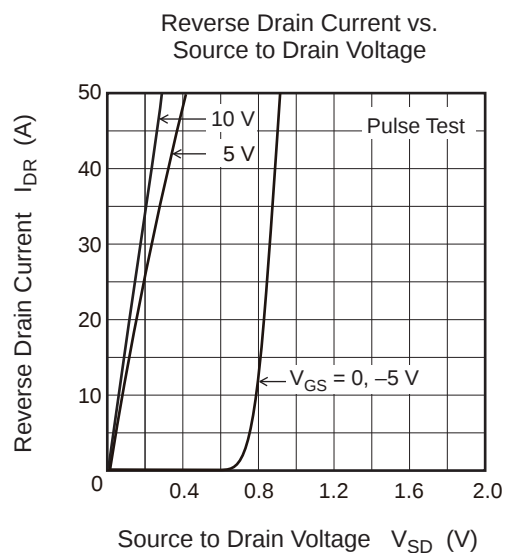
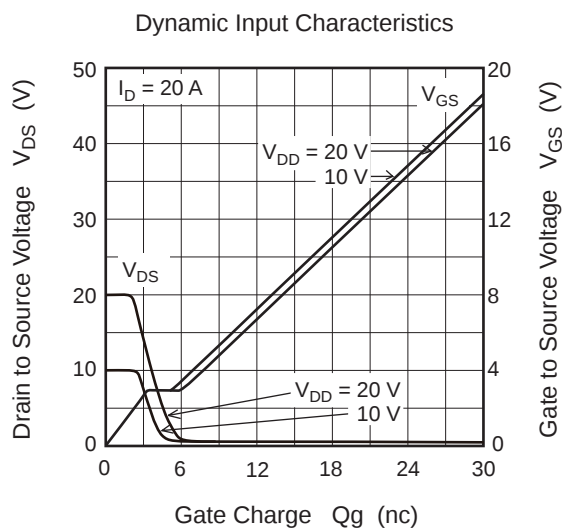
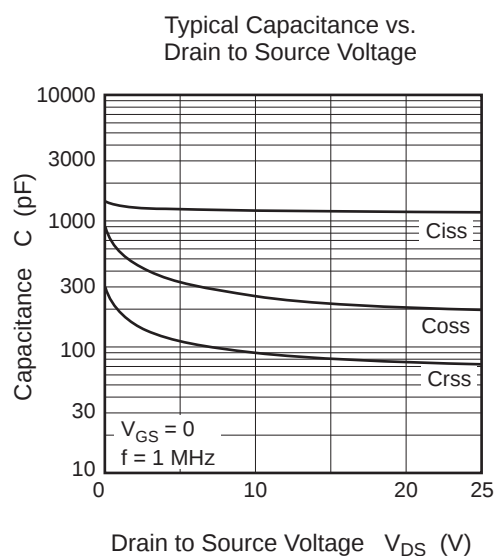
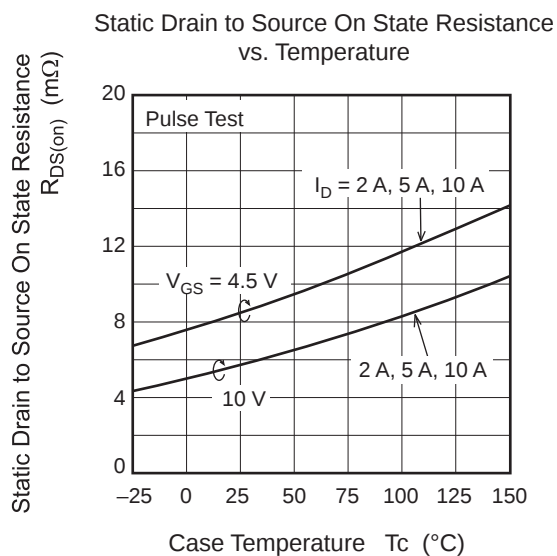
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.5	μA	$V_{GS} = \pm 12 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	mA	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.5	1.9	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 8 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	1.7	2.2	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	140	—	S	$I_D = 25 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	6980	9650	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	900	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	580	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.0	2.2	Ω	
Total gate charge	Q_g	—	45	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	19	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	12	—	nC	$I_D = 50 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = 8 \text{ V}$, $I_D = 25 \text{ A}$
Rise time	t_r	—	9.5	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	$R_L = 0.4 \Omega$
Fall time	t_f	—	25	—	ns	$R_g = 4.7 \Omega$
Schottky Barrier diode forward voltage	V_F	—	0.39	—	V	$I_F = 2 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	37	—	ns	$I_F = 50 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse

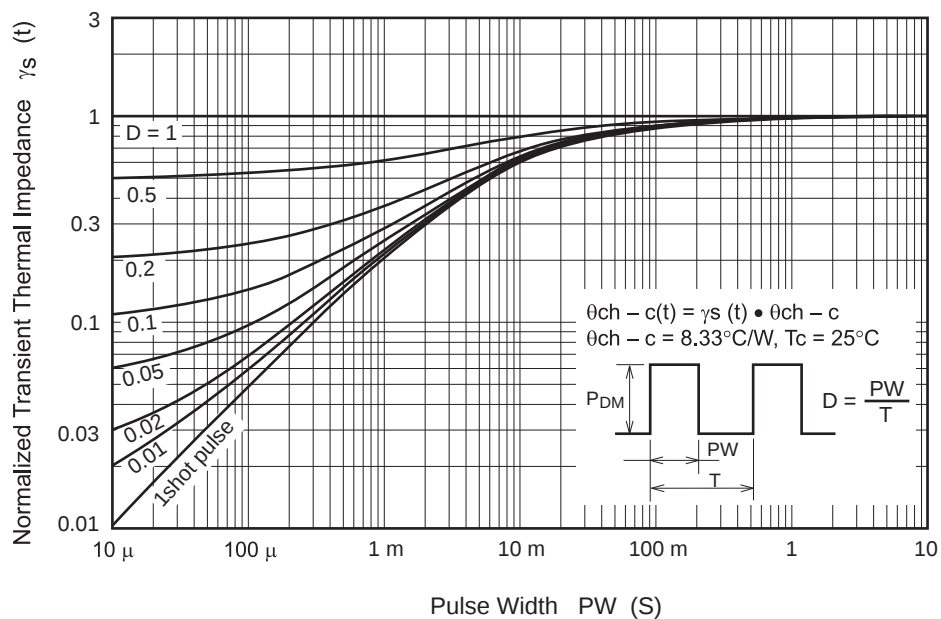
Main Characteristics

• MOS1

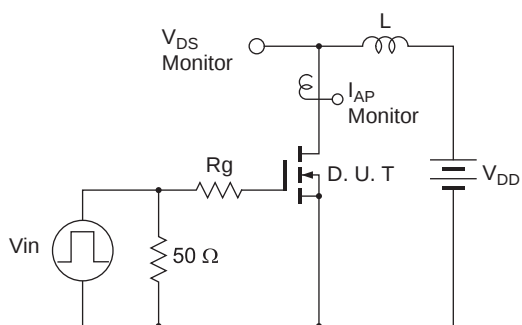




Normalized Transient Thermal Impedance vs. Pulse Width

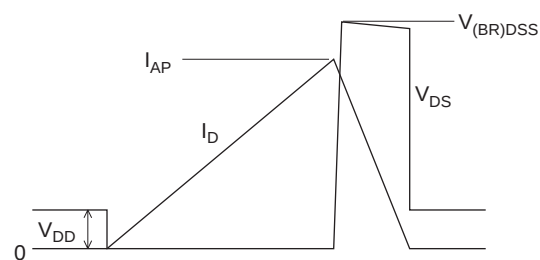


Avalanche Test Circuit

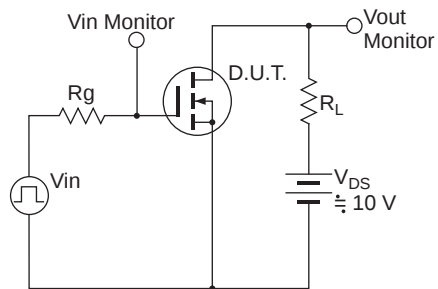


Avalanche Waveform

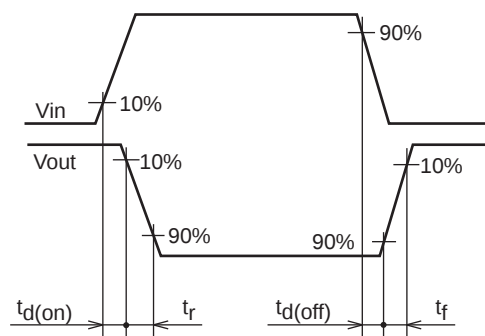
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



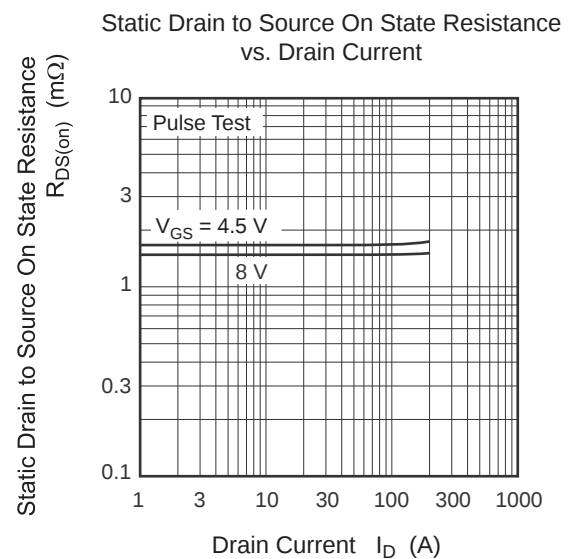
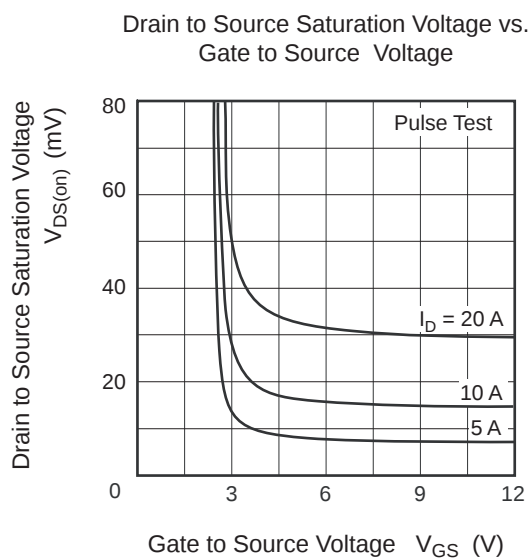
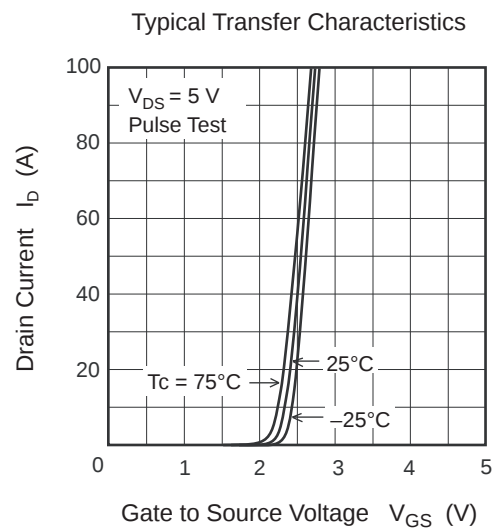
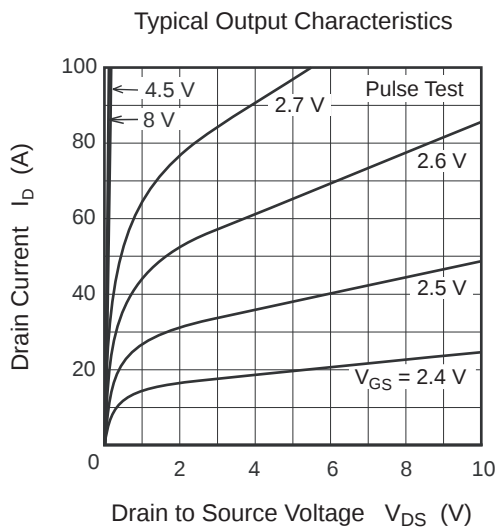
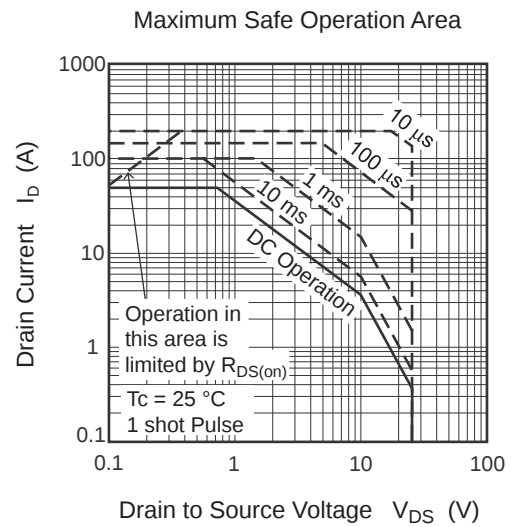
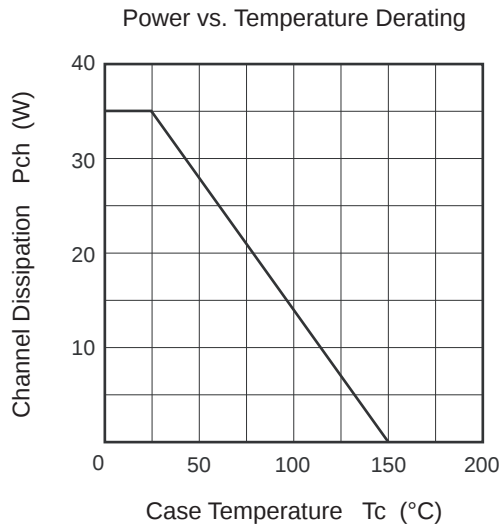
Switching Time Test Circuit

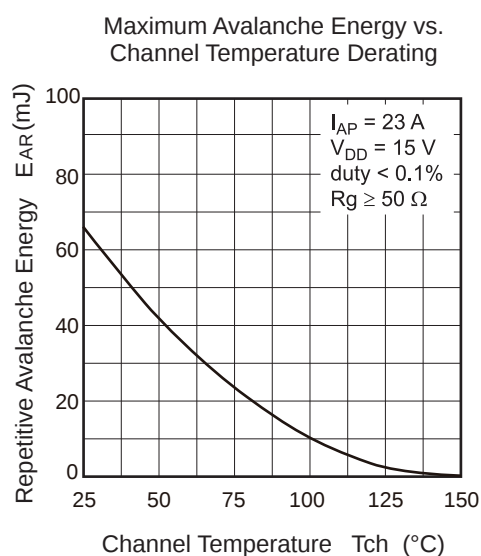
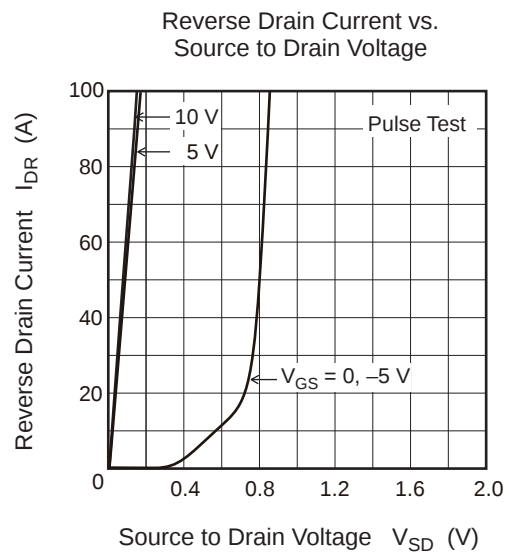
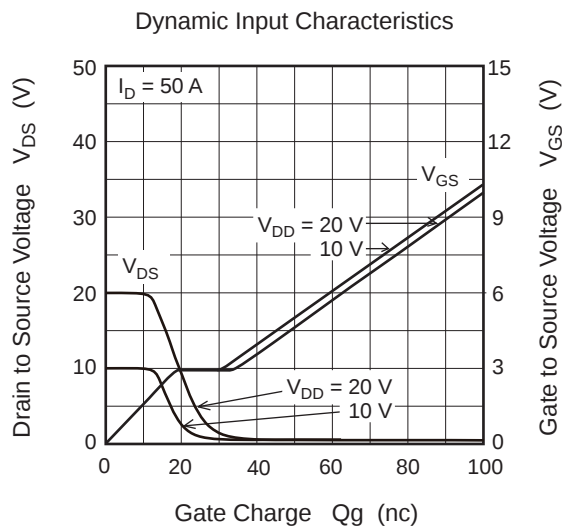
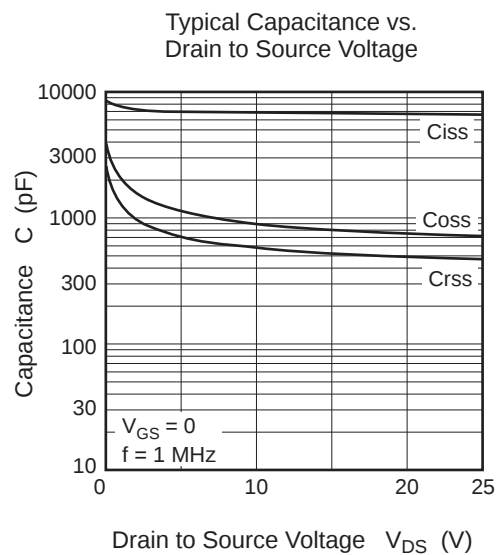
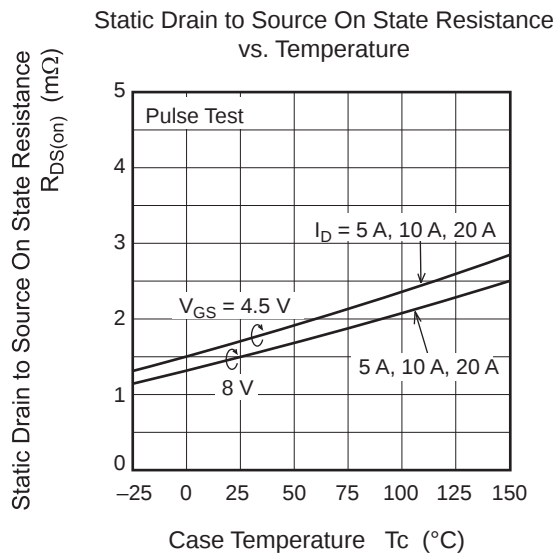


Switching Time Waveform

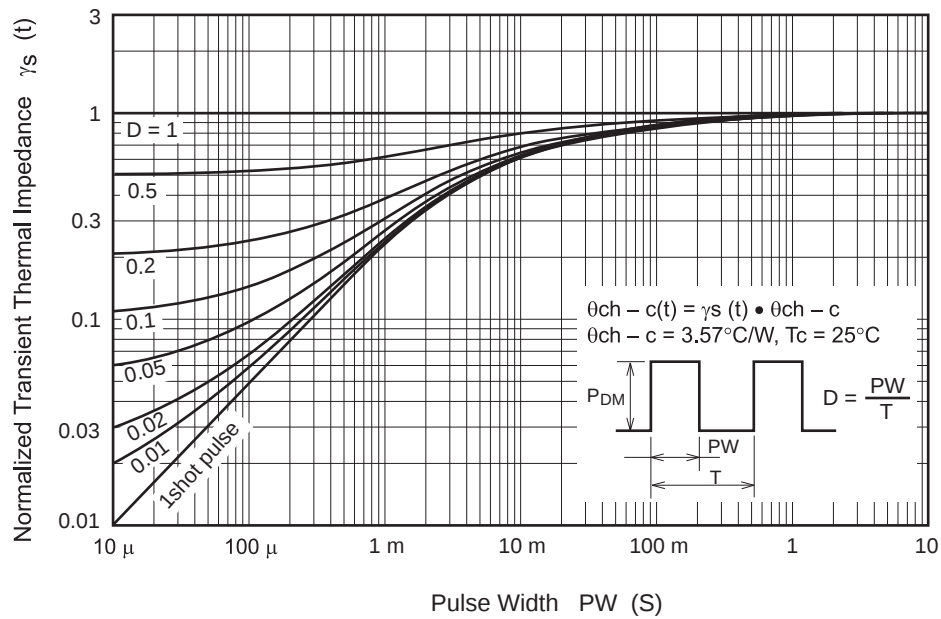


• MOS2 and Schottky Barrier Diode

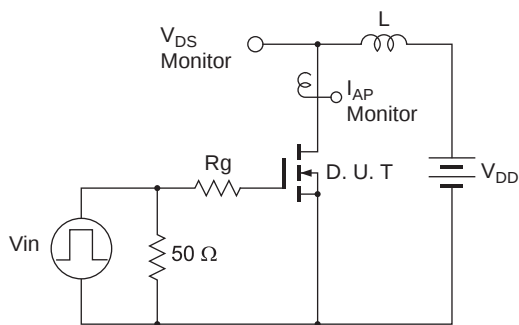




Normalized Transient Thermal Impedance vs. Pulse Width

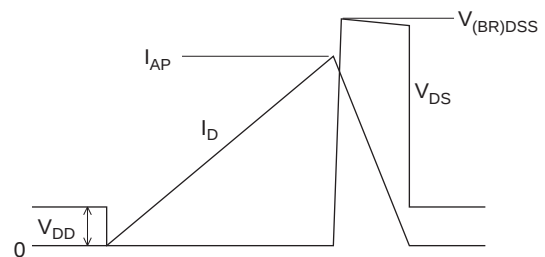


Avalanche Test Circuit

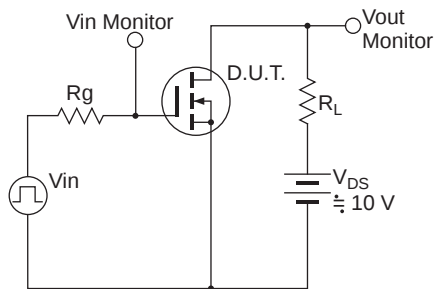


Avalanche Waveform

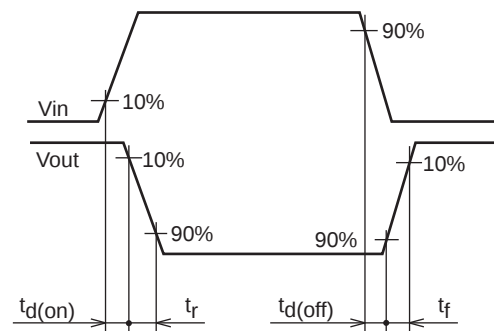
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



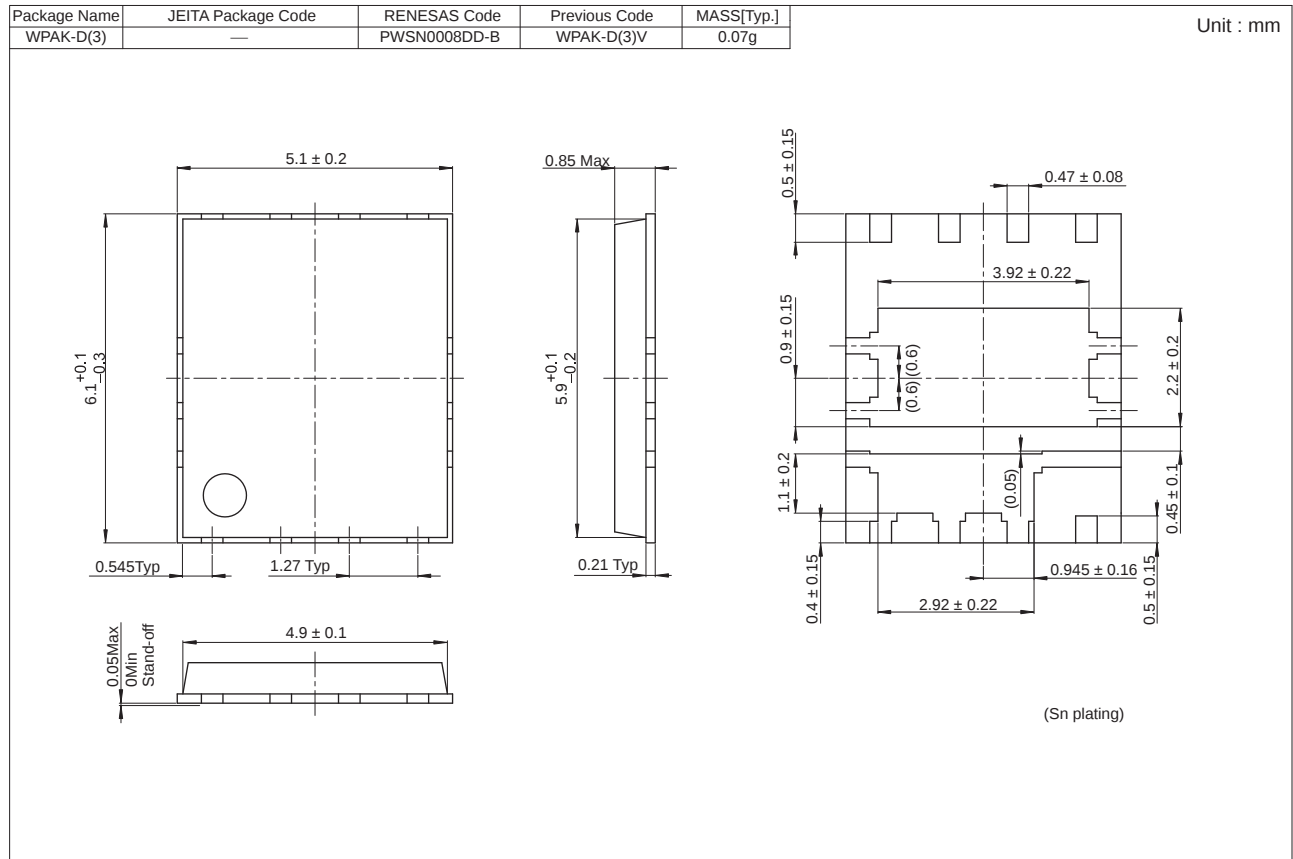
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK0230DPA-00-J5A	3000 pcs	Taping

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