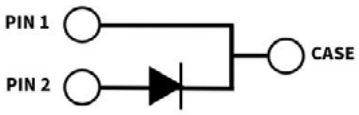
E4D02120E

1200 V, 2 A Silicon Carbide Schottky Diode

Description

With the performance advantages of a Silicon Carbide (SiC) Schottky Barrier diode, power electronics systems can expect to meet higher efficiency standards than Si-based solutions, while also reaching higher frequencies and power densities. SiC diodes can be easily paralleled to meet various application demands, without concern of thermal runaway. In combination with the reduced cooling requirements and improved thermal performance of SiC products, SiC diodes are able to provide lower overall system costs in a variety of diverse applications.

TO-252-2



Package Types: TO-252-2
PN's: E4D02120

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Applications

- Bootstrap diode
- Boost diodes in PFC
- Automotive power conversion
- PV inverters
- Outdoor power conversion

Features

- Low forward voltage (V_F) drop with positive temperature coefficient
- Zero reverse recovery current/forward recovery voltage
- Temperature-independent switching behavior
- AEC-Q101 + HV-H3TRB qualified, PPAP capable

Maximum Ratings (T_C = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Value	Unit	Test Conditions	Note
Repetitive Peak Reverse Voltage	V_{RRM}	1200	V		
DC Blocking Voltage	V_{DC}	1200			
Continuous Forward Current	I_F	8	A	T_C = 25 °C	Fig. 3
		4		T_C = 135 °C	
		2		T_C = 160 °C	
Repetitive Peak Forward Surge Current	I_{FRM}	11		T_C = 25 °C, t_P = 10 ms, Half Sine Wave	
		7		T_C = 110 °C, t_P = 10 ms, Half Sine Wave	
Power Dissipation	P_{tot}	50	W	T_C = 25 °C	Fig. 4
		21		T_C = 110 °C	

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Electrical Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Forward Voltage	V_F	1.4	1.8	V	I_F = 2 A, T_J = 25 °C	Fig. 1
		1.9			I_F = 2 A, T_J = 175 °C	
Reverse Current	I_R	10	50	µA	V_R = 1200 V, T_J = 25 °C	Fig. 2
		40			V_R = 1200 V, T_J = 175 °C	
Total Capacitive Charge	Q_C	16		nC	V_R = 800 V, T_J = 25 °C	Fig. 5
Total Capacitance	C	153		pF	V_R = 0 V, T_J = 25 °C, f = 1 MHz	Fig. 6
		17			V_R = 400 V, T_J = 25 °C, f = 1 MHz	
		14			V_R = 800 V, T_J = 25 °C, f = 1 MHz	
Capacitance Stored Energy	E_C	5.6		µJ	V_R = 800 V	Fig. 7

Note: SiC Schottky Diodes are majority carrier devices, so there is no reverse recovery charge.

Thermal & Mechanical Characteristics

Parameter	Symbol	Value	Unit	Note
Thermal Resistance, Junction to Case (Typ.)	$R_{\theta, JC}$	2.99	°C/W	
Operating Junction & Storage Temperature	T_J, T_{stg}	-55 to +175	°C	Fig. 8
Moisture Sensitivity Level	MSL	MSL 3		

Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Value
Human Body Model	HBM	Class 3B (≥ 8000 V)
Charge Device Model	CDM	Class C3 (≥ 1000 V)

Typical Performance

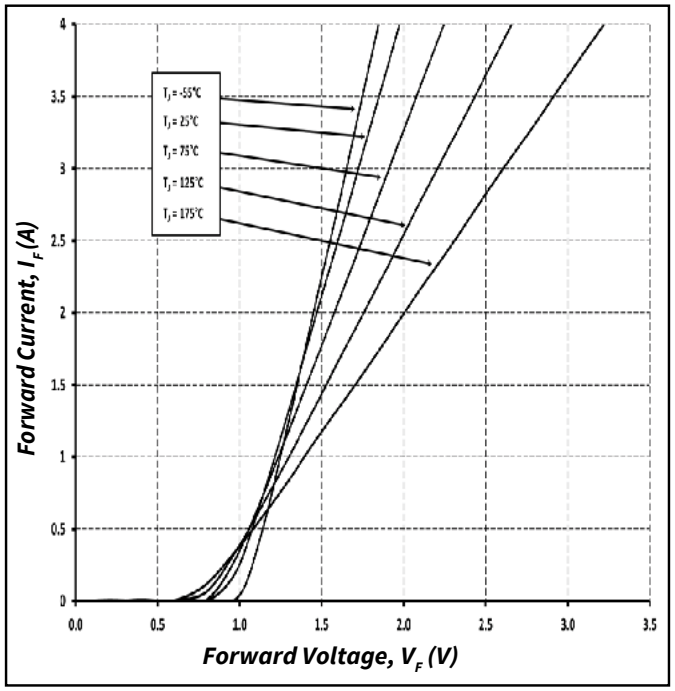


Figure 1. Forward Characteristics

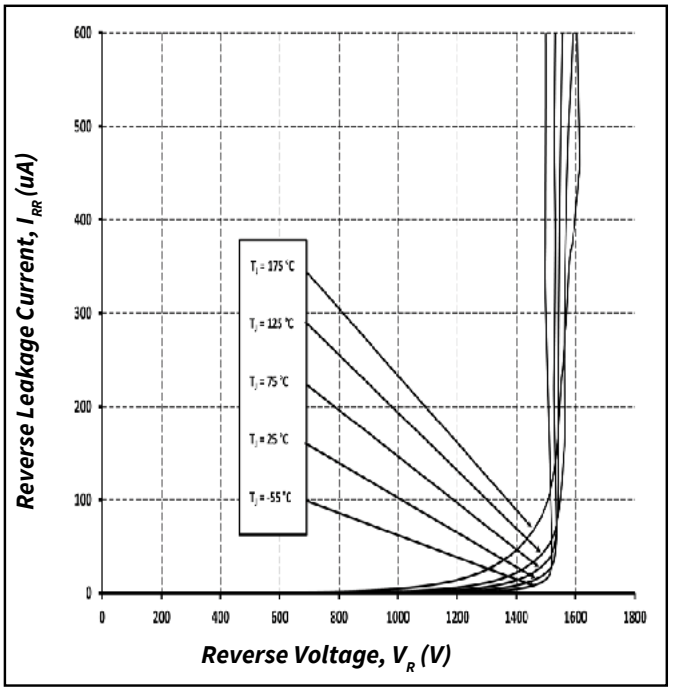


Figure 2. Reverse Characteristics

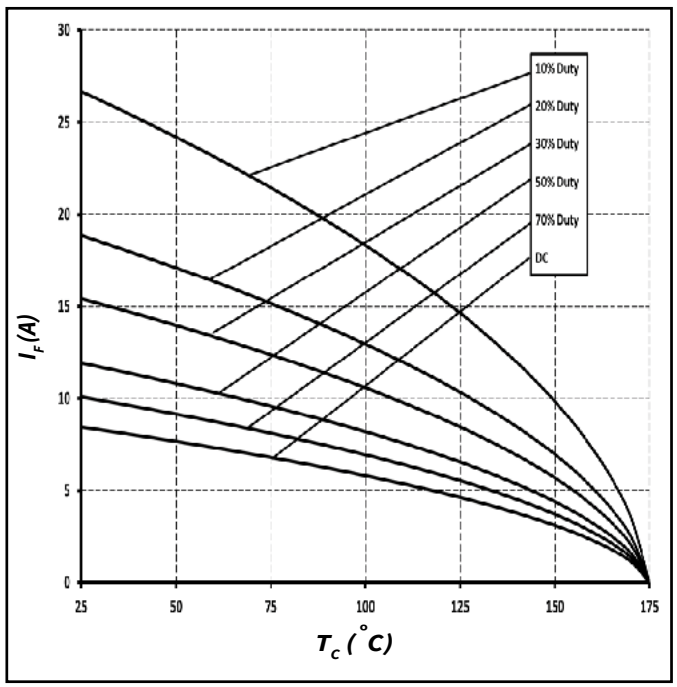


Figure 3. Current Derating

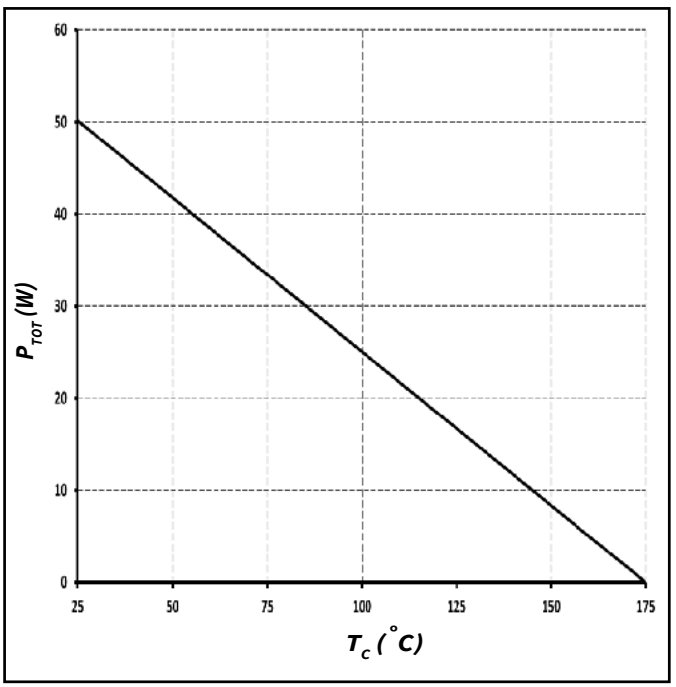


Figure 4. Power Derating

Typical Performance

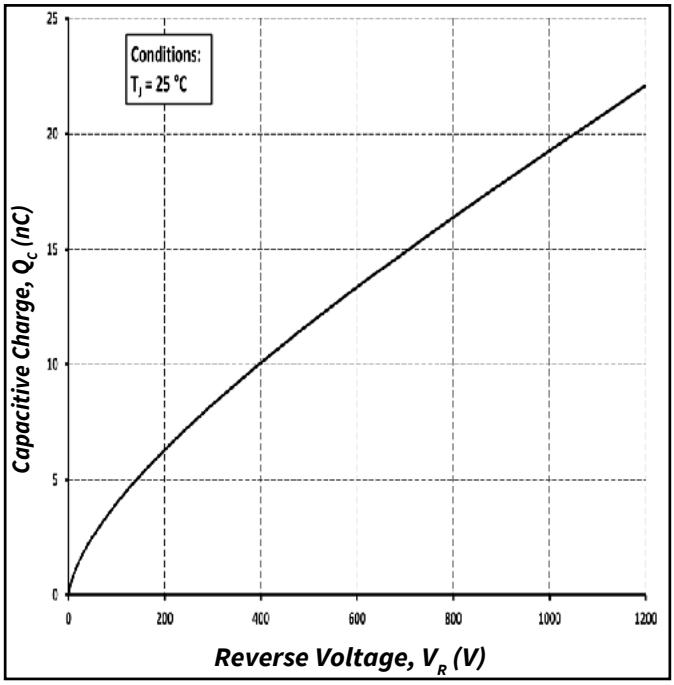


Figure 5. Total Capacitance Charge vs. Reverse Voltage

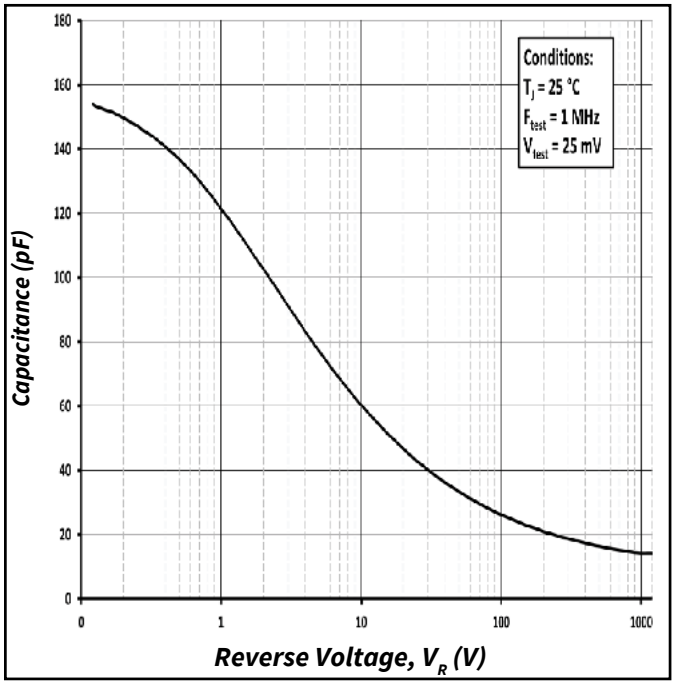


Figure 6. Capacitance vs. Reverse Voltage

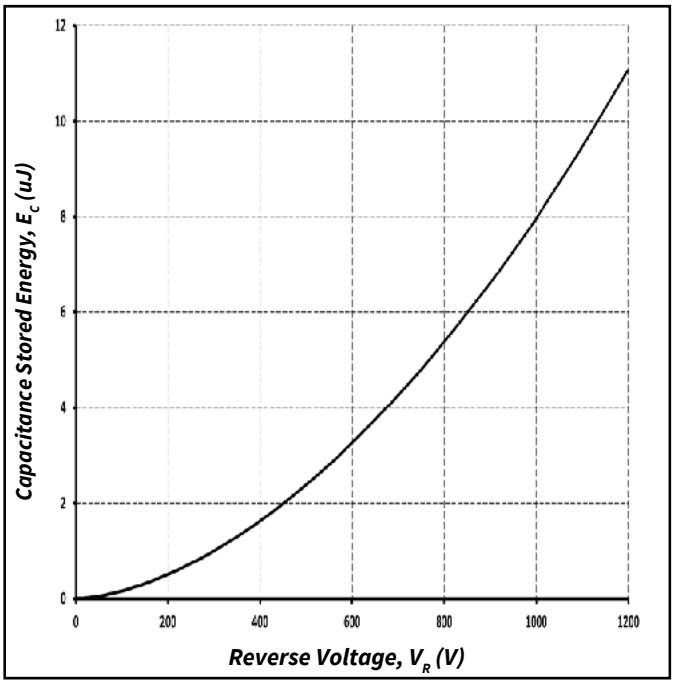


Figure 7. Capacitance Stored Energy

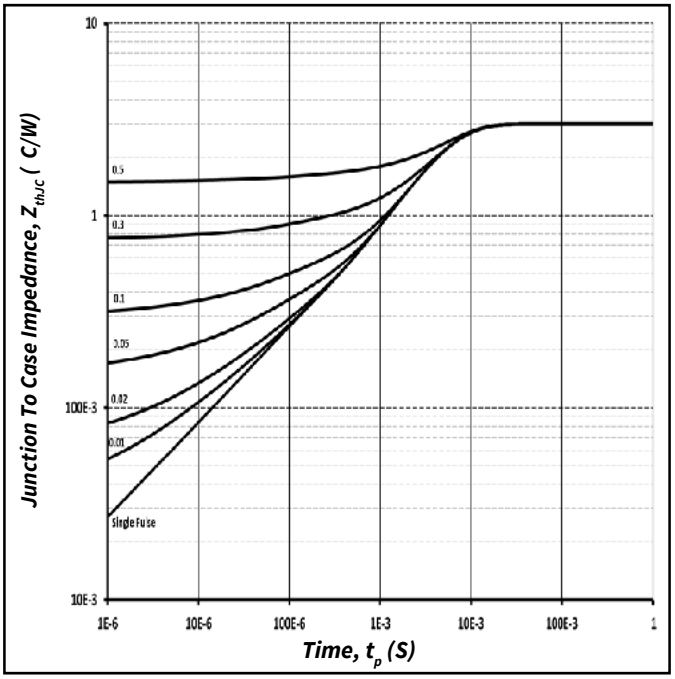
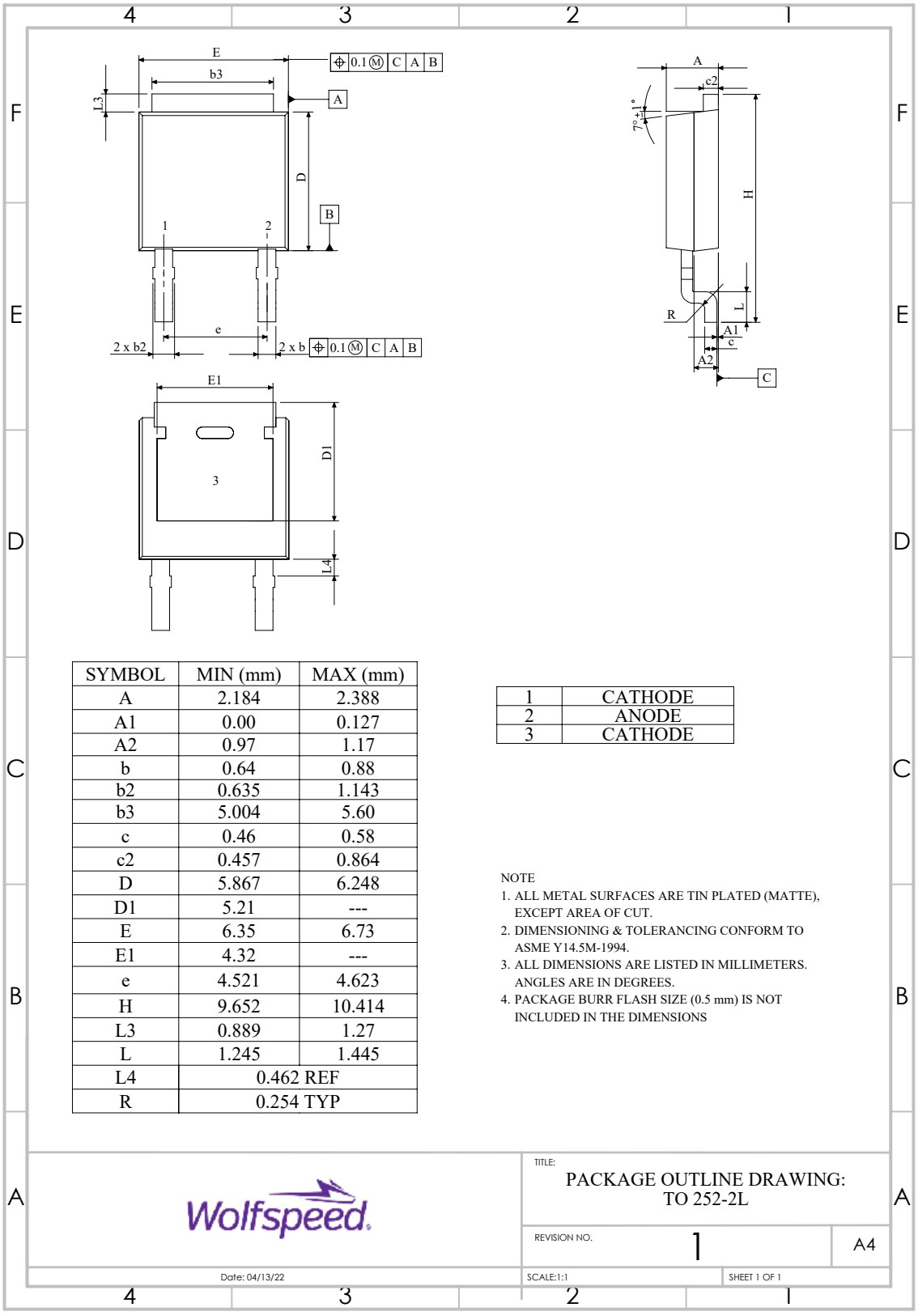


Figure 8. Transient Thermal Impedance

Package Dimensions

Package: TO-252-2



SYMBOL	MIN (mm)	MAX (mm)
A	2.184	2.388
A1	0.00	0.127
A2	0.97	1.17
b	0.64	0.88
b2	0.635	1.143
b3	5.004	5.60
c	0.46	0.58
c2	0.457	0.864
D	5.867	6.248
D1	5.21	---
E	6.35	6.73
E1	4.32	---
e	4.521	4.623
H	9.652	10.414
L3	0.889	1.27
L	1.245	1.445
L4	0.462 REF	
R	0.254 TYP	

1	CATHODE
2	ANODE
3	CATHODE

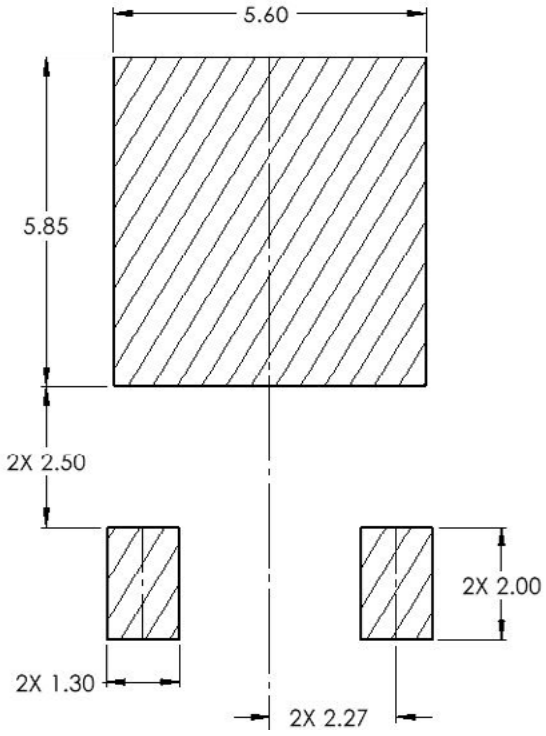
NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

TITLE: PACKAGE OUTLINE DRAWING: TO 252-2L

REVISION NO. 1 | A4

Date: 04/13/22 | SCALE:1:1 | SHEET 1 OF 1

Recommended Solder Pad Layout



Part Number	Package	Marking
E4D02120E	TO-252-2	E4D02120

Revision History

Current Revision	Date of Release	Description of Changes
0	October-2021	Initial Release
1	October-2023	Updated Wolfspeed branding, package drawing, and solder pad layout Removed max. processing temperature characteristic

Notes & Disclaimer

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