DDR Termination Regulator

General Description

The RT2568A is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT2568A possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 10μF x 3 ceramic output capacitors. The RT2568A supports remote sensing functions and all features required to power the DDRIII and Low Power DDRIII / DDRIV VTT bus termination according to the JEDEC specification. In addition, the RT2568A provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The RT2568A is available in the thermal efficient package, WDFN-10L 3x3.

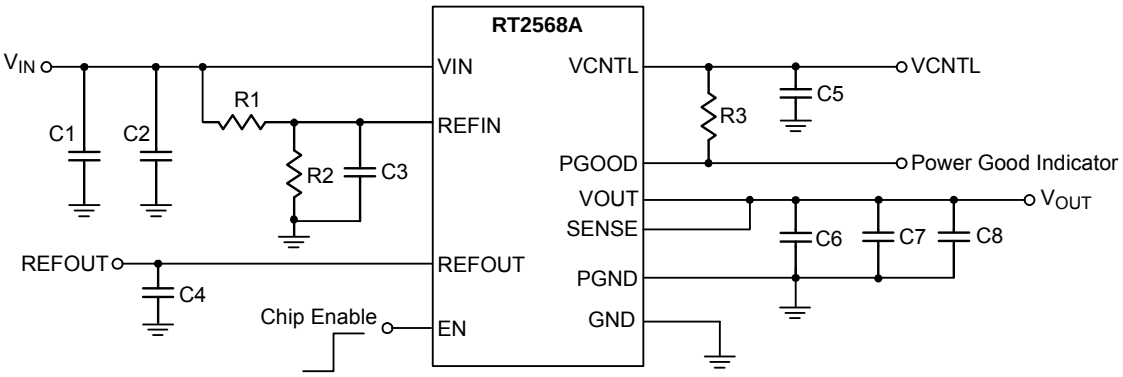
Features

- **VIN Input Voltage Range : 1.1V to 3.5V**
- **VCNTL Input Voltage Range : 2.9V to 5.5V**
- **Support Ceramic Capacitors**
- **Power Good Indicator**
- **10mA Source/Sink Reference Output**
- **Meet DDRI, DDRII JEDEC Spec**
- **Supports DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT Applications**
- **Soft-Start Function**
- **UVLO and OCP Protection**
- **Thermal Shutdown**

Applications

- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

Simplified Application Circuit



Ordering Information

RT2568A □□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

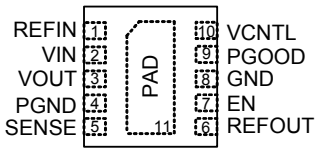
***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

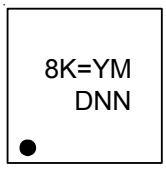
Pin Configuration

(TOP VIEW)



WDFN-10L 3x3

Marking Information



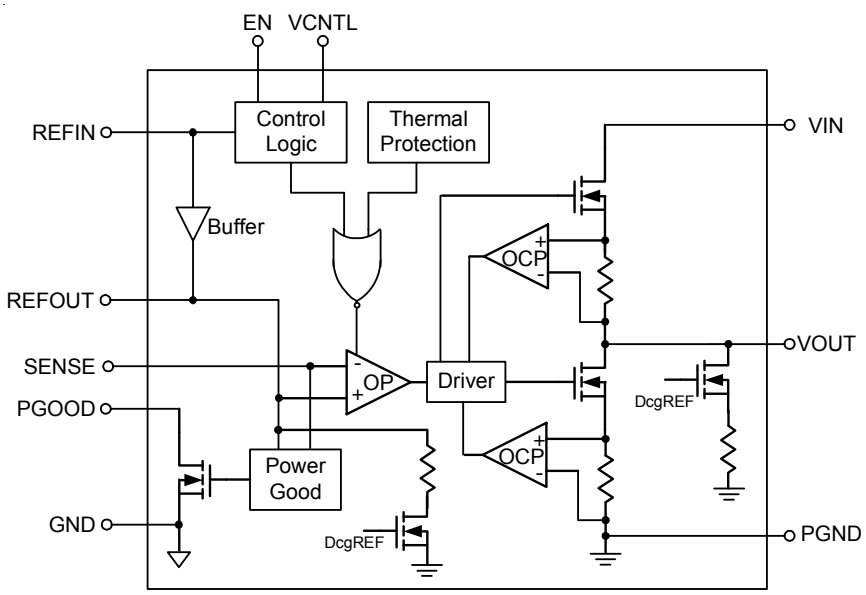
8K= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	REFIN	Reference input.
2	VIN	Power input of the regulator.
3	VOUT	Power output of the regulator.
4	PGND	Power ground of the regulator.
5	SENSE	Voltage sense input for the regulator. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	Reference output. Connect to GND through a 0.1μF ceramic capacitor.
7	EN	Enable control input. Control the device ON/OFF function.
9	PGOOD	Power good open-drain output. Connect a pull-up resistor between this pin and VCNTL pin.
10	VCNTL	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A ceramic decoupling capacitor with value range from 1μF to 4.7μF is suggested.
8	GND	Analog ground. Connect to negative terminal of the output capacitor.
11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

Functional Block Diagram



Operation

The RT2568A is a linear sink/source DDR termination regulator with current capability up to 3A. The RT2568A builds in a high-side N-MOSFET which provides current sourcing and a low-side N-MOSFET which provides current sinking. All the control circuits are supplied by the power VCNTL. In normal operation, the error amplifier OP adjusts the gate driving voltage of the power MOSFET to achieve SENSE voltage well tracking the REFIN voltage.

Buffer

This function provides REFOUT output which is equal to V_{REFIN} with 10mA source/sink current capability.

Power Good

When the SENSE voltage is in the power good window and lasts for a certain delay time, then the PGOOD pin will be high impedance and the PGOOD voltage will be pulled high by the external resistor.

Over-Current Protection

The device continuously monitors the output current to protect the pass transistor against abnormal operations. Both the source and sink currents are detected by the internal sensing resistor, and the OCP function will work to limit the current to a designed value when overload happens.

Control Logic

This block includes VCNTL UVLO, REFIN UVLO and Enable/Disable functions, and provides logic control to the whole chip.

Thermal Protection

Both the high-side and low-side power MOSFETs will be turned off when the junction temperature is higher than typically 160°C.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN, VCNTL ---------- –0.3V to 6V
- Input Voltage, EN, REFIN, SENSE ---------- –0.3V to 6V
- Output Voltage, VOUT, REFOUT, PGOOD ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 3x3 ---------- 3.27W
- Package Thermal Resistance (Note 2)
  WDFN-10L 3x3, θ_{JA} ---------- 30.5°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Control Input Voltage, VCNTL ---------- 2.9V to 5.5V
- Supply Input Voltage, VIN ---------- 1.1V to 3.5V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 1.5V, V_{EN} = V_{CNTL} = 3.3V, V_{REFIN} = V_{SENSE} = 0.75V, C_{OUT} = 10µF x 3, T_A = –40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCNTL Supply Current	I_{VCNTL}	V_{EN} = V_{CNTL}, no load	--	0.7	1	mA
VCNTL Shutdown Current	I_{SHDN_VCNTL}	V_{EN} = 0V, V_{REFIN} = 0V, no load	--	65	80	µA
		V_{EN} = 0V, V_{REFIN} > 0.4V, no load	--	200	400	
VIN Supply Current	I_{VIN}	V_{EN} = V_{CNTL}, no load	--	1	50	µA
VIN Shutdown Current	I_{SHDN_VIN}	V_{EN} = 0V, no load	--	0.1	50	µA
Output						
VTT Output Voltage	V_{OUTO}	V_{IN} = 1.5V, V_{REFIN} = 0.75V, I_{OUT} = 0A	--	0.75	--	V
		V_{IN} = 1.35V, V_{REFIN} = 0.675V, I_{OUT} = 0A	--	0.675	--	
		V_{IN} = 1.2V, V_{REFIN} = 0.6V, I_{OUT} = 0A	--	0.6	--	
VTT Output Voltage Offset	V_{OUT_OS}	I_{OUT} < ±2A, V_{LDOIN} = 1.5V, V_{OUT_OS} = V_{OUT} – V_{OUTO}	–25	--	25	mV
		I_{OUT} < ±2A, V_{LDOIN} = 1.35V, V_{OUT_OS} = V_{OUT} – V_{OUTO}	–25	--	25	
		I_{OUT} < ±2A, V_{LDOIN} = 1.2V, V_{OUT_OS} = V_{OUT} – V_{OUTO}	–25	--	25	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Source Current Limit	$I_{LIM\_VOUT\_SR}$	VOUT in PGOOD window	3	4.5	--	A
VOUT Sink Current Limit	$I_{LIM\_VOUT\_SK}$	VOUT in PGOOD window	3	4.5	--	A
VOUT Discharge Resistance	$R_{DISCHARGE}$	V_{REFIN} = 0V, V_{OUT} = 0.3V, V_{EN} = 0V	--	18	25	Ω
Power Good Comparator						
PGOOD Threshold	V_{TH_PGOOD}	V_{SENSE} lower threshold with respect to REFOUT	--	–20	--	%
		V_{SENSE} upper threshold with respect to REFOUT	--	20	--	
		PGOOD hysteresis	--	5	--	
PGOOD Start-Up Delay	$T_{PGDELAY1}$	Start-up rising delay, V_{SENSE} within PGOOD range	--	2	--	ms
Output Low Voltage	V_{LOW_PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
PGOOD Falling Delay	$T_{PGDELAY2}$	Falling delay, V_{SENSE} is out of PGOOD range	--	10	--	μs
Leakage Current	$I_{LEAKAGE\_PGOOD}$	V_{SENSE} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{CNTL} + 0.2V	--	--	1	μA
REFIN and REFOUT						
REFIN Input Current	I_{REFIN}	V_{EN} = V_{CNTL}	--	--	1	μA
REFIN Voltage Range	V_{REFIN}		0.5	--	1.8	V
REFIN Under-Voltage Lockout	V_{UVLO_REFIN}	REFIN rising	360	390	420	mV
		Hysteresis	--	20	--	
REFOUT Voltage Tolerance to VREFIN	V_{TOL_REFOUT}	–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.75V	–15	--	15	mV
		–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.675V	–13.5	--	13.5	
		–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.6V	–12	--	12	
REFOUT Source Current Limit	$I_{LIM\_REFOUT\_SR}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit	$I_{LIM\_REFOUT\_SK}$	V_{REFOUT} = REFIN + 1V	10	40	--	mA
UVLO/EN						
UVLO Threshold	V_{UVLO_VCNTL}	Rising	2.5	2.7	2.85	V
		Hysteresis	--	120	--	mV
EN Input Voltage Logic-High	V_{IN_H}		1.7	--	--	V
EN Input Voltage Logic-Low	V_{IN_L}		--	--	0.3	
EN Turn On Delay	t_{DELAY}	EN is turned on to VOUT rising T_A = 25°C (reference Note 5)	--	--	7	μs
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	Shutdown temperature (Note 5)	--	160	--	°C
		Hysteresis (Note 6)	--	15	--	

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

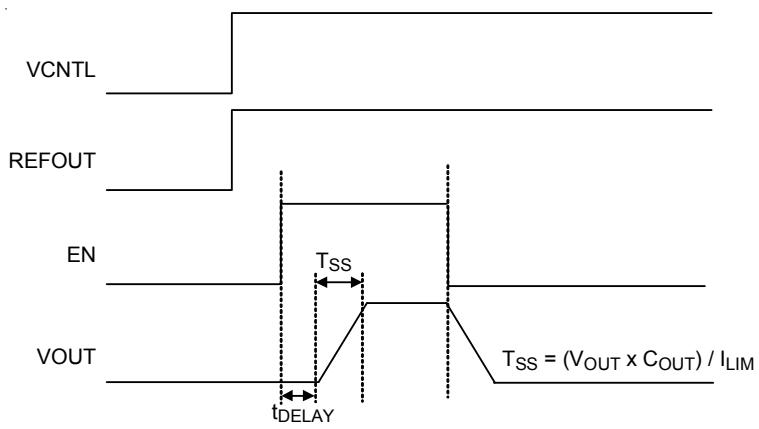
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. t_{DELAY} is the maximum period form EN turn on to V_{OUT} rising period as follows diagram. While T_{SS} is the rising period of V_{OUT}, the formula used to calculated this rising period is $T_{SS} = (V_{OUT} \times C_{OUT})/I_{LIM}$, it's base on the value of output capacitor C_{OUT}, the settled output voltage V_{OUT} and the output current limit I_{LIM}.

Note 6. Guarantee by design.



Typical Application Circuit

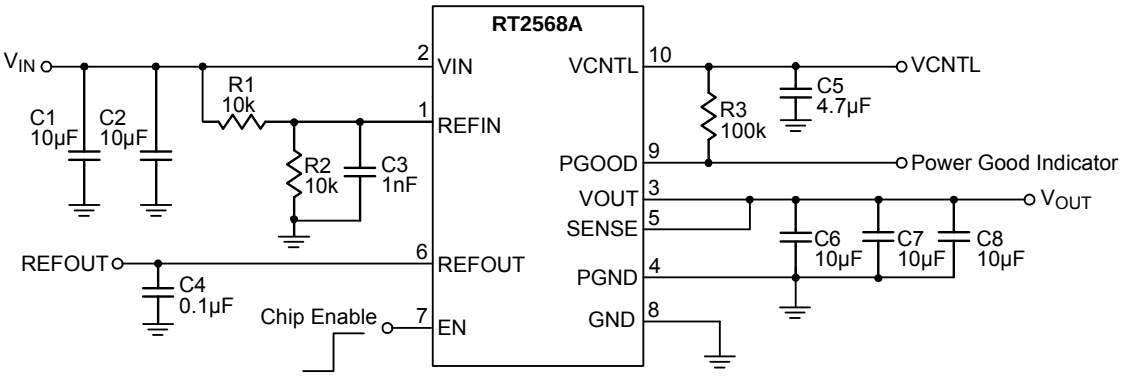
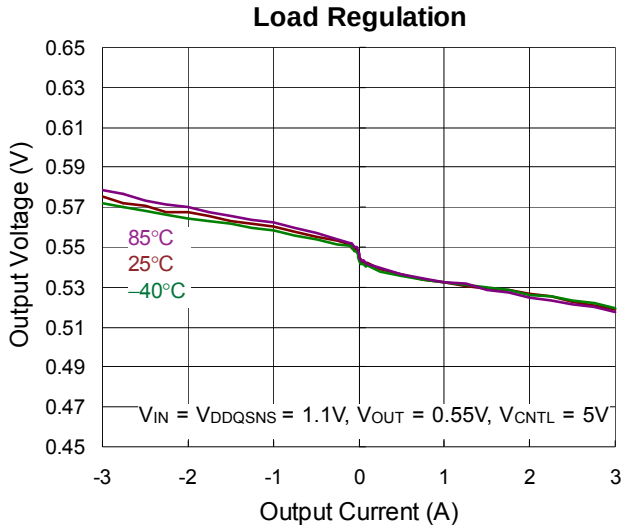
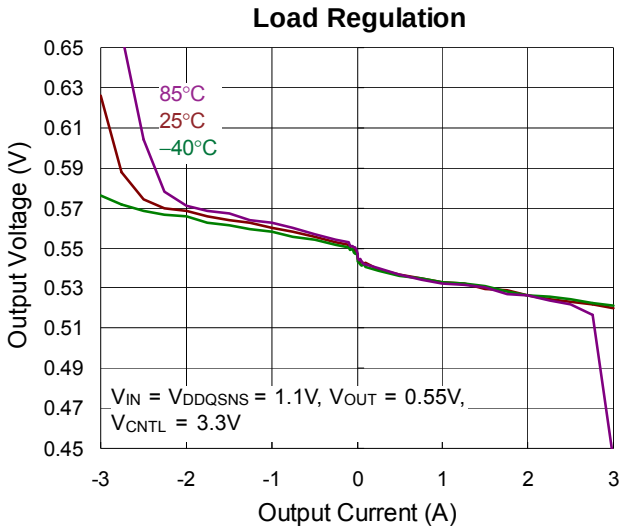


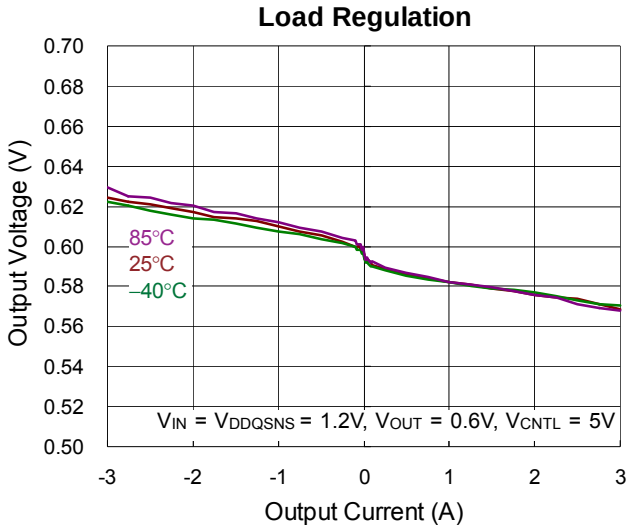
Table 1. Recommended External Components

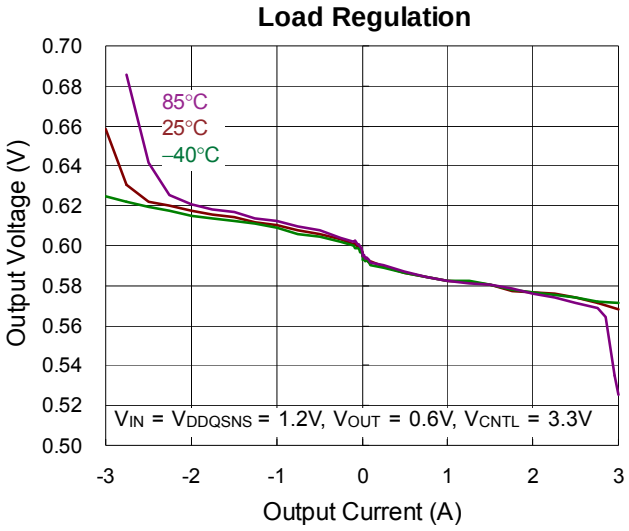
Component	Description	Vendor P/N
C1, C2, C6, C7, C8	10µF, 6.3V, X7R, 0805	GRM21BR70J106KE76L (Murata) CGA4J1X7R0J106K125AC (TDK)
C3	1nF, 50V, X7R, 0603	GCD188R71H102KA01D (Murata) CGA3E2X7R1H102K080AA (TDK)
C4	0.1µF, 16V, X7R, 0603	GCJ188R71C104KA01D (Murata)
C5	4.7µF, 6.3V, X5R, 0603	GRT188R60J475ME01D (Murata) CGB3B3X5R0J475M055AB(TDK)

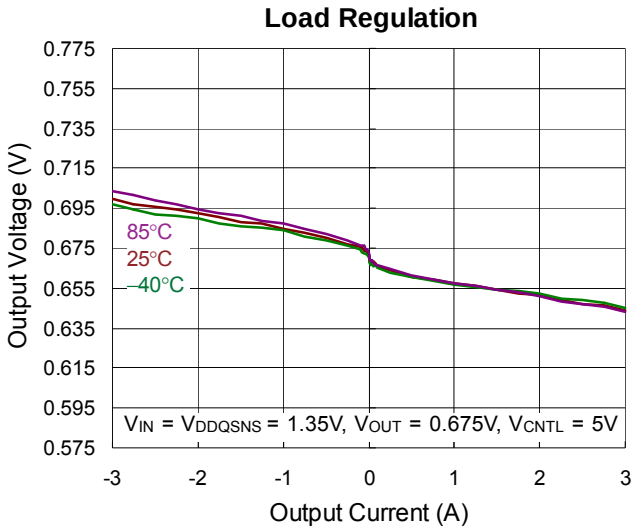
Typical Operating Characteristics

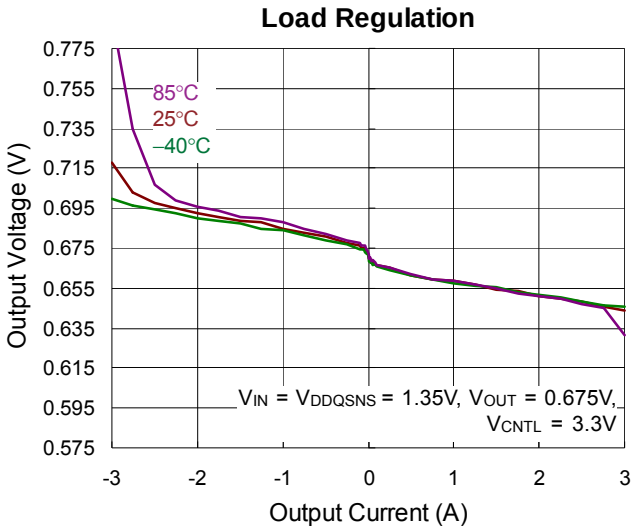




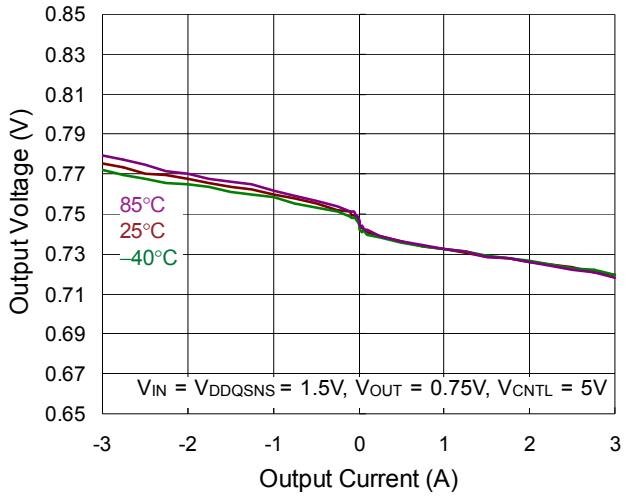








Load Regulation



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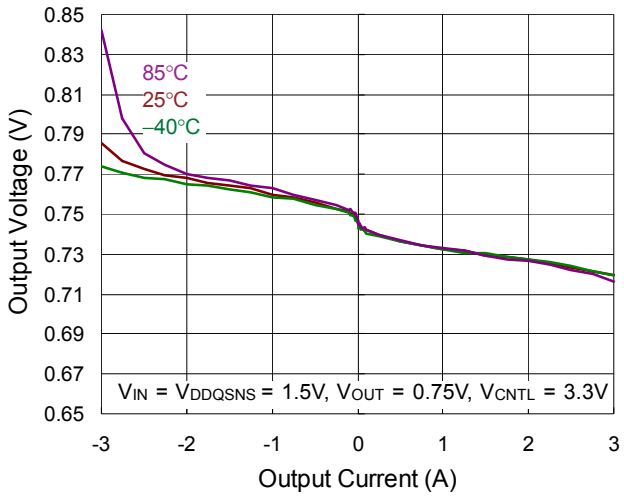

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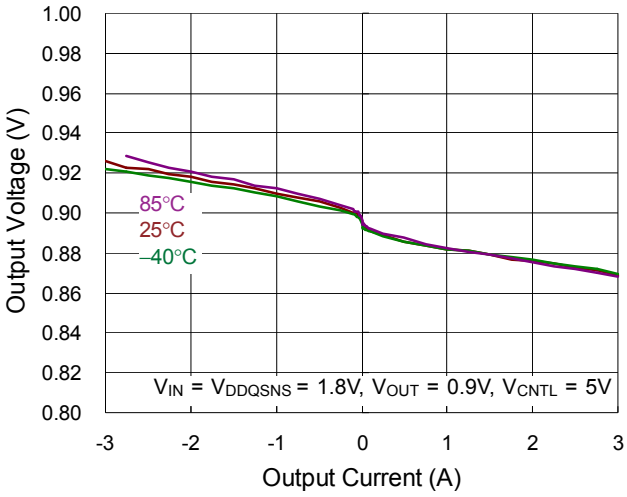

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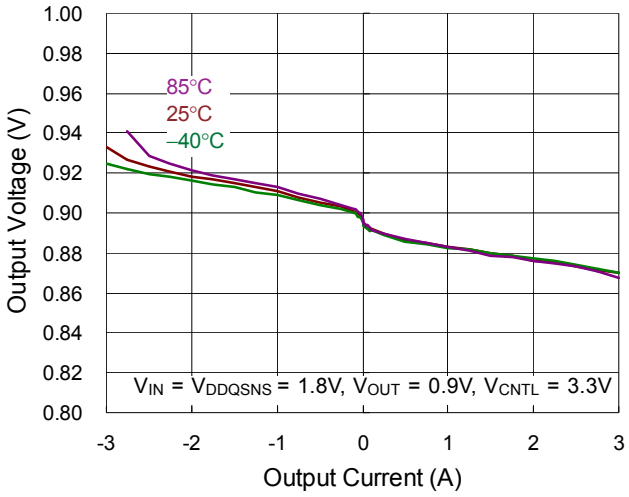

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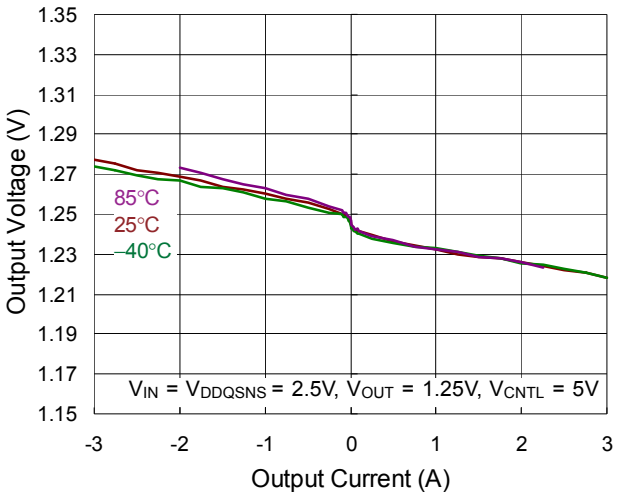
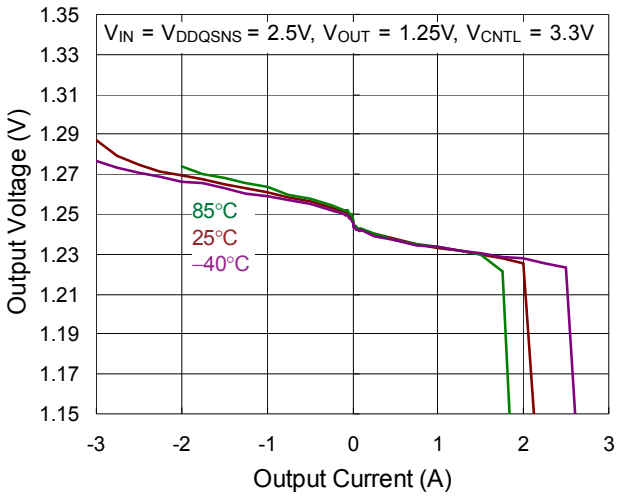
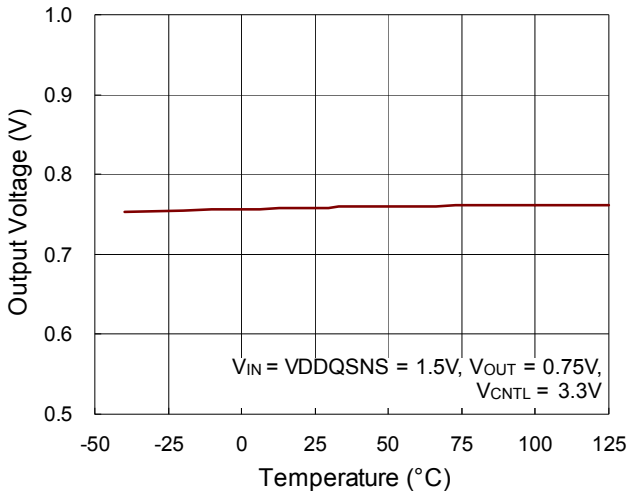


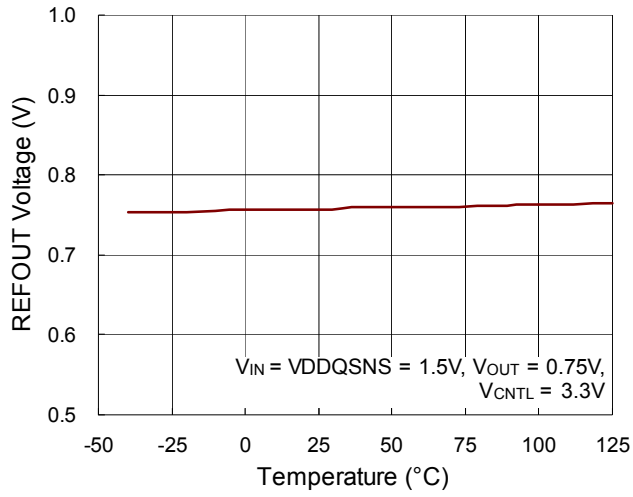
Load Regulation



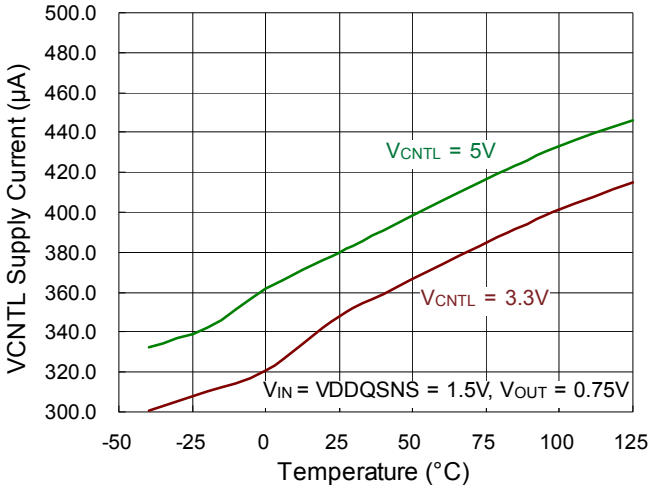
Output Voltage vs. Temperature



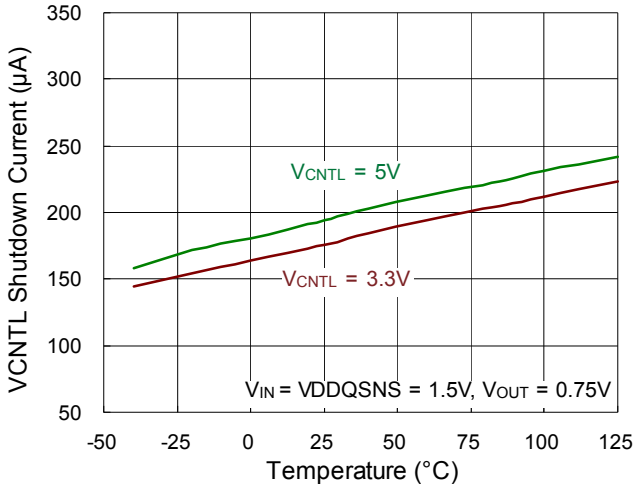
REFOUT Voltage vs. Temperature



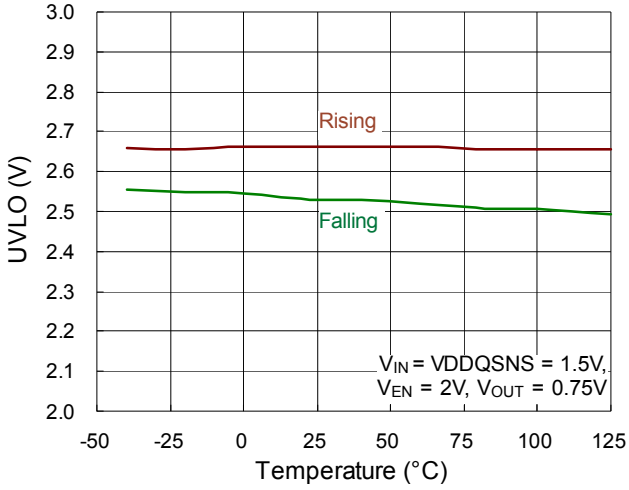
VCNTL Supply Current vs. Temperature



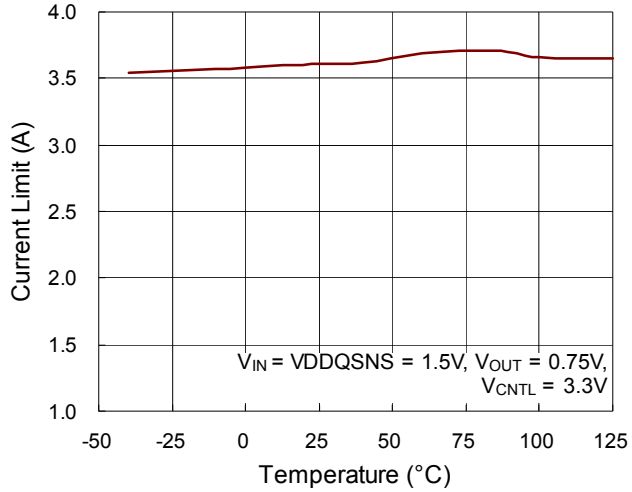
VCNTL Shutdown Current vs. Temperature



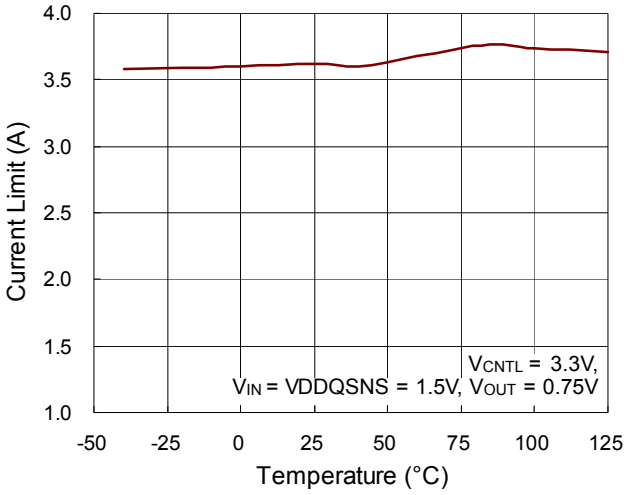
UVLO vs. Temperature



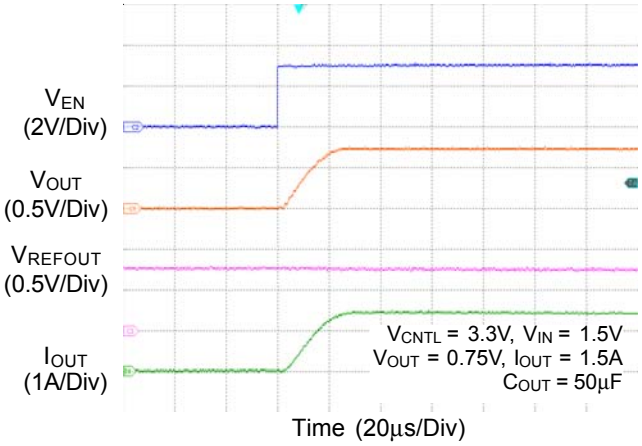
Sourcing Current Limit vs. Temperature



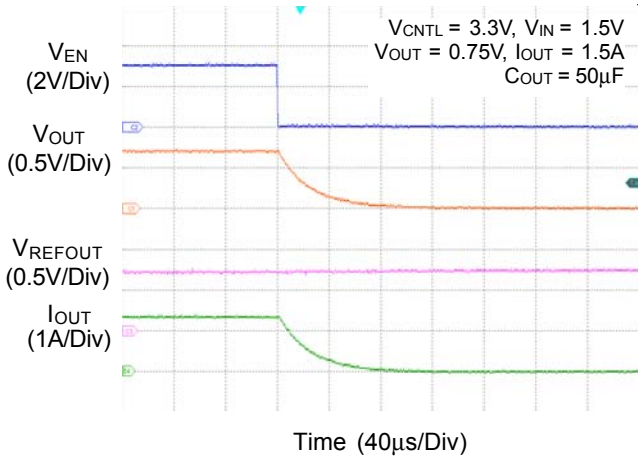
Sinking Current Limit vs. Temperature



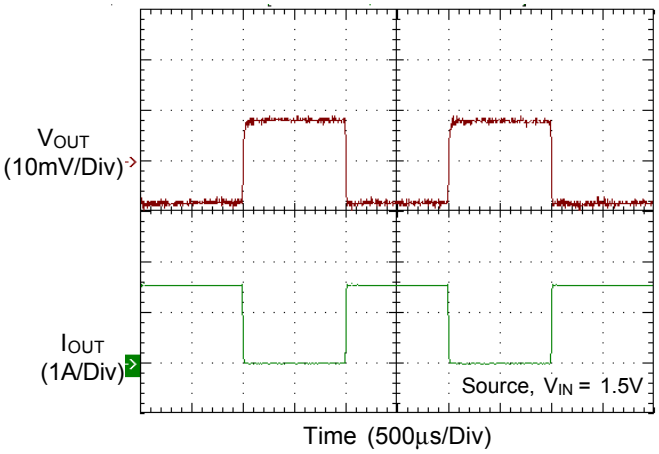
Power On from EN



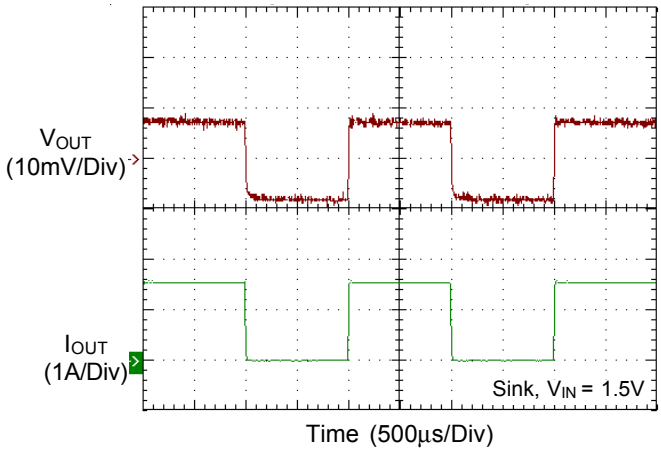
Power Off from EN



0.75V_{OUT} @ 1.5A Transient Response



0.75V_{OUT} @ 1.5A Transient Response



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT2568A is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count system such as notebook PC applications. The RT2568A possesses a high speed operating amplifier that provides fast load transient response and only requires two 10μF ceramic input capacitors and three 10μF ceramic output capacitors.

Capacitor Selection

Good bypassing is recommended from VIN to GND to help improve AC performance. A 10μF or greater input capacitor located as close as possible to the IC is recommended. The input capacitor must be located at a distance of less than 0.5 inches from the VIN pin of the IC.

The 1μF ceramic capacitor added close to the VCNTL pin should be kept away from any parasitic impedance from the supply power. For stable operation, the total capacitance of the ceramic capacitor at the VTT output terminal must be larger than 30μF. The RT2568A is designed specifically to work with low ESR ceramic output capacitor in space saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. The output capacitor should be located near the VTT output terminal pin as close as possible.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 3.27W for a WDFN-10L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

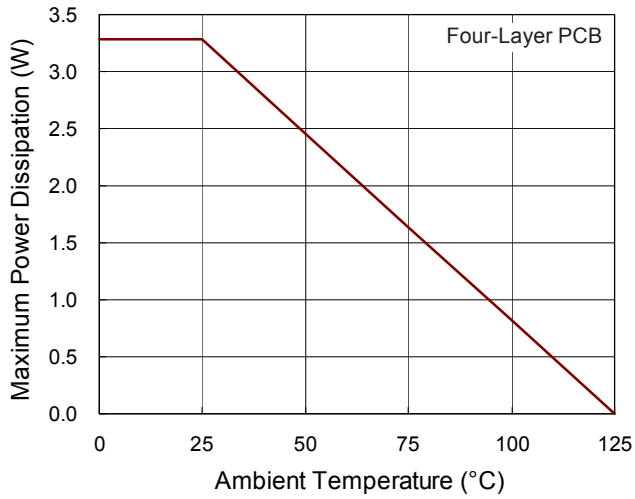


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT2568A, the PCB layout suggestions below are highly recommend :

- With wide and short connection plane between capacitors and pins for trace impedance minimization.
- The ground plane connected by a wide copper surface for good thermal dissipation, add via connection also helps reduce the GND loop trace.
- Connect the SENSE pin to the positive node of output capacitor at V_{OUT} terminal for output target level remote sensing.
- Since the output voltage V_{OUT} setting follows the REFIN pin input voltage level V_{REFIN} (V_{OUT} = V_{REFIN}), the REFIN pin can connected with independent voltage source for stable input signal and good V_{OUT} target accuracy. For the application which V_{REFIN} sinks the voltage source divided from VIN power trace, with separate connection trace between R1 and VIN terminal side not only makes sure the V_{REFIN} signal stability, but also avoids the reference voltage level shrink down caused by V_{IN} trace loss at high load operation.

Figure 2 shows an example for the layout reference that reduces conduction trace loop, helping minimize inductive parasitic minimize reduce, load transient, and increase circuit stability.

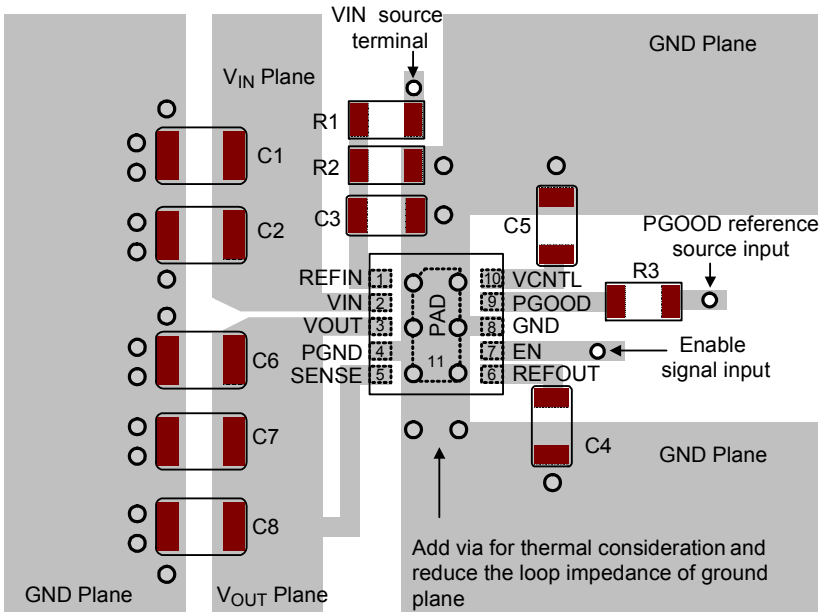
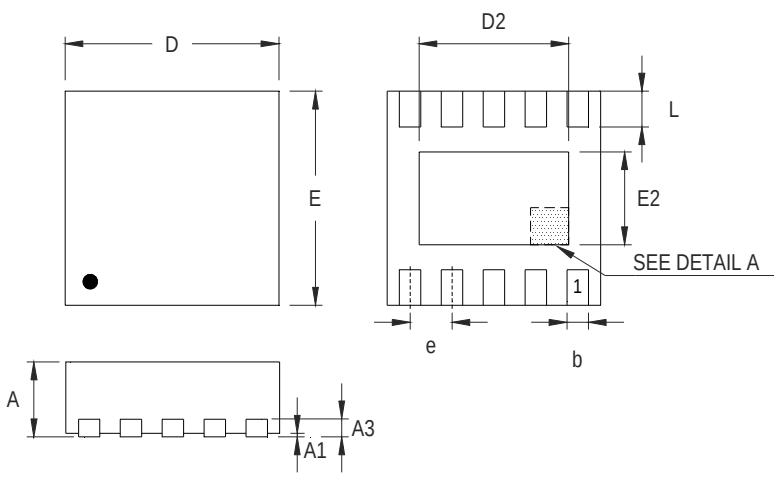
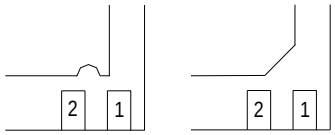


Figure 2. PCB Layout Guide

Outline Dimension





DETAIL A

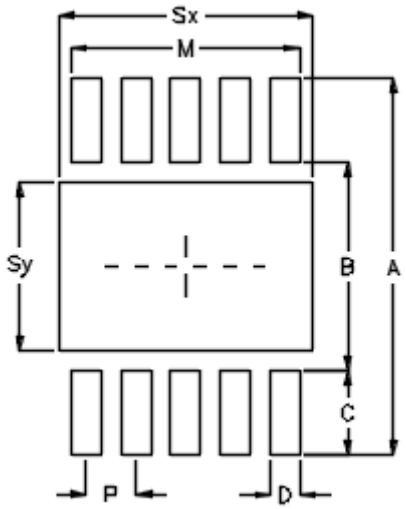
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

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Datasheet Revision History

Version	Date	Description	Item
02	2023/5/23	Modify	Features on P1 Electrical Characteristics on P5 Application Information on P12

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