

Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Bvdss

-40V

Rdson

10mΩ

ID

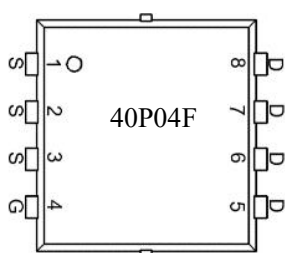
-40A

Application

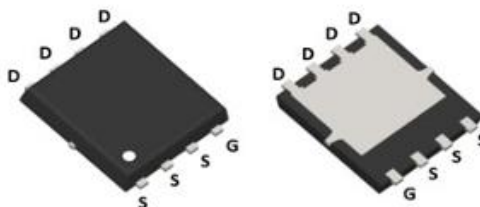
- PWM applications
- Power management functions
- Synchronous-rectification applications

RoHS

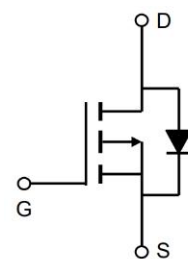
Package



Marking and pin assignment



PDFN5*6-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
40P04	40P04F	PDFN5*6-8L	5000

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-40	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ¹	I _D	-40	A
Continuous Drain Current ¹	I _D	-25	A
Pulsed Drain Current ²	I _{DM}	-160	A
Single Pulsed Avalanche Energy ³	E _{AS}	144	mJ
Avalanche Current	I _{AS}	-30	A
Power Dissipation ⁴	P _d	45	W
Junction Temperature	T _J	-55~+150	°C
Storage Temperature	T _{STG}	-55~+150	°C



Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Case ¹	$R_{\theta JC}$	--	3.6	°C/W
Thermal Resistance, Junction-to-Ambient ¹	$R_{\theta JA}$	--	62	°C/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL40P04F	PDFN5*6	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V _{DSS}	V _{GS} =0V I _D =-250μA	-40	-	-	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	-1	μA
Gate- Source Forward Leakage	I _{GSS (F)}	V _{GS} =+20V	-	-	100	nA
Gate- Source Reverse Leakage	I _{GSS (R)}	V _{GS} =-20V	-	-	-100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.7	-2.5	V
Drain-Source On-State Resistance ³	R _{DS(ON)}	V _{GS} =-10V, I _D =-20A	-	10	13	mΩ
		V _{GS} =-4.5V, I _D =-10A	-	14	17	
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V, F=1.0MHz	-	3800	-	pF
Output Capacitance	C _{oss}		-	329	-	pF
Reverse Transfer Capacitance	C _{rss}		-	289	-	pF
Resistive Switching Characteristics						
Turn-on Delay Time	T _{d(on)}	V _{DD} =-20V, I _D =-20A, V _{GS} =-10V, R _{GEN} =2.4Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	82	-	nS
Turn-Off Delay Time	T _{d(off)}		-	93	-	nS
Turn-Off Fall Time	T _f		-	74	-	nS
Total Gate Charge	Q _g	V _{DS} =-20V, I _D =-20A, V _{GS} =-10V	-	68	-	nC
Gate-Source Charge	Q _{gs}		-	10	-	nC
Gate-Drain Charge	Q _{gd}		-	14	-	nC
Source-Drain Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-30A	-	-0.8	-1.2	V
Maximum Continuous Drain to Source Diode Forward Current	I _S	-	-	-	-40	A
Maximum Pulsed Drain to Source Diode Forward Current	I _{SM}		-	-	-160	A
Reverse Recovery Time	t _{rr}	V _{GS} =0V, I _S =-30A	-	20	-	nS



Reverse Recovery Charge	Q_{rr}	$di/dt = 300A/\mu s$	-	13	-	nC
-------------------------	----------	----------------------	---	----	---	----

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^\circ C$, $V_{DD} = -20V$, $V_G = -10V$, $L = 0.5mH$, $R_G = 25\Omega$, $I_{AS} = -24A$
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure 1. Output Characteristics

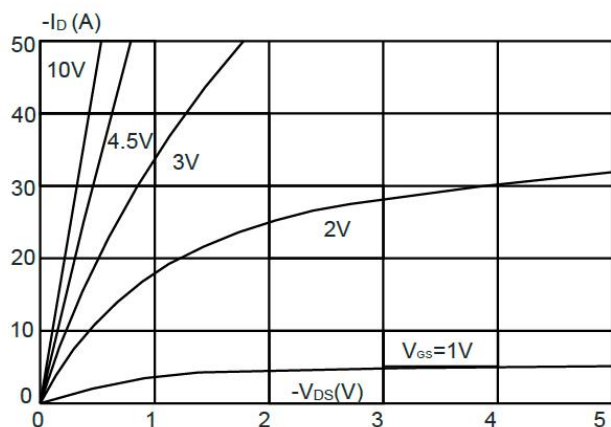


Figure 2. Typical Transfer Characteristics

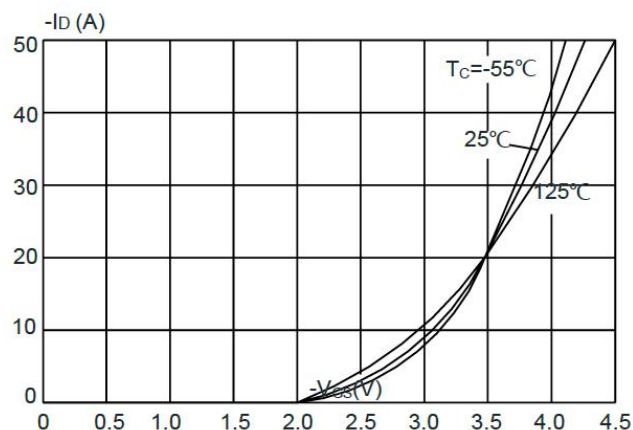


Figure 3. On-resistance vs. Drain Current

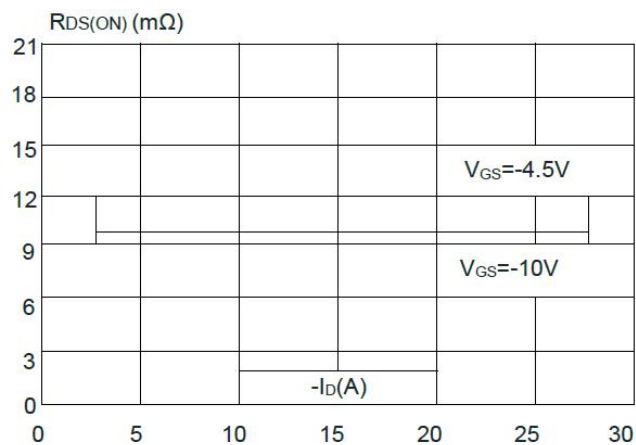


Figure 4. Body Diode Characteristics

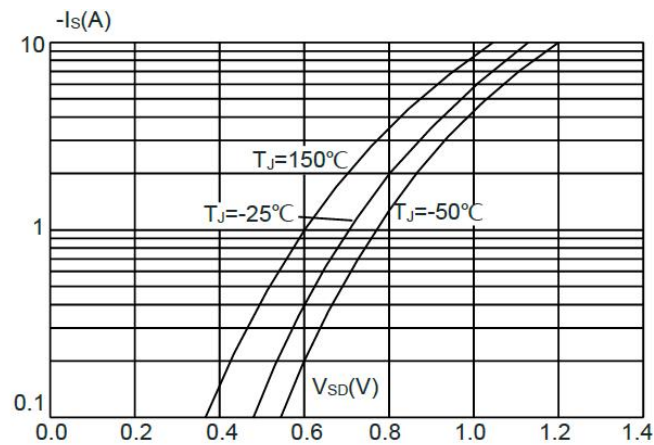


Figure 5: Gate Charge Characteristics

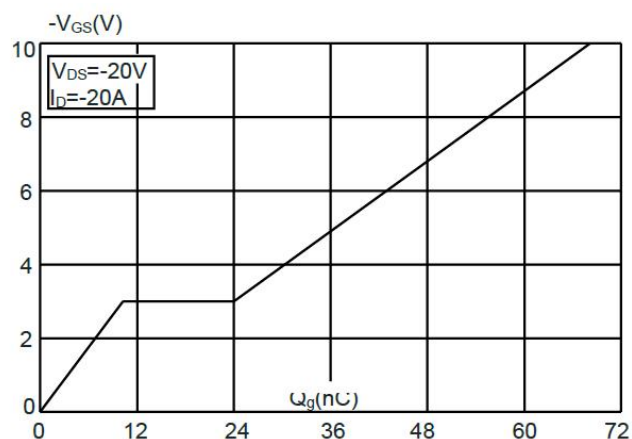


Figure 6: Capacitance Characteristics

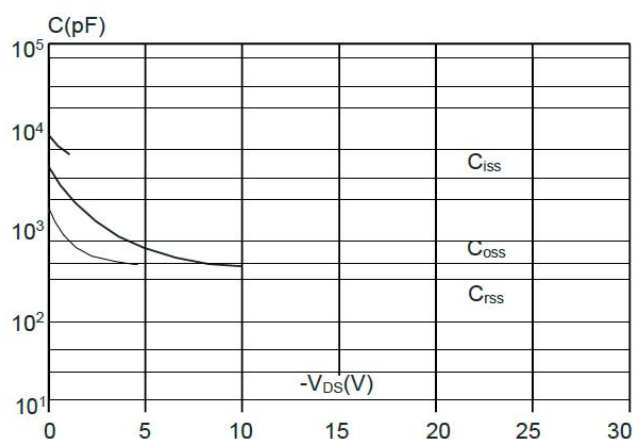


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

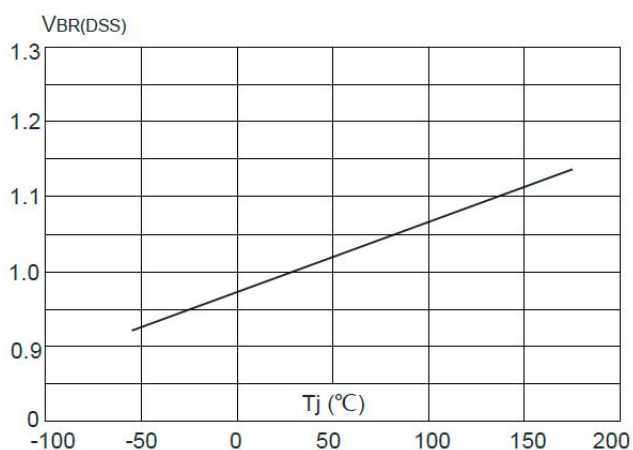


Figure 8: Normalized on Resistance vs. Junction Temperature

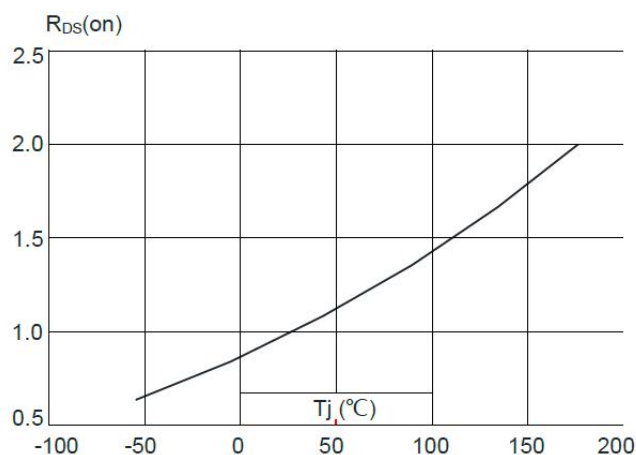


Figure 9: Maximum Safe Operating Area

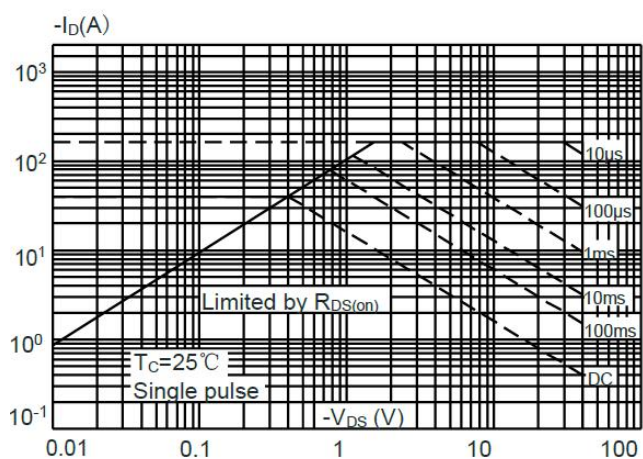


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

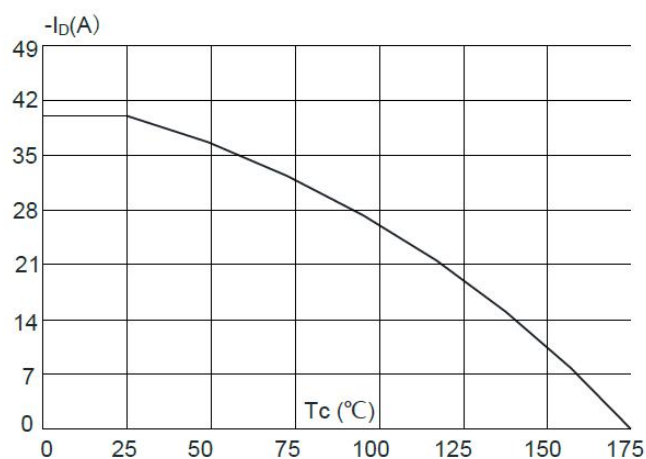
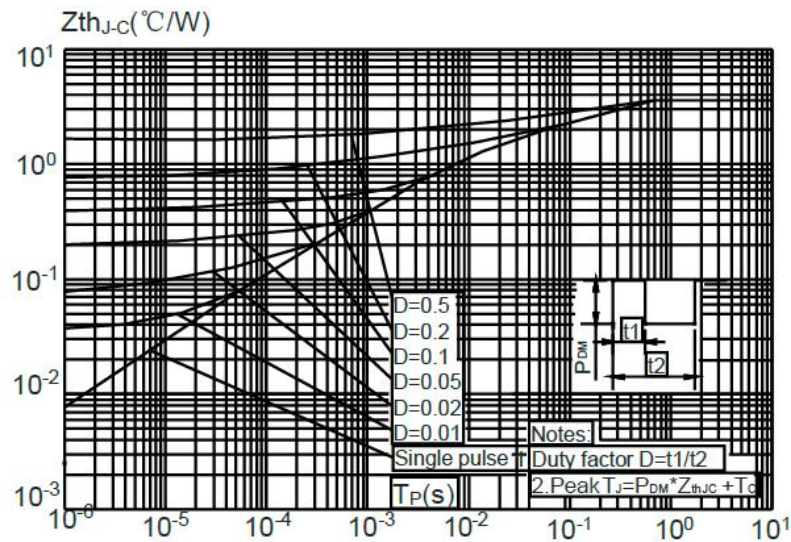


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

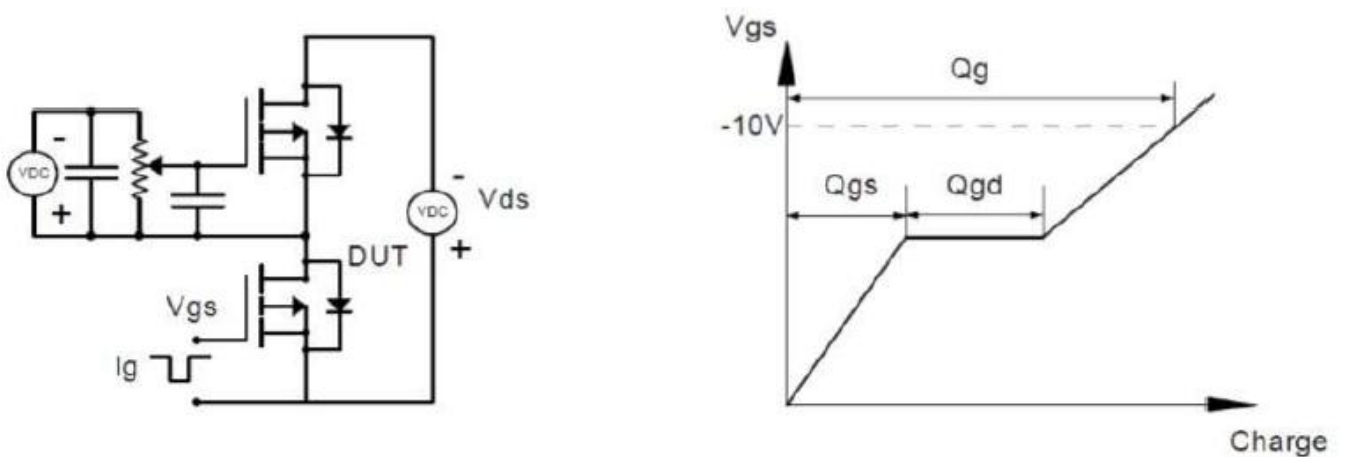


Figure.1: Gate Charge Test Circuit & Waveform

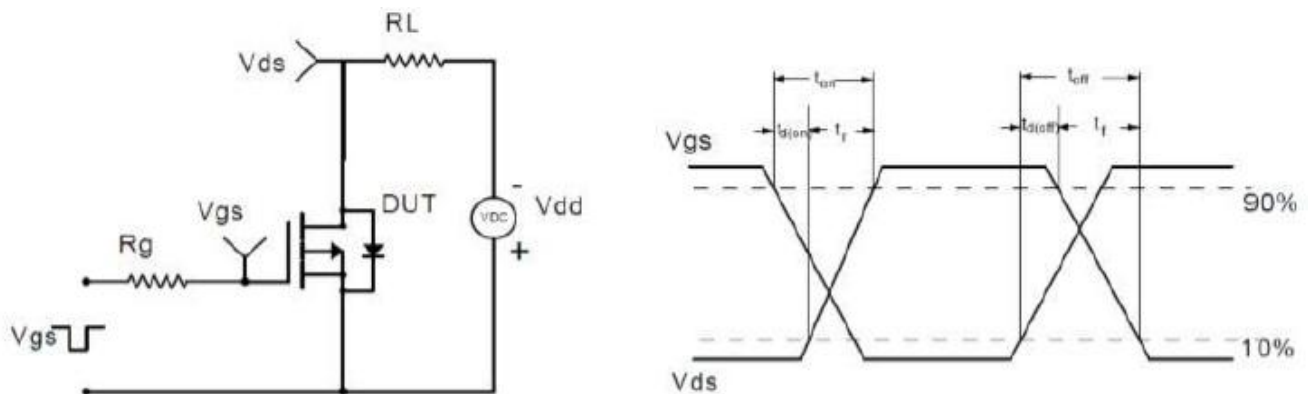


Figure.2: Resistive Switching Test Circuit & Wave forms

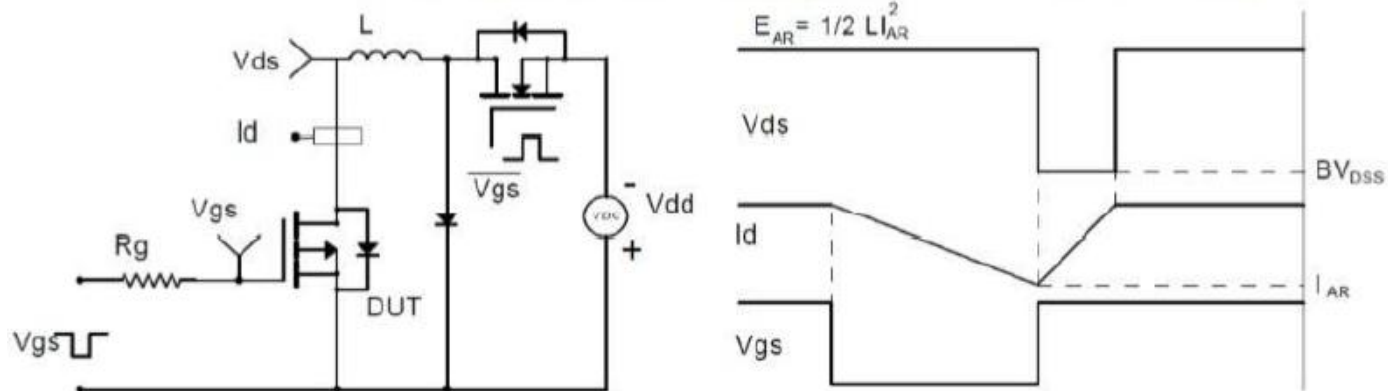


Figure.3: Unclamped inductive Switching (UIS) Test Circuit & Wave forms

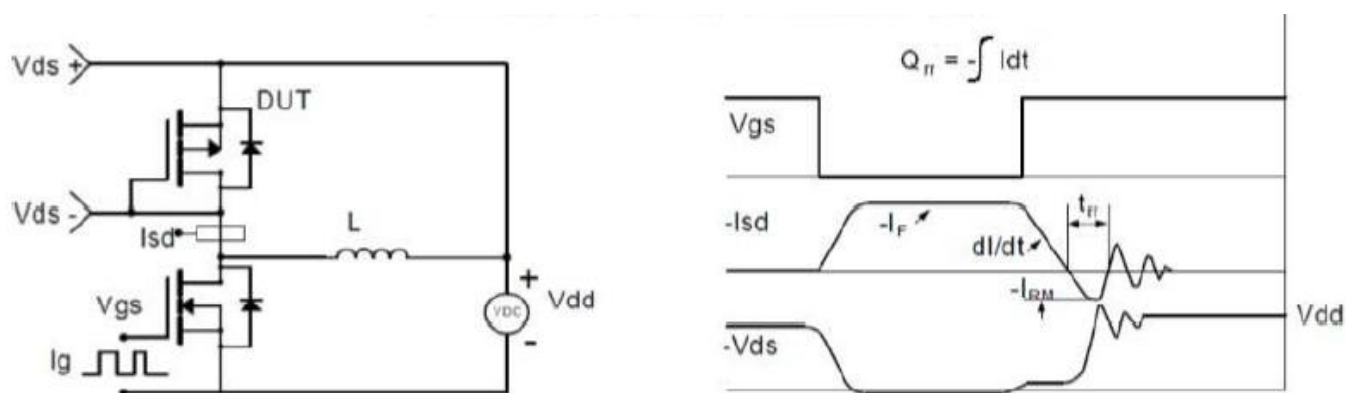
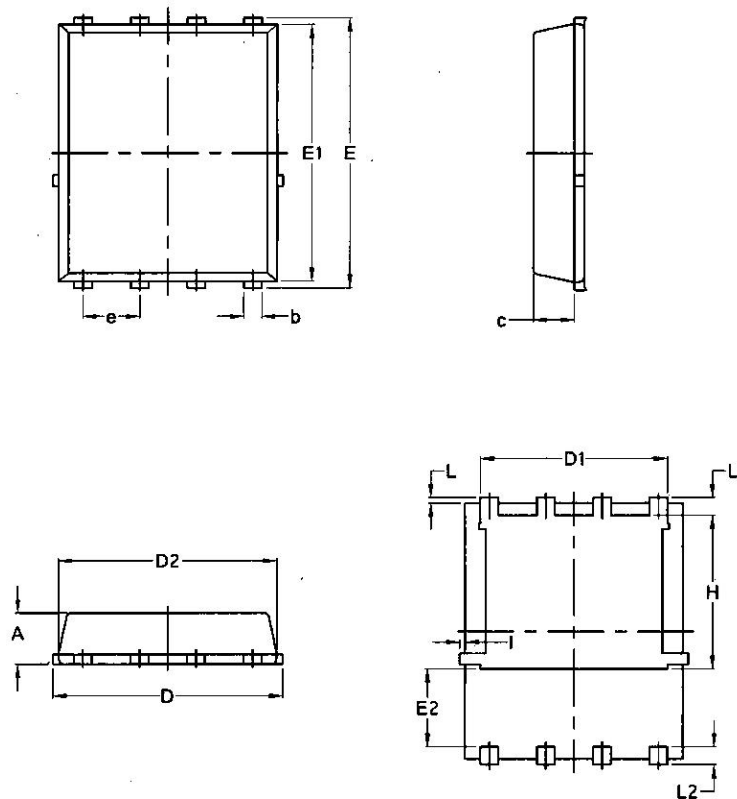


Figure.4: Diode Recovery Test Circuit & Wave form



Package Dimensions PDFN5x6-8L



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



Important Notice and Disclaimer

HL Microelectronics reserves the right to make changes to this document and its products and specifications at any time without notice.

Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

HL Microelectronics makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, not does HL Microelectronics assume any liability for application assistance or customer product design.

HL Microelectronics does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

No license is granted by implication or otherwise under any intellectual property rights of HL Microelectronics.

HL Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of HL Microelectronics.