Complete DDRII/DDRIII/Low-Power DDRIII/DDRIV/Low-Power DDRIV Memory Power Supply Controller

General Description

The RT8207P provides a complete power supply for both DDRII/DDRIII/Low-Power DDRIII/DDRIV/Low-Power DDRIV memory systems. It integrates a synchronous PWM buck controller with a 1.5A sink/source tracking linear regulator and buffered low noise reference.

The PWM controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage chipset RAM supplies in notebook computers. The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8207P achieves high efficiency at a reduced cost by eliminating the current sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The buck conversion allows this device to directly step down high voltage batteries for the highest possible efficiency.

The 1.5A sink/source LDO maintains fast transient response, only requiring 20µF of ceramic output capacitance. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The RT8207P supports all of the sleep state controls placing VTT at high-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5.

The RT8207P has all of the protection features including thermal shutdown and is available in a WQFN-20L 3x3 packages.

Applications

- DDRI/II/III/Low-Power DDRIII/DDRIV/Low-Power DDRIV Memory Power Supplies
- Notebook Computers
- SSTL18, SSTL15 and HSTL Bus Termination

Features

- **PWM Controller**
  - **Resistor Programmable Current Limit by Low Side $R_{DS(ON)}$ Sense**
  - **Quick Load Step Response within 100ns**
  - **1% V_{VDDQ} Accuracy Over Line and Load**
  - **Fixed 1.8V (DDRII), 1.5V (DDRIII) or Adjustable 0.75V to 3.3V Output Range for 1.35V (Low-Power DDRIII), 1.2V (DDRIV) and 1.1V (Low-Power DDRIV)**
  - **4.5V to 26V Battery Input Range**
  - **Resistor Programmable Frequency**
  - **Over/Under Voltage Protection**
  - **Internal Current Limit Ramp Soft-Start**
  - **Drives Large Synchronous-Rectifier FETs**
  - **Power Good Indicator**
- **1.5A LDO (VTT), Buffered Reference (VTTREF)**
  - **Capable to Sink and Source 1.5A**
  - **External Input Available to Minimize Power Losses**
  - **Integrated Divider Tracks 1/2 VDDQ for Both VTT and VTTREF**
  - **Buffered Low Noise 10mA VTTREF Output**
  - **Remote Sensing (VTTSNS)**
  - **±20mV Accuracy for Both VTTREF and VTT**
  - **Supports High-Z in S3 and Soft-Off in S4/S5**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT8207P□□

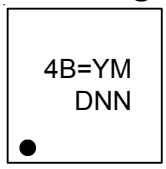
- Package Type
  QW : WQFN-20L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

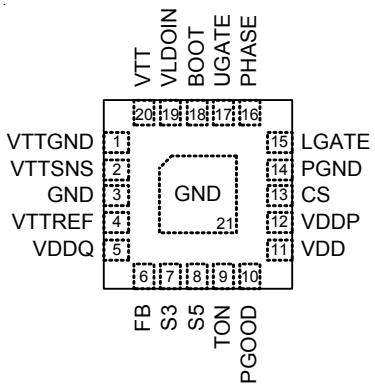


4B= : Product Code

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-20L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VTTGND	Power ground output for VTT LDO.
2	VTTSNS	Voltage sense input for VTT LDO. Connect to the terminal of the VTT LDO output capacitor.
3, 21 (Exposed Pad)	GND	Analog ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
4	VTTREF	Buffered reference output.
5	VDDQ	Reference input for VTT and VTTREF. Discharge current sinking terminal for VDDQ non-tracking discharge. Output voltage feedback input for VDDQ output if the FB pin is connected to VDD or GND.
6	FB	VDDQ output setting. Connect to GND for DDR3 (V_{VDDQ} = 1.5V) power supply. Connect to VDD for DDR2 (V_{VDDQ} = 1.8V) power supply. Or connect to a resistive voltage divider from VDDQ to GND to adjust the output of PWM from 0.75V to 3.3V.
7	S3	S3 signal input.
8	S5	S5 signal input
9	TON	Set the UGATE on time through a pull-up resistor connecting to V_{IN}.
10	PGOOD	Power good open drain output. In High state when VDDQ output voltage is within the target range.
11	VDD	Supply input for analog supply.
12	VDDP	Supply input for LGATE gate driver.
13	CS	Current limit threshold setting input. Connect to VDD through the voltage setting resistor.
14	PGND	Power ground for low side MOSFET.
15	LGATE	Low side gate driver output for VDDQ.
16	PHASE	Switch node. External inductor connection for VDDQ and behave as the current sense comparator input for Low Side MOSFET $R_{DS(ON)}$ sensing.
17	UGATE	High side gate driver output for VDDQ.
18	BOOT	Boost flying capacitor connection for VDDQ.
19	VLDOIN	Power supply for VTT LDO.
20	VTT	Power output for VTT LDO.

Typical Application Circuit

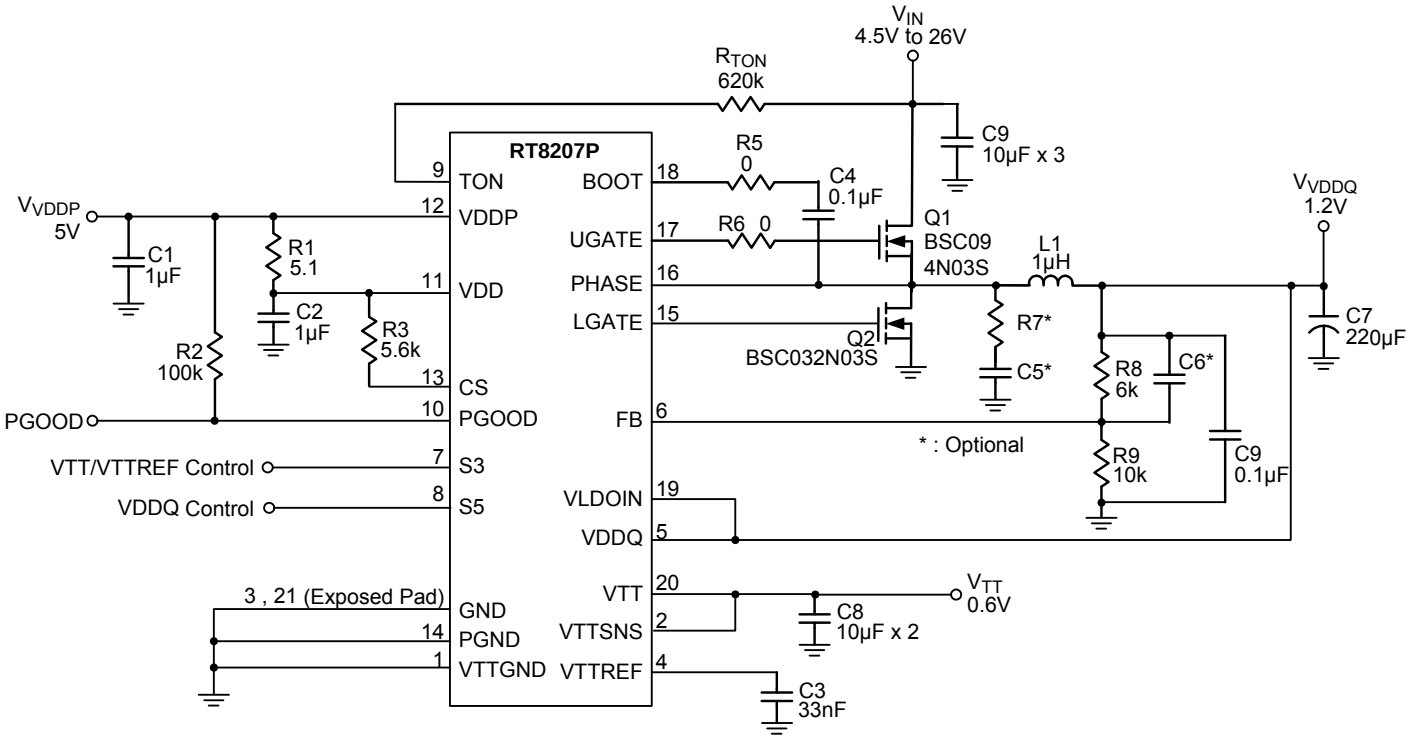


Figure 1. Adjustable Voltage Regulator

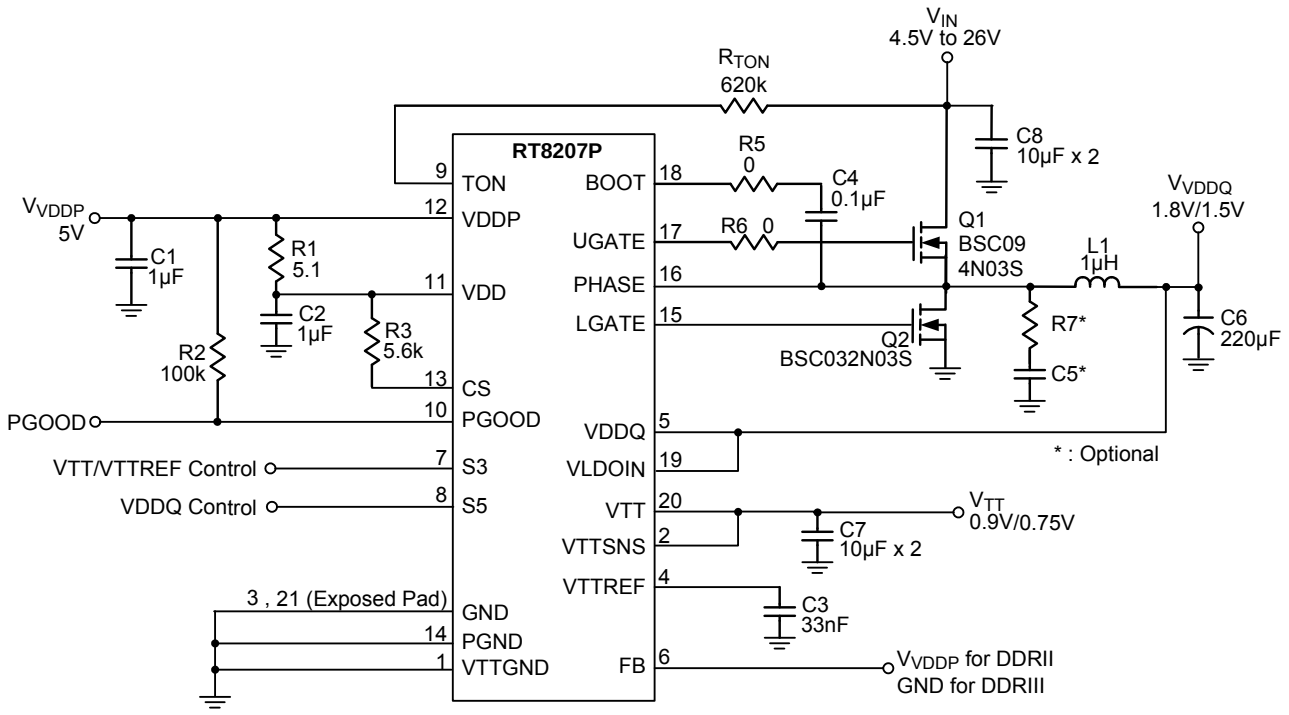
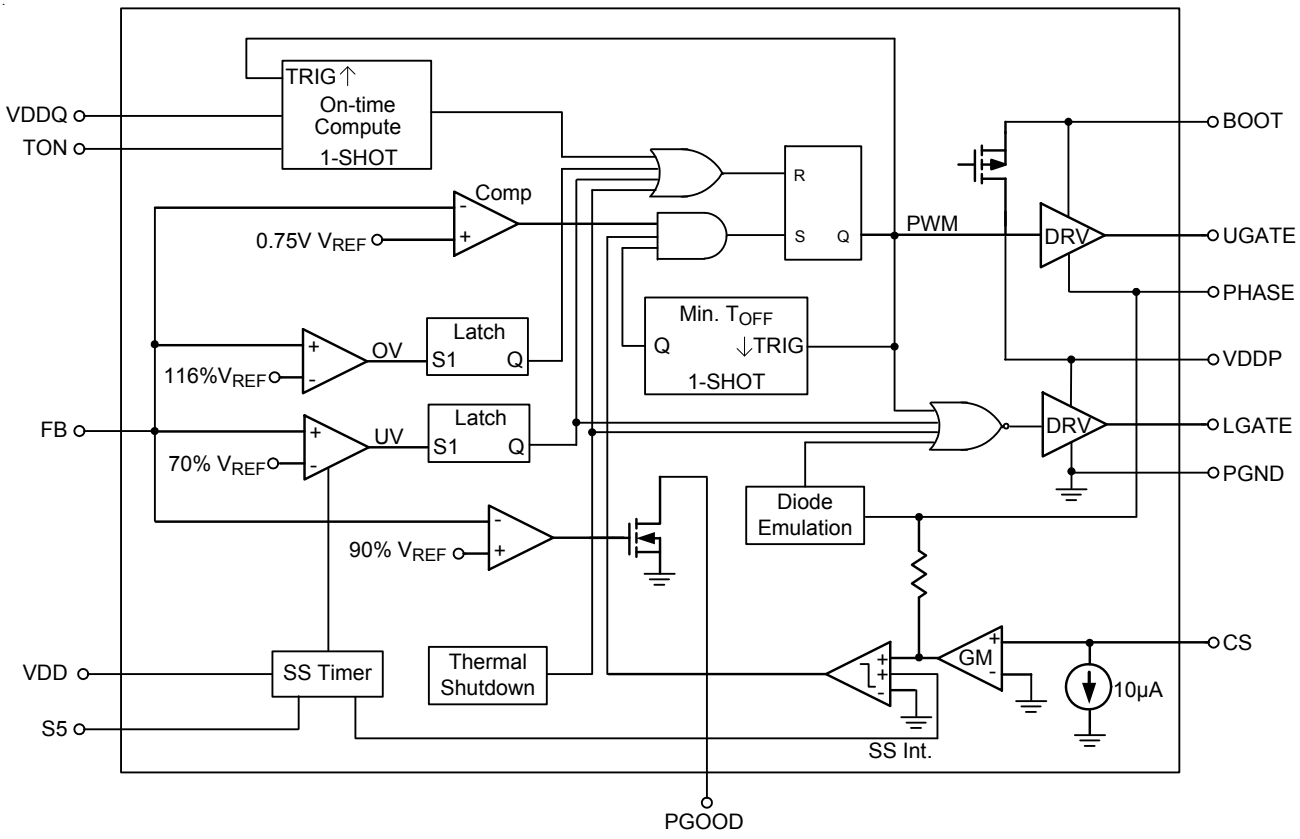


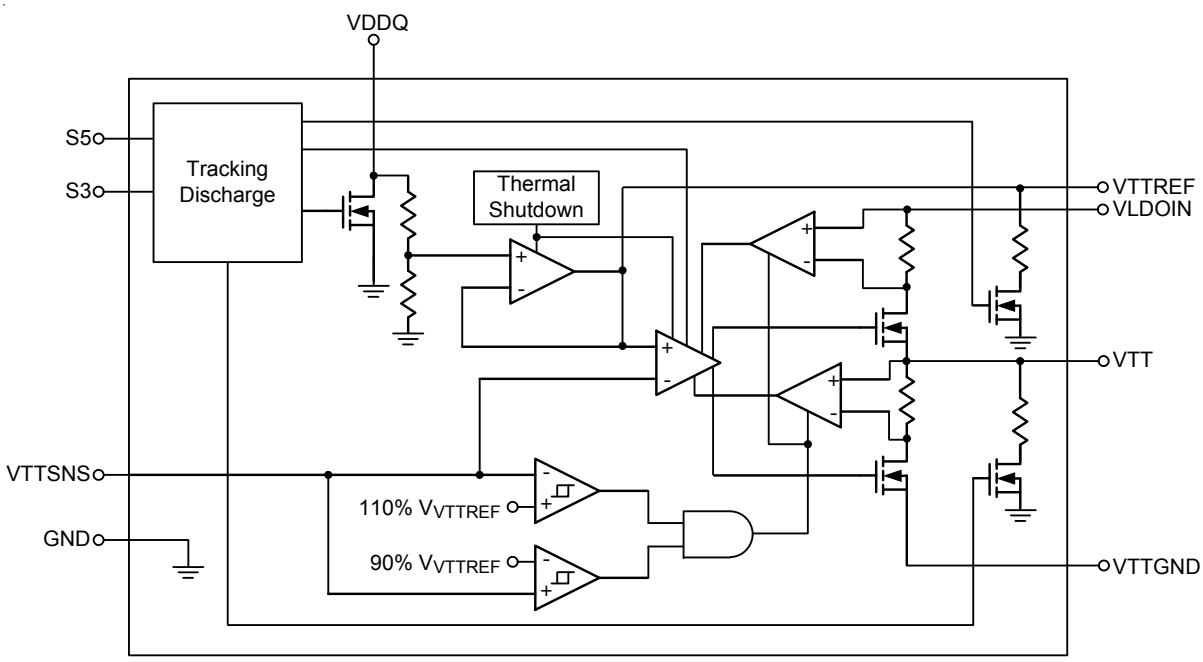
Figure 2. Fixed Voltage Regulator for

Functional Block Diagram

Buck Controller



VTT LDO



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, TON to GND ---------- –0.3V to 32V
- BOOT to GND
  - DC ---------- –0.3V to 36V
  - < 100ns ---------- –5V to 42V
- BOOT to PHASE
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –5V to 7.5V
- VDD, VDDP, CS, S3, S5, VTTSNS, VDDQ, VTTREF, VTT, VLDOIN, FB, PGOOD to GND ---------- –0.3V to 6V
- PGND, VTTGND to GND ---------- –0.3V to 0.3V
- PHASE to GND
  - DC ---------- –5V to 30V
  - < 100ns ---------- –10V to 42V
- UGATE to GND
  - DC ---------- –5V to 36V
  - < 100ns ---------- –10V to 42V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –5V to 7.5V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - < 100ns ---------- –5V to 7.5V
- The Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-20L 3x3 ---------- 1.471W
- Package Thermal Resistance (Note 2)
  - WQFN-20L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 26V
- Control Voltage, VDD, VDDP ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 15V, V_{DD} = V_{VDDP} = 5V, R_{TON} = 1MΩ, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Quiescent Supply Current (V_{DD} + V_{DDP})		FB forced above the regulation point, V_{S5} = 5V, V_{S3} = 0V	--	470	1000	μA
TON Operating Current		R_{TON} = 1MΩ	--	15	--	μA
I_{VLDOIN} BIAS Current		V_{S5} = V_{S3} = 5V, V_{TT} = No Load	--	1	--	μA
I_{VLDOIN} Standby Current		V_{S5} = 5V, V_{S3} = 0V, V_{TT} = No Load	--	0.1	10	μA
Shutdown Current (V_{S5} = V_{S3} = 0V)	I_{SHDN}	V_{DD} + V_{VDDP}	--	1	10	μA
		TON	--	0.1	5	
		S5/S3 = 0V	–1	0.1	1	
		I_{VLDOIN}	--	0.1	1	
FB Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V	0.742	0.75	0.758	V
Fixed VDDQ Output Voltage		FB = GND	--	1.5	--	V
		FB = V_{DD}	--	1.8	--	
FB Input Bias Current		FB = 0.75V	–1	0.1	1	μA
VDDQ Voltage Range			0.75	--	3.3	V
On-Time		R_{TON} = 1MΩ, V_{VDDQ} = 1.25V	267	334	401	ns
Minimum Off-Time			250	400	550	ns
VDDQ Input Resistance			--	100	--	kΩ
VDDQ Shutdown Discharge Resistance		V_{S5} = GND	--	15	--	Ω
Current Sensing						
CS Sink Current		V_{CS} > 4.5V	9	10	11	μA
Current Limit Comparator Offset		(V_{VDD-CS} – $V_{GND-PHASE}$), R_{CS} = 10kΩ	–15	--	15	mV
Zero Crossing Threshold		GND – PHASE	–5	--	10	mV
Current Limit Threshold Setting Range		V_{DD} – V_{CS}	50	--	200	mV
Fault Protection						
Under Voltage Protection Threshold	V_{UVP}		60	70	80	%
Over Voltage Protection Threshold	V_{OVP}	With respect to error comparator threshold	113	116	120	%
Over Voltage Fault Delay		FB forced above over voltage threshold	--	20	--	μs
VDD POR Threshold		Rising edge, hysteresis = 120mV, PWM disabled below this level	3.9	4.2	4.5	V
Under Voltage Blank Time		From S5 signal going high	--	5	--	ms
Thermal Shutdown	T_{SD}		--	165	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Driver On-Resistance						
UGATE Driver Source	$R_{UGATEsr}$	BOOT – PHASE Forced to 5V	--	2.5	5	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOT – PHASE Forced to 5V	--	1.5	3	Ω
LGATE Driver Source	$R_{LGATEsr}$	DL, High State	--	2.5	5	Ω
LGATE Driver Sink	$R_{LGATEsk}$	DL, Low State	--	0.8	1.6	Ω
Dead Time		LGATE Rising (PHASE = 1.5V)	--	40	--	ns
		UGATE Rising	--	40	--	
Internal Boost Charging Switch On Resistance		VDDP to BOOT, 10mA	--	--	80	Ω
Logic I/O						
Logic Input Low Voltage		S3, S5 Low	--	--	0.8	V
Logic Input High Voltage		S3, S5 High	2	--	--	V
Logic Input Current		S3, S5 = VDD/GND	–1	0	1	μA
PGOOD (upper side threshold decide by Over Voltage threshold)						
Trip Threshold (Falling)		Measured at FB, with respect to reference, no load	–13	–10	–7	%
Trip Threshold (Hysteresis)			--	3	--	%
Fault Propagation Delay		Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current	I_{LEAK}	High state, forced to 5V	--	--	1	μA
VTT LDO						
VTT Output Tolerance	V_{VTTTOL}	V_{VDDQ} = V_{LDOIN} = 1.2V/1.35/1.5V/1.8V, $\lvert I_{VTT} \rvert$ = 0A	–20	--	20	mV
		V_{VDDQ} = V_{LDOIN} = 1.2V/1.35/1.5V/1.8V, $\lvert I_{VTT} \rvert$ < 1A	–30	--	30	
		V_{VDDQ} = V_{LDOIN} = 1.2V/1.35, $\lvert I_{VTT} \rvert$ < 1.2A	–40	--	40	
		V_{VDDQ} = V_{LDOIN} = 1.5V/1.8V, $\lvert I_{VTT} \rvert$ < 1.5A	–40	--	40	
VTT Source Current Limit	$I_{VTTOCLSRC}$	$V_{TT} = \left(\frac{V_{VDDQ}}{2}\right) \times 0.95$ PGOOD = High	1.6	2.6	3.6	A
		V_{TT} = 0V	--	1.3	--	
VTT Sink Current Limit	$I_{VTTOCLSNK}$	$V_{TT} = \left(\frac{V_{VDDQ}}{2}\right) \times 1.05$, PGOOD = High	1.6	2.6	3.6	A
		V_{TT} = V_{VDDQ}	--	1.3	--	
VTT Leakage Current	I_{VTTLK}	S5 = 5V, S3 = 0V, $V_{TT} = \left(\frac{V_{VDDQ}}{2}\right)$	–10	--	10	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VTTSNS Leakage Current	$I_{VTTSNSLK}$	I_{SINK} = 1mA	−1	--	1	μA
VTT Discharge Current	I_{DSCHRG}	V_{VDDQ} = 0V, V_{TT} = 0.5V, S5 = S3 =0V	10	30	--	mA
VTTREF Output Voltage	V_{VTTREF}	$V_{VTTREF} = \left(\frac{V_{VDDQ}}{2}\right)$	--	0.9 / 0.75	--	V
VDDQSNS/2, VTTREF Output Voltage Tolerance	$V_{VTTREFTOL}$	V_{LDOIN} = V_{VDDQ} = 1.5V, | I_{VTTREF} | <10mA	−15	--	15	mV
		V_{LDOIN} = V_{VDDQ} = 1.8V, | I_{VTTREF} | <10mA	−18	--	18	
VTTREF Source Current Limit	$I_{VTTREFOCL}$	V_{VTTREF} = 0V	10	40	80	mA

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

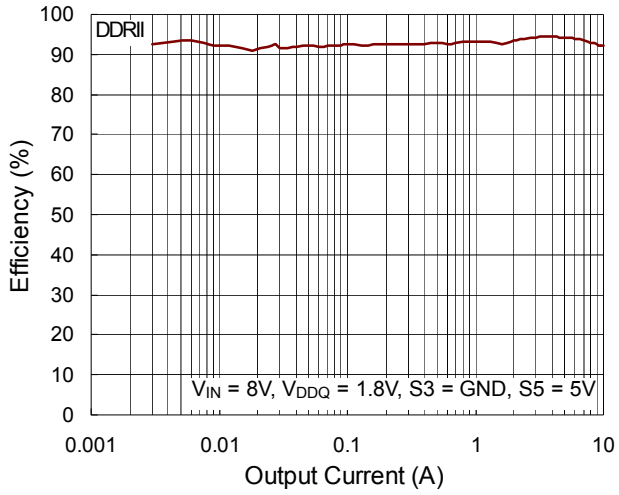
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

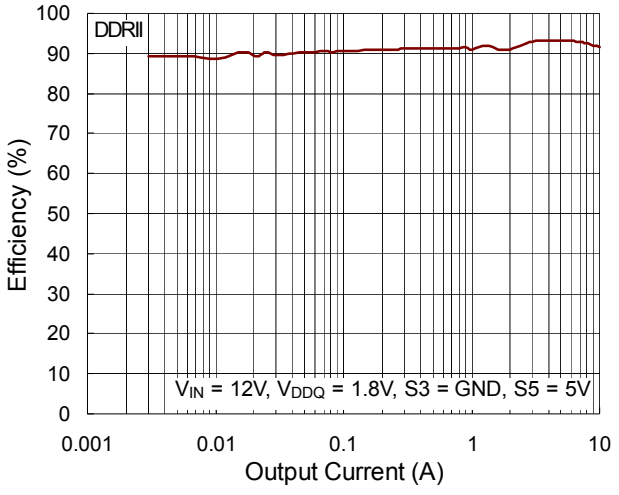
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

VDDQ Efficiency vs. Output Current



VDDQ Efficiency vs. Output Current



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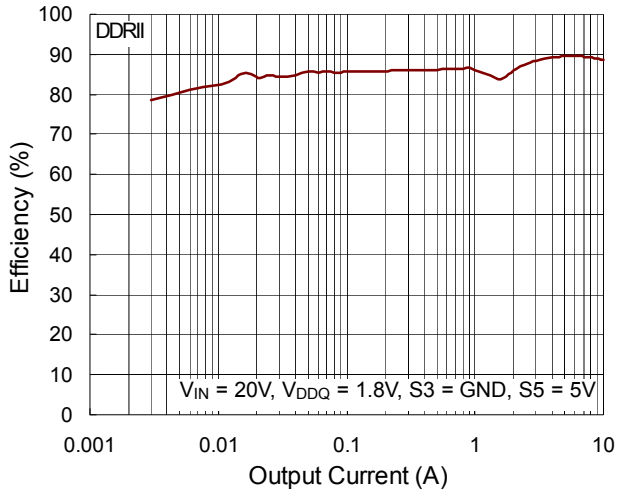

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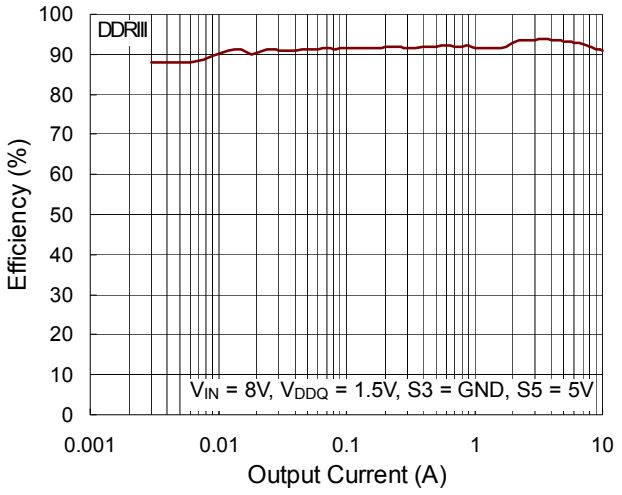

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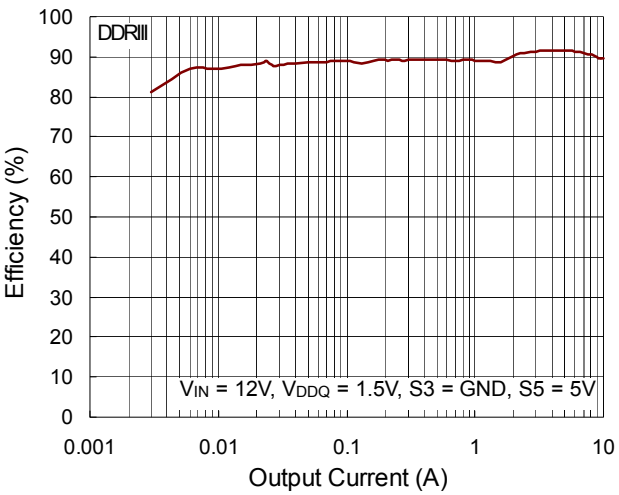

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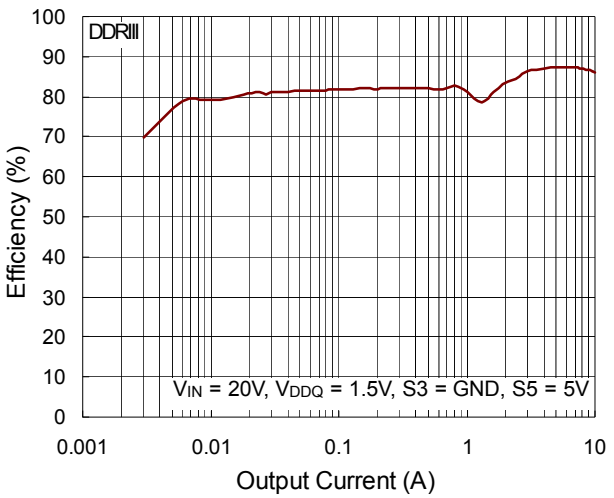
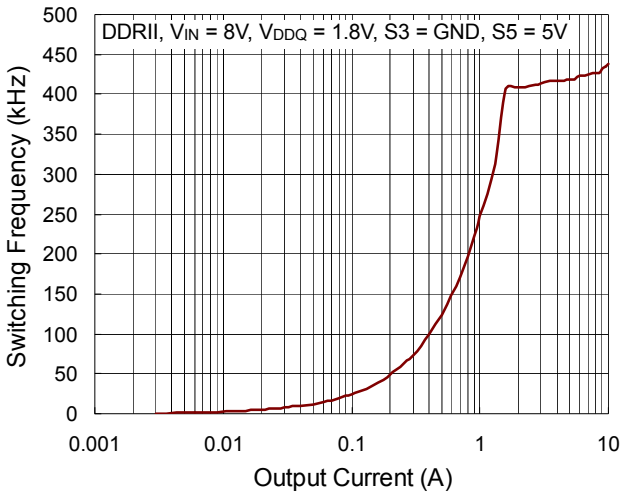


Switching Frequency vs. Output Current



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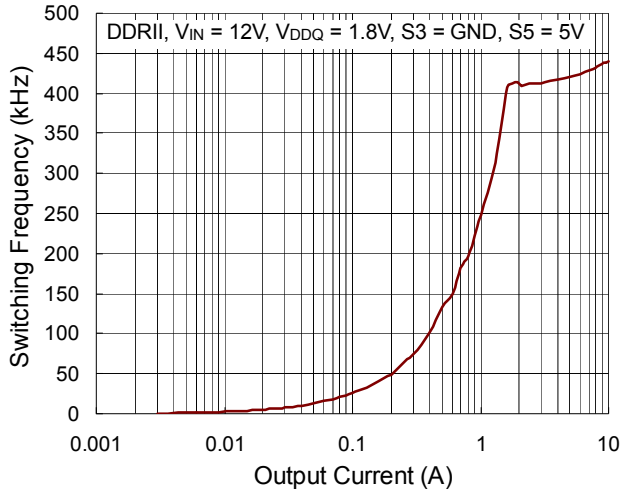

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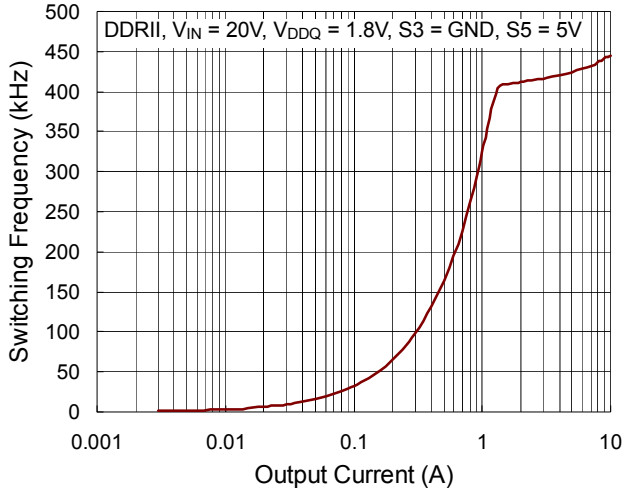

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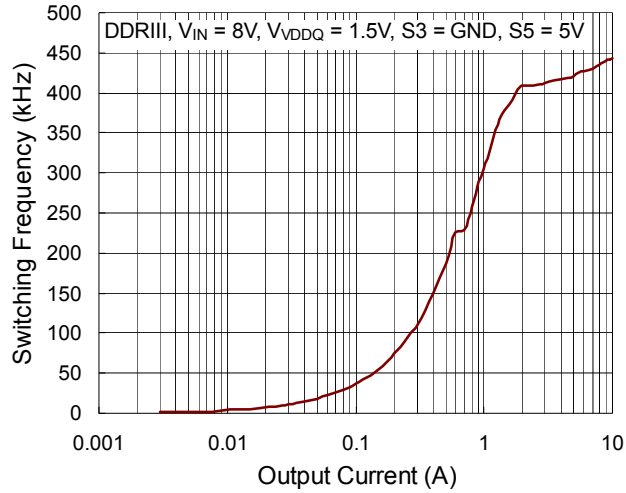

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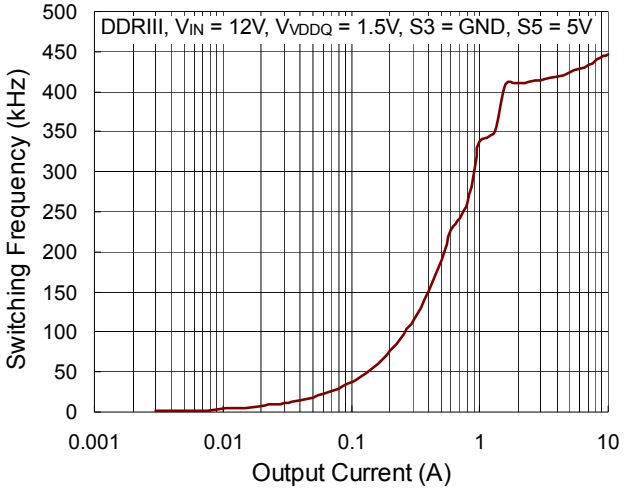

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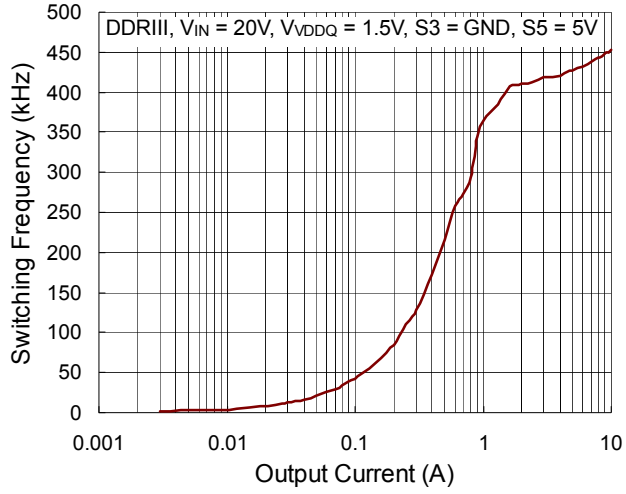
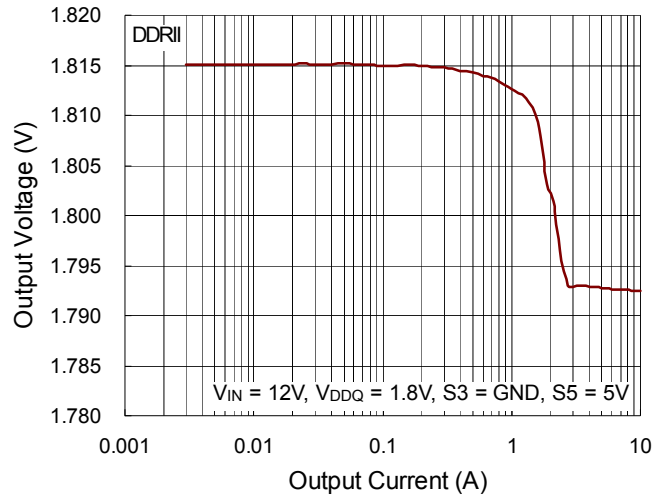
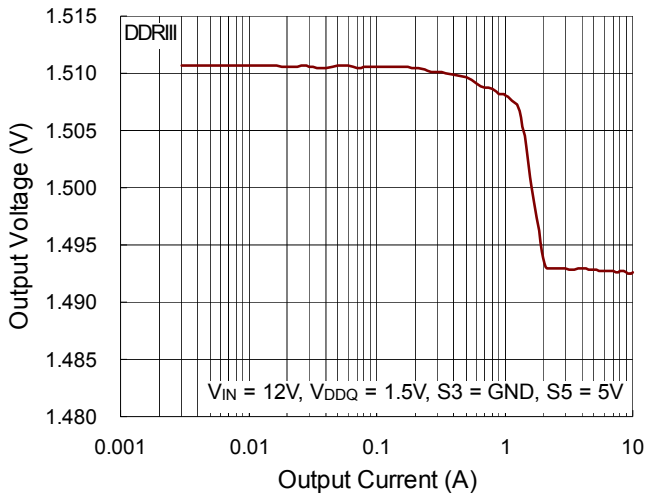


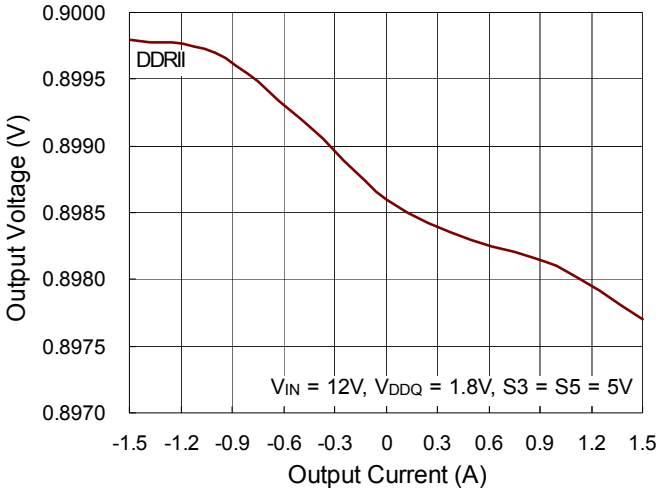
VDDQ Output Voltage vs. Output Current



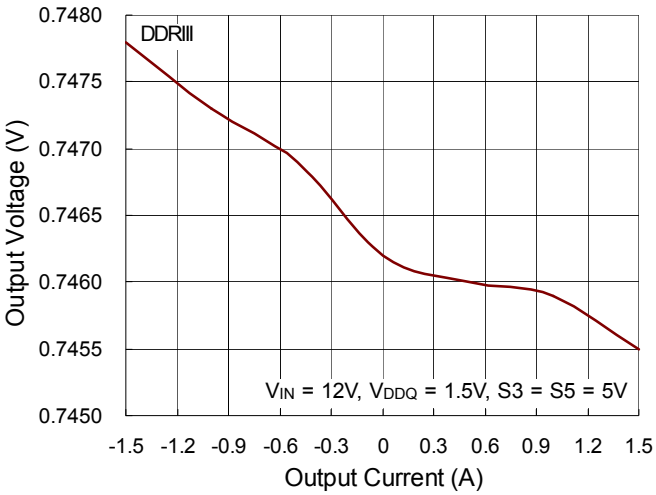
VDDQ Output Voltage vs. Output Current



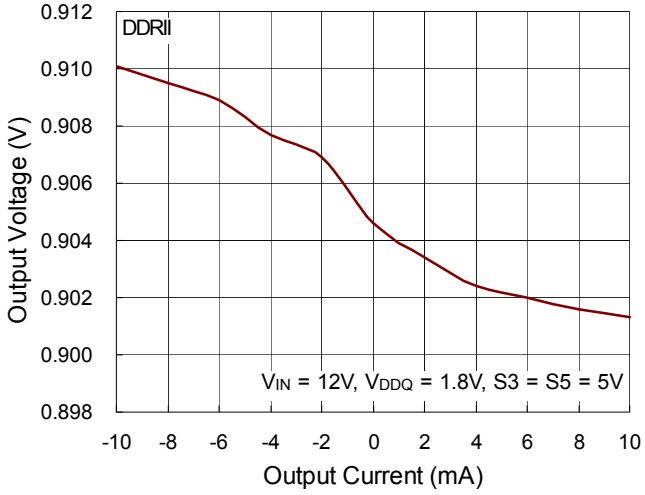
VTT Output Voltage vs. Output Current



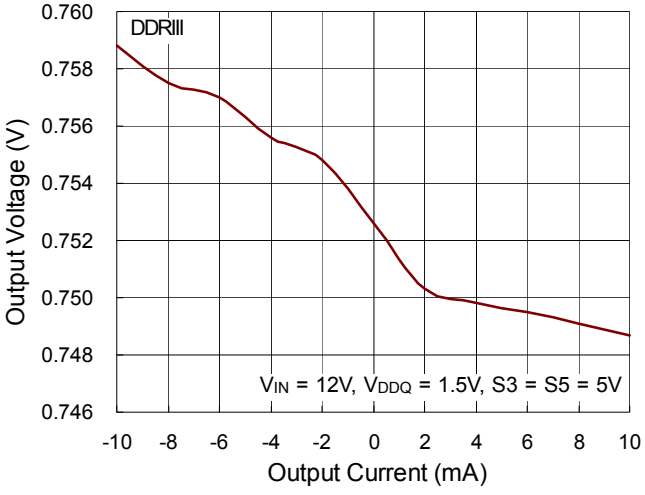
VTT Output Voltage vs. Output Current



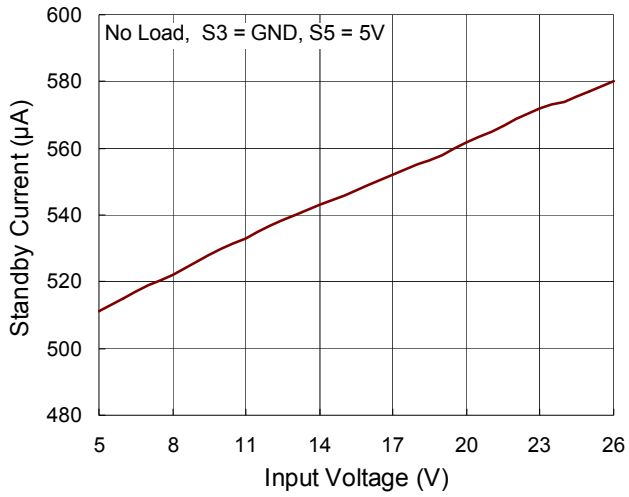
VTTREF Output Voltage vs. Output Current



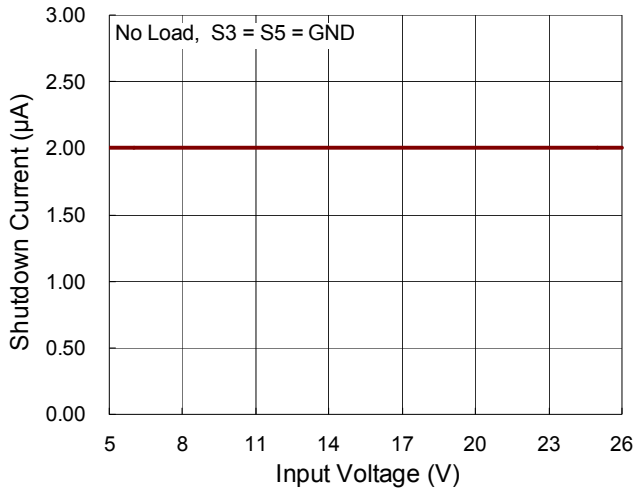
VTTREF Output Voltage vs. Output Current



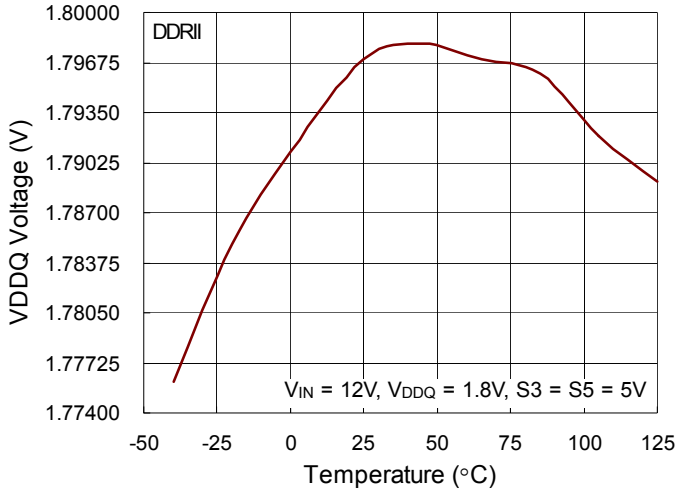
Standby Current vs. Input Voltage



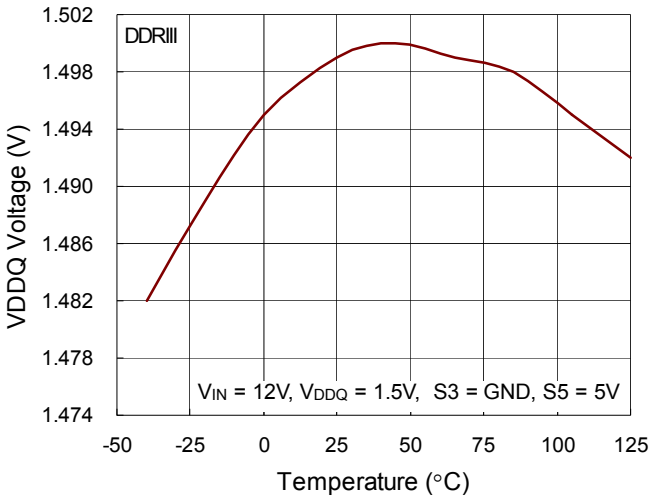
Shutdown Current vs. Input Voltage



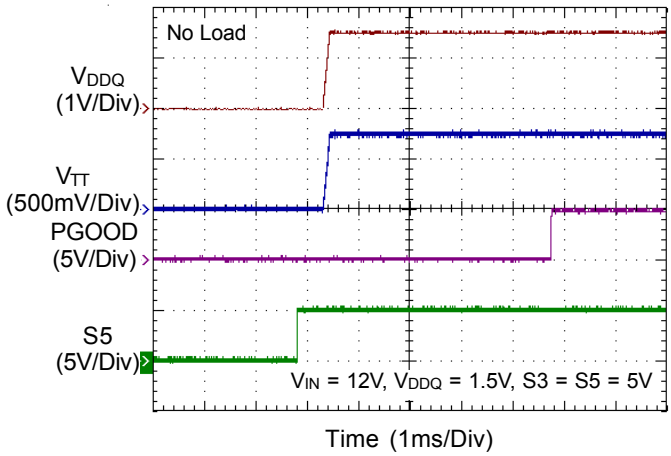
VDDQ Voltage vs. Temperature



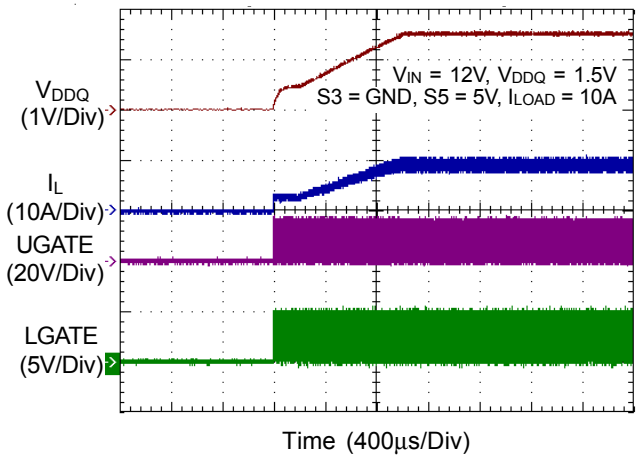
VDDQ Voltage vs. Temperature



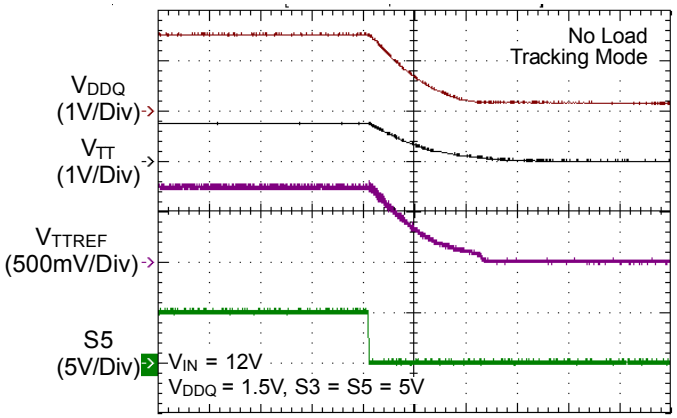
VDDQ and VTT Start Up



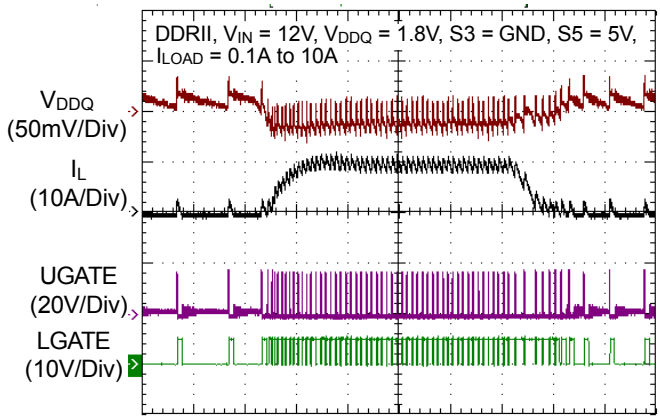
VDDQ Start Up



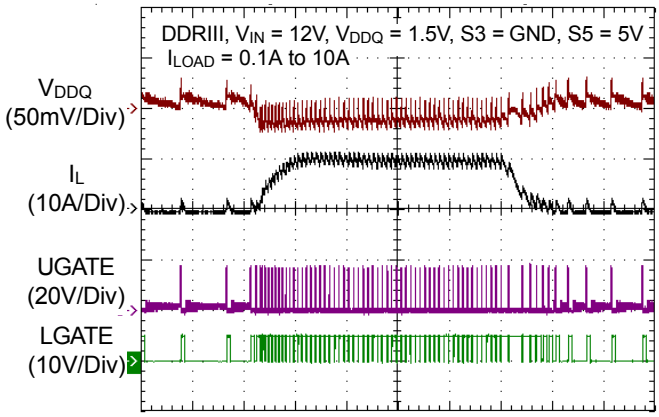
Shutdown



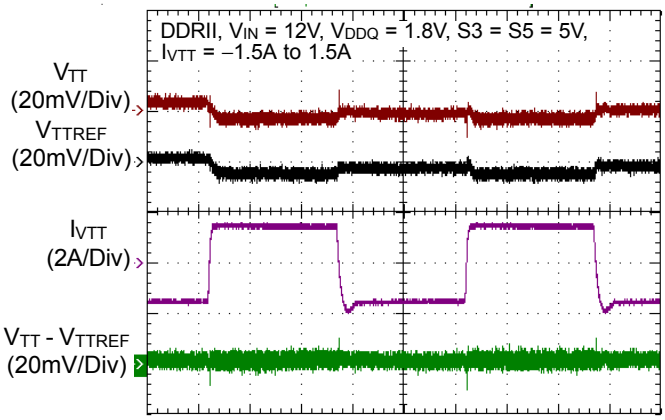
VDDQ Load Transient Response



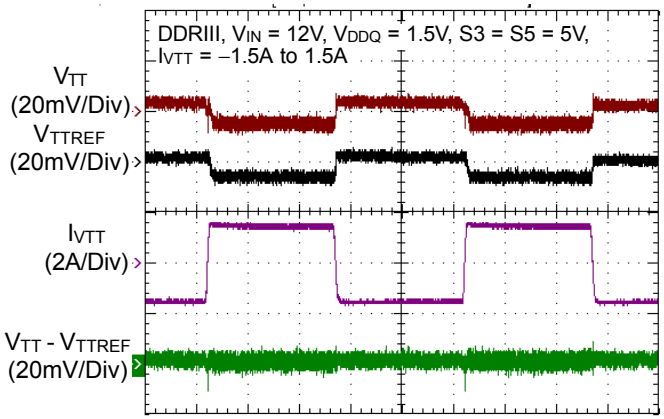
VDDQ Load Transient Response



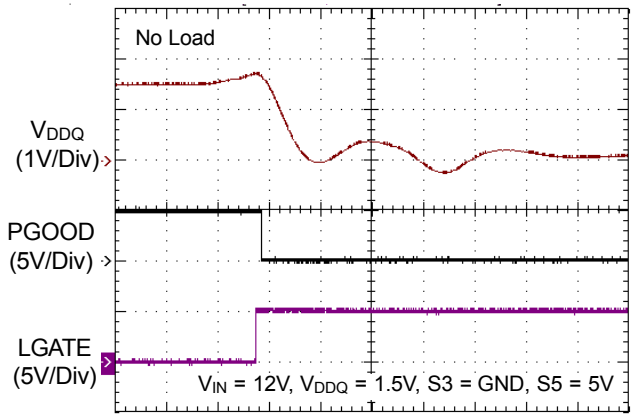
VTT Load Transient Response



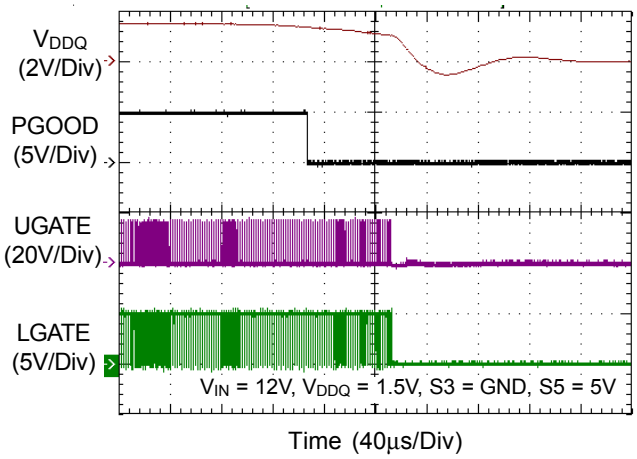
VTT Load Transient Response



OVP



UVP



Application Information

The RT8207P PWM controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage chipset RAM supplies in notebook computers. Richtek's Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs, while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

The 1.5A sink/source LDO maintains fast transient response, only requiring 20μF of ceramic output capacitance. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The RT8207P supports all of the sleep state controls, placing VTT at high-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. Referring to the function diagrams of the RT8207P, the synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one-shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{VDDQ}, thereby making the on-time of the high side switch directly proportional to the output voltage and inversely proportional to the input voltage. This implementation results in a nearly constant switching frequency without the need of a clock generator, as shown below :

$$t_{ON} = 3.85p \times R_{TON} \times V_{VDDQ} / (V_{IN} - 0.5)$$

And then the switching frequency is :

$$f = V_{VDDQ} / (V_{IN} \times t_{ON})$$

where R_{TON} is the resistor connected from V_{IN} to the TON pin.

Diode-Emulation Mode

In diode-emulation mode, the RT8207P automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly without increasing VDDQ ripples or load regulation. As the output current decreases from heavy load condition, the inductor current will also be reduced and eventually come to the point where its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current to flow when the inductor freewheeling current reaches negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy load condition. In contrast, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light load operation is shown in below figure and can be calculated as follows :

$$I_{LOAD(SKIP)} \approx \frac{V_{IN} - V_{VDDQ}}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

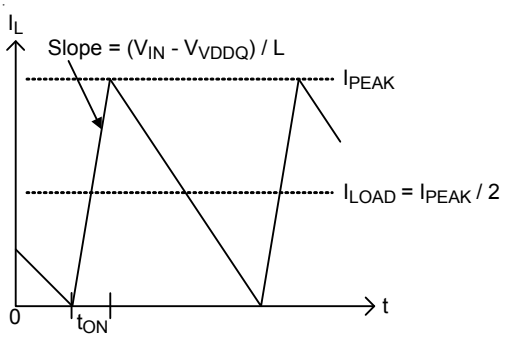


Figure 3. Boundary Condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light load efficiency. Trade offs in DEM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

Current Limit Setting for VDDQ (CS)

The RT8207P provides cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery and output voltage.

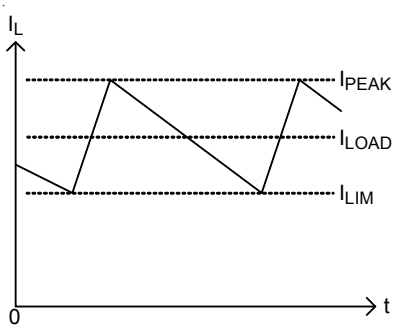


Figure 4. "Valley" Current Limit

The RT8207P uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The setting resistor, R_{ILIM}, between the CS pin and VDD sets the current limit threshold. The CS pin sinks an internal 10μA (typ.) current source at room temperature. This current has a 4700ppm/°C temperature slope to compensate the temperature dependency of $R_{DS(ON)}$. When the voltage drop across the low side MOSFET equals the voltage across the R_{ILIM} setting resistor, the positive current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the low side MOSFET falls below the current limit threshold.

Choose a current limit setting resistor via the following equation :

$$R_{ILIM} = I_{LIMIT} \times R_{DS(ON)} / 10\mu A$$

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal seen by PHASE and PGND.

Current Protection for VTT

The LDO has an internally fixed constant over current limiting of 2.6A while operating at normal condition. After the first time VTT voltage comes to within 16% of its set voltage, this over current point is reduced to 1.3A. From then on, when the output voltage goes outside 20% of its set voltage, the internal power good signal will transit from high to low.

MOSFET Gate Driver (UGATE, LGATE)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the VDDP supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOT and PHASE pins.

A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on.

The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The internal pull down transistor that drives LGATE low is robust, with a 0.8Ω typical on resistance. A 5V bias voltage is delivered from the VDDP supply. The instantaneous drive current is supplied by the flying capacitor between VDDP and PGND.

For high current applications, some combinations of high and low side MOSFETs may cause excessive gate drain coupling, which leads to efficiency killing, EMI producing shoot through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on rising time of the high side MOSFET without degrading the turn-off time (Figure 5).

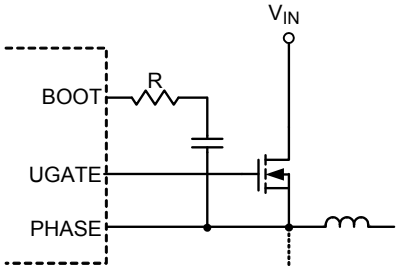


Figure 5. Increasing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open drain output that requires a pull up resistor. When the output voltage is 15% above or 10% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over and the output reaches 93% of its set voltage. There is a 2.5μs delay built into PGOOD circuitry to prevent false transition.

POR Protection

The RT8207P has a VDDP supply power on reset protection (POR). When the VDDP voltage is higher than 4.2V (typ.), VDDQ, VTT and VTTREF will be activated. This is a non-latch protection.

Soft-Start

The RT8207P provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. Soft-start (SS) automatically begins once the chip is enabled. During soft-start, internal current limit circuit gradually ramps up the inductor current from zero. The maximum current-limit value is set externally as described in previous section. The soft-start time is determined by the current limit level and output capacitor value. If the current limit threshold is set for 200mV, the typical soft-start duration is 3ms after S5 is enabled.

The soft-start function of VTT is achieved by the current limit and VTTREF voltage through the internal RC delay ramp up after S3 is high. During VTT startup, the current limit level is 2.6A. This allows the output to start up smoothly and safely under enough source/sink ability.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage. If the output exceeds 16% of its set voltage threshold, over voltage protection is triggered and the LGATE low side gate driver is forced high. This activates the low side MOSFET switch which rapidly discharges the output capacitor and reduces the input voltage. There is a 5μs latch delay built into the over voltage protection circuit. The RT8207P will be latched if the output voltage remains above the OV threshold after the latch delay period and can then only be released by VDD power on reset or S5.

Note that latching the LGATE high will cause the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over voltage condition is caused by a short in high side switch, turning the low side MOSFET on 100% will create an electrical short between the battery and GND, hence blowing the fuse and disconnecting the battery from the output.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage. When enabled, the under voltage protection is triggered if the output is less than 70% of its set voltage threshold. Then, both UGATE and LGATE gate drivers will be forced low while entering soft discharge mode. During soft-start, the UVP has a blanking time around 5ms.

Thermal Protection

The RT8207P monitors the temperature of itself. If the temperature exceeds the threshold value, 165°C (typ.), the PWM output, VTTREF and VTT will be shut off. The RT8207P is latched once thermal shutdown is triggered and can only be released by VDD power on reset or S5.

Output Voltage Setting (FB)

The RT8207P can be used as DDR2 (V_{VDDQ} = 1.8V) and DDR3 (V_{VDDQ} = 1.5V) power supply or as an adjustable output voltage (0.75V < V_{VDDQ} < 3.3V) by connecting the FB pin according to Table 1.

Table 1. FB and output voltage setting

FB	VDDQ (V)	VTTREF and VTT	NOTE
VDD	1.8	V_{VDDQ} / 2	DDR2
GND	1.5	V_{VDDQ} /2	DDR3
FB Resistors	Adjustable	V_{VDDQ} / 2	0.75V < V_{VDDQ} < 3.3V

Connect a resistive voltage divider at FB between VDDQ and GND to adjust the respective output voltage between 0.75V and 3.3V (Figure 6). Choose R2 to be approximately 10kΩ and solve for R1 using the equation as follows :

$$V_{VDDQ} = V_{REF} \times \left(1+\left(\frac{R1}{R2}\right)\right)$$

where V_{REF} is 0.75V (typ.).

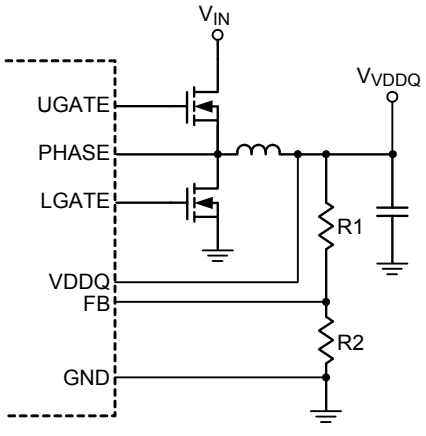


Figure 6. Setting VDDQ with a Resistive Voltage Divider

VTT Linear Regulator and VTTREF

The RT8207P integrates a high performance low dropout linear regulator that is capable of sourcing and sinking currents up to 1.5A. This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough for keeping track of VTTREF within 40mV at all conditions, including fast load transient. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of the VTT output capacitor(s) as a separate trace from the VTT pin. For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 20μF. It is recommended to attach two 10μF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If ESR of the output capacitor is greater than 2mΩ, insert an RC filter between the output and VTTSNS input to achieve loop stability. The RC filter time constant should be almost the same or slightly lower than the time constant made by the output capacitor and its ESR. The VTTREF block consists of on-chip 1/2 divider, LPF and buffer. This regulator also has sink and source capability up to 10mA. Bypass VTTREF to GND with a 33nF ceramic capacitor for stable operation.

VDD sources the load of VTTREF to follow half voltage of VDDQ. If VTTREF capacitor is so large that the VTTREF is unable to follow half VDDQ voltage at time during soft start period, VTTREF will sink large current from VDD which causes large voltage drop at VDDP to VDD resistor and has the opportunity of UVLO. The following equation provides the maximum value of VTTREF capacitor calculation.

$$\frac{0.03}{1.1\times R_{VDD}+12}\times T_{SS} = C_{VTTREF}\times\frac{V_{VDDQ}}{2}$$

$$T_{SS} = \frac{V_{VDDQ}\times C_{OUT}}{\frac{0.03}{R_{DS}}+t_{ON}\times\frac{V_{IN}}{2L}}$$

$$C_{VTTREF} = \frac{2}{V_{VDDQ}}\times\frac{0.03}{1.1\times R_{VDD}+12}\times\frac{V_{VDDQ}\times C_{OUT}}{\frac{0.03}{R_{DS}}+t_{ON}\times\frac{V_{IN}}{2L}}$$

Where R_{VDD} is the resistor between VDDP and VDD pin. R_{DS} is the turn on resistor of low-side MOSFET. C_{VTTREF} is the capacitor on the VTTREF pin. T_{SS} is the soft start time for VDDQ at the no load condition.

Output Management by S3, S5 Control

In DDR2/DDR3 memory applications, it is important to always keep VDDQ higher than VTT/VTTREF, even during start up and shutdown. The RT8207P provides this management by simply connecting both S3 and S5 terminals to the sleep-mode signals such as SLP_S3 and SLP_S5 in notebook PC system. All VDDQ, VTTREF and VTT are turned on at S0 state (S3 = S5 = high). In S3 state (S3 = low, S5 = high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance (high-Z) state. The VTT output is floated and does not sink or source current in this state. In S4/S5 states (S3 = S5 = low), all of the three outputs are disabled. The code of each state represents the following: S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 2)

Table 2. S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

VDDQ and VTT Discharge Control

The RT8207P discharges VDDQ, VTTREF and VTT outputs when S5 is low or in the S4/S5 state.

When in tracking discharge mode, the RT8207P discharges outputs through the internal VTT regulator transistors and VTT output tracks half of the VDDQ voltage during this discharge. Note that the VDDQ discharge current flows via VLDOIN to VTTGND; thus VLDOIN must be connected to VDDQ in this mode. The internal LDO can handle up to 1.5A and discharge quickly. After VDDQ is discharged down to 0.15V, the terminal LDO will be turned off and the operation mode is changed to the non-tracking discharge mode.

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or L_{IR}) determine the inductor value as follows :

$$L = \frac{t_{ON} \times (V_{IN} - V_{VDDQ})}{L_{IR} \times I_{LOAD(MAX)}}$$

where L_{IR} is the ratio of the peak-to-peak ripple current to the maximum average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left[(L_{IR}/2) \times I_{LOAD(MAX)} \right]$$

This inductor ripple current also impacts transient-response performance, especially at low $V_{IN} - V_{VDDQ}$ differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient (V_{SAG}) is also a function of the output transient. V_{SAG} also features a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \times V_{VDDQ} \times \left[V_{IN} \times t_{ON} - V_{VDDQ} \times (t_{ON} + t_{OFF(MIN)}) \right]}$$

where minimum off-time, $t_{OFF(MIN)}$, is 400ns typically.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{L_{IR} \times I_{LOAD(MAX)}}$$

where V_{P-P} is the peak-to-peak output voltage ripple.

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

For low input-to-output voltage differentials (V_{IN}/V_{VDDQ} < 2), additional output capacitance is required to maintain stability and good efficiency in ultrasonic mode.

The amount of overshoot due to stored inductor energy can be calculated as :

$$V_{SOAR} = \frac{(I_{PEAK})^2 \times L}{2 \times C_{OUT} \times V_{VDDQ}}$$

where I_{PEAK} is the peak inductor current.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting VDDQ or the FB voltage divider close to the inductor.

Unstable operation manifests itself in two related and distinctly different ways: double-pulsing and feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output in the form of line or load perturbations, which can trip the over voltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or over-shoot.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 68°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) = 1.471W for a WQFN-20L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

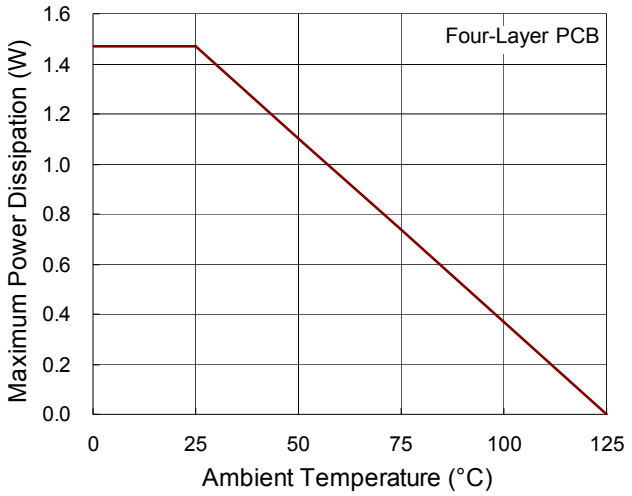


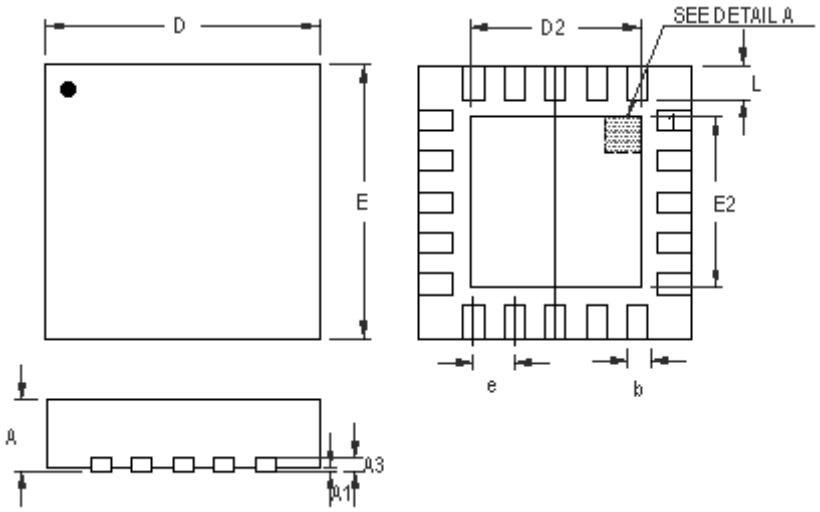
Figure 7. Derating Curve of Maximum Power Dissipation

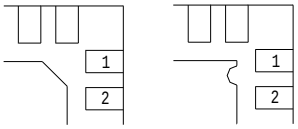
Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for the RT8207P.

- Connect an RC low pass filter from VDDP to VDD; 1μF and 5.1Ω are recommended. Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VDDQ, FB, PGND, PGOOD, CS, VDD, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, and BOOT to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- VLDOIN should be connected to VDDQ output with short and wide trace. If different power source is used for VLDOIN, an input bypass capacitor should be placed as close as possible to the pin with short and wide trace.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- It is strongly recommended to connect VTTSNS to the positive node of VTT output capacitor(s) as a separate trace from the high current power line to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. It is also recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor(s).
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed as close to the IC as possible to minimize loops and reduce losses.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

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