BLSC9G2731XS-200

LDMOS S-band radar power transistor

AMPLEON

Rev. 1 — 22 February 2019 **Product data sheet**

1. Product profile

1.1 General description

200 W LDMOS power transistor for S-band radar applications in the frequency range from 2.7 GHz to 3.1 GHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 300 µs; δ = 10 %; I_{Dq} = 200 mA; in a class-AB demo circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D
	(GHz)	(V)	(W)	(dB)	(%)
pulsed RF	2.7 to 3.1	32	200	14	45

1.2 Features and benefits

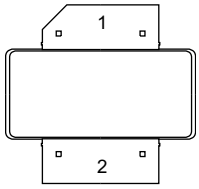
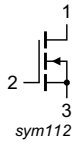
- High efficiency
- Excellent ruggedness
- Designed for S-band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- S-band radar applications in the frequency range 2.7 GHz to 3.1 GHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLSC9G2731XS-200	-	air cavity plastic earless flanged package; 2 leads	SOT1270-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	65	V
V_{GS}	gate-source voltage	–6	+13	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 200 W		
		t_p = 100 µs; δ = 10 %	0.205	K/W
		t_p = 200 µs; δ = 10 %	0.230	K/W
		t_p = 300 µs; δ = 10 %	0.250	K/W
		t_p = 500 µs; δ = 10 %	0.278	K/W
		t_p = 1 ms; δ = 10 %	0.322	K/W
		t_p = 100 µs; δ = 20 %	0.234	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 180 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	-	36	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 20 V; I_D = 180 mA	-	1.7	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	-	0.079	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 300 µs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 200 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 200 W	13	14	-	dB
η_D	drain efficiency	P_L = 200 W	41	45	-	%
RL_{in}	input return loss	P_L = 200 W	-	−10	-	dB
$P_{droop(pulse)}$	pulse droop power	P_L = 200 W	-	0.0	0.3	dB
t_r	rise time	P_L = 200 W	-	6	50	ns
t_f	fall time	P_L = 200 W	-	6	50	ns
$P_{L(2dB)}$	output power at 2 dB gain compression		-	200	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLSC9G2731XS-200 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 200 mA; P_L = 200 W; t_p = 300 µs; δ = 10 %.

7.2 Impedance information

Table 8. Typical impedance

f	Z_S	Z_L
(GHz)	(Ω)	(Ω)
2.7	2.2 – j5.3	1.8 – j5.0
2.8	2.0 – j4.2	2.0 – j4.1
2.9	1.9 – j3.1	2.4 – j3.2
3.0	2.0 – j2.0	3.2 – j2.4
3.1	2.1 – j0.9	4.6 – j2.0

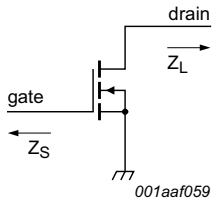
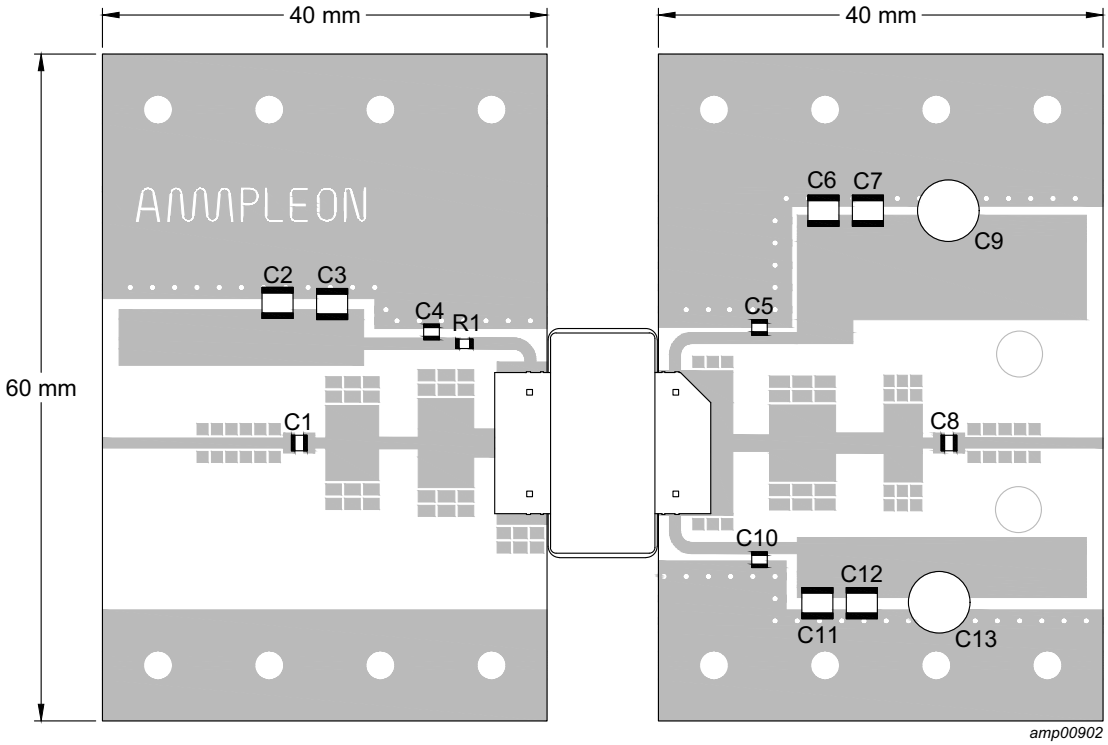


Fig 1. Definition of transistor impedance

7.3 Test circuit information



Printed-Circuit Board (PCB): Rogers 4360G2; thickness = 0.61 mm; ε_r = 6.15; thickness of copper plating = 35 µm

See Table 9 for a list of components.

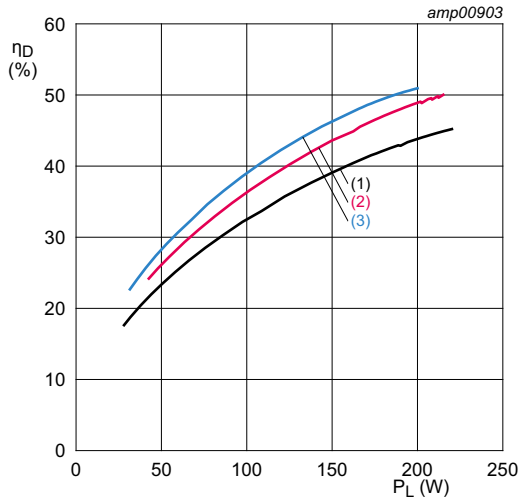
Fig 2. Component layout

Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C8	multilayer ceramic chip capacitor	15 pF	ATC 800A
C4, C5, C10	multilayer ceramic chip capacitor	15 pF	ATC 100A
C3, C6, C11	multilayer ceramic chip capacitor	1 nF	ATC 100B
C2, C7, C12	multilayer ceramic chip capacitor	10 µF	Murata: GRM55DR61H106KA88L
C9, C13	electrolytic capacitor	100 µF, 63 V	
R1	resistor	5 Ω	SMD 0603

7.4 Graphical data



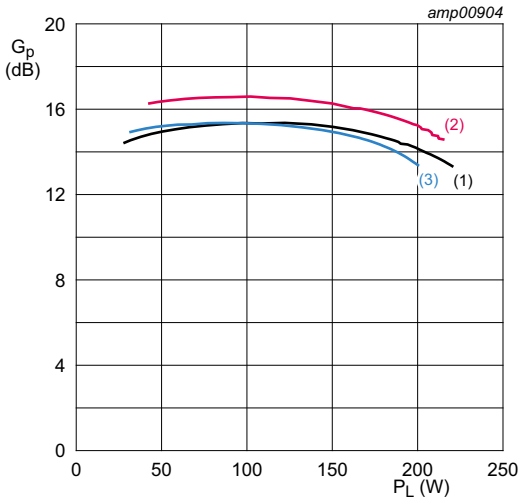
V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 300 µs; δ = 10 %.

(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 3. Drain efficiency as a function of output power; typical values



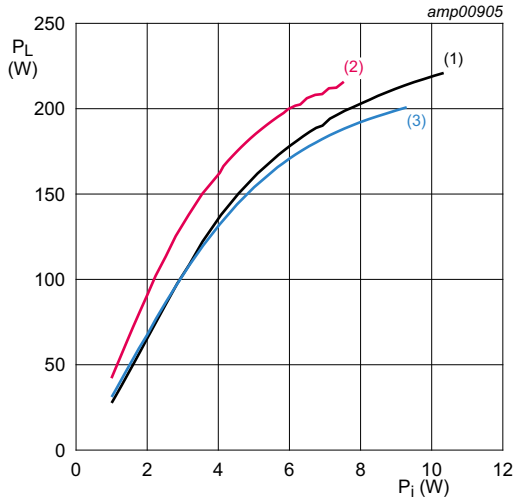
V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 300 µs; δ = 10 %.

(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 4. Power gain as a function of output power; typical values



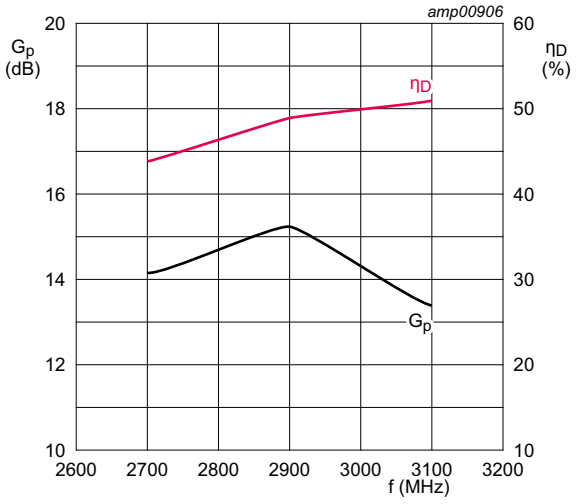
V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 300 µs; δ = 10 %.

(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 5. Output power as a function of input power; typical values

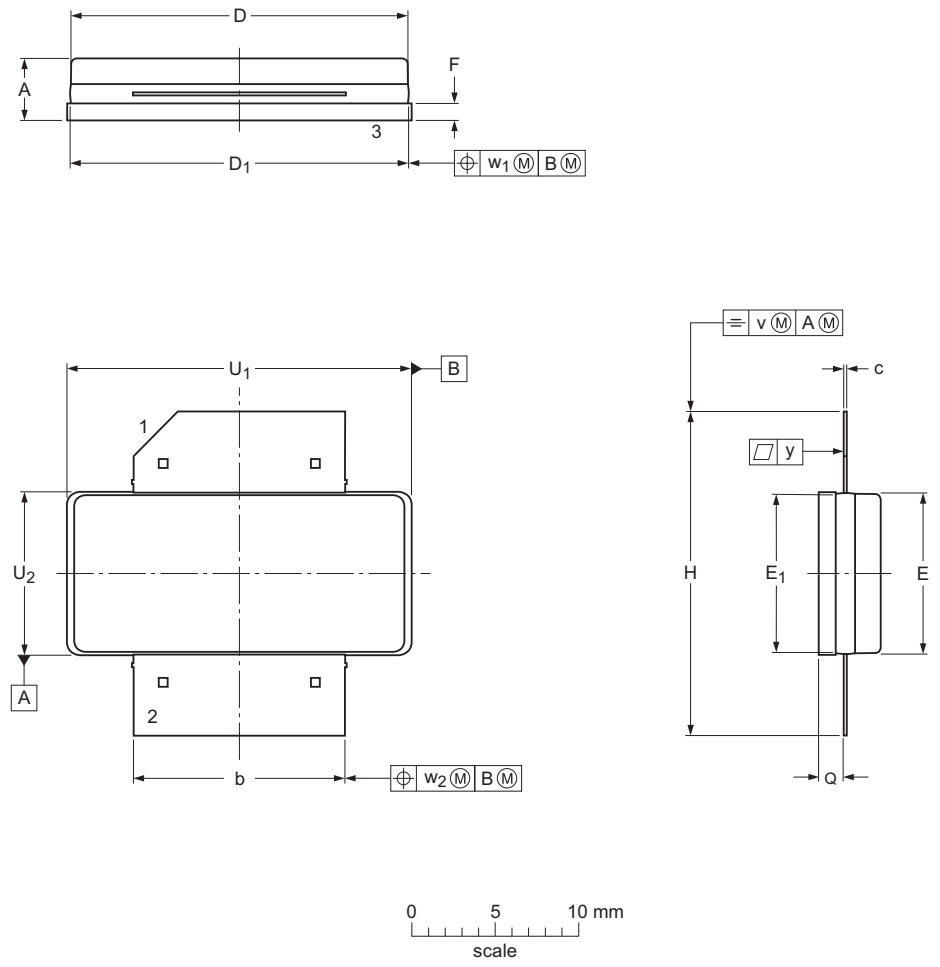


V_{DS} = 32 V; I_{Dq} = 200 mA; P_L = 200 W; t_p = 300 µs; δ = 10 %.

Fig 6. Power gain and drain efficiency as function of frequency; typical values

8. Package outline

Air cavity plastic earless flanged package; 2 leads **SOT1270-1**



Dimensions

Unit		A	b	c	D	D_1	E	E_1	F	H	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	12.80	0.18	20.42	20.37	9.80	9.75	1.14	19.53	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom																
	min	3.40	12.60	0.13	20.12	20.17	9.50	9.55	0.94	19.33	1.45	20.50	9.70				

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1270-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1270-1						~~16-09-28~~ 16-11-15

Fig 7. Package outline SOT1270-1

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
S-band	Short wave Band
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLSC9G2731XS-200 v.1	20190222	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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