

Dual Type D Master-Slave Flip-Flop

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

Dual Type D Master-Slave Flip-Flop

The MC10131 is a dual master–slave type D flip–flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and \overline{Clock} \overline{Enable} (C_E) inputs. Each flip–flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip–flop, the \overline{Clock} \overline{Enable} inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

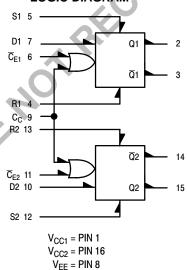
- $P_D = 235 \text{ mW typ/pkg (No Load)}$
- $F_{Tog} = 160 \text{ MHz typ}$
- $t_{pd} = 3.0 \text{ ns typ}$
- t_r , $t_f = 2.5$ ns typ (20%–80%)

DIP PIN ASSIGNMENT V_{CC1} 16 V_{CC2} Q1 2 15 Q2 Q2 Q1 3 14 R1 13 R2 S2 S1 5 12 \overline{C}_{E1} 6 11 \overline{C}_{E2} D1 7 10 D2 9 V_{EE}

Pin assignment is for Dual–in–Line Package.

For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

LOGIC DIAGRAM





ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS



CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot

YY = Year

WW = Work Week

CLOCKED TRUTH TABLE

С	D	Q _{n+1}
L	Х	Q _n
Н	L	L
Н	Н	Н

 $C = C_{\text{\ensuremath{\mathsf{E}}}} + C_{C}.A$ clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q _{n+1}
L	L	Q _n
L	Н	Н
Н	L	L
Н	Н	N.D.

N.D. = Not Defined

ORDERING INFORMATION

Device	Package	Shipping
MC10131L	CDIP-16	25 Units / Rail
MC10131P	PDIP-16	25 Units / Rail
MC10131FN	PLCC-20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

			Test Limits							
		Pin Under	-30°C +25°C +85°C		5°C					
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain Current	Ι _Ε	8		62		45	56		62	mAdc
Input Current	l _{inH}	4 5 6 7 9		525 525 350 390 425			330 330 220 245 265		330 330 220 245 265	μAdc
	I _{inL}	4, 5* 6, 7, 9*	0.5 0.5		0.5 0.5			0.3 0.3		μAdc
Output Voltage Logic 1	V _{OH}	2 2†	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc
Output Voltage Logic 0	V _{OL}	2 3†	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	2 2†	-1.080 -1.080		-0.980 -0.980			-0.910 -0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	2 3†		-1.655 -1.655			-1.630 -1.630		-1.595 -1.595	Vdc
Switching Times (50Ω Load) Clock Input										ns
Propagation Delay	t ₉₊₂₋ t ₉₊₂₊ t ₆₊₂₊ t ₆₊₂₋	2 2 2 2	1.7 1.7 1.7 1.7	4.6 4.6 4.6 4.6	1.8 1.8 1.8 1.8	3.0 3.0 3.0 3.0	4.5 4.5 4.5 4.5	1.8 1.8 1.8 1.8	5.0 5.0 5.0 5.0	
Rise Time (20 to 80%)	t ₂₊	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Fall Time (20 to 80%)	t ₂₋	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Set Input Propagation Delay	t ₅₊₂₊ t ₁₂₊₁₅₊ t ₅₊₃₋ t ₁₂₊₁₄₋	2 15 3 14	1.7 1.7 1.7 1.7	4.4 4.4 4.4 4.4	1.8 1.8 1.8 1.8	2.8 2.8 2.8 2.8	4.3 4.3 4.3 4.3	1.8 1.8 1.8 1.8	4.8 4.8 4.8 4.8	ns
Reset Input			18/1							ns
Propagation Delay	t ₄₊₂ - t ₁₃₊₁₅ - t ₄₊₃ - t ₁₃₊₁₄₊	2 15 3 14	1.7 1.7 1.7 1.7	4.4 4.4 4.4 4.4	1.8 1.8 1.8 1.8	2.8 2.8 2.8 2.8	4.3 4.3 4.3 4.3	1.8 1.8 1.8 1.8	4.8 4.8 4.8 4.8	
Setup Time	t _{setup}	7	2.5		2.5			2.5		ns
Hold Time	t _{hold}	7	1.5		1.5			1.5		ns
Toggle Frequency (Max)	f _{tog}	2	125		125	160		125		MHz

^{*} Individually test each input applying V_{IH} or V_{IL} to input under test.

 V_{IHmax} \dagger Output level to be measured after a clock pulse has been applied to the \overline{C}_{E} Input (Pin 6)

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)					
	@ Test Te	mperature	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
		–30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
		+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
		+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
		Pin	TEST V	OLTAGE A	PPLIED TO I	PINS LISTED E	BELOW	
Characteristic	Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	(V _{CC}) Gnd
Power Supply Drain Current	Ι _Ε	8					8	1, 16
Input Current	I _{inH}	4 5 6 7 9	4 5 6 7 9				8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
	I _{inL}	4, 5* 6, 7, 9*		*			8	1, 16 1, 16
Output Voltage Logic 1	V _{OH}	2 2†	5 7			<	8 8	1, 16 1, 16
Output Voltage Logic 0	V _{OL}	2 3†	5 7			Mr.	8 8	1, 16 1, 16
Threshold Voltage Logic 1	V _{OHA}	2 2†			5 7	9	8 8	1, 16 1, 16
Threshold Voltage Logic 0	V _{OLA}	2 3†			5 7	9	8 8	1, 16 1, 16
Switching Times (50 Ω Load) Clock Input			+1.11Vdc		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₉₊₂₋ t ₉₊₂₊ t ₆₊₂₊ t ₆₊₂₋	2 2 2 2	7 7	(ID)	9966	2 2 2 2	8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time (20 to 80%)	t ₂₊	2	7) `	9	2	8	1, 16
Fall Time (20 to 80%)	t ₂₋	2	16		9	2	8	1, 16
Set Input Propagation Delay	t ₅₊₂₊ t ₁₂₊₁₅₊ t ₅₊₃₋ t ₁₂₊₁₄₋	2 15 3 14	6 9		5 12 5 12	2 15 3 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Reset Input Propagation Delay	t ₄₊₂₋ t ₁₃₊₁₅₋ t ₄₊₃₋ t ₁₃₊₁₄₊	2 15 3 14	6 9		4 13 4 13	2 15 3 14	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Setup Time		7			6, 7	2	8	1, 16
	t _{setup}				-,			
Hold Time	t _{hold}	7			6, 7	2	8	1, 16

^{*} Individually test each input applying V_{IH} or V_{IL} to input under test.

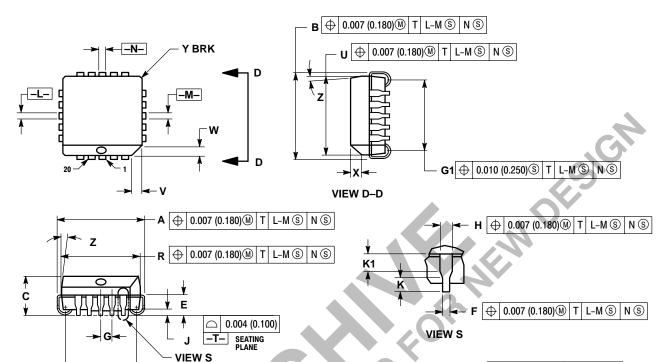
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibitum has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

 $[\]dagger$ Output level to be measured after a clock pulse has been applied to the \overline{C}_E Input (Pin 6)

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF MICE. NOT PERSON

- IOTES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

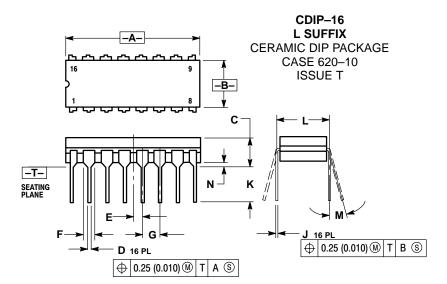
 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982.
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIN	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50
Z	2°	10°	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

PACKAGE DIMENSIONS



NOTES:

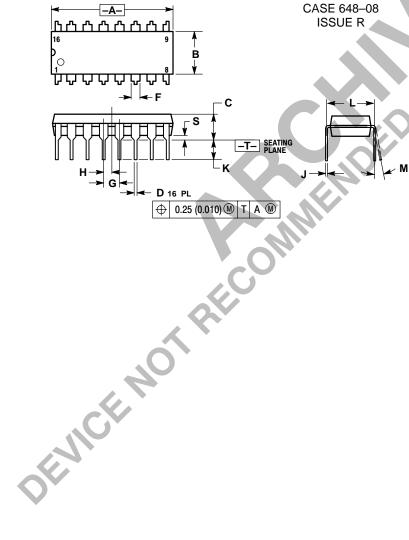
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
C		0.200		5.08	
D	0.015	0.020	0.39	0.50	
E	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62		
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
C	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

Notes



Notes





ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada **Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada

Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center 4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031

Phone: 81–3–5740–2700 **Email**: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local

Sales Representative.