Rochester Electronics

Datasheet

PART NUMBER

54ACT11004FK^B

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete Vendor CAGE 18714. Add vendor CAGE 27014. Editorial changes throughout.	91-08-28	M. A. Frye
B	Add vendor CAGE 01295 for device type 01. Change boiler plate to add device class V criteria.	97-08-04	Monica L. Poelking

REV																				
SHEET																				
REV	B																			
SHEET	15																			
REV STATUS OF SHEETS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
91-08-28

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, DIGITAL, ADVANCED CMOS, HEX INVERTER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89734**

SHEET 1 OF 15

DESC FORM 193
JUL 94

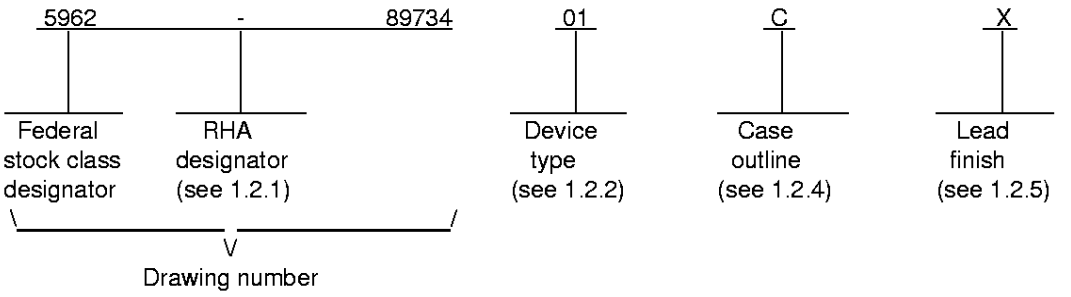
5962-E074-97

1. SCOPE

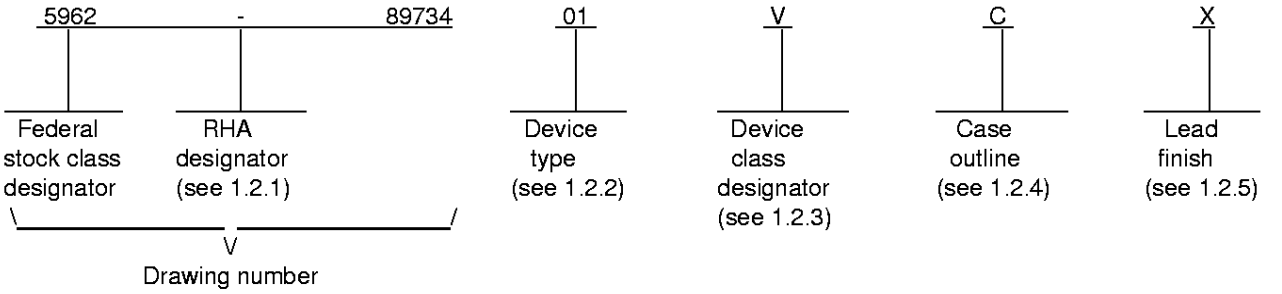
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT04	Hex inverter, TTL compatible inputs
02	54ACT11004	Hex inverter, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current	±20 mA
DC output diode current (per pin)	±50 mA
DC output source or sink current	±50 mA
DC V_{CC} or GND current	±150 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC})	4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum input rise or fall rate ($\Delta t/\Delta V$):	0 to 8 ns/V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Unused inputs must be held high or low to prevent them from floating.
6/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

JEDEC Standard No. 17 - Standardized for Description of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified		Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
							Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 18 mA		All V	4.5 V	1, 2, 3		5.7	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -18 mA		All V	4.5 V	1, 2, 3		-1.2	V
High level output voltage 3006	V_{OH} 4/	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND	I_{OH} = -50 µA	All All	4.5 V	1, 2, 3	4.4		V
					5.5 V		5.4		
			I_{OH} = -24 mA		4.5 V		3.7		
					5.5 V		4.7		
			I_{OH} = -50 mA		5.5 V		3.85		
Low level output voltage 3007	V_{OL} 4/	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs V_{IN} = V_{CC} or GND	I_{OH} = 50 µA	All All	4.5 V	1, 2, 3		0.1	V
					5.5 V			0.1	
			I_{OH} = 24 mA		4.5 V			0.5	
					5.5 V			0.5	
			I_{OH} = 50 mA		5.5 V			1.65	
High level input voltage	V_{IH} 5/			All All	4.5 V	1, 2, 3	2.0		V
					5.5 V		2.0		
Low level input voltage	V_{IL} 5/			All All	4.5 V			0.8	V
					5.5 V			0.8	
Input leakage current high 3010	I_{IH}	V_{IN} = 5.5 V		All All	5.5 V	1, 2, 3		1.0	µA
Input leakage current low 3009	I_{IL}	V_{IN} = 0.0 V		All All	5.5 V	1, 2, 3		-1.0	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 6/	V_{IL} = 0.0 V, V_{IH} = V_{CC} - 2.1 V		All All	5.5 V	1, 2, 3		1.6	mA
Quiescent supply current 3005	I_{CC}	V_{IN} = V_{CC} or GND I_{OUT} = 0.0 µA		All All	5.5 V	1, 2, 3		80	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Input capacitance 3012	C_{IN}	See 4.4.1c $T_C = +25°C$	All All	GND	4		10.0	pF
Power dissipation capacitance	C_{PD} 7/	See 4.4.1c $T_C = +25°C$ f = 1 MHz	01 All	5.0 V	4		80	pF
			02 All				40	
Latch-up input/output over-voltage	I_{CC} (O/V1) 8/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5$ ms $5\ \mu s \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $V_{over} = 10.5$ V See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up input/output positive over-current	I_{CC} (O/I1+) 8/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5$ ms $5\ \mu s \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $I_{trigger} = +120$ mA See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up input/output negative over-current	I_{CC} (O/I1-) 8/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5$ ms $5\ \mu s \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $I_{trigger} = -120$ mA See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 8/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5$ ms $5\ \mu s \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $V_{over} = 9.0$ V See 4.4.1d	All V	5.5 V	2		100	mA
Functional tests 3014	9/	Verify output V_{OUT} See 4.4.1b $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V	All All	4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
Propagation delay time, input to output 3003	t_{PLH} 10/	$C_L = 50$ pF $R_L = 500\Omega$ See figure 4	01 All	4.5 V	9	1.0	9.0	ns
			02 All			1.0	9.0	
			01 All		10, 11	1.0	10.0	
			02 All			1.0	10.2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, input to output 3003	t_{PHL} 10/	C_L = 50 pF R_L = 500Ω See figure 4	01 All		9	1.0	8.5	ns
			02 All			1.0	8.7	
			01 All		10, 11	1.0	9.5	
			02 All			1.0	10.3	

1/ For tests not listed in the referenced MIL-STD-883, (e.g. ΔICC), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. Additional detailed information on qualified devices (i.e., pin for pin conditions and testing sequence) is available from the qualifying activity (DSCC-VQ) upon request.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ The V_{OH} and V_{OL} tests shall be tested at V_{CC} = 4.5 V. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for V_{CC} = 5.5 V. Limits shown apply to operation at V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. when $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

5/ The V_{IH} and V_{IL} tests are not required and shall be applied as forcing functions for V_{OH} and V_{OL} tests.

6/ ΔI_{CC} (max)/pin ≤ 1.6 mA (preferred method), or ΔI_{CC}/package ≤ 1.6 mA x the number of input pins/package where ΔI_{CC} (max)/data pin ≤ 1.6 mA and ΔI_{CC} (max)/control pin ≤ 3.0 mA (alternate method).

7/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption where:
$P_D = (C_{PD} + C_L)\ (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$.
$I_S = (C_{PD} + C_L)\ V_{CC}f + I_{CC} + n \times d \times$
ΔI_{CC}. For both C_{PD} and I_S, n is the number of device inputs at TTL levels, f is the frequency of the input signal, d is the duty cycle of the input signal, and C_L is the output load capacitance.

8/ See JEDEC STD. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$, and V_{over} are to be accurate within ±5 percent.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883 V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs L ≤ 0.8 V, H ≥ 2.0 V.

10/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum AC limits for V_{CC} = 5.5 V are 5.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 5.5 ns. For propagation delay tests, all paths must be tested.

Device types	01		02	
Case outlines	C, D	2	R	2
Terminal number	Terminal symbol			
1	1A	NC	1Y	V_{CC}
2	1Y	1A	2Y	NC
3	2A	1Y	3Y	3A
4	2Y	2A	GND	2A
5	3A	NC	GND	1A
6	3Y	2Y	GND	1Y
7	GND	NC	GND	2Y
8	4Y	3A	4Y	3Y
9	4A	3Y	1Y	GND
10	1Y	GND	6Y	GND
11	1A	NC	6A	GND
12	6Y	6Y	1A	GND
13	6A	6A	4A	4Y
14	V_{CC}	1Y	NC	1Y
15	- - -	NC	V_{CC}	6Y
16	- - -	1A	V_{CC}	6A
17	- - -	NC	NC	1A
18	- - -	4Y	3A	4A
19	- - -	4A	2A	NC
20	- - -	V_{CC}	1A	V_{CC}

Pin description	
Terminal symbol	Description
mA (m = 1 to 6)	Data inputs
mY (m = 1 to 6)	Data outputs

FIGURE 1. Terminal connections.

Inputs	Outputs
H	L
L	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

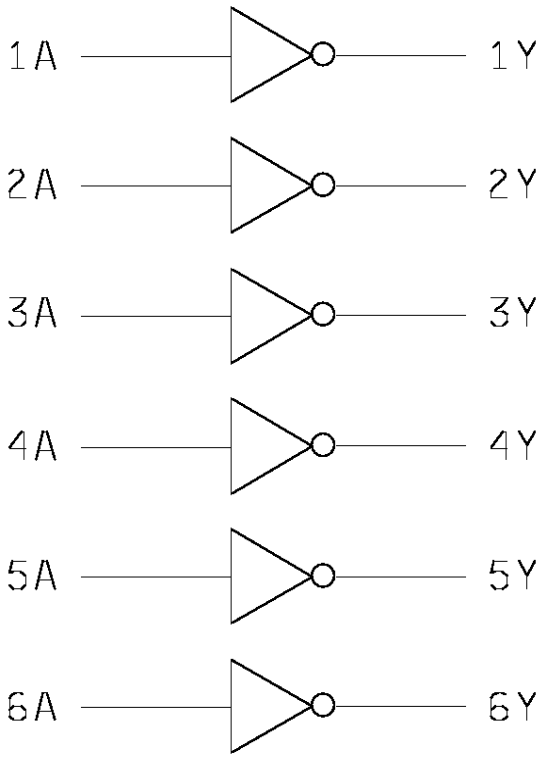
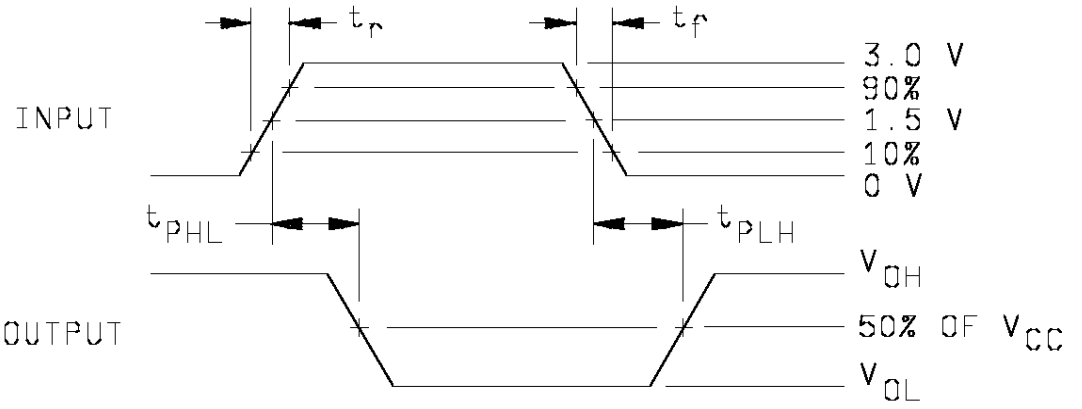
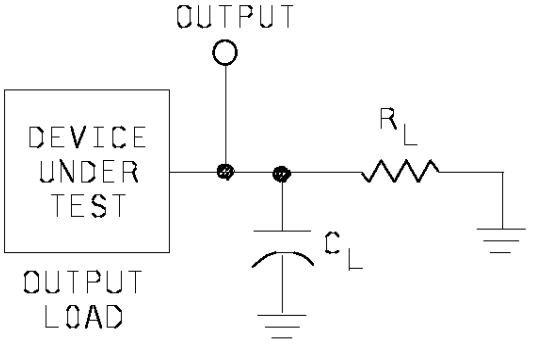


FIGURE 3. Logic diagram.



INPUT t_r, t_f = 3.0 ns, UNLESS OTHERWISE SPECIFIED



NOTES:

1. C_L = 10 pF per table I (includes test jig and probe capacitance).
2. R_L = 100Ω or equivalent.

FIGURE 4. Switching waveforms and test circuit .

4.3.1 Electrostatic discharge sensitivity qualification inspection . Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. Latch-up tests are required for device class V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 5692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-08-04

Approved sources of supply for SMD 5962-89734 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8973401CA	27014	54ACTQ04DMQB
	01295	SNJ54ACT04J
5962-8973401DA	27014	54ACTQ04FMQB
	01295	SNJ54ACT04W
5962-89734012A	27014	54ACTQ04LMQB
	01295	SNJ54ACT04FK
5962-8973402CX	3/	
5962-89734022X	3/	
5962-8973401VCA	27014	54ACTQ04J-QMLV
5962-8973401VDA	27014	54ACTQ04W-QMLV
5962-8973401V2A	27014	54ACTQ04E-QMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P. O. Box 58090 Santa Clara, CA 95052-8090 Point of contact: 5 Foden Road South Portland, ME 04506
01295	Texas Instruments Incorporated 53500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 5788 Midland, TX 79755-0448