M62368GP

3 V Type 8-bit 6ch D/A Converter with Buffer Amplifiers

REJ03D0878-0201
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Description

The M62368GP is a CMOS semiconductor IC, containing 6 channels of 8-bit D/A converters. It is operable with a low supply voltage between 2.7 to 3.6 V, and is easy to use due to serial data input, and 3-pin (DI, CLK, LD) connection with microcomputer.

The IC also contains D_O pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer.

Features

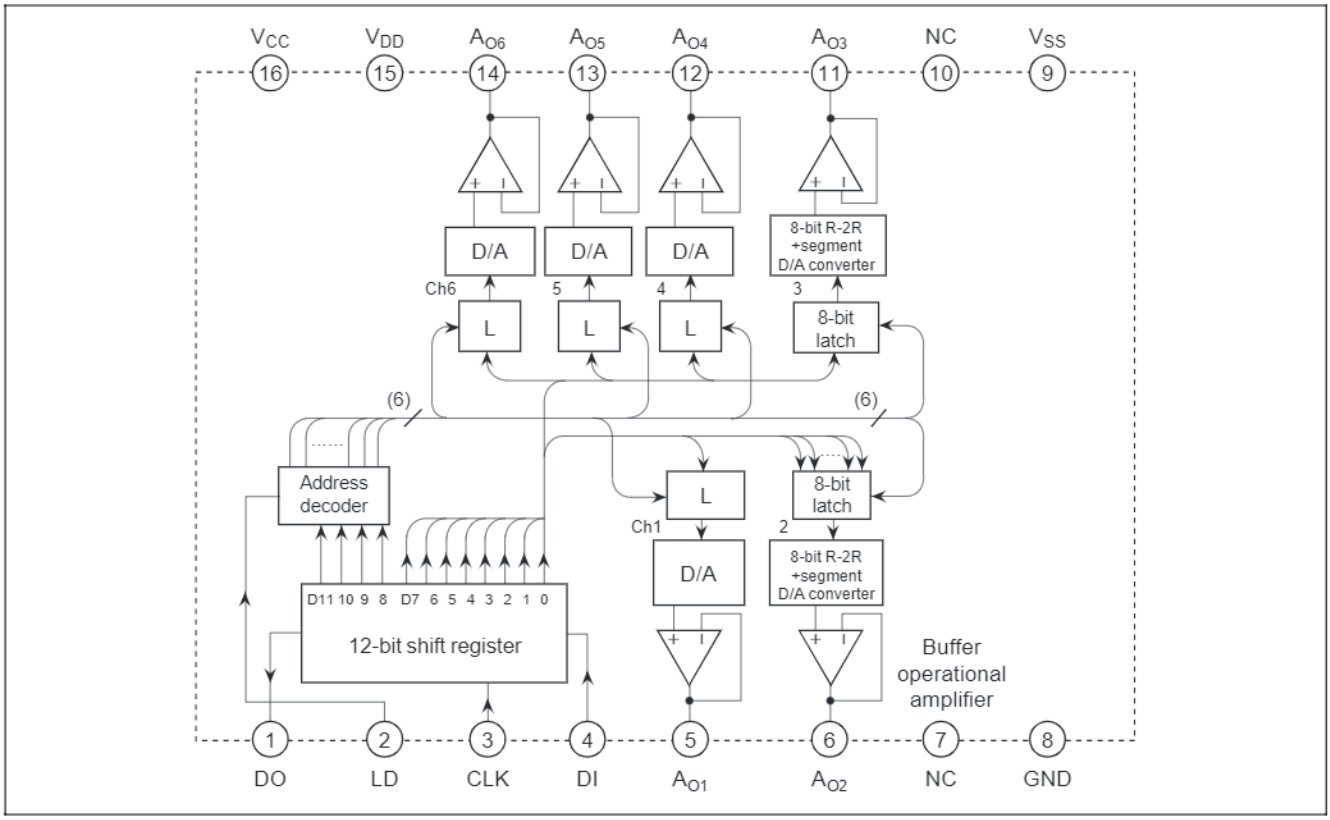
- Operable with a low voltage between 2.7 to 3.6 V
- 12-bit serial data input (connected via 3 pins: DI, CLK, LD)
- 6 channels of R-2R and segment type high-performance 8-bit D/A converters
- 6 buffer operational amplifiers with full swing of output voltage between V_{CC} and GND
- High oscillation stability against the capacitive load of buffer operational amplifiers

Application

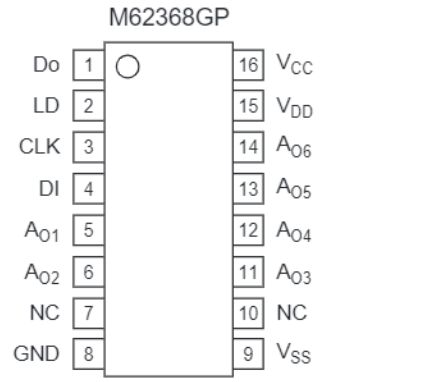
Digital/analog conversion in industrial or home-use electronic equipment.

Automatic control in combination with EEPROM and microcomputer (Substitute for conventional semi-fixed resistor).

Block Diagram



Pin Arrangement

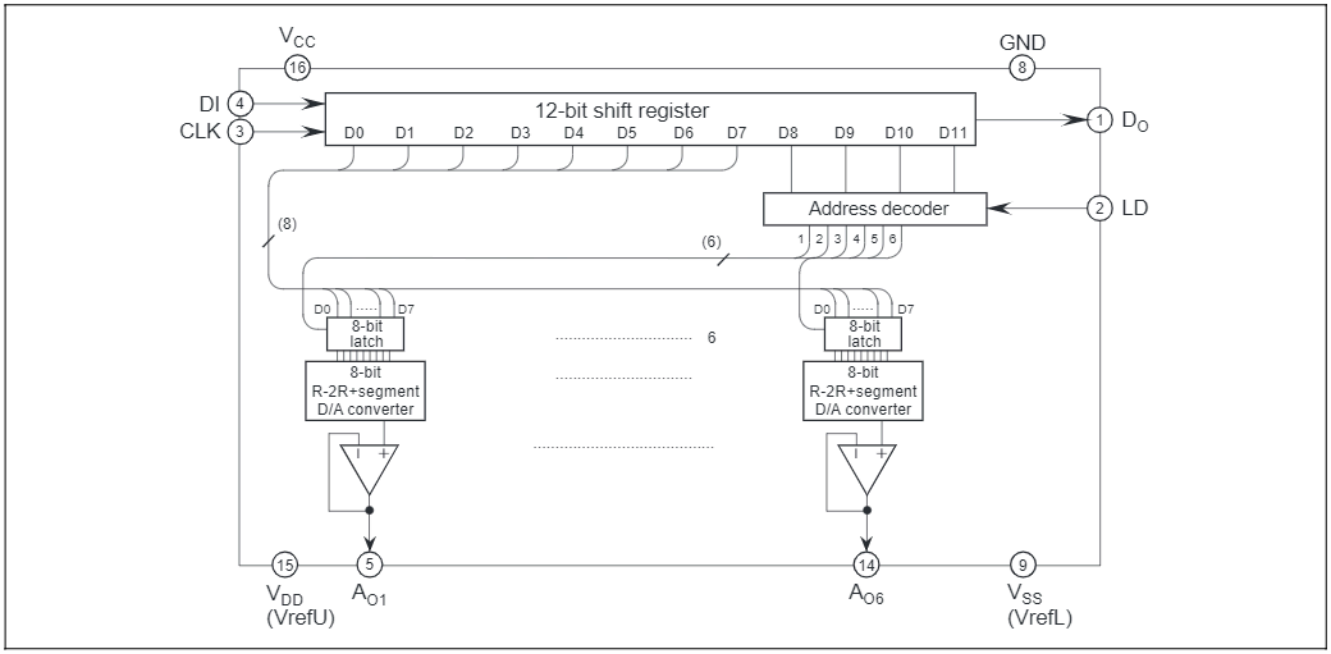


Outline: PLSP0016JA-A (16P2E-A)

Pin Description

Pin No.	Pin Name	Function
4	DI	Serial data input terminal to input 12-bit long serial data
1	D_O	Terminal to output MSB data of 12-bit shift register
3	CLK	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
2	LD	When H-level signal is input to this terminal, the value stored in 12-bit shift register is loaded in decoder and D/A converter output register.
5	A_{O1}	8-bit D/A converter output terminal
6	A_{O2}	
11	A_{O3}	
12	A_{O4}	
13	A_{O5}	
14	A_{O6}	
16	V_{CC}	Power supply terminal
8	GND	GND terminal
15	V_{DD}	D/A converter upper reference voltage input terminal
9	V_{SS}	D/A converter lower reference voltage input terminal

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Upper reference voltage of D/A converter	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_O	–0.3 to V_{CC} + 0.3	V
Power dissipation	Pd	150	mW
Operating temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–40 to +125	°C

Electrical Characteristics

<Digital Part>

(V_{CC}, VrefU = +3 V ± 10%, V_{CC} ≥ VrefU, GND, VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
Circuit current	I_{CC}	—	—	3.5	mA	CLK = 1 MHz operation, V_{CC} = 3 V, I_{AO} = 0 µA
Input leak current	I_{ILK}	–10	—	10	µA	V_{IN} = 0 to V_{CC}
Input low voltage	V_{IL}	—	—	0.2 V_{CC}	V	
Input high voltage	V_{IH}	0.8 V_{CC}	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA

<Analog Part>

(V_{CC}, VrefU = +3 V ± 10%, V_{CC} ≥ VrefU, Ta = –20 to +85°C, unless otherwise noted.)

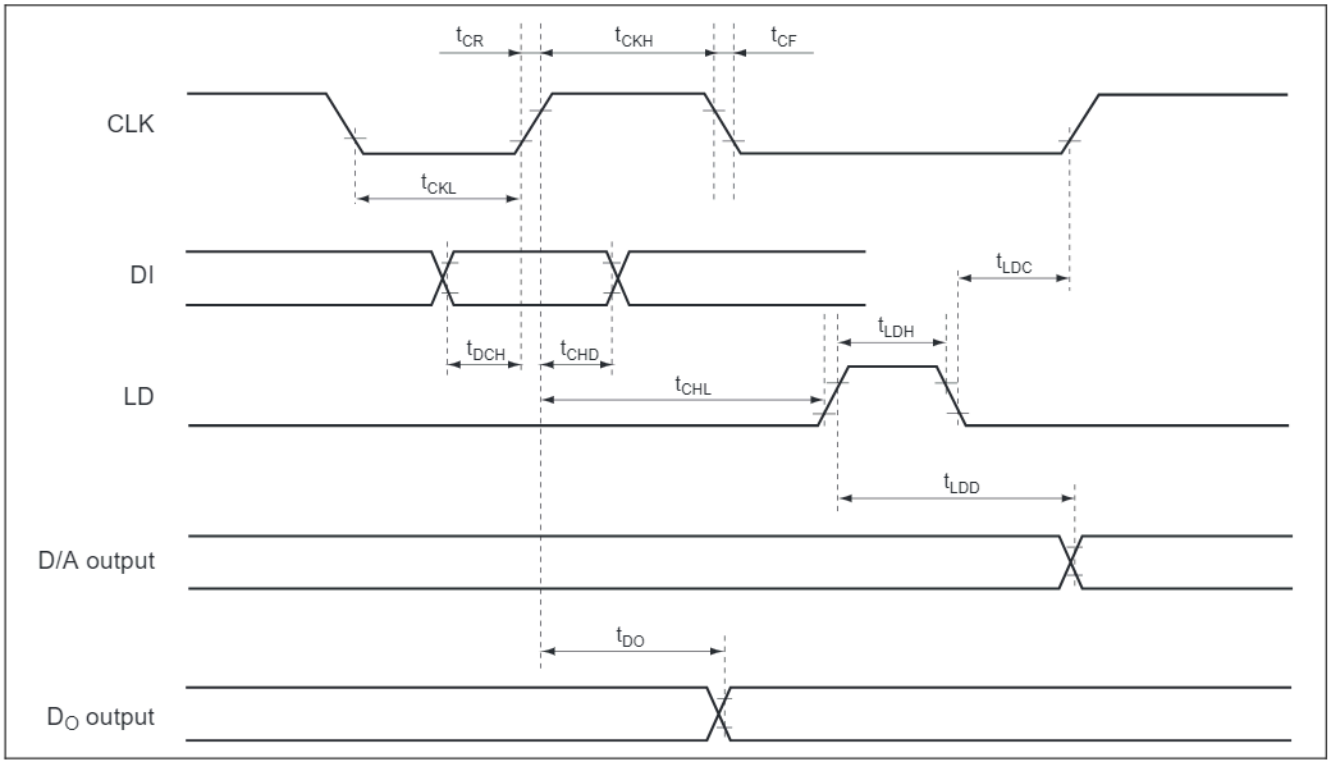
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Current dissipation	IrefU	—	1.4	2.5	mA	VrefU = 3 V, VrefL = 0 V Data condition: at maximum current
D/A converter upper reference voltage range	VrefU	0.7 V_{CC}	—	V_{CC}	V	Reference voltage cannot always be set to any value in this range, because it is restricted to the buffer amplifier output voltage range.
D/A converter lower reference voltage range	VrefL	GND	—	0.3 V_{CC}	V	
Buffer amplifier output voltage range	V_{AO}	0.1	—	V_{CC} – 0.1	V	I_{AO} = ±500 µA
		0.2	—	V_{CC} – 0.2	V	I_{AO} = +500 µA –200 µA
Buffer amplifier output driving range	I_{AO}	–0.3	—	1	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Differential nonlinearity error	S_{DL}	–1.0	—	1.0	LSB	V_{CC} = 2.760 V VrefU = 2.610 V VrefL = 0.050 V (10 mV/LSB) Without load (I_{AO} = ±0)
Nonlinearity error	S_L	–1.5	—	1.5	LSB	
Zero code error	S_{ZERO}	–2	—	2	LSB	
Full scale error	S_{FULL}	–2	—	2	LSB	
Output capacitive load	C_O	—	—	0.1	µF	
Buffer amplifier output impedance	R_O	—	5	—	Ω	

AC Characteristics

(V_{CC}, VrefU = +3 V ± 10%, V_{CC} ≥ VrefU, GND, VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	30	—	—	ns	
Data hold time	t_{CHD}	60	—	—	ns	
LD setup time	t_{CHL}	200	—	—	ns	
LD hold time	t_{LDC}	100	—	—	ns	
LD "H" pulse duration time	t_{LDH}	100	—	—	ns	
Data output delay time	t_{DO}	70	—	350	ns	C_L = 100 pF
D/A output setting time	t_{LDD}	—	—	300	µs	C_L ≥ 100 pF, V_{AO}: 0.1 ↔ 2.6 V This time until the output becomes the final value of 1/2 LSB

Timing Chart



Digital Data Format

DAC Data

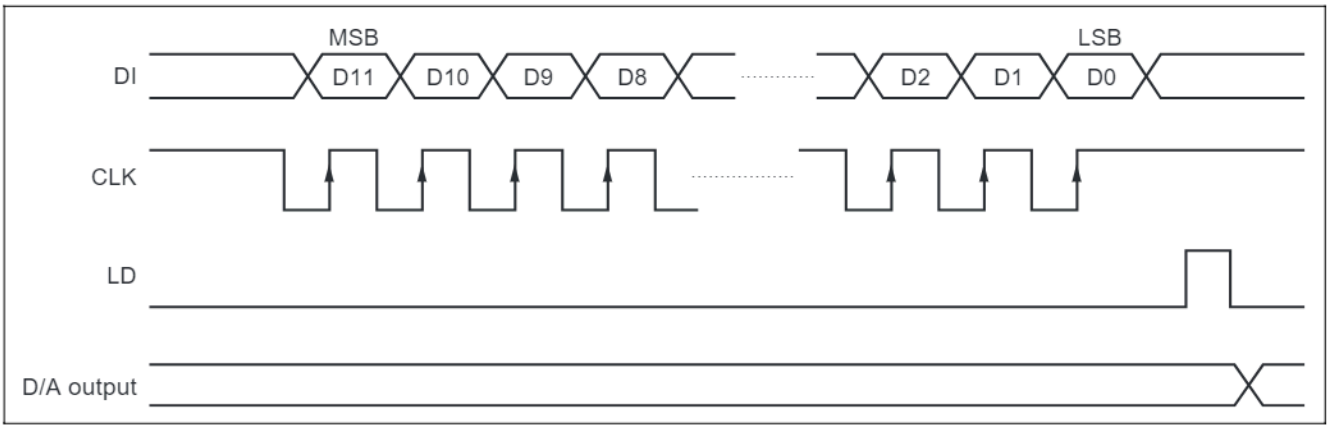
D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 1 + VrefL
1	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 2 + VrefL
0	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 3 + VrefL
1	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 4 + VrefL
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	(VrefU – VrefL) / 256 × 255 + VrefL
1	1	1	1	1	1	1	1	VrefU

Note: VrefU = V_{DD}, VrefL = V_{SS}

DAC Select Data

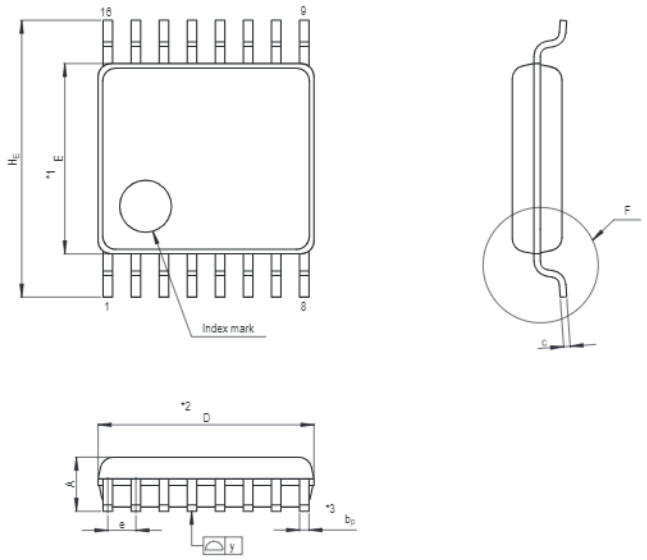
D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	A_{O1} selection
0	0	1	0	A_{O2} selection
0	0	1	1	A_{O3} selection
0	1	0	0	A_{O4} selection
0	1	0	1	A_{O5} selection
0	1	1	0	A_{O6} selection
0	1	1	1	Don't care
1	0	0	0	Don't care
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP16-4.4x5-0.65	PLSP0016JA-A	16P2E-A	0.06g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

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