Rochester Electronics

Datasheet

PART NUMBER

SCAN18374T^MXA

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change in accordance with notice of revision 5962-R073-94 -jak	93-12-30	Monica L. Poelking
B	Change in accordance with notice of revision 5962-R237-94 -tvn	94-07-14	Monica L. Poelking
C	Add bottom brazed flat pack to figure 1. Update the boilerplate paragraphs in accordance with the latest MIL-PRF-38535 requirements. - jak	11-11-01	Thomas M. Hess
D	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	17-07-27	Thomas M. Hess
E	Update Positive and Negative input clamp voltage (V_{IC}^+ and V_{IC}^-) test condition V_{CC} = 5.5 V to 4.5 V. Correct input and output capacitance (Cin, Cout) values to table I. Update devices supplier CAGE 3V146 information to bulletin page. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. – TTM	24-01-24	Muhammad A. Akbar

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Joseph A. Kerby	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thanh V. Nguyen APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 93-11-24 REVISION LEVEL E	MICROCIRCUIT, DIGITAL, ADVANCED CMOS, SERIALLY CONTROLLED ACCESS NETWORK, D-TYPE FLIP-FLOP WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON SIZE: A CAGE CODE: **67268** **5962-93207** SHEET 1 OF 28

DSCC FORM 2233
APR 97

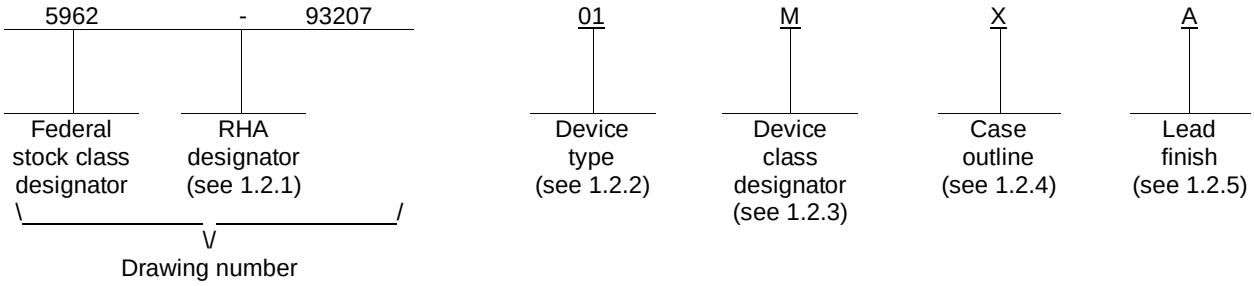
5962-E482-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	SCAN18374T	Serially controlled access network, D-type flip-flop with three-state outputs, TTL compatible inputs and outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDFP1-F56 or figure 1	56	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input clamp current (I_{IK}) (V_{IN} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output current (I_{OUT}) per output pin	±70 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±1330 mA 4/
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	750 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Minimum high level input voltage (V_{IH})	2.0 V
Maximum low level input voltage (V_{IL})	0.8 V
Case operating temperature range (T_C)	-55°C to +125°C
Input edge rate ($\Delta V/\Delta t$) minimum:	
from V_{IN} = 0.8 V to 2.0 V, 2.0 V to 0.8 V	125 mV/ns
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+48 mA

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ This value represents the maximum total current flowing into or out of all V_{CC} or GND pins.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at https://standards.ieee.org/standard/index.html.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1 .

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2 .

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3 .

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Description of boundary-scan circuitry. The description of the boundary-scan circuitry shall be as specified on figure 5.

3.2.6 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 6.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage 3006	V_{OH}	For -all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND	$I_{OH} = -50\ \mu A$	4.5 V	1, 2, 3	3.15		V
				5.5 V		4.15		
			$I_{OH} = -24\ mA$	4.5 V		2.40		
				5.5 V		2.40		
			$I_{OH} = -27\ mA$ 4/	5.5V		2.00		
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test $V_{IN} = V_{IH} = 2.0\ V$ or $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND	$I_{OL} = +50\ \mu A$	4.5 V	1, 2, 3		0.10	V
				5.5 V			0.10	
			$I_{OL} = +48\ mA$	4.5 V			0.55	
				5.5 V			0.55	
			$I_{OL} = +63\ mA$ 4/	5.5V			0.80	
Positive input clamp voltage 3022	$V_{IC}+$	For input under test $I_{IN} = +18\ mA$		4.5 V 18/	1, 2, 3		5.7	V
Negative input clamp voltage 3022	$V_{IC}-$	For input under test $I_{IN} = -18\ mA$		4.5 V 18/	1, 2, 3		-1.2	V
Three state leakage current high 3021	I_{OZH} 5/	$\overline{AOE}$ or $\overline{BOE} = 2.0\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $V_{OUT} = 4.5\ V$		4.5 V	1		+0.5	µA
					2, 3		+10.0	
				5.5V	1		+0.5	µA
					2, 3		+10.0	
Three state leakage current low 3020	I_{OZL} 5/	$\overline{AOE}$ or $\overline{BOE} = 2.0\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = GND		4.5 V	1		-0.5	µA
					2, 3		-10.0	
				5.5V	1		-0.5	µA
					2, 3		-10.0	
Input current high 3010	I_{IH}	For input under test $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND	TDI, TMS inputs	5.5 V	1		2.8	µA
					2, 3		3.7	
			All other inputs		1		0.1	
					2, 3		1.0	
Input current low 3009	I_{IL}	For input under test V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND	TDI, TMS inputs	5.5 V	1, 2, 3	-160	-385	µA
			All other inputs		1		-0.1	
					2, 3		-1.0	
Output short circuit current 3011	I_{OS} 6/	For all inputs, $V_{IN} = V_{CC}$ or GND $V_{OUT} = 0.0\ V$		5.5 V	1, 2, 3	-100		mA
Quiescent supply current 3005	I_{CC}	For all other inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = open	TDI,TMS = V_{CC}	5.5 V	1		16.0	µA
					2, 3		168.0	
			TDI,TMS = GND		1		750.0	
					2, 3		930.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 method	Symbol	Test conditions -55°C ≤ T_C ≤ +125°C 2/ 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Quiescent supply current delta, TTL input levels	ΔI_{CC} 7/	For input under test V_{IN} = V_{CC} – 2.1 V For all other inputs V_{IN} = V_{CC} or GND	TDI/TMS inputs	5.5 V	1, 2, 3		2.15	mA
			All other inputs				2.00	
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C		5.0 V	4		10.0	pF
Output capacitance 3012	C_{OUT} 5/			5.0 V	4		23.0	pF
Power dissipation capacitance	C_{PD} 8/			5.0 V	4		35.0	pF
Low level ground bounce noise	V_{OLP} 9/	V_{IH} = 3.0 V, V_{IL} = 0.0 V T_C = +25°C See figure 6 See 4.4.1b		5.0 V	4		800	mV
Low level ground bounce noise	V_{OLV} 9/			5.0 V	4		-800	mV
High level V_{CC} bounce noise	V_{OHP} 9/			5.0 V	4		(V_{OH} +800)	mV
High level V_{CC} bounce noise	V_{OHV} 9/			5.0 V	4		(V_{OH} -800)	mV
Functional tests 3014	10/	For all inputs, V_{IN} = 2.0 V or 0.8 V Verify output voltage, V_{OUT} See 4.4.1d		4.5 V	7, 8	L	H	
				5.5 V				
NORMAL OPERATION								
Propagation delay time, ACP, BCP to AO_n, BO_n 3003	t_{PLH1} 11/	C_L = 50 pF minimum R_L = 500Ω See figure 7		4.5 V	9	2.5	9.5	ns
					10, 11	2.5	11.0	
	t_{PHL1} 11/				9	2.5	10.3	
					10, 11	2.5	12.0	
Propagation delay time output enable $\overline{AOE}$, $\overline{BOE}$ to AO_n, BO_n 3003	t_{PZH1} 11/			4.5 V	9	2.0	10.0	ns
					10, 11	2.0	11.0	
	t_{PZL1} 11/				9	2.0	12.0	
					10, 11	2.0	13.5	
Propagation delay time output disable $\overline{AOE}$ / $\overline{BOE}$ to AO_n / BO_n 3003	t_{PHZ1} 11/			4.5 V	9	1.5	9.0	ns
					10, 11	1.5	10.3	
	t_{PLZ1} 11/				9	1.5	9.0	
					10, 11	1.5	10.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
NORMAL OPERATION – Continued.							
Setup time, high or low, AI_n, BI_n to ACP, BCP	t_{s1} 12/	C_L = 50 pF minimum R_L = 500Ω See figure 7	4.5 V	9,10,11	3.0		ns
Hold time, high or low, ACP, BCP to AI_n, BI_n	t_{h1} 12/		4.5 V	9,10,11	1.5		ns
Pulse width, high or low, ACP, BCP	t_{w1} 12/		4.5 V	9,10,11	5.0		ns
Output skew	t_{OSHL} t_{OSLH} 13/		4.5 V	9,10,11		1.0	ns
Maximum clock frequency, ACP, BCP	f_{MAX} 12/		4.5 V	9	100		MHz
				10, 11	70		
SCAN TEST OPERATION							
Propagation delay time, TCK to TDO 3003	t_{PHL2} 11/	C_L = 50 pF minimum R_L = 500Ω See figure 7	4.5 V	9	3.5	13.2	ns
				10, 11	3.5	15.5	
	t_{PLH2} 11/			9	3.5	13.0	ns
				10, 11	3.5	15.8	
Propagation delay time, output enable TCK to TDO 3003	t_{PZH2} 11/		4.5 V	9	3.0	13.0	ns
				10, 11	3.0	15.0	
	t_{PZL2} 11/			9	4.5	14.5	ns
				10, 11	4.5	16.7	
Propagation delay time, output disable TCK to TDO 3003	t_{PHZ2} 11/		4.5 V	9	2.5	11.5	ns
				10, 11	2.5	12.6	
	t_{PLZ2} 11/			9	2.5	11.0	ns
				10, 11	2.5	12.8	
Propagation delay time, TCK to data out, during update -DR state 3003	t_{PLH3} 11/		4.5 V	9	5.0	17.8	ns
				10, 11	5.0	21.2	
	t_{PHL3} 11/			9	5.0	18.0	ns
				10, 11	5.0	21.7	
Propagation delay time, output disable, TCK to data out, during update-DR state 3003	t_{PLZ3} 11/		4.5 V	9	4.5	16.2	ns
				10, 11	4.5	19.6	
	t_{PHZ3} 11/			9	4.0	16.4	ns
				10, 11	4.0	18.9	
Propagation delay time, output enable, TCK to data out, during update-DR state 3003	t_{PZL3} 11/		4.5 V	9	6.0	18.9	ns
				10, 11	6.0	22.6	
	t_{PZH3} 11/			9	5.0	16.5	ns
				10, 11	5.0	19.7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
SCAN TEST OPERATION – Continued.							
Propagation delay time, TCK to data out, during update-IR state 3003	t_{PLH4} 11/	C_L = 50 pF minimum R_L = 500Ω See figure 7	4.5 V	9	5.0	17.8	ns
				10, 11	5.0	21.2	
	t_{PHL4} 11/			9	5.0	18.6	ns
				10, 11	5.0	21.0	
Propagation delay time, output disable, TCK to data out, during update-IR state 3003	t_{PLZ4} 11/		4.5 V	9	5.0	19.0	ns
				10, 11	5.0	22.4	
	t_{PHZ4} 11/			9	5.0	19.5	ns
				10, 11	5.0	22.4	
Propagation delay time, output enable, TCK to data out, during update-IR state 3003	t_{PZL4} 11/		4.5 V	9	7.0	22.4	ns
				10, 11	7.0	26.2	
	t_{PZH4} 11/			9	6.5	19.9	ns
				10, 11	6.5	23.1	
Propagation delay time, TCK to data out, during test logic reset 3003	t_{PLH5} 11/		4.5 V	9	5.5	18.8	ns
				10, 11	5.5	21.5	
	t_{PHL5} 11/			9	5.5	19.9	ns
				10, 11	5.5	23.0	
Propagation delay time, output enable TCK to data out, during test logic reset 3003	t_{PZL5} 11/		4.5 V	9	5.0	23.8	ns
				10, 11	5.0	27.4	
	t_{PZH5} 11/			9	5.0	21.4	ns
				10, 11	5.0	24.5	
Propagation delay time, output disable TCK to data out, during test logic reset 3003	t_{PLZ5} 11/		4.5 V	9	5.0	19.8	ns
				10, 11	5.0	23.3	
	t_{PHZ5} 11/			9	5.0	19.9	ns
				10, 11	5.0	22.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 2/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
SCAN TEST OPERATION – Continued.							
Setup time, high or low, data to TCK	t_{S2} 12/ 14/	C_L = 50 pF minimum R_L = 500Ω See figure 7	4.5 V	9, 10, 11	3.0		ns
Minimum hold time, high or low, TCK to data	t_{h2} 12/ 14/		4.5 V	9, 10, 11	4.5		ns
Setup time, high or low, $\overline{AOE}$, $\overline{BOE}$ to TCK	t_{s3} 12/ 15/		4.5 V	9, 10, 11	3.0		ns
Hold time, high or low, TCK to $\overline{AOE}$, $\overline{BOE}$	t_{h3} 12/ 15/		4.5 V	9, 10, 11	4.5		ns
Setup time, high or low, internal $\overline{AOE}$, $\overline{BOE}$ to TCK	t_{s4} 12/ 16/		4.5 V	9, 10, 11	3.0		ns
Hold time, high or low TCK to Internal $\overline{AOE}$, $\overline{BOE}$	t_{h4} 12/ 16/		4.5 V	9, 10, 11	3.0		ns
Setup time, high or low, ACP, BCP to TCK	t_{s5} 12/ 17/		4.5 V	9, 10, 11	3.0		ns
Setup time, high or low, TCK to ACP, BCP	t_{h5} 12/ 17/		4.5 V	9, 10, 11	3.5		ns
Minimum setup time, high or low TMS to TCK	t_{s6} 12/		4.5 V	9, 10, 11	8.0		ns
Minimum hold time, high or low, TCK to TMS	t_{h6} 12/		4.5 V	9, 10, 11	2.0		ns
Minimum setup time, high or low, TDI to TCK	t_{s7} 12/		4.5 V	9, 10, 11	4.0		ns
Minimum hold time, high or low, TCK to TDI	t_{h7} 12/		4.5 V	9, 10, 11	4.5		ns
Pulse width, TCK high	t_{w2} 12/		4.5 V	9, 10, 11	12.0		ns
Pulse width, TCK low	t_{w3} 12/		4.5	9, 10, 11	5.0		ns
Maximum TCK clock frequency	f_{MAX} 12/		4.5 V	9, 10, 11	25		MHz
Wait time power-up to TCK	tpu 12/		4.5 V	9, 10, 11		100	ns
Power-down delay time	tpd 12/		4.5 V	9, 10, 11		100	ms

See footnotes on next page.

1/ For the method not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the ΔI_{CC} and I_{CC} tests, the output terminals shall be open. When performing the ΔI_{CC} and I_{CC} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet the limits specified in table I, as applicable, at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

5/ Three-state output conditions are required.

6/ This test shall be performed on output at a time with a maximum 2 ms duration.

7/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ -2.1 V (alternate method). When the test is performed using the alternate test method, the maximum limits is equal to the number of inputs at a high TTL input level times 2.0 mA or 2.15 mA, as applicable; and the preferred method and limits are guaranteed. When testing the TDI input, the TMS input shall be open. When testing the TMS input, the TDI input shall be open.

8/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). Where

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$

and f is the frequency of the input signal, n is the number of device inputs at TTL levels; and d is the duty cycle of the input signal.

9/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 5). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested that, whenever possible, this distance be kept to less than .25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 6). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 6). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

TABLE I. Electrical performance characteristics - Continued.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. For V_{OUT} measurements: H ≥ 1.5 V and L < 1.5 V.

11/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum propagation delay time limits for V_{CC} = 5.5 V shall be guaranteed to be no more than 0.5 ns less than those specified at V_{CC} = 4.5 V in table I, herein. For propagation delay tests, all paths must be tested.

12/ This parameter shall be guaranteed, if not tested, to the limits in table I, herein.

13/ This parameter is guaranteed, if not tested, to the limits specified in table I herein. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device: AO_m and AO_k; AO_m and BO_n; BO_m and BO_k; where k = 0 to 8, m = 0 to 8, and n = 0 to 8, and where m ≠. k. The specification applies to any outputs switching in the same direction, either high-to-low (t_{OSHL}) or low-to-high (t_{OSLH}). The limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V.

14/ This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26, and 27-35.

15/ This timing parameter pertains to boundary-scan register 38 and 41 only.

16/ This delay represents the timing relationship between $\overline{AOE}$ / $\overline{BOE}$ and TCK for scan cells 36 and 39 only.

17/ This timing parameter pertains to boundary-scan registers 37 and 40 only.

18/ Manufacturer (CAGE 3V146) tested Positive and Negative input clamp voltage (V_{IC}^+ and V_{IC}^-) at test condition V_{CC} = 4.5 V.

Bottom brazed flat pack

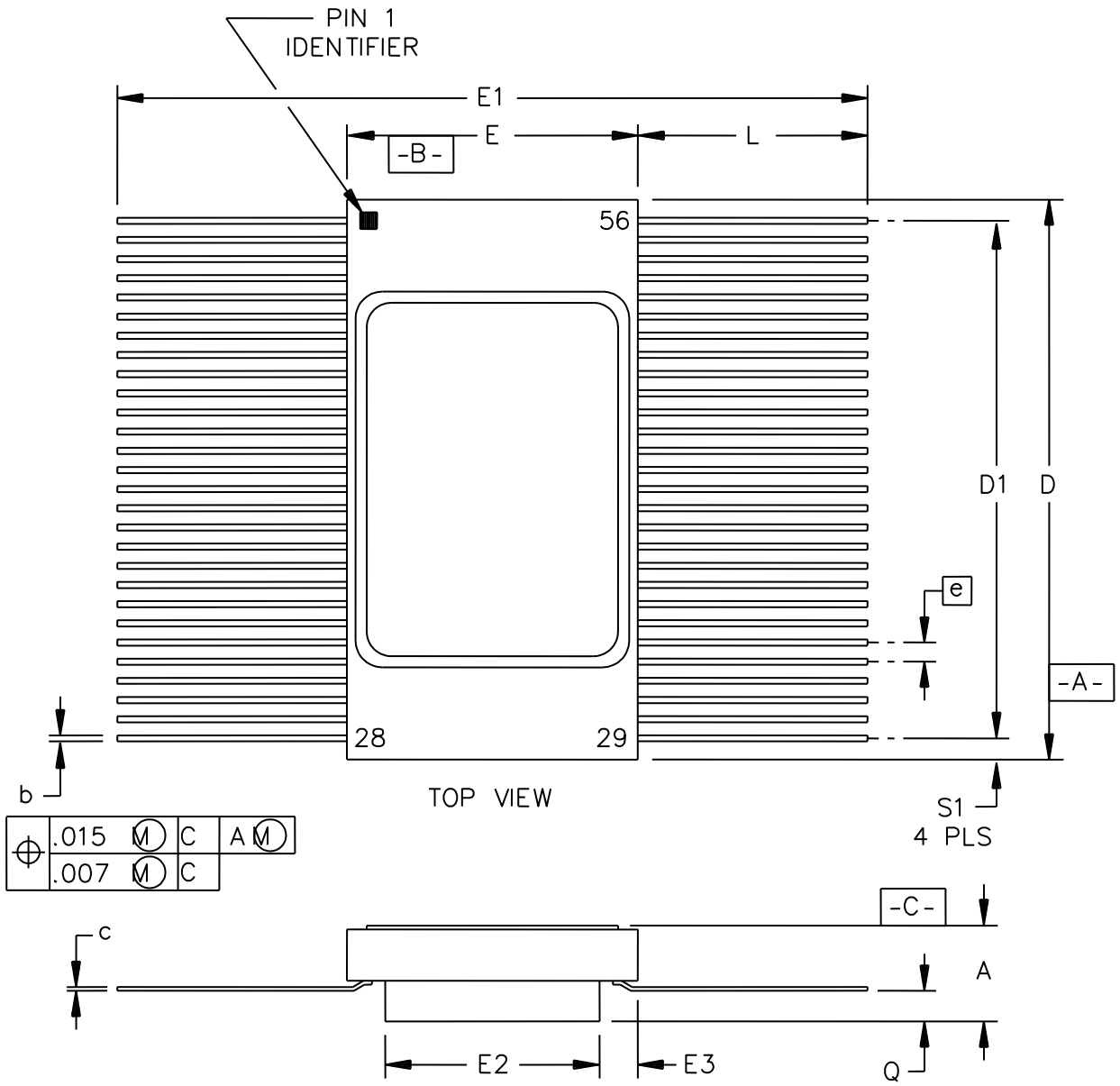


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-93207
		REVISION LEVEL E	SHEET 13

1/ Symbol	All dimensions are in inches			
	F-20 Configuration B			
	Min	Nom	Max	Note
A	.075	0.98	.120	2
b	.006	0.08	.013	
b1	.006	0.08	.010	
c	.004	.006	.009	
c1	.004	.005	.006	
D	- - -	- - -	.740	3
D1				
E	.370	.380	.390	
E1	- - -	- - -	.410	3
E2	.270			
E3	.030			4
E4				
E5				
e	.025 BSC			
k	.003	.005	.007	5
l	.250	.310	.370	
Q	.026	0.35	.045	6
S1	.005	- - -	- - -	
S2				
α				
M	- - -	- - -	.0015	
N	56			

NOTES:

1/. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dimension k) may be used to identify pin one. This tab may be located on either side of terminal one as shown in detail A, or it may be located on terminal one as shown in detail B.

2/ Dimension "A" controls the overall package thickness. When a window lid is used, dimension "A" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).

3/ This dimension allows for off-center lid, meniscus, and glass overrun.

4/ For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

5/ If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.

6/. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by .0015 inch (0.038 mm) maximum when solder dip lead finish is applied.

FIGURE 1. Case outline – Continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	TMS	15	BO_0	29	TCK	43	AI_8
2	AO_0	16	BO_1	30	BI_8	44	AI_7
3	$\overline{AOE}$	17	GND	31	BCP	45	GND
4	AO_1	18	BO_2	32	BI_7	46	AI_6
5	AO_2	19	BO_3	33	BI_6	47	AI_5
6	GND	20	V_{CC}	34	GND	48	V_{CC}
7	AO_3	21	BO_4	35	BI_5	49	AI_4
8	AO_4	22	BO_5	36	BI_4	50	AI_3
9	V_{CC}	23	GND	37	V_{CC}	51	GND
10	AO_5	24	BO_6	38	BI_3	52	AI_2
11	AO_6	25	BO_7	39	BI_2	53	AI_1
12	GND	26	$\overline{BOE}$	40	GND	54	ACP
13	AO_7	27	BO_8	41	BI_1	55	AI_0
14	AO_8	28	TDO	42	BI_0	56	TDI

Terminal descriptions	
Terminal symbol	Description
AI_n, BI_n (n = 0 to 8)	Data Inputs
AO_n, BO_n (n = 0 to 8)	Outputs
$\overline{AOE}$, $\overline{BOE}$	Output enable control inputs
ACP	Clock pulse A inputs
BCP	Clock pulse B inputs
TDI	Test data input
TDO	Test data output
TMS	Test mode select input
TCK	Test clock input

FIGURE 2. Terminal connections.

Inputs			Outputs
ACP	$\overline{AOE}$	AI_n	AO_n
X	H	X	Z
↑	L	L	L
↑	L	H	H

Inputs			Outputs
BCP	$\overline{BOE}$	BI_n	BO_n
X	H	X	Z
↑	L	L	L
↑	L	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
↑ = Low-to-high clock transition

FIGURE 3. Truth table.

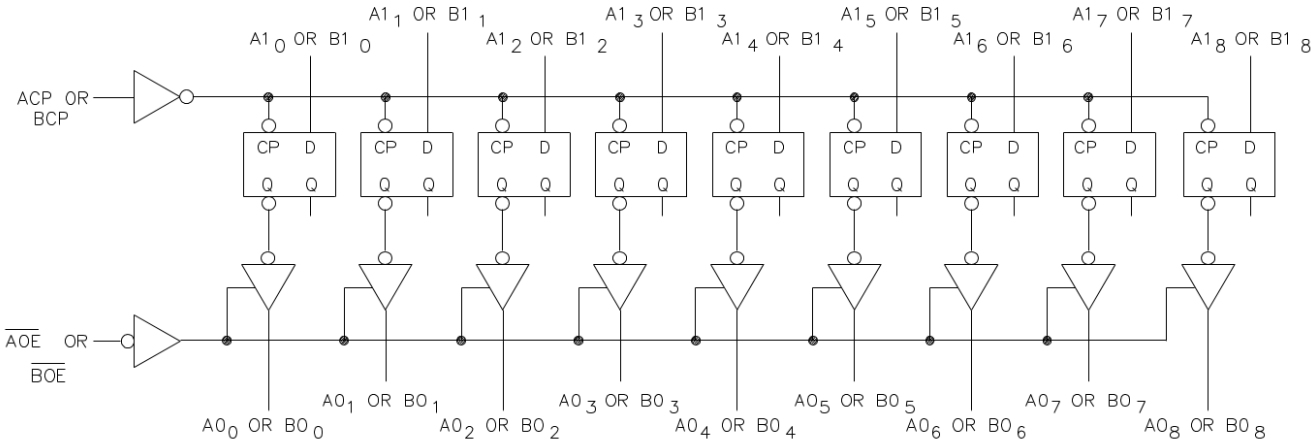
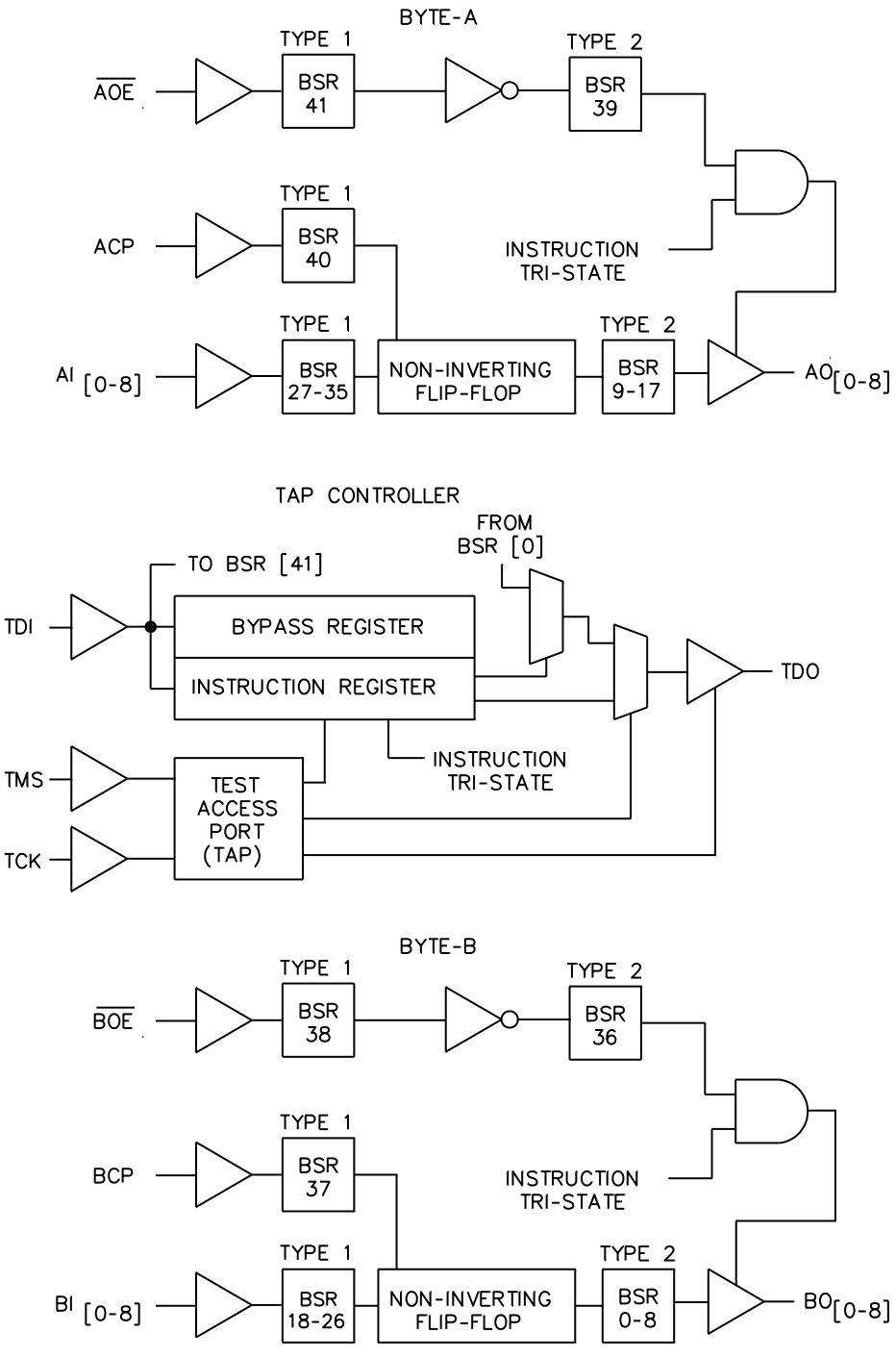


FIGURE 4. Block diagram.



NOTES:
1. BSR = Boundary scan register.
2. See figure 5 for further description.

FIGURE 4. Block diagram – Continued.

Boundary scan register scan chain definition

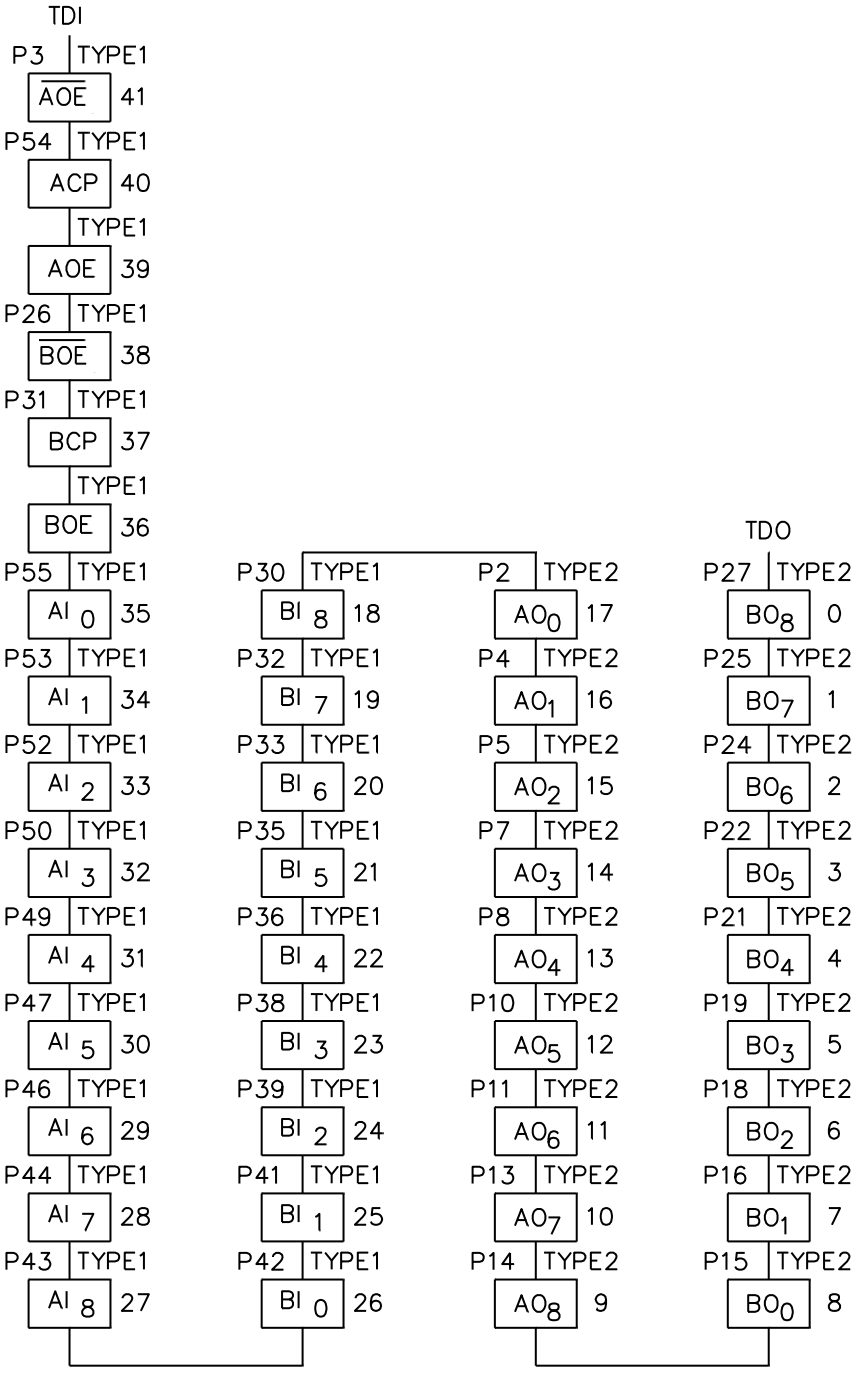
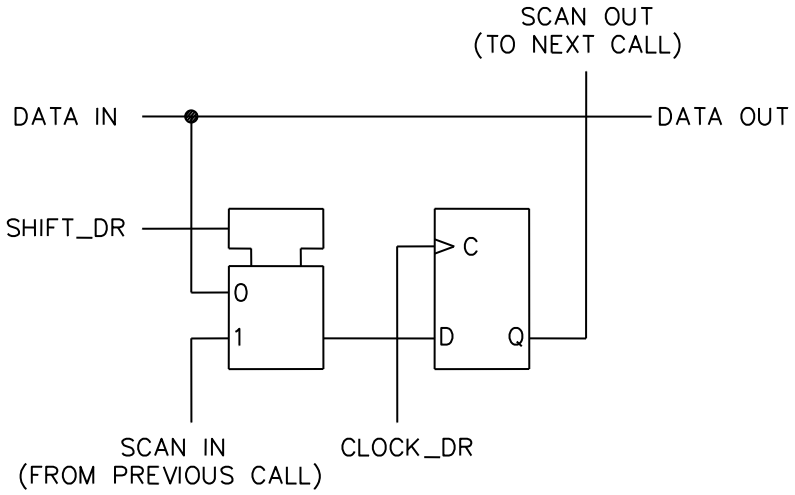


FIGURE 5. Description of boundary-scan circuitry.

The scan cells used in the boundary-scan register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 for a further description of the scan cells.)

Scan Cell TYPE1
Located on each system input pin



Scan Cell TYPE2
Located at each system output pin as well as at each
of the two internal active-high output enable signals

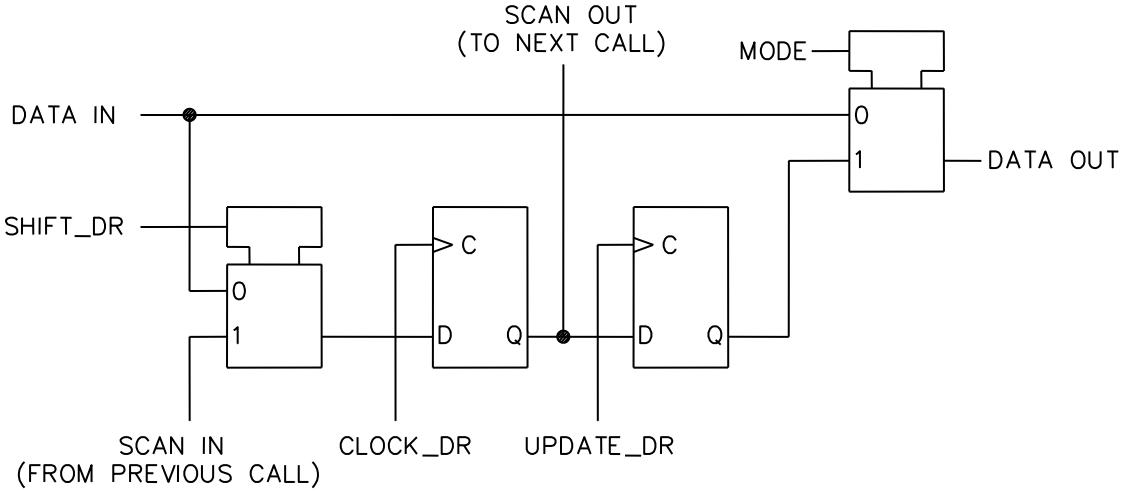
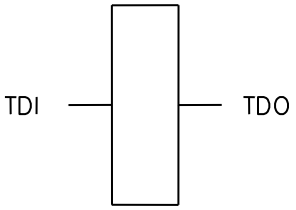


FIGURE 5. Description of boundary-scan circuitry – Continued.

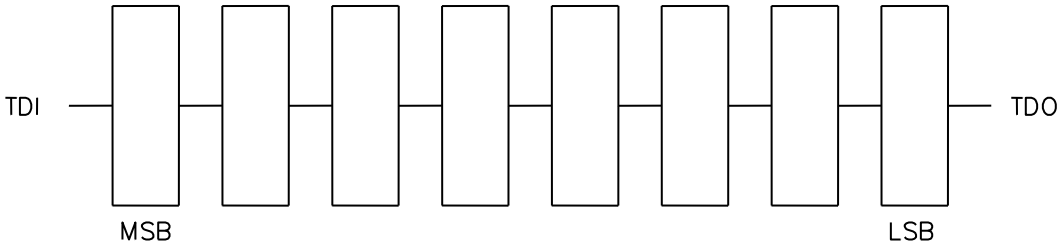
The bypass register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass register scan chain definition
Logic 0



The instruction register is an eight-bit register which captures the value 00011101.

Instruction register scan chain definition

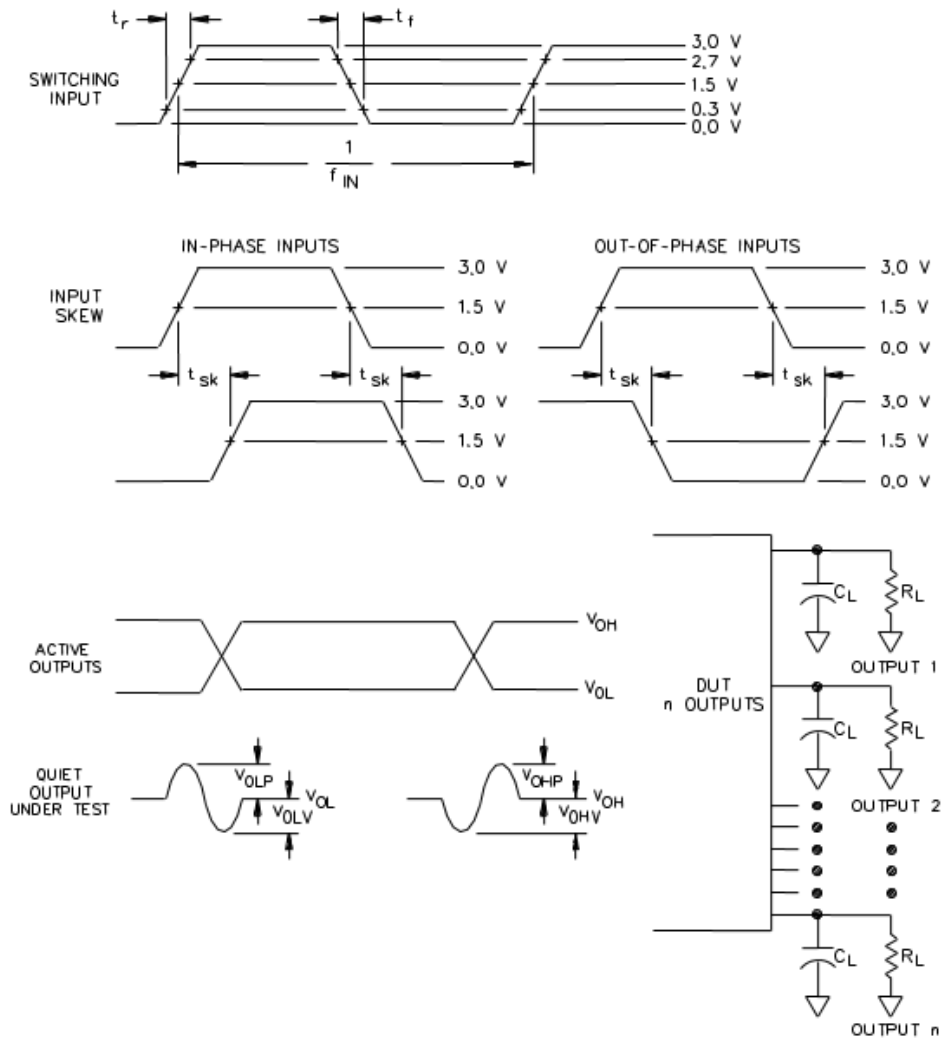


MSB → LSB

Instruction code	Instruction
00000000	EXTEXT
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All others	BYPASS

Note: For further information on boundary-scan circuitry, see IEEE 1149.1.

FIGURE 5. Description of boundary-scan circuitry – Continued.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 6. Ground bounce load circuit and waveforms.

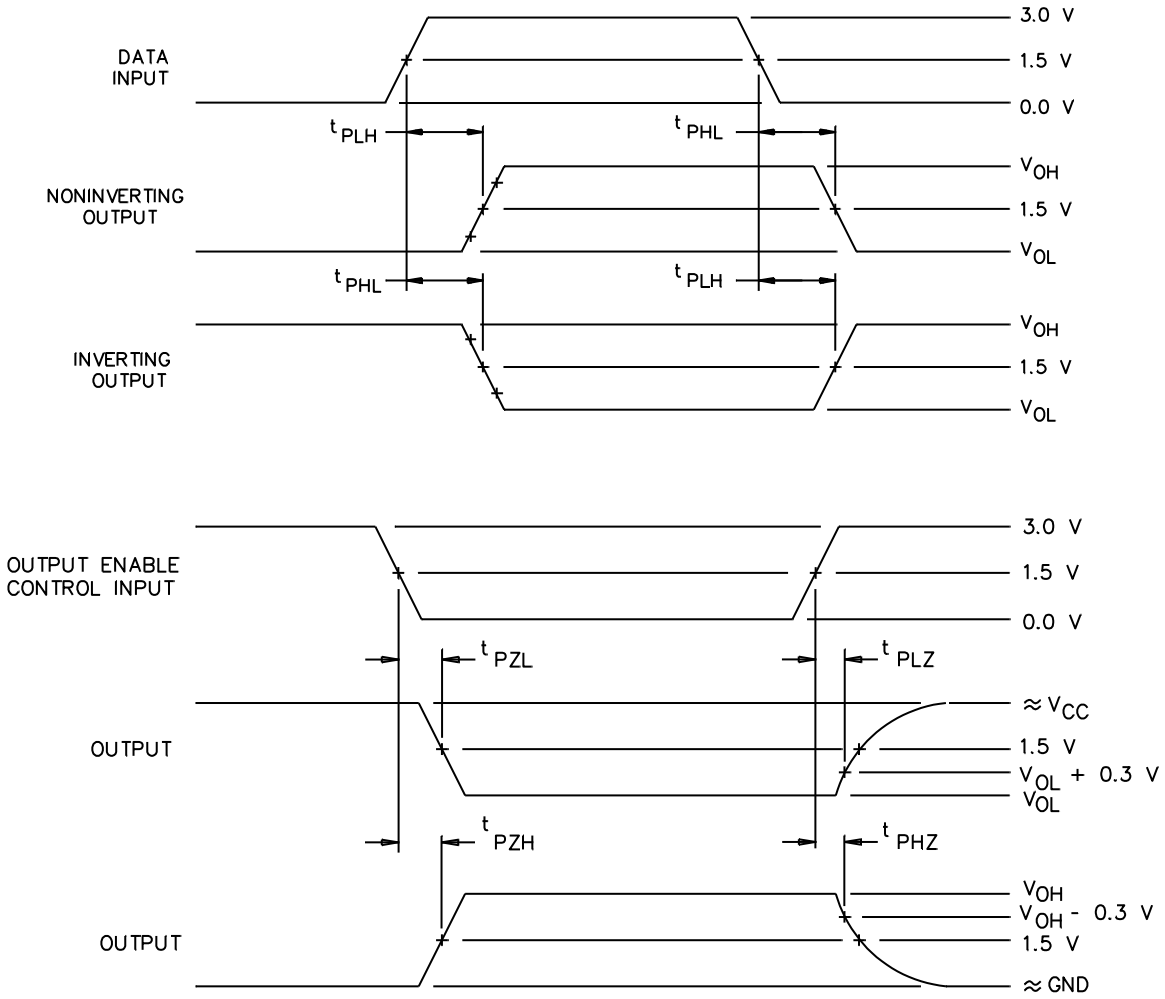


FIGURE 7. Switching waveforms and test circuit.

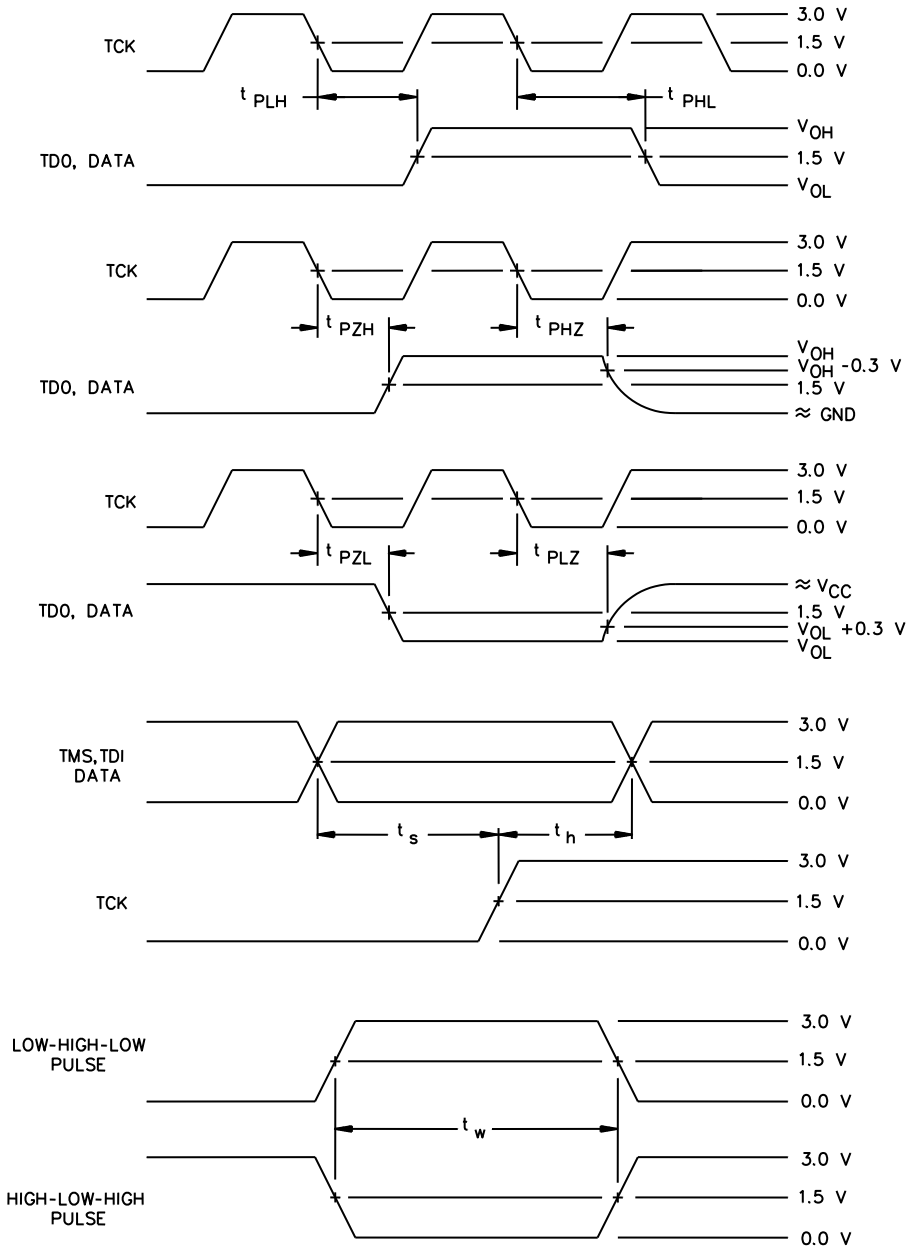
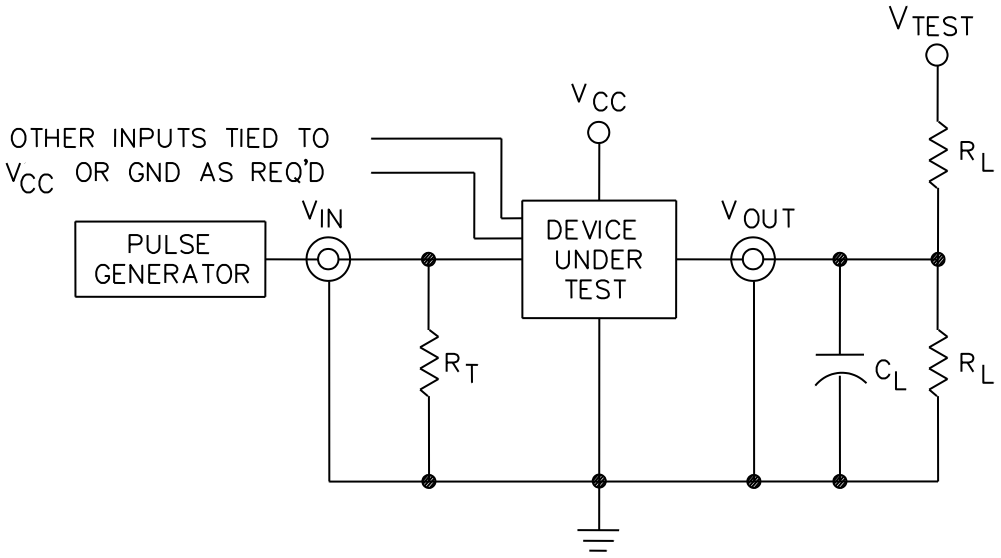


FIGURE 7. Switching waveforms and test circuit – Continued.



NOTES:

1. When measuring t_{PLZ} and t_{PZL} : V_{test} = 7.0 V
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL} : V_{test} = open
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is low at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is high at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance)
5. R_L = 500Ω or equivalent
6. R_T = 50Ω or equivalent
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; duty cycle = 50 percent; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V, and 2.7 V to 0.3 V, respectively.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 7. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime -VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime -VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime -VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test."

For V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV} tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

c. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD-20 and table I, herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

For C_{IN}, C_{OUT}, and C_{PD}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN}, C_{OUT}, and C_{PD} tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DLA Land and Maritime -VA the device functions listed in each functional group and the test results for each device tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1	1
Final electrical parameters (see 4.2)	1/ 1,2,3,7,8,9	1/ 1, 2, 3 ,7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9. 10, 11
Group A test requirements (see 4.4)	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8, 9, 10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1, 2, 3	1, 2 , 3, 4, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1,2,3	1, 2, 3	1, 2, 3, 4, 7, 8, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1,7,9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-01-24

Approved sources of supply for SMD 5962-93207 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply a https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9320701MXA	3/	SCAN18374TFMQB
	3V146	SCAN18374T/MXA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics, LLC 16 Malcolm Hoyt Drive Newburyport, MA 01950