Rochester Electronics

Datasheet

PART NUMBER

54175BEA-ROCS

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Rochester Electronics®

Datasheet

54174, 54175

Microcircuits, Digital, TTL, Flip-Flops, Monolithic Silicon

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FOR REFERENCE ONLY

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INCH POUND

MIL-M-38510/17B
3 May 2005
SUPERSEDING
MIL-M-38510/17A(USAF)
1 May 1979

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

Inactive for new design after 7 September 1995.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic, silicon, TTL, bistable logic gating microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	Hex, D-type, positive edge triggered flip-flops with clear and single outputs
02	Quad, D-type, positive edge triggered flip-flops with clear and complementary outputs

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat-pack

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -12 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation per flip-flop, (P_D) 1/	
Device type 01	73 mW
Device type 02	65 mW
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	(See MIL-STD-1835)
Junction temperature (T_J) 2/	175°C

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc
Normalized fanout (each output) 3/	10 maximum
Case operating temperature range (T_C)	-55°C to 125°C
Input setup time	
Data input	25 ns
Clear inactive state	30 ns
Input hold time	5 ns

2.0 APPLICABLE DOCUMENT

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Must withstand the added P_D due to short circuit condition (e.g. I_{OS}).
2/ Maximum junction temperature should not be exceeded except in accordance with allowable short duration burn-in screening condition in accordance with MIL-PRF-38535.
3/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Logic diagram and terminal connections. The logic diagram terminal connections shall be as specified on figure 1 and 2, respectively.

3.3.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 3.

3.3.3 Schematic circuit. The schematic circuit shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.4 Case outlines. Case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. Lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table 1 and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 3 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -800 µA	All	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V; I_{IN} = 16 mA	All		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; I_{IN} = -12 mA; T_C = 25°C	All		-1.5	V
Low-level input current	I_{IL1}	V_{CC} = 5.5 V; V_{IN} = 0.4 V 2/	All	-0.3	-1.6	mA
	I_{IL2}	V_{CC} = 5.5 V; V_{IN} = 0.4 V 3/	All	-0.4	-1.6	mA
	I_{IL3}	V_{CC} = 5.5 V; V_{IN} = 0.4 V 4/	All	-0.3	-0.8	mA
High-level input current	I_{IH1}	V_{CC} = 5.5 V; V_{IN} = 2.4 V	All		40	µA
	I_{IH2}	V_{CC} = 5.5 V; V_{IN} = 5.5 V	All		100	µA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V; V_{IN} = 0	All	-20	-57	mA
Supply current per device	I_{CC}	V_{CC} = 5.5 V; V_{IN} = 5.5 V	01		65	mA
			02		45	mA
Maximum clock frequency	f_{MAX}	V_{CC} = 5 V; C_L = 50 pF ± 10% R_L = 390 Ω ± 5%	All	25		MHz
Propagation delay to high logic level (clear to $\overline{Q}$)	t_{PLH1}		02	5	36	ns
Propagation delay to low logic level (clear to Q)	t_{PHL1}		All	5	50	ns
Propagation delay to high logic level (clock to Q)	t_{PLH2}		All	5	43	ns
Propagation delay to low logic level (clock to Q)	t_{PHL2}		All	5	43	ns
Propagation delay to high logic level (clock to $\overline{Q}$)	t_{PLH3}		02	5	43	ns
Propagation delay to low logic level (clock to $\overline{Q}$)	t_{PHL3}		02	5	43	ns

1/ See table III for complete terminal conditions.
2/ Clock input for device types 01 and 02.
3/ Clear input for device types 01 and 02.
4/ All D inputs for device types 01 and 02.

TABLE II. Electrical test requirements.

MIL-PRF-38535 Test requirement	Subgroups (see table III)	
	Class S Devices	Class B Devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9,
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3, 9, 10, 11	N/A
Groups C end point electrical parameters	1, 2, 3, 9, 10, 11	1, 2, 3
Additional electrical subgroups for Group C periodic inspections	None	10, 11
Group D end point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6, shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.

c. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

DEVICE TYPE 01

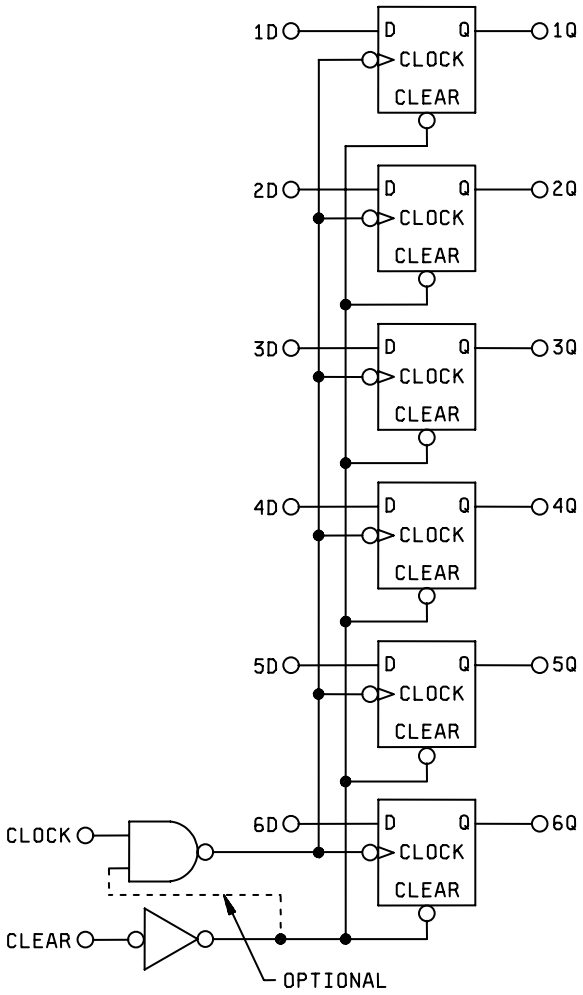


Figure 1. Logic diagrams.

DEVICE TYPE 02

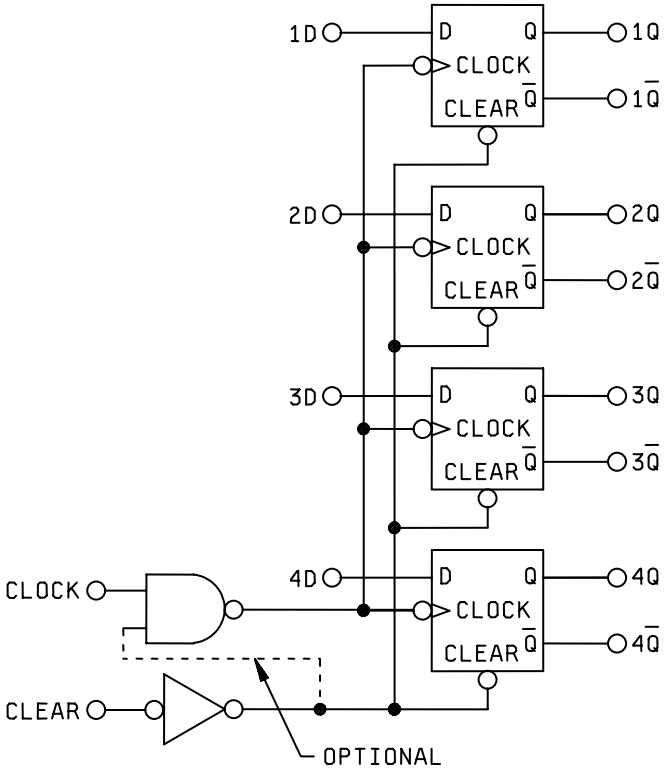


Figure 1. Logic diagrams - Continued.

Terminal number	Device type 01	Device type 02
	Cases E and F	Cases E and F
1	CLEAR	CLEAR
2	1Q	1Q
3	1D	$1\overline{Q}$
4	2D	1D
5	2Q	2D
6	3D	$2\overline{Q}$
7	3Q	2Q
8	GND	GND
9	CLOCK	CLOCK
10	4Q	3Q
11	4D	$3\overline{Q}$
12	5Q	3D
13	5D	4D
14	6D	$4\overline{Q}$
15	6Q	4Q
16	V_{CC}	V_{CC}

Figure 2. Terminal connections.

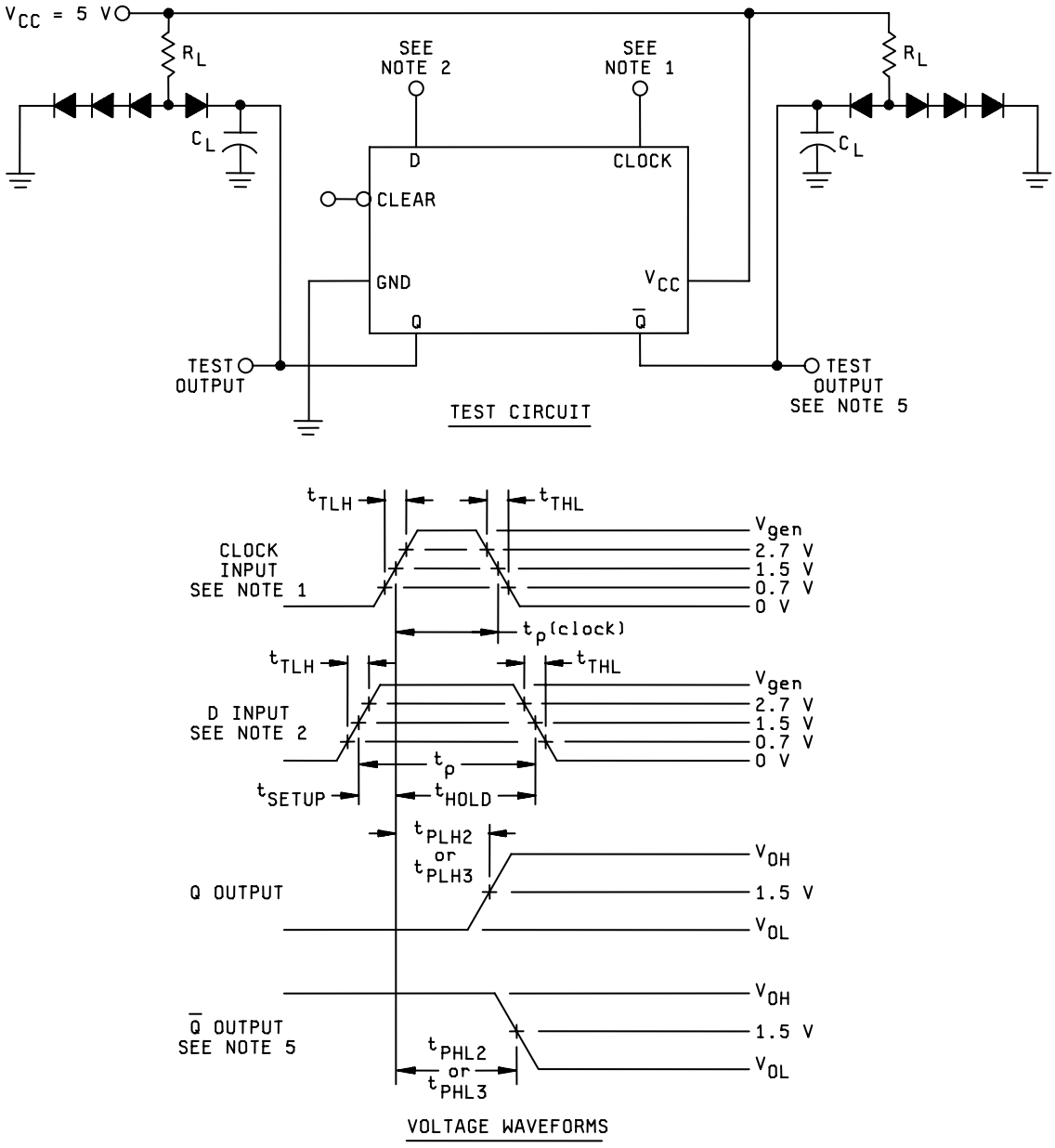
Truth table for each flip-flop				
CLEAR	CLOCK	D	Q	$\overline{Q}$ *
L	X**	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q0	$\overline{Q}$ 0

* Device type 02 only.

** Input may be high, low or open circuit.

NOTE:
Clear is independent of clock. Information at the D input meeting the setup time requirements is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive going pulse. When the clock input is either high or low level, the D input signal has no effect at the output.

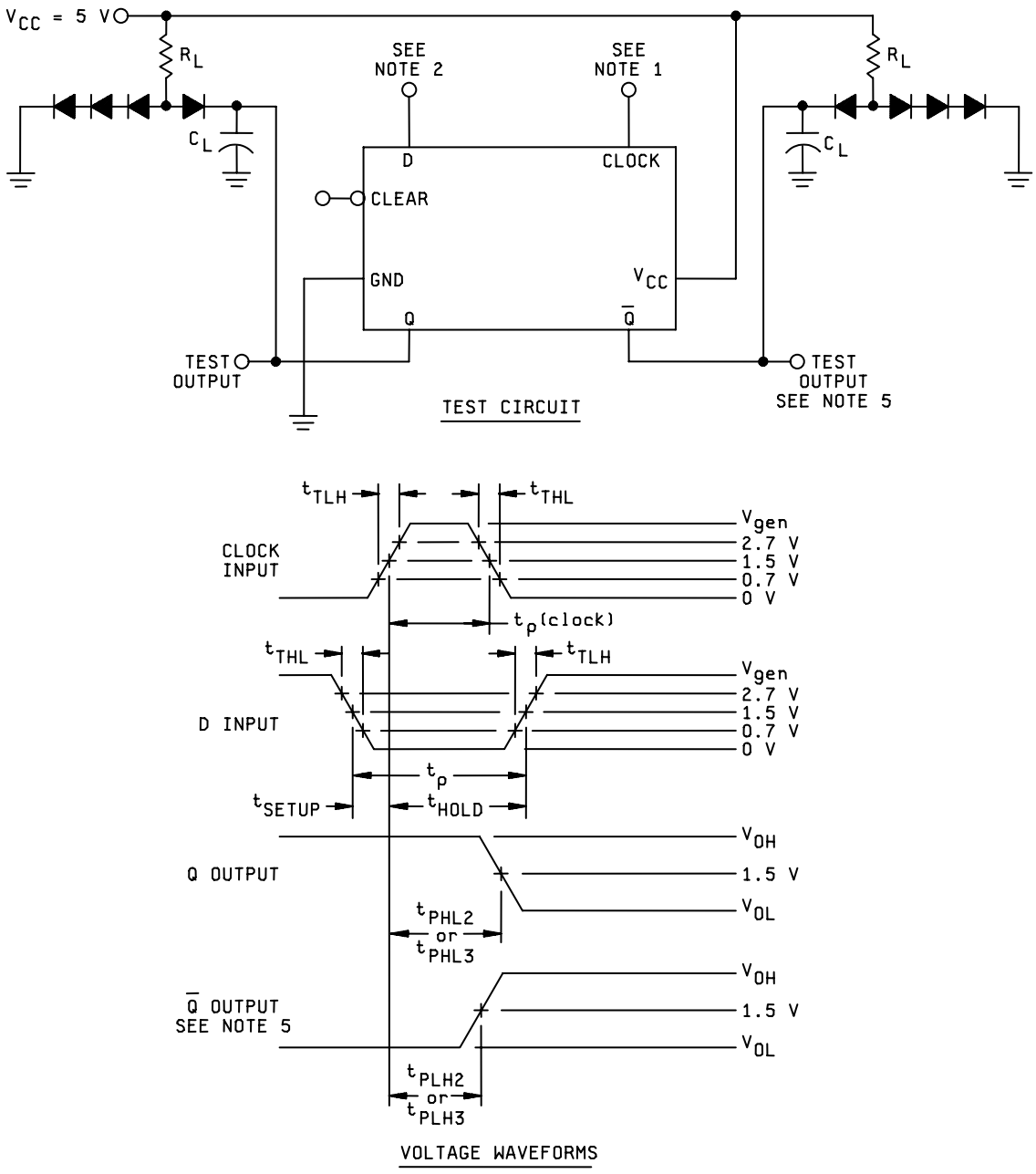
FIGURE 3. Truth table.



NOTES:

1. Clock input has the following characteristics: Vgen = 3 V minimum, t_P = 20 ns, $t_{THL} = t_{TLH} \leq 10$ ns, and PRR $\leq$ 1 MHz. When testing f_{MAX} PRR = 25 MHz.
2. D input pulse has the following characteristics: Vgen = 3 V minimum, $t_{THL} = t_{TLH} \leq 10$ ns, t_P = 30 ns, t_{SETUP} = 25 ns, t_{HOLD} = 5 ns and PRR $\leq$ 0.5 MHz. When testing f_{MAX} PRR = 12.5 MHz at 50% $\pm$ 15% duty cycle.
3. R_L = 390 $\Omega \pm$ 5%; C_L = 50 pF $\pm$ 10% (including jig and probe capacitance).
4. All diodes are 1N3064 or equivalent.
5. $\overline{Q}$ output applies to device type 02 only.

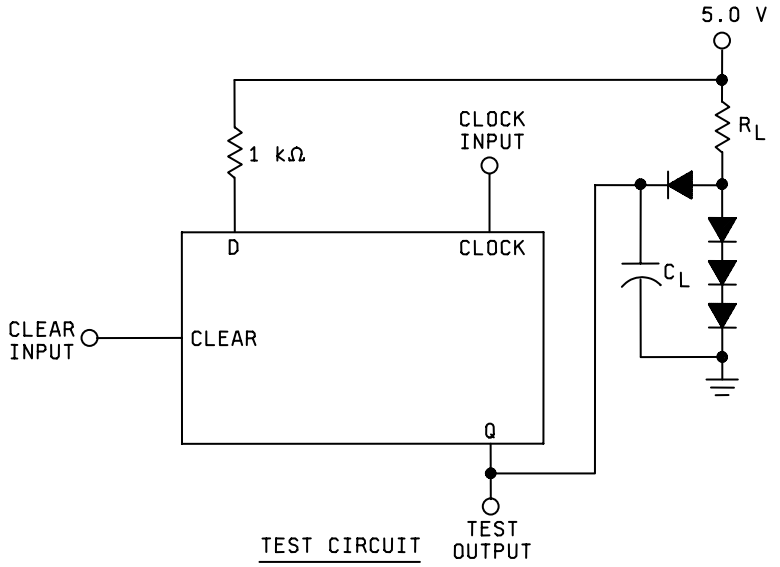
Figure 4. Synchronous switching test circuit (high level data) for device types 01 and 02.



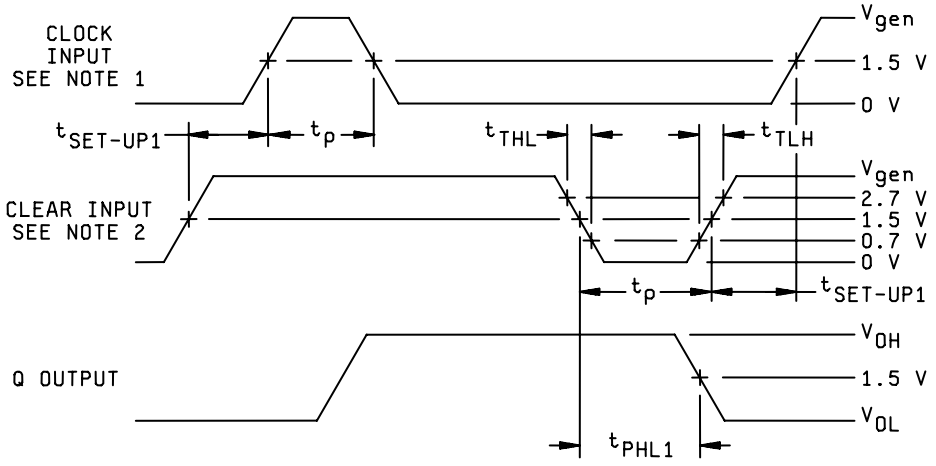
NOTES:

1. Clock input has the following characteristics: Vgen = 3 V minimum, t_P = 20 ns, $t_{THL} = t_{TLH} \leq 10$ ns, and PRR $\leq$ 1 MHz. When testing f_{MAX} PRR = 25 MHz.
2. D input pulse has the following characteristics: Vgen = 3 V minimum, $t_{THL} = t_{TLH} \leq 10$ ns, t_P = 30 ns, t_{SETUP} = 25 ns, t_{HOLD} = 5 ns and PRR $\leq$ 0.5 MHz. When testing f_{MAX} PRR = 12.5 MHz at 50% $\pm$ 15% duty cycle.
3. R_L = 390 $\Omega \pm$ 5%; C_L = 50 pF $\pm$ 10% (including jig and probe capacitance).
4. All diodes are 1N3064 or equivalent.
5. $\overline{Q}$ output applies to device type 02 only.

Figure 5. Synchronous switching test circuit (low level data) for device types 01 and 02.



TEST CIRCUIT

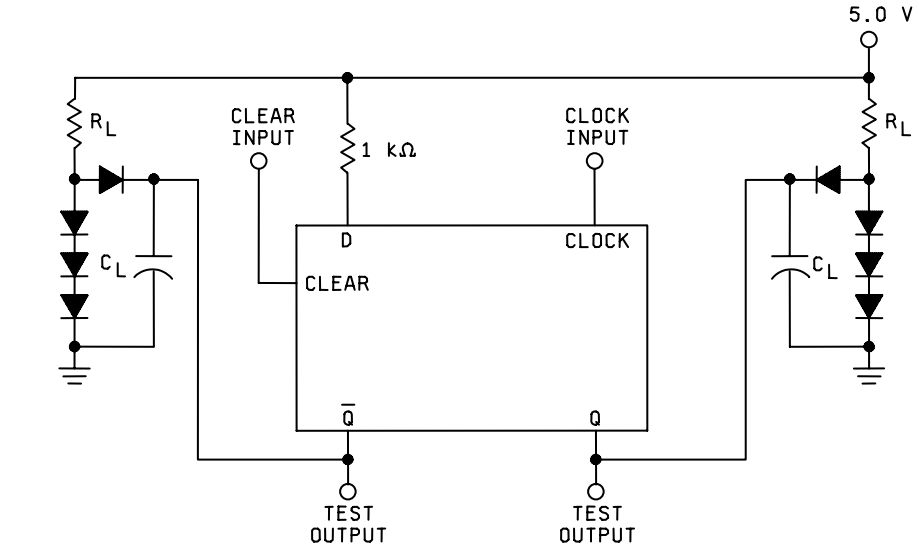


VOLTAGE WAVEFORMS

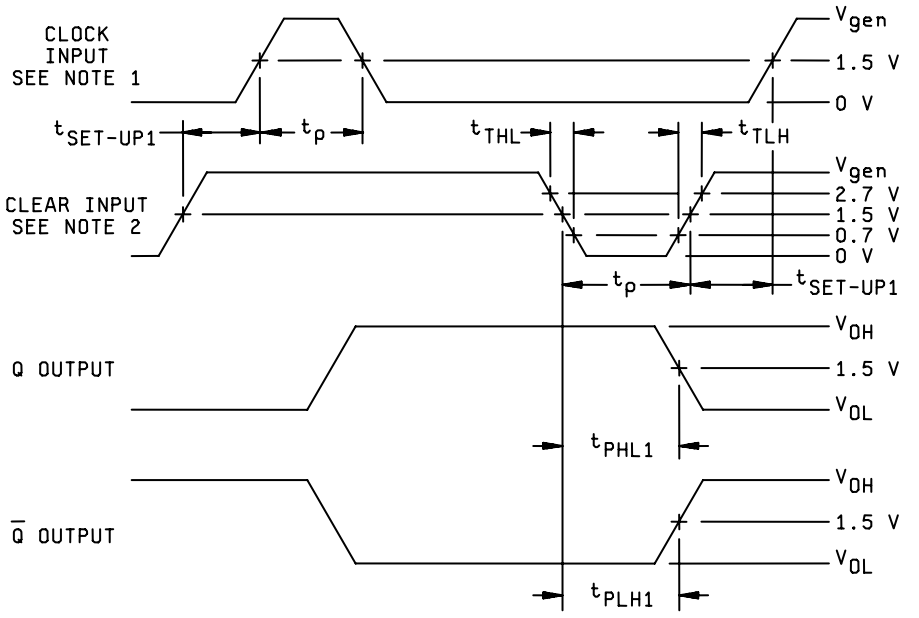
NOTES:

1. Clock input pulse is a preconditioning pulse and has the following characteristics: Vgen = 3 V minimum, $t_P \leq 100$ ns, $t_{SETUP} = 25$ ns, and PRR ≤ 1 MHz.
2. Clear input pulse has the following characteristics: Vgen = 3 V minimum, $t_{THL} = t_{TLH} \leq 10$ ns, $t_P = 30$ ns, and PRR ≤ 1 MHz.
4. All diodes are 1N3064 or equivalent.
3. $R_L = 390\ \Omega \pm 5\%$; $C_L = 50$ pF $\pm$ 10% (including jig and probe capacitance).

Figure 6. Clear switching test circuit and waveforms for device type 01.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

1. Clock input pulse is a preconditioning pulse and has the following characteristics: Vgen = 3 V minimum, $t_P \leq 100$ ns, $t_{SETUP} = 25$ ns, and PRR ≤ 1 MHz.
2. Clear input pulse has the following characteristics: Vgen = 3 V minimum, $t_{THL} = t_{TLH} \leq 10$ ns, $t_P = 30$ ns, and PRR ≤ 1 MHz.
4. All diodes are 1N3064 or equivalent.
3. $R_L = 390\ \Omega \pm 5\%$; $C_L = 50$ pF $\pm 10\%$ (including jig and probe capacitance).

Figure 7. Clear switching test circuit and waveforms for device type 02.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be high ≥ 2.0V or low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clear	2 1Q	3 1D	4 2D	5 2Q	6 3D	7 3Q	8 GND	9 Clock	10 4Q	11 4D	12 5Q	13 5D	14 6D	15 6Q	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1 T_C = 25°C	V_{IC}		1	-12mA		-12mA					GND								4.5V	Clear		-1.5	V
	"		2				-12mA		-12mA		"								"	1D		"	"
	"		3								"								"	2D		"	"
	"		4								"	-12mA							"	3D		"	"
	"		5								"								"	Clock		"	"
	"		6								"			-12mA					"	4D		"	"
	"		7								"					-12mA			"	5D		"	"
	"		8								"						-12mA		"	6D		"	"
	V_{OH}	3007	9	2.0V	-.8mA	2.0V					"	B							"	1Q	2.4		"
	"	"	10	"	"		2.0V	-.8mA			"	"							"	2Q	"		"
	"	"	11	"	"				2.0V	-.8mA	"	"							"	3Q	"		"
	"	"	12	"	"						"	"	-.8mA	2.0V					"	4Q	"		"
	"	"	13	"	"						"	"			-.8mA	2.0V			"	5Q	"		"
	"	"	14	"	"						"	"					2.0V	-.8mA	"	6Q	"		"
	V_{OL}	3008	15	0.8V	16mA			16mA			"								"	1Q		0.4	"
	"	"	16	"	"					16mA	"								"	2Q		"	"
	"	"	17	"	"						"		16mA						"	3Q		"	"
	"	"	18	"	"						"				16mA				"	4Q		"	"
	"	"	19	"	"						"								"	5Q		"	"
	"	"	20	"	"						"							16mA	"	6Q		"	"
	I_{IL1}	3009	21 CKT A,C,D								"	0.4V							5.5V	Clock	-0.7	-1.6	mA
	"	"	21 CKT B								"	0.4V							"	Clock	-0.3	-0.8	"
	"	"	21 CKT E								"	0.4V							"	Clock	-0.4	-1.3	"
	I_{IL2}	"	22 CKT A,D,E	0.4V							"								"	Clear	-0.4	-1.3	"
	I_{IL2}	"	22 CKT B,C	0.4V							"								"	Clear	-0.7	-1.6	"
	I_{IL3}	"	23			0.4V					"								"	1D	-0.3	-0.8	"
	"	"	24				0.4				"								"	2D	"	"	"
	"	"	25						0.4V		"								"	3D	"	"	"
	"	"	26								"			0.4V					"	4D	"	"	"
	"	"	27								"					0.4V			"	5D	"	"	"
	"	"	28								"						0.4V		"	6D	"	"	"
	I_{IH1}	3010	29	2.4V		2.4V					"								"	Clear		40	µA
	"	"	30				2.4V				"								"	1D		"	"
	"	"	31						2.4V		"								"	2D		"	"
	"	"	32								"	2.4V							"	3D		"	"
	"	"	33								"			2.4V					"	Clock		"	"
	"	"	34								"								"	4D		"	"
	"	"	35								"					2.4V			"	5D		"	"
	"	"	36								"						2.4V		"	6D		"	"
	I_{IH2}	3010	37	5.5V		5.5V					"								"	Clear		100	µA
	"	"	38				5.5V				"								"	1D		"	"
	"	"	39						5.5V		"								"	2D		"	"
	"	"	40								"	5.5V							"	3D		"	"
	"	"	41								"			5.5V					"	Clock		"	"
	"	"	42								"					5.5V			"	4D		"	"
	"	"	43								"						5.5V		"	5D		"	"
	"	"	44								"								"	6D		"	"
	I_{OS}	3011	45	5.5V	GND	5.5V					"	B							"	1Q	-20	-57	mA
	"	"	46	"			5.5V	GND			"	"							"	2Q	"	"	"
	"	"	47	"					5.5V	GND	"	"							"	3Q	"	"	"
	"	"	48	"							"	"	GND	5.5V					"	4Q	"	"	"
	"	"	49	"							"	"			GND	5.5V			"	5Q	"	"	"
	"	"	50	"							"	"					5.5V	GND	"	6Q	"	"	"
	I_{CC}	3005	51	5.5V		5.5V	5.5V		5.5V			B		5.5V		5.5V	5.5V		"	V_{CC}		65	"

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01. – Continued.
Terminal conditions (pins not designated may be high ≥ 2.0V or low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clear	2 1Q	3 1D	4 2D	5 2Q	6 3D	7 3Q	8 GND	9 Clock	10 4Q	11 4D	12 5Q	13 5D	14 6D	15 6Q	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
2	Same tests, terminal conditions and limits as subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																						
7 2/ 4/ T_C = 25°C	Truth table test	3014	52 53 54 55 56 57 58 59 60 61 62 63 64	B B B A “ “ “ “ “ “ “ “ B	L “ “ “ “ H H H L L H H L	A “ “ “ “ “ B B B A “ “ “	A “ “ “ “ “ B B B A “ “ “	L “ “ “ “ H H H L L H H L	A “ “ “ “ “ B B B A “ “ “	L “ “ “ “ H H H L L H H L	GND “ “ “ “ “ “ “ “ “ “ “ “	B A B B B A A B A B A B B	L “ “ “ “ H H H L L H H L	A “ “ “ “ “ B B B A “ “ “	L “ “ “ “ H H H L L H H L	A “ “ “ “ “ B B B A “ “ “	A “ “ “ “ “ B B B A “ “ “	L “ “ “ “ H H H L L H H L	5.0 V “ “ “ “ “ “ “ “ “ “ “ “	All outputs “ “ “ “ “ “ “ “ “ “ “ “	3/		
8 2/ 4/	Repeat subgroup 7 at T_C = 125°C and T_C = -55°C.																						
9 T_C = 25°C	f_{MAX} 5/	(Fig 4)	65 66 67 68 69 70	5.0 V “ “ “ “ “	OUT “ “ “ “ “	IN “ “ “ “ “	IN	OUT	IN	OUT	GND “ “ “ “ “	IN “ “ “ “ “	OUT	IN	OUT	IN	IN	OUT	5.0 V “ “ “ “ “	1Q 2Q 3Q 4Q 5Q 6Q	25 “ “ “ “ “		MHz “ “ “ “ “
	t_{PHL1}	3003 (Fig 6)	71 72 73 74 75 76	IN “ “ “ “ “	OUT “ “ “ “ “	5.0 V “ “ “ “ “	5.0 V	OUT	5.0 V	OUT	“ “ “ “ “ “	“ “ “ “ “ “	OUT	5.0 V	OUT	5.0 V	5.0 V	OUT	“ “ “ “ “ “	Clear-1Q Clear-2Q Clear-3Q Clear-4Q Clear-5Q Clear-6Q	5 “ “ “ “ “	38 “ “ “ “ “	ns “ “ “ “ “
	t_{PLH2}, t_{PHL2}	3003 (Fig 4 & 5)	77 & 78 79 & 80 81 & 82 83 & 84 85 & 86 87 & 88	5.0 V “ “ “ “ “	OUT “ “ “ “ “	IN “ “ “ “ “	IN	OUT	IN	OUT	“ “ “ “ “ “	“ “ “ “ “ “	OUT	IN	OUT	IN	IN	OUT	“ “ “ “ “ “	Clock-1Q Clock-2Q Clock-3Q Clock-4Q Clock-5Q Clock-6Q	“ “ “ “ “ “	33 “ “ “ “ “	“ “ “ “ “ “
10 T_C = 125°C	f_{MAX} 5/	(Fig 4)	89 90 91 92 93 94	5.0 V “ “ “ “ “	OUT “ “ “ “ “	IN “ “ “ “ “	IN	OUT	IN	OUT	“ “ “ “ “ “	“ “ “ “ “ “	OUT	IN	OUT	IN	IN	OUT	“ “ “ “ “ “	1Q 2Q 3Q 4Q 5Q 6Q	25 “ “ “ “ “		MHz “ “ “ “ “
	t_{PHL1}	3003 (Fig 6)	95 96 97 98 99 100	IN “ “ “ “ “	OUT “ “ “ “ “	5.0 V “ “ “ “ “	5.0 V	OUT	5.0 V	OUT	“ “ “ “ “ “	“ “ “ “ “ “	OUT	5.0 V	OUT	5.0 V	5.0 V	OUT	“ “ “ “ “ “	Clear-1Q Clear-2Q Clear-3Q Clear-4Q Clear-5Q Clear-6Q	5 “ “ “ “ “	50 “ “ “ “ “	ns “ “ “ “ “
	t_{PLH2}, t_{PHL2}	3003 (Fig 4 & 5)	101 & 102 103 & 104 105 & 106 107 & 108 109 & 110 111 & 112	5.0 V “ “ “ “ “	OUT “ “ “ “ “	IN “ “ “ “ “	IN	OUT	IN	OUT	“ “ “ “ “ “	“ “ “ “ “ “	OUT	IN	OUT	IN	IN	OUT	“ “ “ “ “ “	Clock-1Q Clock-2Q Clock-3Q Clock-4Q Clock-5Q Clock-6Q	“ “ “ “ “ “	43 “ “ “ “ “	“ “ “ “ “ “
11	Same tests, terminal conditions and limits as subgroup 10, except T_C = -55°C.																						

TABLE III. Group A inspection for device type 01. – Continued.
Terminal conditions (pins not designated may be high ≥ 2.0V or low ≤ 0.8 V or open).

1/ B = Momentary GND, then V_{CC}.
2/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.
3/ Output voltages shall be either:
(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high-speed checker double comparator, or
(b) H > 1.5 V and L < 1.5 V when using a high-speed checker single comparator.
4/ Only a summary of attributes data is required.
5/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be high ≥ 2.0V or low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clear	2 1Q	3 $1\overline{Q}$	4 1D	5 2D	6 $2\overline{Q}$	7 2Q	8 GND	9 Clock	10 3Q	11 $3\overline{Q}$	12 3D	13 4D	14 $4\overline{Q}$	15 4Q	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1 T_C = 25°C	V_{IC}		1	-12 mA							GND								4.5 V	Clear		-1.5	V
	"		2				-12 mA				"								"	1D		"	"
	"		3					-12 mA			"								"	2D		"	"
	"		4								"	-12 mA							"	Clock		"	"
	"		5								"				-12 mA				"	3D		"	"
	"		6								"					-12 mA			"	4D		"	"
	V_{OH}	3007	7	2.0 V	-.8 mA		2.0 V				"	B							"	1Q	2.4		"
	"	"	8	"				2.0 V		-.8 mA	"	"							"	2Q	"		"
	"	"	9	"							"	"	-.8 mA		2.0 V				"	3Q	"		"
	"	"	10	"							"	"				2.0 V		-.8 mA	"	4Q	"		"
	"	"	11	0.8 V		-.8 mA					"								"	$1\overline{Q}$	"		"
	"	"	12	"					-.8 mA		"								"	$2\overline{Q}$	"		"
	"	"	13	"							"			-.8 mA					"	$3\overline{Q}$	"		"
	"	"	14	"							"						-.8 mA		"	$4\overline{Q}$	"		"
	V_{OL}	"	15	2.0 V		16 mA	2.0 V				"	B							"	$1\overline{Q}$		0.4 V	"
	"	"	16	"				2.0 V	16 mA		"	"							"	$2\overline{Q}$		"	"
	"	"	17	"							"	"		16 mA	2.0 V				"	$3\overline{Q}$		"	"
	"	"	18	"							"	"				2.0 V	16 mA		"	$4\overline{Q}$		"	"
	"	"	19	0.8 V	16 mA						"								"	1Q		"	"
	"	"	20	"						16 mA	"								"	2Q		"	"
	"	"	21	"							"		16 mA						"	3Q		"	"
	"	"	22	"							"							16 mA	"	4Q		"	"
	I_{IL1}	3009	23 CKT A,C,D								"	0.4 V							5.5 V	Clock	-0.7	-1.6	mA
	"	"	23 CKT B								"	0.4 V							"	Clock	-0.3	-0.8	"
	"	"	23 CKT E								"	0.4 V							"	Clock	-0.4	-1.3	"
	I_{IL2}	"	24 CKT A,D,E	0.4 V							"								"	Clear	-0.4	-1.3	"
	I_{IL2}	"	24 CKT B,C	0.4 V							"								"	Clear	-0.7	-1.6	"
	I_{IL3}	"	25				0.4 V				"								"	1D	-0.3	-0.8	"
	"	"	26					0.4 V			"								"	2D	"	"	"
	"	"	27								"				0.4 V				"	3D	"	"	"
	"	"	28								"					0.4 V			"	4D	"	"	"
	I_{IH1}	3010	29	2.4 V							"								"	Clear		40	µA
	"	"	30				2.4 V				"								"	1D		"	"
	"	"	31					2.4 V			"								"	2D		"	"
	"	"	32								"	2.4 V							"	Clock		"	"
	"	"	33								"				2.4 V				"	3D		"	"
	"	"	34								"					2.4 V			"	4D		"	"
	I_{IH2}	"	35	5.5 V							"								"	Clear		100	"
	"	"	36				5.5 V				"								"	1D		"	"
	"	"	37					5.5 V			"								"	2D		"	"
	"	"	38								"	5.5 V							"	Clock		"	"
	"	"	39								"				5.5 V				"	3D		"	"
	"	"	40								"					5.5 V			"	4D		"	"

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be high ≥ 2.0V or low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clear	2 1Q	3 $1\overline{Q}$	4 1D	5 2D	6 $2\overline{Q}$	7 2Q	8 GND	9 Clock	10 3Q	11 $3\overline{Q}$	12 3D	13 4D	14 $4\overline{Q}$	15 4Q	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1 T_C = 25°C	I_{OS}	3011	41	5.5 V	GND		5.5 V				GND	B							5.5 V	1Q	-20	-57	mA
	"	"	42	"				5.5 V		GND	"	"							"	2Q	"	"	"
	"	"	43	"							"	"	GND		5.5 V				"	3Q	"	"	"
	"	"	44	"							"	"				5.5 V		GND	"	4Q	"	"	"
	"	"	45	GND		GND					"								"	$1\overline{Q}$	"	"	"
	"	"	46	"					GND		"								"	$2\overline{Q}$	"	"	"
	"	"	47	"							"			GND					"	$3\overline{Q}$	"	"	"
	"	"	48	"							"						GND		"	$4\overline{Q}$	"	"	"
	I_{CC}	3005	49	5.5 V			5.5 V	5.5 V				B			5.5 V	5.5 V				V_{CC}		45	"
2	Same tests, terminal conditions and limits as subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																						
7 2/ 4/ T_C = 25°C	I_{OS}	3014	50	B	L	H	A	A	H	L	GND	B	L	H	A	A	H	L	5.0 V	All outputs	3/		
	"	"	51	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"	"	"			
	"	"	52	B	"	"	"	"	"	"	"	B	"	"	"	"	"	"	"	"				
	"	"	53	A	"	"	"	"	"	"	"	B	"	"	"	"	"	"	"	"				
	"	"	54	"	H	L	"	"	L	H	"	A	H	L	"	"	L	H	"	"				
	"	"	55	"	H	L	"	"	L	H	"	B	H	L	"	"	L	H	"	"				
	"	"	56	"	H	L	B	B	L	H	"	B	H	L	B	B	L	H	"	"				
	"	"	57	"	L	H	B	B	H	L	"	A	L	H	B	B	H	L	"	"				
	"	"	58	"	L	H	B	B	H	L	"	B	L	H	B	B	H	L	"	"				
	"	"	59	"	L	H	A	A	H	L	"	B	L	H	A	A	H	L	"	"				
	"	"	60	"	H	L	"	"	L	H	"	A	H	L	"	"	L	H	"	"				
	"	"	61	"	H	L	"	"	L	H	"	B	H	L	"	"	L	H	"	"				
	"	"	62	B	L	H	"	"	H	L	"	B	L	H	"	"	H	L	"	"				
8 2/ 4/	Repeat subgroup 7 at T_C = 125°C and T_C = -55°C.																						
9 T_C = 25°C	f_{MAX}	Fig 4	63	5.0 V	OUT		IN				GND	IN							5.0 V	1Q	25		MHz
	5/	"	64	"				IN		OUT	"	"							"	2Q	"		"
	"	"	65	"							"	"	OUT		IN				"	3Q	"		"
	"	"	66	"							"	"				IN		OUT	"	4Q	"		"
	t_{PLH1}	3003	67	IN		OUT	5.0 V				"	"							"	Clear-$1\overline{Q}$	5	28	ns
	"	Fig 7	68	"				5.0 V	OUT		"	"							"	Clear-$2\overline{Q}$	"	"	"
	"	"	69	"							"	"		OUT	5.0 V				"	Clear-$3\overline{Q}$	"	"	"
	"	"	70	"							"	"				5.0 V	OUT		"	Clear-$4\overline{Q}$	"	"	"
	t_{PHL1}	"	71	"	OUT		5.0 V				"	"							"	Clear-1Q	"	38	"
	"	"	72	"				5.0 V		OUT	"	"							"	Clear-2Q	"	"	"
	"	"	73	"							"	"	OUT		5.0 V				"	Clear-3Q	"	"	"
	"	"	74	"							"	"				5.0 V		OUT	"	Clear-4Q	"	"	"
	t_{PLH2},	3003	75 & 76	5.0 V	OUT		IN				"	"							"	Clock-1Q	"	33	"
	t_{PHL2}	Fig 4 & 5	77 & 78	"				IN		OUT	"	"							"	Clock-2Q	"	"	"
	"	"	79 & 80	"							"	"	OUT		IN				"	Clock-3Q	"	"	"
	"	"	81 & 82	"							"	"				IN		OUT	"	Clock-4Q	"	"	"
	t_{PLH3},	"	83 & 84	"		OUT	IN				"	"							"	Clock-$1\overline{Q}$	"	"	"
	t_{PHL3}	"	85 & 86	"				IN	OUT		"	"							"	Clock-$2\overline{Q}$	"	"	"
	"	"	87 & 88	"							"	"		OUT	IN				"	Clock-$3\overline{Q}$	"	"	"
	"	"	89 & 90	"							"	"				IN	OUT		"	Clock-$4\overline{Q}$	"	"	"

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be high ≥ 2.0V or low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clear	2 1Q	3 $1\overline{Q}$	4 1D	5 2D	6 $2\overline{Q}$	7 2Q	8 GND	9 Clock	10 3Q	11 $3\overline{Q}$	12 3D	13 4D	14 $4\overline{Q}$	15 4Q	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
10	f_{MAX}	Fig 4	91	5.0 V	OUT		IN				GND	IN							5.0 V	1Q	25		MHz
T_C = 125°C	5/	"	92	"				IN		OUT	"	"							"	2Q	"		"
	"	"	93	"							"	"	OUT		IN				"	3Q	"		"
	"	"	94	"							"	"				IN		OUT	"	4Q	"		"
	t_{PLH1}	3003	95	IN		OUT	5.0 V				"	"							"	$\text{Clear-1}\overline{Q}$	5	36	ns
	"	Fig 7	96	"				5.0 V	OUT		"	"							"	$\text{Clear-2}\overline{Q}$	"	"	"
	"	"	97	"							"	"		OUT	5.0 V				"	$\text{Clear-3}\overline{Q}$	"	"	"
	"	"	98	"							"	"				5.0 V	OUT		"	$\text{Clear-4}\overline{Q}$	"	"	"
	t_{PHL1}	"	99	"	OUT		5.0 V				"	"							"	Clear-1Q	"	50	"
	"	"	100	"				5.0 V		OUT	"	"							"	Clear-2Q	"	"	"
	"	"	101	"							"	"	OUT		5.0 V				"	Clear-3Q	"	"	"
	"	"	102	"							"	"				5.0 V		OUT	"	Clear-4Q	"	"	"
	t_{PLH2},	3003	103 & 104	5.0 V	OUT		IN				"	"							"	Clock-1Q	"	43	"
	t_{PHL2}	Fig 4 & 5	105 & 106	"				IN		OUT	"	"							"	Clock-2Q	"	"	"
	"	"	107 & 108	"							"	"	OUT		IN				"	Clock-3Q	"	"	"
	"	"	109 & 110	"							"	"				IN		OUT	"	Clock-4Q	"	"	"
	t_{PLH3},	"	111 & 112	"		OUT	IN				"	"							"	$\text{Clock-1}\overline{Q}$	"	"	"
	t_{PHL3}	"	113 & 114	"				IN	OUT		"	"							"	$\text{Clock-2}\overline{Q}$	"	"	"
	"	"	115 & 116	"							"	"		OUT	IN				"	$\text{Clock-3}\overline{Q}$	"	"	"
	"	"	117 & 118	"							"	"				IN	OUT		"	$\text{Clock-4}\overline{Q}$	"	"	"
11	Same tests, terminal conditions and limits as subgroup 10, except T_C = -55°C.																						

1/ B = Momentary GND, then V_{CC}.
2/ The tests in subgroups 7 and 8 shall be performed in the sequence specified.
3/ Output voltages shall be either:
(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
(b) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Only a summary of attributes data is required.
5/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one half of the input frequency.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.
b. PIN and compliance identifier, if applicable (see 1.2).
c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirement for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to acquiring activity in addition to notification to the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of method 5003), corrective action and reporting of results, if applicable.
g. Requirements for product assurance options.
h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
i. Requirements for "JAN" marking.
j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND ..... Electrical ground (common terminal)
V_{IN} ..... Voltage level at an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer lead lengths and lead forming shall not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Device type	Commercial type
01	54174
02	54175

6.8 Manufacturers" designations. Manufacturers" circuits included in this specification are designated as shown in table IV.

Table IV. Manufacturers" designations

Device type	National Semiconductor	Texas Instruments	Signetics	Motorola Inc.	Fairchild
	Circuits				
	A	B	C	D	E
01	X	X	X	X	X
02	X	X	X	X	X

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

(Project 5962-2106)

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force - 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.