



# SANYO Semiconductors

## DATA SHEET

# LV24030LP — Bi-CMOS IC

## FM Tuner IC for Small Portable Equipment

### Overview

The LV24030LP is FM tuner IC's that requires absolutely no external components for tuning.

They incorporates not only the FM tuner functions as well in a compact VQLP package with dimensions of only 4.0×4.0×0.8mm.

These IC's are simply ideal for incorporating FM tuner functions into mobile phones and other small mobile set where space is always at a premium.

### Functions

- FM FE
- FM IF
- MPX stereo decoder
- Tuning
- Standby

### Features

- No external components
- No alignments necessary
- Fully integrated low IF (140kHz) selectivity and demodulation
- Built in adjacent channel interface total reduction (no 114kHz, no 190kHz)
- Due to new tuning concept, the tuning is independent of the channel spacing
- Very high sensitivity due to integrated low noise RF input amplifier
- Very low power standby mode. No power switch circuitry required
- MPX output for RDS application
- 3-wire bus interface (Data, Clock, NR-W)
- Digital AFC-Tuner locks to frequency after tuning sequence
- 4 level programmable Soft Mute
- 4 level Programmable Stereo Blend

Continued on next page.

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**SANYO Semiconductor Co., Ltd.**

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## LV24030LP

Continued from preceding page.

- In combination with the host, fast, low power operation of present mode, manual search, automatic search and automatic present store are possible
- Covers all Japanese, European and US bands
- Built in voltage stabilizer
- Stereo pilot signal Cancellor

### Specifications

**Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max	Analog block supply voltage	5.0	V
	$V_{DD}$ max	Digital block supply voltage	4.5	V
Digital input voltage	$V_{IN1}$ max	Clock, Data, NR_W	$V_{DD}+0.3$	V
	$V_{IN2}$ max	External_clk_in	$V_{DD}+0.3$	V
Allowable power dissipation	$P_d$ max	$T_a \leq 70^\circ\text{C}$ , Mounted on a specified board *	140	mW
Operating temperature	$T_{opr}$		-20 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

Note: Mounted on a specified board: 40mm×50mm×0.8mm, glass epoxy

**Operating Condition** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}$	Analog block supply voltage	3.0	V
	$V_{DD}$	Digital block supply voltage	3.0	V
Operating supply voltage range	$V_{CC}$ op		2.6 to 4.0	V
	$V_{DD}$ op		2.5 to 4.0	V
	$V_{IO}$ op	Interface voltage	1.8 to 4.0	V

Note: The  $V_{IO}$  application voltage must be either equivalent to  $V_{DD}$  or the  $V_{DD}$  value or less. ( $V_{IO} \leq V_{DD}$ )

**Interface Block Allowable Operation Range** at  $T_a = -20$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		2.5		4.0	V
Digital block input (including the external clock)	$V_{IH}$	High level input voltage range	$0.7V_{IO}$		$V_{IO}$	V
	$V_{IL}$	Low level input voltage range	0		0.6	V
Digital block output	$I_{OL}$	Output current at Low level	2.0			mA
	$V_{OL}$	Output voltage at Low level $I_{OL}=2\text{mA}$			0.6	V
Clock input operating frequency	fclk	(Pin5) clock frequency for 3wire_bus			0.7	MHz
External clock operating frequency	fclk_ext	(Pin12) clock frequency for external input	32k		20M	Hz

Note: External clock input (pin12) allows also input of the sine wave signal.

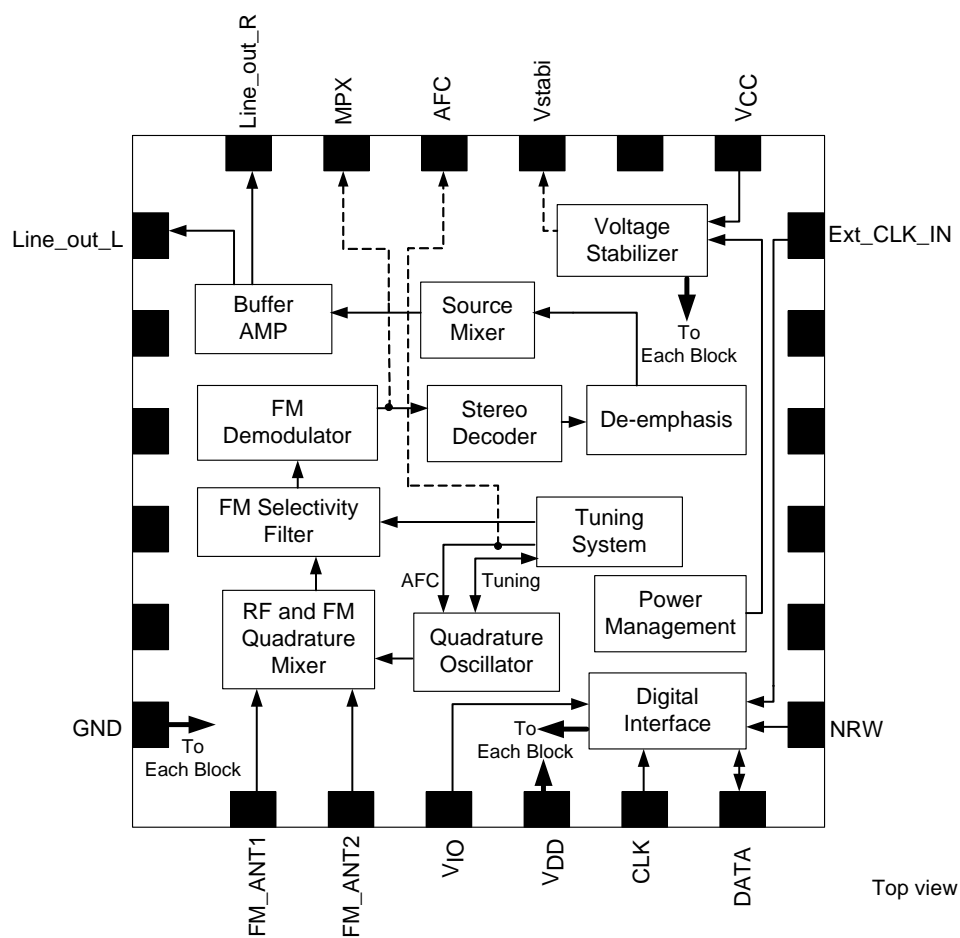
## LV24030LP

**Operating Characteristics** at Ta=25°C, V<sub>CC</sub>=3.0V, V<sub>DD</sub>=3.0V, Soft Mute/Soft Stereo=off, with the specified test circuit.

Output level setting is for the maximum output setting by setting Bit 4 and Bit 5 (Audio output level bits) of Address 04h of the control register map to "1" respectively. In other cases, the IF<sub>BW</sub> set Bit value is when the value has been set to 65% of the IF<sub>OSC</sub> set Bit value.

(Register setting for IF<sub>OSC</sub> set =140kHz and IF<sub>BW</sub>=140kHz\*0.65)

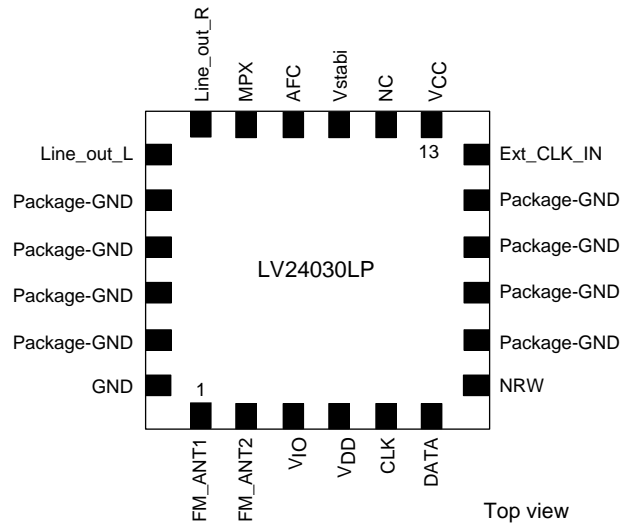
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain (in operation)	ICCA	Measurement at pin 13 with 60dBμ input in the analog block, Monaural input		12	17	mA
	ICCD	Measurement at pins 3 and 4 with 60dBμ input in the digital block		0.3	0.8	
Current drain (in standby)	ICCA	Measurement at pin 13 in the standby mode of the analog block		3	30	μA
	ICCD	Measurement at pins 3 and 4 in the standby mode of the digital block.		3	30	
FM receive band	F_range	When mounted to PCB with SANYO recommended conditions	76		108	MHz
<b>FM receiving characteristics MONO</b>						
: fc=80MHz, fm=1kHz, 22.5kHz dev. Note that Soft_stereo, Soft_and mute functions are OFF.						
3dB sensitivity	-3dB LS	60dBμV, 22.5kHz dev. output standard, -3dB input.		5	17	dBμV EMF
Practical sensitivity 1	QS1	Input level with S/N=30dB De-emphasis=75μs SG open display		8	16	dBμV
Practical sensitivity 2 (Reference)	QS2	Input level with S/N=26dB De-emphasis=75μs, SG terminal display		1.1		μV
Demodulator output	V <sub>O</sub>	60dBμV, pin 18, pin 19 output	80	110	160	mV
Channel balance	CB	60dBμV, pin 18 / pin 19 output	-2	0	2	dB
Signal-to-noise ratio	S/N	60dBμV, pin 18, pin 19 output	48	58		dB
Total harmonic distortion 1 (MONO)	THD1	60dBμV, pin 18, pin 19 output, 22.5kHz dev.		0.4	1.5	%
Total harmonic distortion 2 (MONO)	THD2	60dBμV, pin 18, pin 19 output, 75kHz dev.		1.3	3.0	%
Field intensity display level	FS	Input level at which FS1 changes to FS2, Reg04_bit3=0	3	10	20	dBμ
Mute attenuation	Mute-Att	60dBμV, pin 18, pin 19 output	60	70		dB
<b>FM receive characteristic STEREO characteristics</b>						
: fc=80MHz, fm=1kHz, V <sub>N</sub> =60dBμV, Pilot=10%(7.5kHz dev.)						
Separation	SEP	L-mod, Pin19, pin18 output L+R signals ≈30%(22.5kHz dev.)	20	35		dB
Total harmonic distortion (Main)	THD-ST	Main-mod (for L+R input), Pin19, pin18 output IHF_BPF, L+R=30%(22.5kHz dev.)		0.6	1.8	%



# LV24030LP

## Pin Discription

Pin	Name	Description	Remarks	DC_bias
1	FM-ANT1	Antenna input	FM signal input point	1V
2	FM-ANT2	Antenna GND	Connect to GND with capacitor	1V
3	VI/O	Digital interface supply voltage	Connect to power supply	
4	V <sub>DD</sub>	Digital supply voltage	Connect to power supply	
5	CLOCK	Digital interface Clock	Control pin	
6	DATA	Digital interface DATA	Control pin	
7	NR_W	Digital interface Read/Write	Control pin	
8	Package-GND	GND for package-shield	Connect to GND	
9	Package-GND	GND for package-shield	Connect to GND	
10	Package-GND	GND for package-shield	Connect to GND	
11	Package-GND	GND for package-shield	Connect to GND	
12	Ext_CLK_IN	Reference clock-source input for measurement	Control pin Connect to GND if not used	
13	V <sub>CC</sub>	Analog supply voltage	Connect to power supply	
14	NC		Open	
15	Vstabi.	Stabilizer voltage	Open	2.5V
16	AFC	AFC control bias	Put capacitor between 16 pin and GND Otherwise, open if not used	1.1
17	MPX	MPX-signal output	Open	2.3V
18	LINE-OUT-R	Radio Rch Line-output	Output pin	1V
19	LINE-OUT-L	Radio Lch Line-output	Output pin	1V
20	Package-GND	GND for package-shield	Connect to GND	
21	Package-GND	GND for package-shield	Connect to GND	
22	Package-GND	GND for package-shield	Connect to GND	
23	Package-GND	GND for package-shield	Connect to GND	
24	GND	GND (Analog and Digital GND)	Connect to GND	



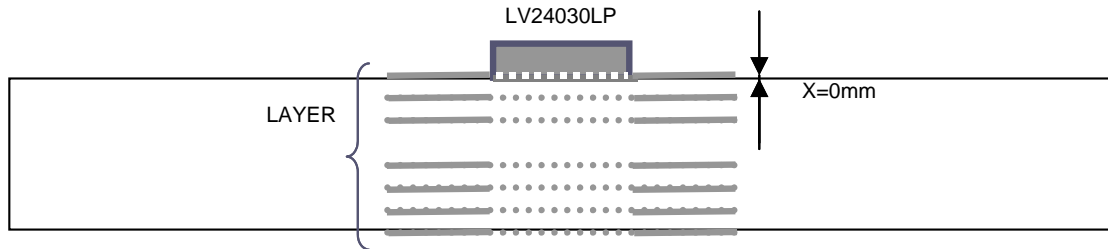
## LV24030LP

### The PCB mounting conditions which cover FM receiving frequency range 76MHz to 108MHz

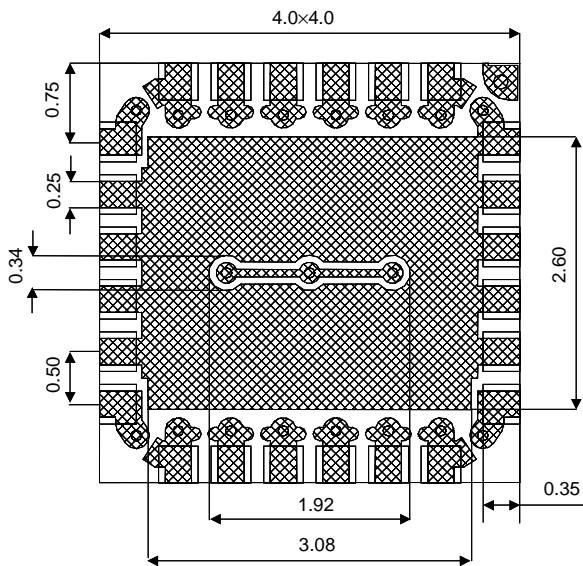
LV24030LP has an inductor for local oscillator on the package bottom side.

In order to cover the receiving frequency range of 76MHz to 108MHz, provide the GND layer to the first layer of Side A of PCB that is directly under the package bottom side, as shown in the figure.

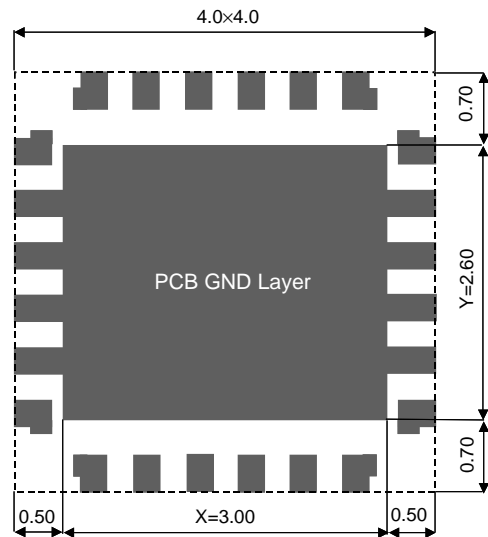
### Printed circuit board



### PCB layout recommendations



IC substrate LV24030LP



Recommended GND layer  
for PCB substrate directly under IC

With this SPL, the receiving frequency is measured under the following conditions:

The X-value can be set freely between Min= $2.4\text{mm}$  and Max= $3.0\text{mm}$  with reference to IC.

(The X-value for SANYO Demo Board is  $2.8\text{mm}$ .)

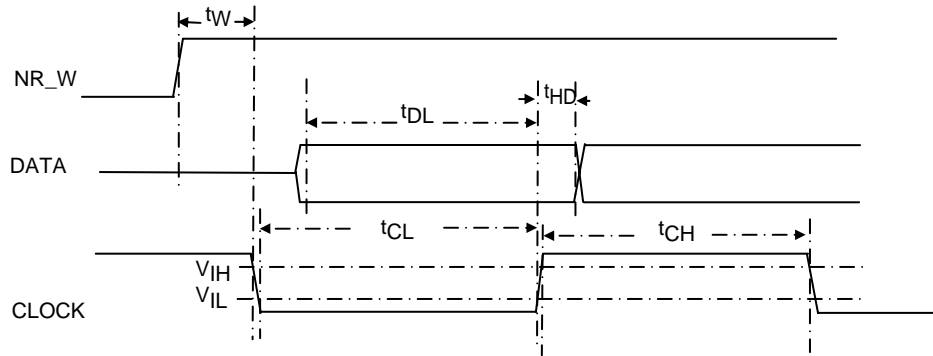
The Y-value can be set freely between Min= $2.0\text{mm}$  and Max= $3.0\text{mm}$  with reference to IC.

(The Y-value for SANYO Demo Board is  $2.6\text{mm}$ .)

Avoid providing another wiring within  $0.4\text{mm}$  of bottom layer of PCB\_GND as much as possible.

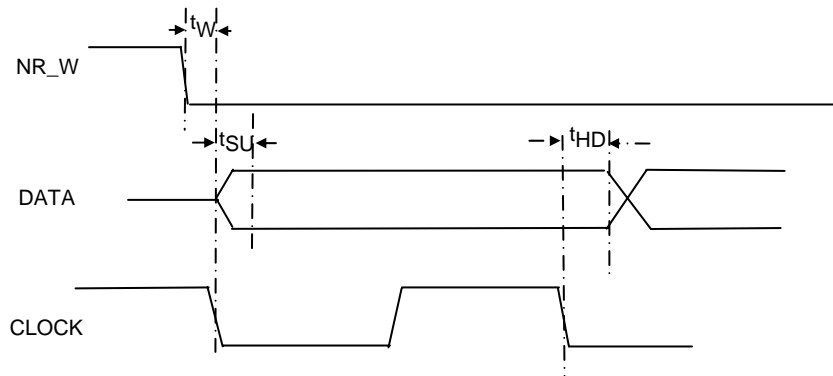
## Serial Data Timing

### • Write timing



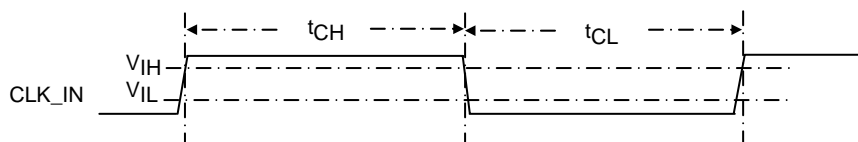
Symbol	Conditions	Ratings			Unit
		min	typ	max	
$t_W$	Delay from command to data	750			ns
$t_{DL}$	Delay from data stable to data latch time	750			ns
$t_{HD}$	Data Hold time	750			ns
$t_{CH}$	Clock High-level time	750			ns
$t_{CL}$	Clock Low-level time	750			ns

### • Read timing



Symbol	Conditions	Ratings			Unit
		min	typ	max	
$t_W$	Delay from command to 1 <sup>st</sup> data bit	350			ns
$t_{SU}$	Data Setup time			350	ns
$t_{HD}$	Data hold time			350	ns

### • External clock timing (Pin 31)



Symbol	Conditions	Ratings			Unit
		min	typ	max	
$t_{CH}$	Clock High-level time	35			ns
$t_{CL}$	Clock Low-level time	35			ns

**Digital Interface Specification (reference)****• 3-wire bus (For communication line)**

Access to the LV24030 is done through the 3-wire bus.

CLOCK	Clock
NR_W	Write/read control
DATA	Data is written into LV24030 when the bidirectional communication line NR_W is H and is read from LV24030 when NR_W is L.

LV24030 has a function to notify occurrence of interruption by means of change in the DATA line.

If interruption is to be made, it is essential that the controller supports interruption by change of the DATA line.

When the timing necessary for frequency measurement cannot be generated from the controller, it is necessary to input the external clock (oscillator or 32kHz crystal) to the CLK\_IN pin of LV24030.

**• Register map**

Address	Register name	Access	Operation
00h	CHIP_ID	R	Chip identification
01h	NA	-	
02h	CNT_L	R	Counter value low byte
03h	FM_OSC	W	DAC control for FM-RF oscillator
04h	AUDIO_CTRL	W	Audio Control
05h	MSRC_SEL	W	Measure source select
06h	CTRL_STAT	R	Control status
07h	RADIO_STAT	R	Radio station status
08h	STEREO_CTRL	W	Stereo Control
09h	FM_CAP	W	FM-RF CAP bank DAC setting
0Ah	PW_SCTRL	W	Power and soft control
0Bh	SD_OSC	W	DAC control for stereo decoder oscillator
0Ch	CNT_CTRL	W	Counter control
0Dh	CNT_STAT	R	Control status
0Eh	IF_OSC	W	DAC control for IF oscillator
0Fh	IF_BW	W	IF Bandwidth
10h	RADIO_CTRL1	W	Radio control 1
11h	CNT_H	R	Counter value high byte

Registers with blank column are not defined and should not be accessed.



# LV24030LP

## Register Description (For each register content)

### Register 00h-CHIP\_ID-Chip Identify Register (Read only)

7	6	5	4	3	2	1	0
ID[7:0]							
Bit 7-0: <b>ID[7:0]</b> : 8-bit chip ID LV24030:02h							

### Register 02h-CNT\_L-Counter Value Low Register (Read-only)

7	6	5	4	3	2	1	0
CNT_LSB[7:0]							
Bit 7-0: <b>CNT_LSB[7:0]</b> : Lower 8-bit value of the 16 bit counter							

### Register 03h-FM\_OSC-FM RF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
FMOSC[7:0]							
Bit 7-0: <b>FMOSC[7:0]</b> : DAC value to control the FM RF oscillator (fine step)							

### Register 04h – AUDIO\_CTRL – Audio Control Register (Write-only)

7	6	5	4	3	2	1	0
Reserved		nVOL1	nVOL0	Reserved	DEEMP	AMUTE_L	SE_FM
Bit 7-6: <b>Reserved</b> : Fixed at 0 Bit 5-4: <b>nVOL[1:0]</b> : Audio output level 11b = Maximum output level 10b = Output level 3 01b = Output level 2 00b = Minimum output level Bit 3: <b>SF5dB</b> 0 = No FS increase by 5dB 1 = FS+5dB Bit 2: <b>DEEMP</b> : De-emphasis bit 0 = De-emphasis 50μs 1 = De-emphasis 70μs Bit 1: <b>AMUTE_L</b> : Audio mute bit 0 = Mute 1 = Mute cancelled Bit 0: <b>SE_FM</b> : FM radio select 0 = FM radio disabled 1 = FM radio enabled							

# LV24030LP

**Register 05h-MSRC\_SEL-Measurement Source Select Register (Write-only)**

7	6	5	4	3	2	1	0
MSR_O	AFC_LVL	DIR_AFC	RST_AFC	MSS_AFCS	MSS_SD	MSS_RF16	MSS_IF
Bit 7	<b>MSR_O:</b> Outputs VCO of IF,SD, and RF frequencies to the data pin (for testing) 0 = No output 1 = Output (for testing)						
Bit 6	<b>AFC_LVL:</b> AFC trigger level 0 = AFC is always active 1 = AFC is only active when field strength is above 20dBμV						
Bit 5	<b>DIR_AFC:</b> AFC operation direction 0 = AFC reverse operation (for testing) 1 = AFC normal operation						
Bit 4	<b>RST_AFC:</b> AFC reset 0 = Normal operation 1 = Resets AFC to the center of control range						
Bit 3	<b>MSS_AFCS:</b> Detects the AFC status by the data line 0 = AFC status read disabled 1 = AFC status read enabled  With this bit set to "1" and with MSR_O = 1, the state outside the AFC control range can be detected from the change of the DATA line.  In case of the state outside the AFC control range, the DATA line changes from L to H.						
Bit 2	<b>MSS_SD:</b> Stereo decoder oscillator measurement 0 = Disable stereo decoder oscillator measurement 1 = Enable stereo decoder oscillator measurement						
Bit 1	<b>MSS_RF16:</b> RF/16 measurement 0 = RF/16 oscillator measurement disabled 1 = RF/16 oscillator measurement enabled						
Bit 0	<b>MSS_IF:</b> IF oscillator measurement 0 = Disable IF oscillator measurement 1 = Enable IF oscillator measurement						
<b>Note:</b> Be sure that only one of MSS_XX bits is enabled.  The FM RF frequency is divided to 1/16 and input into the measuring circuit.							

**Register 06h-CTRL\_STAT-Control Status Register (Read-only)**

7	6	5	4	3	2	1	0
REV3	REV2	REV1	REV0	AFC_UP	AFC_DN	COV_FLG	AFC_FLG
Bit 7-4	REV[3:0]: 0Fh						
Bit 3	AFC_UP: AFC adjustment up-direction 0 = Center value 1 = RF frequency adjusted in the up-direction						
Bit 2	AFC_DN: AFC adjustment down-direction 0 = Center value 1 = RF frequency adjusted in the down-direction						
Bit 1	COV_FLG: Counter overflow flag 0 = No overflow 1 = Counter overflow						
Bit 0	AFC_FLG: AFC out of range bit 0 =AFC is within control range 1 =AFC is out of control range						
Note: COV_FLG is cleared when CLR_CNT1 bit of CNT_CTRL register is set to “1.”							

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**Register 07h – RADIO\_STAT – Radio Station Status Register (Read-only)**

7	6	5	4	3	2	1	0
RSS_MS	RSS_FS						
Bit 7	<b>RSS_MS:</b> mono/stereo determination 0 = mono 1 = stereo						
Bit 6-0	<b>RSS_FS[6:0]:</b> Field Strength bit 1111111b = Field Strength<10dBμV 0111111b = Field Strength 10 to 20dBμV 0011111b = Field Strength 20 to 30dBμV 0001111b = Field Strength 30 to 40dBμV 0000111b = Field Strength 40 to 50dBμV 0000011b = Field Strength 50 to 60dBμV 0000001b = Field Strength>70dBμV						
<b>Note:</b> +5dB for Register 04h bit3 = 1							

**Register 08h-STEREO\_CTRL-Stereo Control Register (Write-only)**

7	6	5	4	3	2	1	0
PICMPS	SD_PM	ST_M	FRCST	IF_PM_L	DCFB_SPD	DCFB_OFF	AGCSP
Bit 7	<b>PICMPS:</b> Pilot compensation 0 = Disable 1 = Enable						
Bit 6	<b>SD_PM:</b> Stereo Decoder PLL Mute 0 = PLL ON (for normal operation) 1 = PLL OFF (for measurement, etc.)						
Bit 5	<b>ST_M:</b> mono/stereo changeover 0 = Stereo 1 = mono						
Bit 4	<b>FRCST:</b> Forced stereo 0 = Normal 1 = Forced stereo (for testing)						
Bit 3	<b>IF_PM_L:</b> IF PLL Mute 0 = PLL OFF (for measurement) 1 = PLL ON (for normal operation)						
Bit 2	<b>DCFB_SPD:</b> DC feedback speed 0 = Normal speed (for normal operation) 1 = High speed (for testing)						
Bit 1	<b>DCFB_OFF:</b> DC Feedback control Fixed at 0						
Bit 0	<b>AGCSP:</b> AGC speed control 0 = Normal speed 1 = High speed						
<b>Note:</b> With this bit ON, rise of the Field strength becomes faster.							

**Register 09h-FM\_CAP-FM RF Capacitor Bank Register (Write-only)**

7	6	5	4	3	2	1	0
FMCAP[7:0]							
Bit 7-0	<b>FMCAP[7:0]:</b> FM RF frequency CAP bank (rough adjustment)						

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**Register 0Ah-PW\_CTRL-Power and Soft Control Register (Write-only)**

7	6	5	4	3	2	1	0
SS_CTRL			SM_CTRL			EXTCLK	PW_RAD
Bit 7-5	<b>SS_CTRL:</b> Soft stereo control 000b = Soft stereo level 3 001b = Soft stereo off 010b = Soft stereo level 1 100b = Soft stereo level 2						
Bit 4-2	<b>SM_CTRL:</b> Soft mute control 000b = Soft mute level 3 001b = Soft mute off 010b = Soft mute level 1 100b = Soft mute level 2						
Bit 1	<b>EXTCLK:</b> External clock type 0 = Crystal 1 = Oscillator						
Bit 0	<b>PW_RAD:</b> Radio power 0 = Radio OFF 1 = Radio ON						

**Register 0Bh-SD\_OSC-Stereo Decoder Oscillator Register (Write-only)**

7	6	5	4	3	2	1	0
SDOSC[7:0]							
Bit 7-0	<b>SDOSC[7:0]:</b> Stereo Decoder oscillator DAC						

**Register 0Ch-CNT\_CTRL-Counters Control Register (Write-only)**

7	6	5	4	3	2	1	0
CNT1_CLR	CTAB2	CTAB1	CTAB0	SWP_CNT_L	CNT_EN	CNT_SEL	CNT_SET
Bit 7	<b>CNT1_CLR:</b> Clears the counter1 0 = Normal mode 1 = Clears the counter1						
Bit 6-4	<b>CTAB[2:0]:</b> Sets the counter2 TAB value 000b Stop after 2 counts 001b Stop after 8 counts 010b Stop after 32 counts 011b Stop after 128 counts 100b Stop after 512 counts 101b Stop after 2048 counts 110b Stop after 8192 counts 111b Stop after 32768 counts						
Bit 3	<b>SWP_CNT:</b> Counter swap control (0 for swap) 0 = Clock source 1 to counter 2, clock source 2 to counter 1 (swapping) 1 = Clock source 1 to counter 1, clock source 2 to counter 2 (no swap)						
Bit 2	<b>CNT_EN:</b> Count start 0 = Count stop 1 = Count start						
Bit 1	<b>CNT_SEL:</b> Counter select 0 = Counter1 used for measurement 1 = Counter2 used for measurement						
Bit 0	<b>CNT_SET:</b> Set counters bit 0 = Normal mode 1 = Set both counter 1 and counter 2 to FFFFh and keep them set						

**Register 0Dh-CNT\_STAT-Counters Status Register (Read-only)**

7	6	5	4	3	2	1	0
Reserved	CNT_RDY	Reserved					
Bit 7	<b>Reserved:</b> 1						
Bit 6	<b>CNT_RDY:</b> Count over flag 0 = Counting 1 = Count over						
<b>Note:</b> CNT_RDY is cleared by setting the CLR_CNT 1 bit of CNT_CTRL register to"1."							
Bit 5-0	Reserved: 0						

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### Register 0Eh-IF\_OSC-IF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
IFOSC[7:0]							
Bit 7-0	IFOSC[7:0]: IF oscillator DAC						

### Register 0Fh-IF\_BW-IF Bandwidth Register (Write-only)

7	6	5	4	3	2	1	0
IFBW[7:0]							
Bit 7-0	IFBW[7:0]: IF band width						

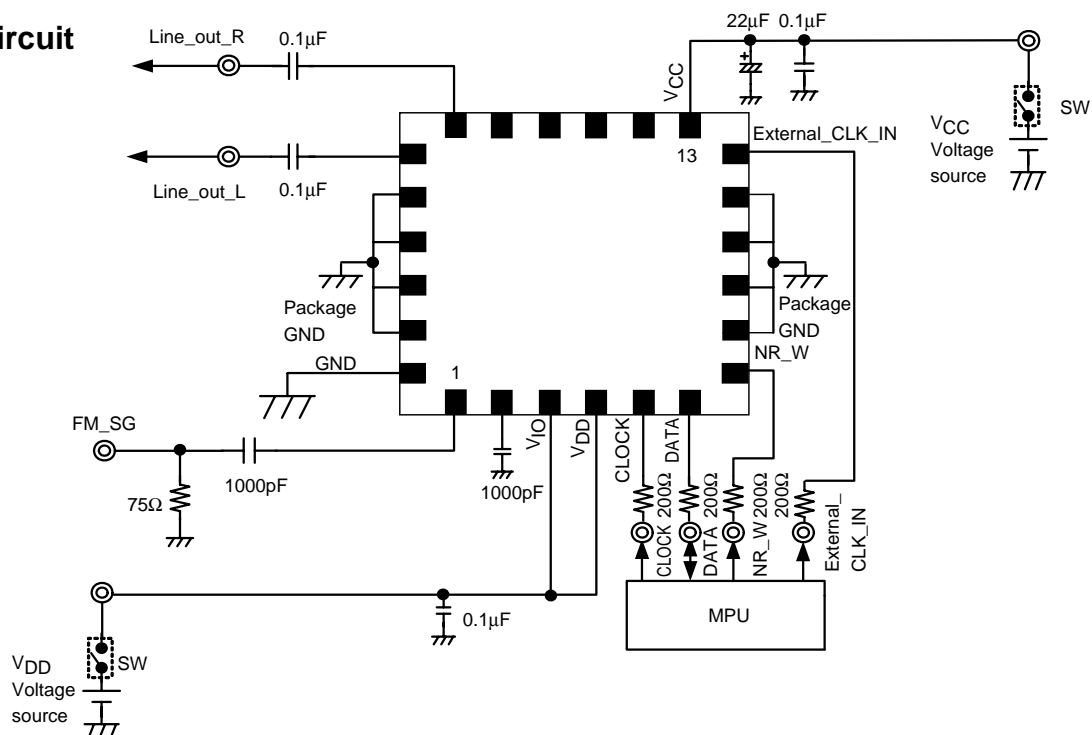
### Register 10h-RADIO\_CTRL1-Radio Control 1 Register (Write-only)

7	6	5	4	3	2	1	0
VREF2	VREF	STABI_BP	EN_MEAS	EN_AFC	AGC_SLVL[1:0]		AFC_SPD
Bit 7	<b>VREF2:</b> VREF2 control bit 0 = VREF2 is ON 1 = VREF2 is OFF						
Bit 6	<b>VREF:</b> VREF control bit 0 = VREF is ON 1 = VREF is OFF						
Bit 5	<b>STABI_BP:</b> Voltage stabilizer (regulator) control 0 = Internal voltage is Vstabi (normal operation) 1 = Internal voltage is V <sub>CC</sub> (stabi bypassed)						
Bit 4	<b>EN_MEAS:</b> Measurement mode 0 = Normal mode 1 = Measurement mode						
Bit 3	<b>EN_AFC:</b> AFC control 0 = AFC OFF 1 = AFC ON						
Bit 2-1	<b>AGC_SLVL[1:0]:</b> AGC set level Default = 0						
Bit 0	<b>AFC_SPD:</b> AFC speed control 0 = AFC speed 3Hz 1 = AFC speed 8kHz (for testing)						

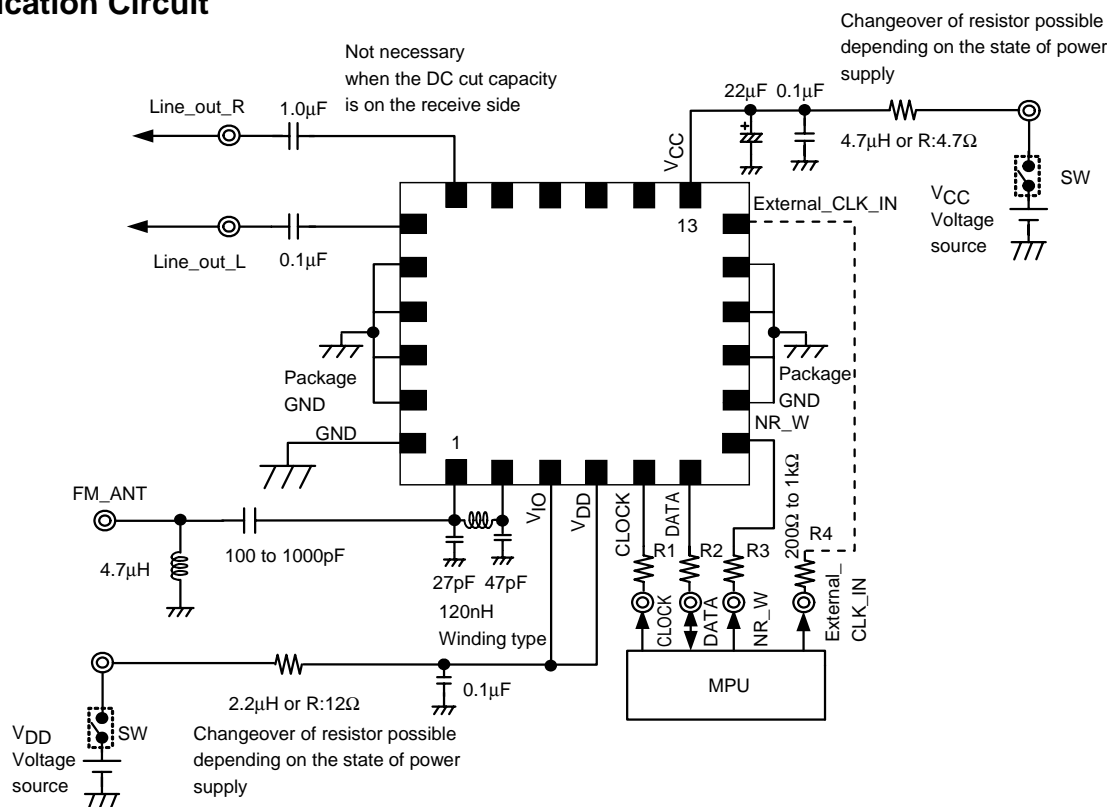
*Register 11h-CNT\_H-Counter Value High Register (Read-only)*

7	6	5	4	3	2	1	0
CNT_MSB[7:0]							
Bit 7-0	CNT_MSB[7:0]: Upper 8-bit value of the 16 bit counter						

## Test Circuit



# Application Circuit



Note1: Vale of Extenal Component is just reference. Please set most sutable value under Acutual\_ operation.

Note2: Please take Consideration of most suitable\_value, as for antenna application

Note3: We recomend to put R1,R2,R3,R4 for interface between MPU and IC.

Note4: Please put Capacitor Between VDD and GND also, put Capacitor Between VCC and GND as shown on application.

Note5: As for AFC pin (16 pin), usually it is recommended not to connect anything. AFC can be operated more smoothly by putting capacitor between 16 pin and GND.

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