3.3V CMOS DUAL J-$\overline{K}$ FLIP-FLOP WITH SET AND RESET, POSITIVE-EDGE TRIGGER, AND 5 VOLT TOLERANT I/O

IDT74LVC109A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.635mm pitch QSOP, 0.65mm pitch SSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of – 40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC109A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

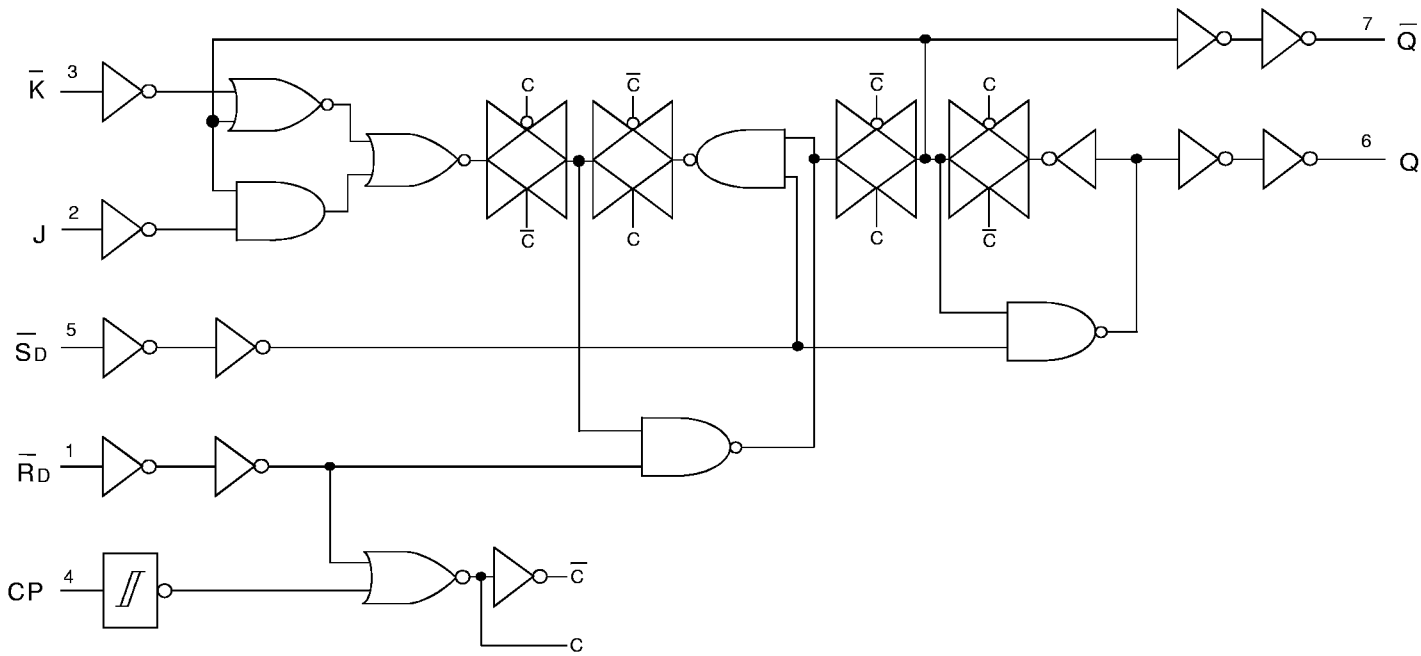
DESCRIPTION:

The LVC109A dual J-$\overline{K}$ flip-flop with set and reset, positive-edge trigger is built using advanced dual metal CMOS technology. This device features individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs. The set and reset are asynchronous active low inputs and operate independently of the clock input. The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the function table. The J and $\overline{K}$ inputs must be stable one setup time prior to the low-to-high clock transition for predictable operation. The J-$\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

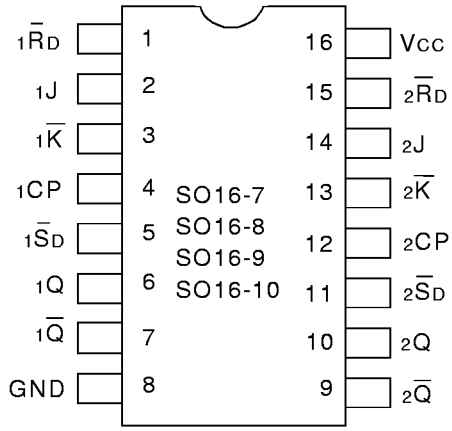
The LVC109A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



NOTE:
Pin numbers are for section 1. Refer to pin configuration for section 2 pin numbers.

PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ TSSOP
TOP VIEW

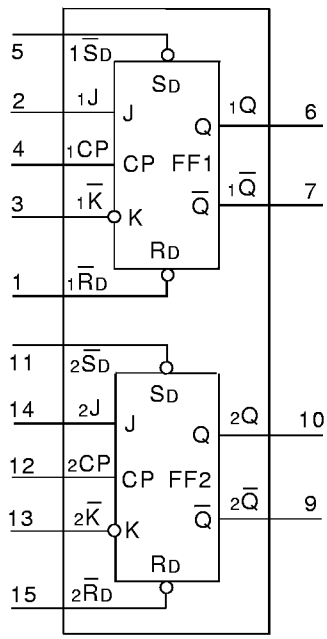
ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	– 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, V_I < 0 or V_O < 0	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

LVC QUAD Link

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

FUNCTIONAL DIAGRAM



CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

LVC QUAD Link

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xCP	Clock Inputs, LOW-to-HIGH, edge-triggered
x$\overline{R}_D$	Asynchronous Reset Input (Active LOW)
x$\overline{S}_D$	Asynchronous Set Inputs (Active LOW)
xJ, x$\overline{K}$	Synchronous Inputs
xQ	True Flip-Flop Outputs
x$\overline{Q}$	Complement Flip-Flop Outputs

FUNCTION TABLE (1)

Inputs						Outputs	
Operating Modes	x$\overline{SD}$	x$\overline{RD}$	xCP	xJ	x$\overline{K}$	xQ	x$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{Q}_0$	Q_0
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	Q_0	$\overline{Q}_0$

NOTE:
1. H = HIGH voltage level
   h = HIGH voltage level of input set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level of input set-up time prior to LOW-to-HIGH CP transition
   X = Don't care
   ↑ = LOW-to-HIGH CP Transition
   Q_0 = Level of Q before the indicated steady-state input conditions were established.
   $\overline{Q}_0$ = Complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: TA = – 40°c to +85°c

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V other inputs at V_{CC} or GND		—	—	500	µA

LVC QUAD Link

NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

LVC QUAD Link

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V±0.2V	Vcc = 3.3V±0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance per flip-flop	C_L = 0pF, f = 10Mhz	—	—	pF

SWITCHING CHARACTERISTICS [1]

Symbol	Parameter	Vcc = 2.5V±0.2V		Vcc = 2.7V		Vcc = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCP to xQ or x$\overline{Q}$	—	9	—	8.5	—	7.5	ns
t_{PLH}	Propagation Delay x$\overline{S}_D$ to xQ or x$\overline{R}_D$ to $\overline{Q}$	—	11	—	9	—	8	ns
t_{PHL}	Propagation Delay x$\overline{S}_D$ to xQ or x$\overline{R}_D$ to $\overline{Q}$	—	10	—	10	—	9	ns
t_{SU}	Set-up Time, xJ, x$\overline{K}$ to xCP	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time, xJ, x$\overline{K}$ to xCP	2	—	2	—	2	—	ns
t_{REM}	Removal Time, x$\overline{S}_D$, x$\overline{R}_D$ to xCP	3	—	3	—	3	—	ns
t_W	Pulse Width CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t_W	Set or Reset Pulse Width, HIGH or LOW	3	—	3	—	3	—	ns
$t_{SK(0)}$	Output Skew[2]	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

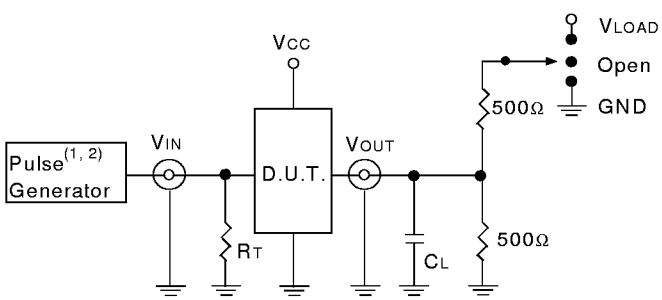
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 2.5V ±0.2V	$V_{CC}^{(2)}$= 3.3V ±0.3V & 2.7V	Unit
V_{LOAD}	2 x Vcc	6	V
V_{IH}	Vcc	2.7	V
V_T	Vcc / 2	1.5	V
V_{LZ}	150	300	mV
V_{HZ}	150	300	mV
C_L	30	50	pF

LVC QUAD Link

TEST CIRCUITS FOR ALL OUTPUTS



LVC QUAD Link

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

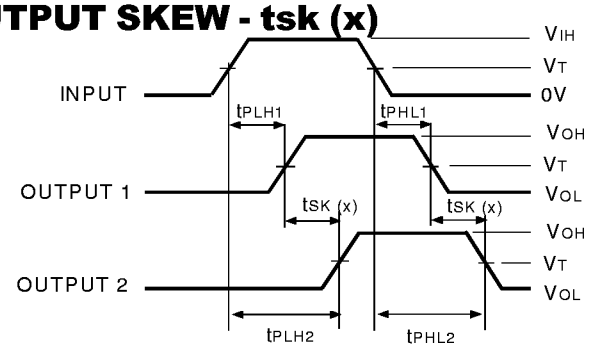
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

LVC QUAD Link

OUTPUT SKEW - tsk (x)



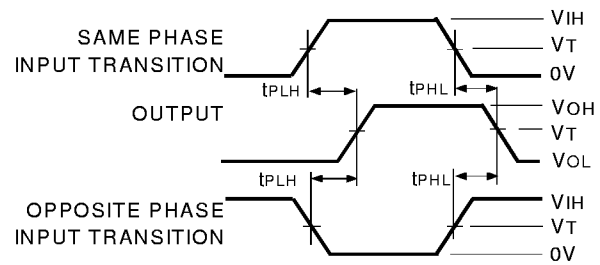
$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

LVC QUAD Link

NOTES:

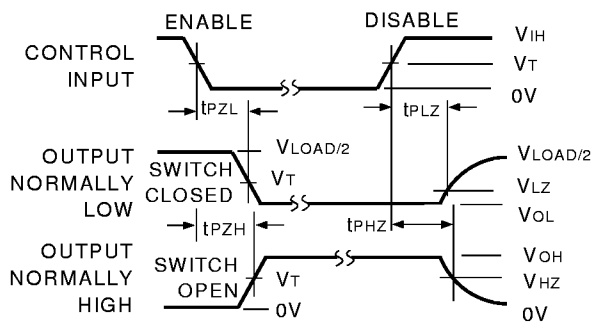
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



LVC QUAD Link

ENABLE AND DISABLE TIMES

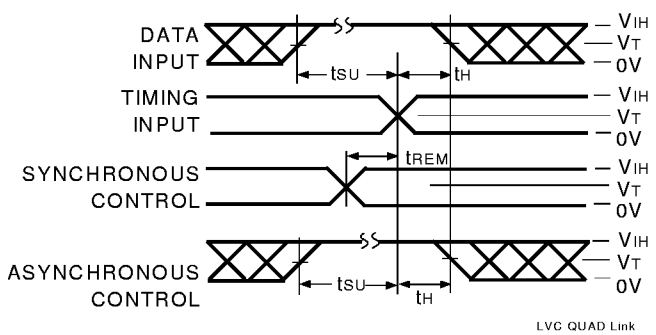


LVC QUAD Link

NOTE:

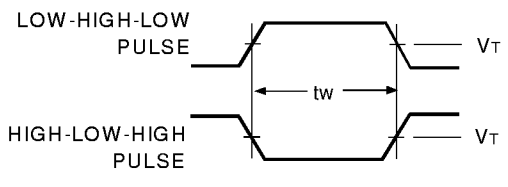
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



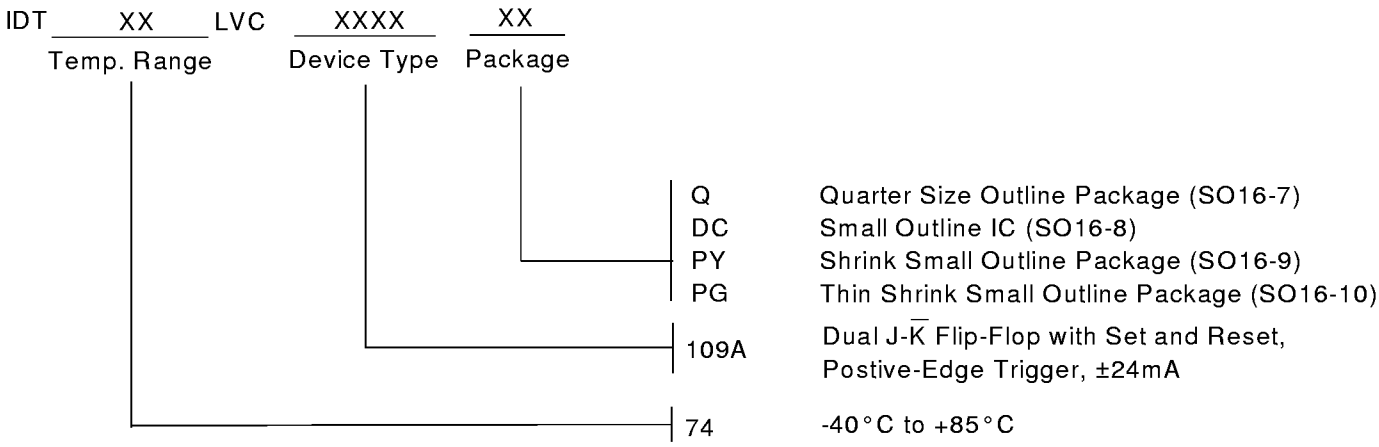
LVC QUAD Link

PULSE WIDTH



LVC QUAD Link

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.