

# NIS5431 Series

## +3.3 Volt Electronic Fuse

The NIS5431 series is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It also includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue operation.

### Features

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- 40 m $\Omega$  Typical
- Internal Charge Pump
- Internal Undervoltage Lockout Circuit
- Internal Overvoltage Clamp
- ESD Ratings: Human Body Model (HBM); 2000 V  
Machine Model (MM); 200 V
- These are Pb-Free Devices and are RoHS Compliant

### Typical Applications

- Mother Board
- Hard Drives
- Fan Drives



**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

## 4.5 AMP, 3.3 VOLT ELECTRONIC FUSE



**WDFN10  
CASE 522AA**

### MARKING DIAGRAM

Pin	Function
1-5	SOURCE
6	I <sub>LIMIT+</sub>
7	I <sub>LIMIT-</sub>
8	Enable/Fault
9	dv/dt
10	GND
11 (flag)	VCC

31 = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Features	Package	Shipping†
NIS5431MT1TXG	Thermal Latching	WDFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## NIS5431 Series

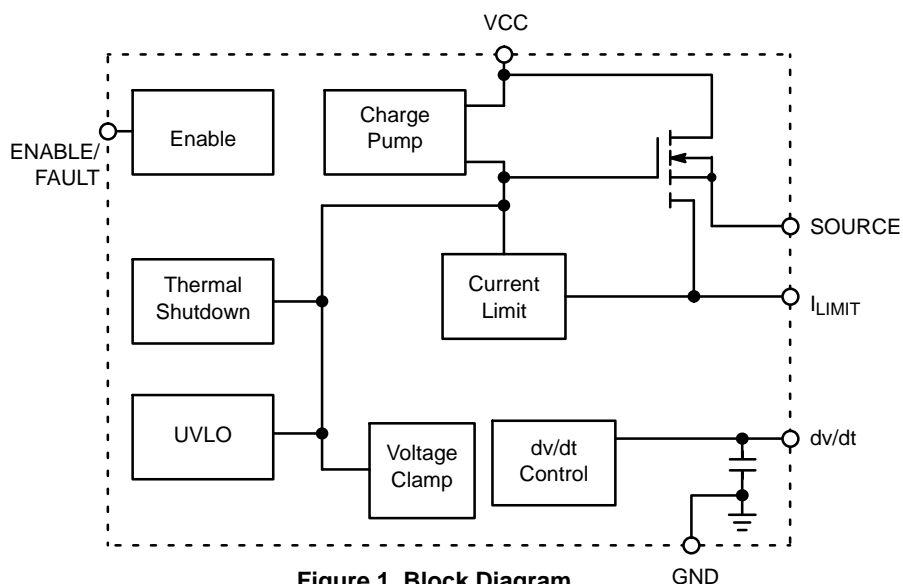


Figure 1. Block Diagram

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
1–5	Source	This pin is the source of the internal power FET and the output terminal of the fuse.
7	$I_{LIMIT}$	A resistor between this pin and the source pin sets the overload and short circuit current limit levels.
8	Enable/Fault	The enable/fault pin is a tri-state, bidirectional interface. It can be used to enable or disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 1.4 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
10	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
11 (belly pad)	$V_{CC}$	Positive input voltage to the device.

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady-state ( $V_{CC}$ to GND, Note 1)	$V_{IN}$	–0.6 to 14	V
Thermal Resistance, Junction-to-Air 0.1 in <sup>2</sup> copper (Note 2) 0.5 in <sup>2</sup> copper (Note 2)	$\theta_{JA}$	227 95	°C/W
Thermal Resistance, Junction-to-Lead (Pin 1)	$\theta_{JL}$	27	°C/W
Thermal Resistance, Junction-to-Case	$\theta_{JC}$	20	°C/W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_{max}$	1.3 10.4	W mW/°C
Operating Temperature Range (Note 3)	$T_J$	–40 to 150	°C
Nonoperating Temperature Range	$T_J$	–55 to 155	°C
Lead Temperature, Soldering (10 Sec)	$T_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the device.
2. 1 oz copper, double-sided FR4.
3. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than the maximum ratings for extended periods of time.

## NIS5431 Series

### ELECTRICAL CHARACTERISTICS

(Unless otherwise noted:  $V_{CC} = 3.3\text{ V}$ ,  $C_{IN} = 2.2\text{ }\mu\text{F}$ ,  $C_L = 70\text{ }\mu\text{F}$ ,  $dv/dt$  pin open,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

#### POWER FET

Delay Time (enabling of chip to $I_D = 100\text{ mA}$ with $1\text{ A}$ resistive load)	$T_{dly}$	10	200	475	$\mu\text{s}$
ON Resistance (Note 4) $T_J = 140^\circ\text{C}$ (Note 5)	$R_{DS(on)}$	35	45 65	55	$\text{m}\Omega$
Off State Output Voltage ( $V_{CC} = 10\text{ V}_{dc}$ , $V_{GS} = 0\text{ V}_{dc}$ , $R_L = 100\text{ k}\Omega$ )	$V_{off}$		50	200	mV
Output Capacitance ( $V_{DS} = 3.3\text{ V}_{DC}$ , $V_{GS} = 0\text{ V}_{DC}$ , $R_L = \infty$ )	$C_{out}$		230		pF
Continuous Current ( $T_A = 25^\circ\text{C}$ , $0.5\text{ in}^2$ pad) (Note 5) ( $T_A = 80^\circ\text{C}$ , minimum copper)	$I_D$ $I_D$		4.5 1.7		A

#### THERMAL LATCH

Shutdown Temperature (Note 5)	$T_{SD}$	150	175	200	$^\circ\text{C}$
Thermal Hysteresis (Decrease in die temperature for turn on, does not apply to latching parts)	$T_{Hyst}$		45		$^\circ\text{C}$

#### UNDER/OVERVOLTAGE PROTECTION

$V_{OUT}$ Maximum ( $V_{CC} = 10\text{ V}$ )	$V_{out-clamp}$	3.6	3.85	4.10	V
Undervoltage Lockout (Turn on, Voltage Going High)	$V_{UVLO}$	1.91	2.35	2.5	V
UVLO Hysteresis	$V_{Hyst}$	0.055	0.10	0.25	V

#### CURRENT LIMIT

Hold Current Limit (Note 6) ( $R_{LIMIT} = 10\text{ }\Omega$ )	$I_{HOLD}$		2.2		A
Trip Current Limit (Note 6) ( $R_{LIMIT} = 10\text{ }\Omega$ )	$I_{TRIP}$		3.1		A

#### dv/dt CIRCUIT

Output Voltage Ramp Time (Enable to $V_{OUT} = 3.0\text{ V}$ )	$t_{slew}$	0.30	0.60	1.2	ms
Maximum Capacitor Voltage	$V_{max}$			$V_{CC}$	V

#### ENABLE/FAULT

Logic Level Low (Output Disabled)	$V_{in-low}$	0.35		0.81	V
Logic Level Mid (Thermal Fault, Output Disabled)	$V_{in-mid}$	0.82	1.4	1.95	V
Logic Level High (Output Enabled)	$V_{in-high}$	1.96	2.2	3.5	V
High State Maximum Voltage	$V_{in-max}$	2.51	3.3	5.2	V
Logic Low Sink Current ( $V_{enable} = 0\text{ V}$ )	$I_{in-low}$		-12	-20	$\mu\text{A}$
Logic High Leakage Current for External Switch ( $V_{enable} = 3.3\text{ V}$ )	$I_{in-leak}$			1.0	$\mu\text{A}$
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	Fan			3.0	Units

#### TOTAL DEVICE

Bias Current (Operational)	$I_{Bias}$		400	750	$\mu\text{A}$
Bias Current (Shutdown)	$I_{Bias}$		80		$\mu\text{A}$
Minimum Operating Voltage (Notes 5 and 7)	$V_{min}$			2.5	V

4. Pulse test: Pulse width  $300\text{ }\mu\text{s}$ , duty cycle 2%.

5. Verified by design.

6. Refer to explanation of short circuit and overload conditions in application note AND8140/D.

7. Device will shut down prior to reaching this level based on actual UVLO trip point.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## NIS5431 Series

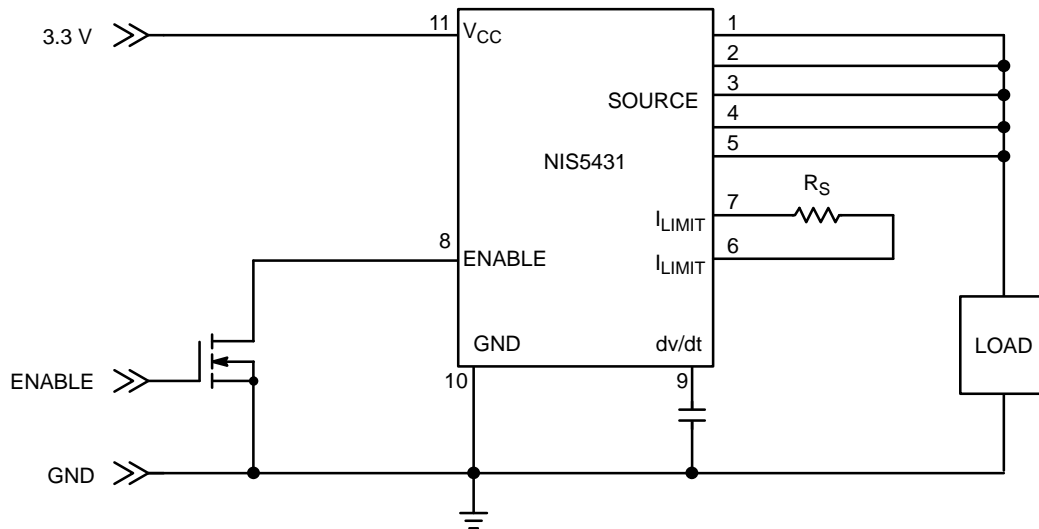


Figure 2. Typical Application Circuit

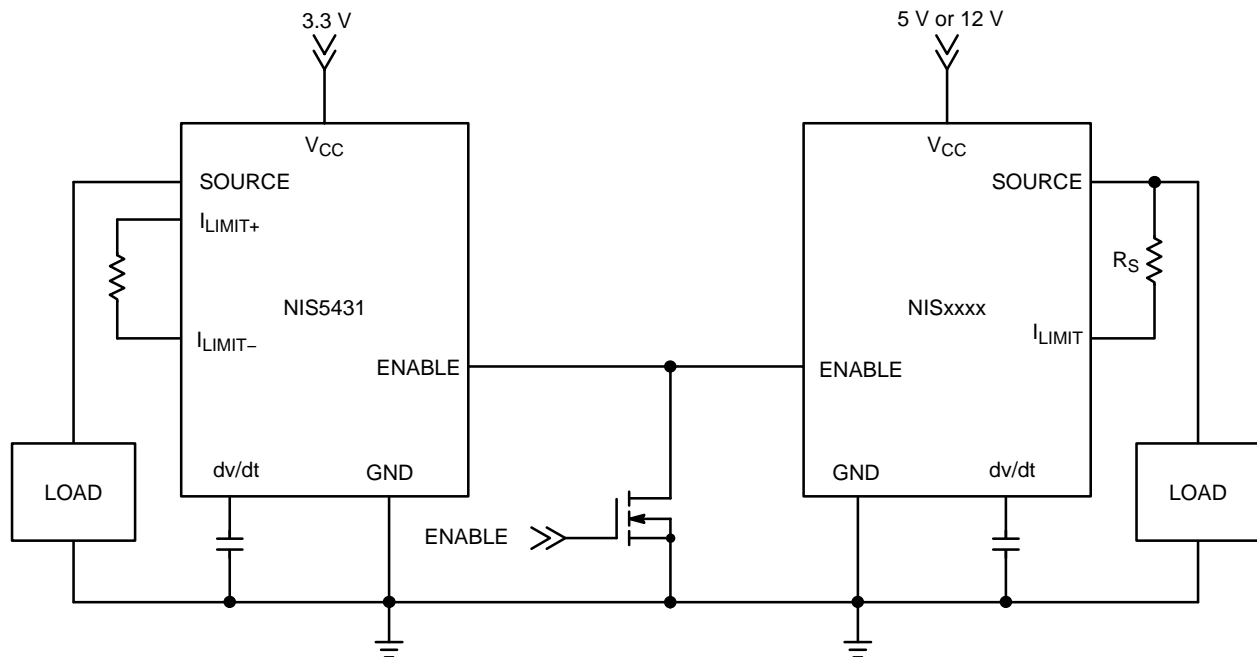


Figure 3. Common Thermal Shutdown

## APPLICATION INFORMATION

### Basic Operation

This device is a self-protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The  $dv/dt$  of the output voltage will be controlled by the internal  $dv/dt$  circuit. The output voltage will slew from 0 V to the rated output voltage in 0.6 ms, unless additional capacitance is added to the  $dv/dt$  pin.

The device will remain on as long as the temperature does not exceed the  $175^{\circ}\text{C}$  limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage to the  $V_{\text{out-clamp}}$  value in the event that the input exceeds that level.

An internal charge pump provides bias for the gate voltage of the internal n-channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage ( $V_{\text{CC}}$ ) and ground.

### Current Limit

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor as well as increasing the value and decreasing the power rating of the sense resistor. Sense resistors are typically in the tens of ohms range with power ratings of several milliwatts making them very inexpensive chip resistors.

The current limit circuit has two limiting values, one for overload events which are defined as the mode of operation in which the gate is high and the FET is fully enhanced. The short circuit mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level. For a more detailed description of this circuit please refer to application note AND8140.

### Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the specified Vout maximum for the device, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

### Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

### dv/dt Circuit

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 0.6 ms. This can be modified by adding an external capacitor at the dv/dt pin. This pin includes an internal current source of approximately 1  $\mu$ A. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

The ramp time from 0 to the nominal output voltage can be determined by the following equation, where  $t$  is in seconds:

$$t_{0-3} = 8.25 \text{ E5} \cdot C_{\text{ext}}$$

Where:

C is in Farads

t is in Seconds

Any time that the unit shuts down due to a fault, enable shut-down, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on.

### Enable/Fault

The Enable/Fault Pin is a multi-function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned-on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit.

To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri-state operation, it should not be connected to any type of logic with an internal pullup device.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family (NIS5232 or NIS5450), a thermal shutdown of one device will cause both devices to disable their outputs.

The outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled.

### Thermal Protection

The NIS5431 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin. Power will automatically be reapplied to the load for auto-retry devices once the die temperature has been reduced by 45°C.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C for extended periods of time.

# NIS5431 Series

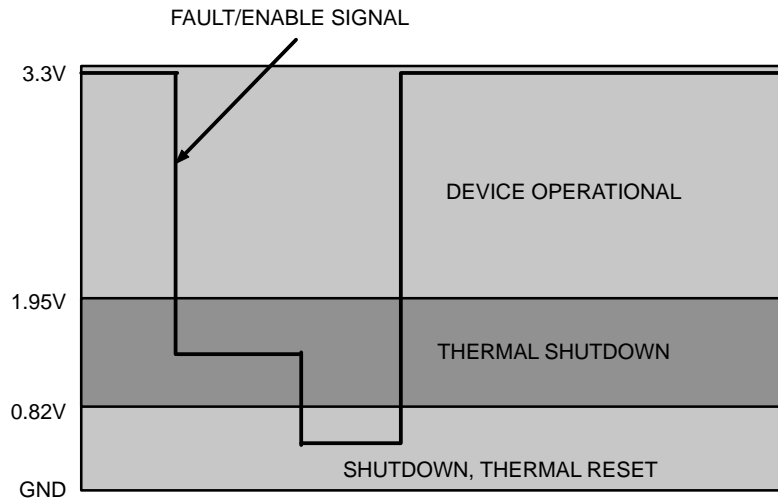


Figure 4. Enable/Fault Signal Levels

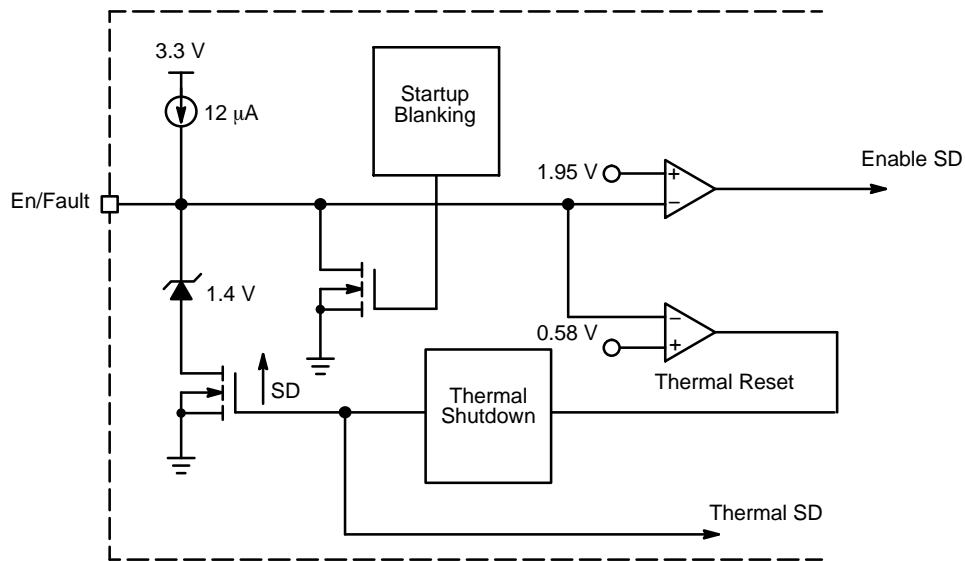


Figure 5. Enable/Fault Simplified Circuit

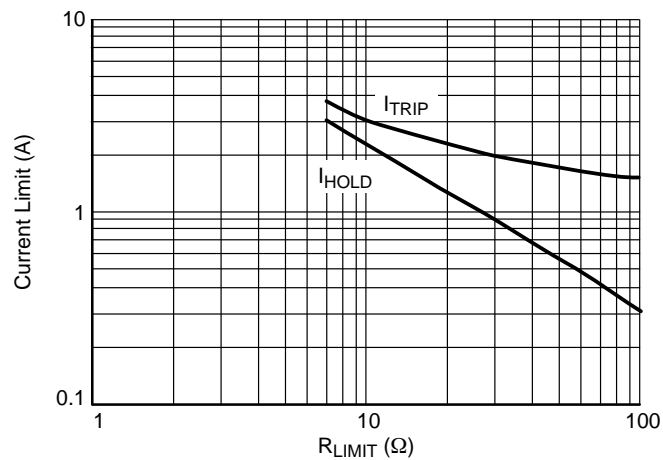
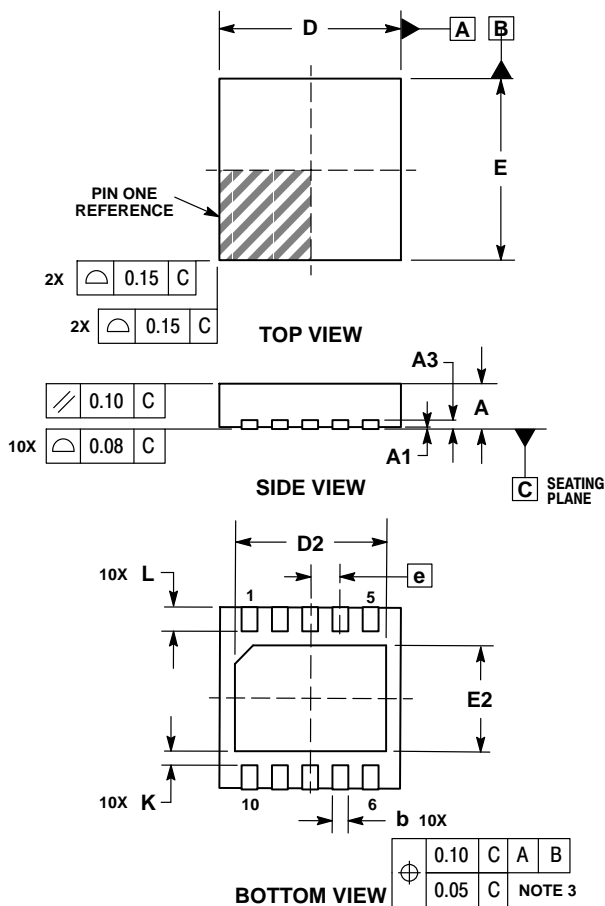


Figure 6. Current Limit vs.  $R_{SENSE}$

# NIS5431 Series

## PACKAGE DIMENSIONS

WDFN10, 3x3, 0.5P  
CASE 522AA  
ISSUE A

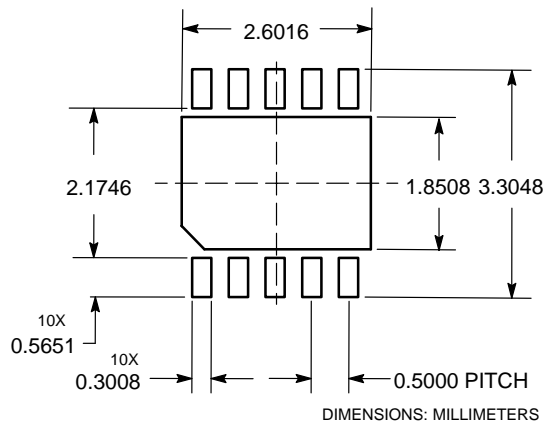


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	2.45	2.50	2.55
E	3.00 BSC		
E2	1.75	1.80	1.85
e	0.50 BSC		
K	0.19 TYP		
L	0.35	0.40	0.45

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5817-1050

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative