

PART NUMBER**54ALS113AJB-ROCV****Rochester Electronics****Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

54ALS113A

Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset (PRE) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A and are characterized for operation over the full military temperature range of -55°C to 125°C.

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FOR REFERENCE ONLY

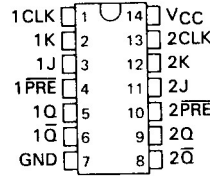
TYPES SN54ALS113A, SN54AS113, SN74ALS113A, SN74AS113 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2661, APRIL 1982—REVISED DECEMBER 1983

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
ALS113A	40 MHz ($C_L = 15$ pF)	6 mW
AS113	175 MHz ($C_L = 50$ pF)	95 mW

SN54ALS113A, SN54AS113 . . . J PACKAGE
SN74ALS113A, SN74AS113 . . . N PACKAGE
(TOP VIEW)

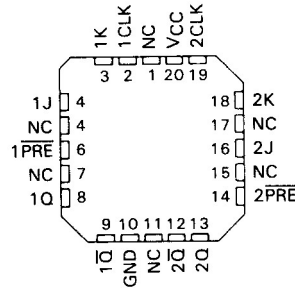


description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset (PRE) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A and SN54AS113 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS113A and SN74AS113 are characterized for operation from 0°C to 70°C .

SN54ALS113A, SN54AS113 . . . FH PACKAGE
SN74ALS113A, SN74AS113 . . . FN PACKAGE
(TOP VIEW)

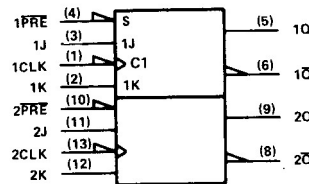


NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLK	J	K	Q	Q-bar
L	X	X	X	H	L
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	\bar{Q}_0

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS113A, SN54AS113	-55°C to 125°C
SN74ALS113A, SN74AS113	0°C to 70°C
Storage temperature range	-65°C to 150°C

TYPES SN54ALS113A, SN74ALS113A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

		SN54ALS113A			SN74ALS113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0	25		0	30		MHz
t _w	Pulse duration	PRE low	15		10			ns
		CLK high	20		16.5			
		CLK low	20		16.5			
t _{su}	Setup time before CLK↓	Data	25		22			ns
		PRE inactive	22		20			
t _h	Hold time, data after CLK↓		0		0			ns
T _A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS113A			SN74ALS113A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA				-1.5			-1.5	V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V _{CC} - 2			V
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4		V
		V _{CC} = 4.5 V, I _{OL} = 8 mA					0.35	0.5		V
I _I	J, K, or CLK	V _{CC} = 5.5 V, V _I = 7 V			0.1			0.1		mA
	PRE				0.2			0.2		
I _{IH}	J, K, or CLK	V _{CC} = 5.5 V, V _I = 2.7 V			20			20		μA
	PRE				40			40		
I _{IL}	J, K, or CLK	V _{CC} = 5.5 V, V _I = 0.4 V			-0.2			-0.2		mA
	PRE				-0.4			-0.4		
I _O †		V _{CC} = 5.5 V, V _O = 2.25 V		-30	-112		-30	-112		mA
I _{CC}		V _{CC} = 5.5 V, See Note 1		2.5	4.5		2.5	4.5		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

†The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54ALS113A		SN74ALS113A		
			MIN	MAX	MIN	MAX	
f _{max}			25		30		MHz
t _{PLH}	PRE	Q or \overline{Q}	3	17	3	14	ns
t _{PHL}			4	20	4	16	
t _{PLH}	CLK	Q or \overline{Q}	3	18	3	15	ns
t _{PHL}			5	23	5	19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54AS113, SN74AS113
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

SN54AS113	SN74AS113
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