

## PART NUMBER

### 54191JB-ROCV

#### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level

#### Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

**SN54190, SN54191, SN54LS190, SN54LS191****SN74190, SN74191, SN74LS190, SN74LS191*****Synchronous Up/Down Counters with Down/Up Mode Control***

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

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SN54190, SN54191, SN54LS190, SN54LS191,  
 SN74190, SN74191, SN74LS190, SN74LS191  
**SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**  
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- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

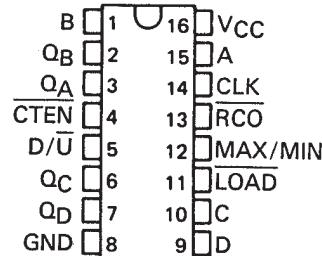
| TYPE           | TYPICAL                   |                         |                           |
|----------------|---------------------------|-------------------------|---------------------------|
|                | AVERAGE PROPAGATION DELAY | MAXIMUM CLOCK FREQUENCY | TYPICAL POWER DISSIPATION |
| '190, '191     | 20ns                      | 25MHz                   | 325mW                     |
| 'LS190, 'LS191 | 20ns                      | 25MHz                   | 100mW                     |

#### description

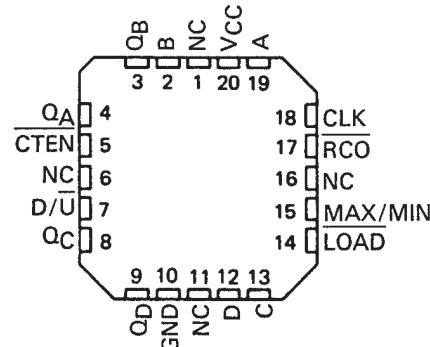
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SN54190, SN54191, SN54LS190,  
 SN54LS191 . . . J PACKAGE  
 SN74190, SN74191 . . . N PACKAGE  
 SN74LS190, SN74LS191 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS190, SN54LS191 . . . FK PACKAGE  
 (TOP VIEW)



NC - No internal connection

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; Series 74' and 74LS' are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

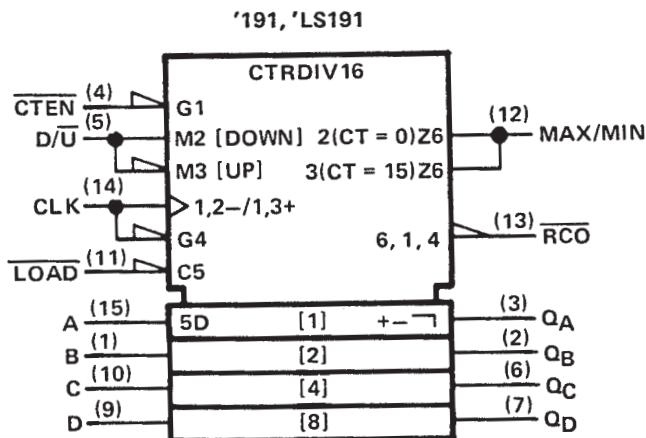
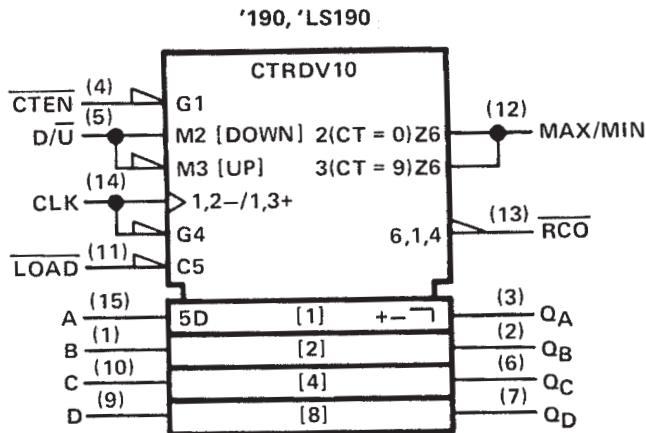
SN54190, SN54191, SN54LS190, SN54LS191,

SN74190, SN74191, SN74LS190, SN74LS191

## SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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### logic symbols†



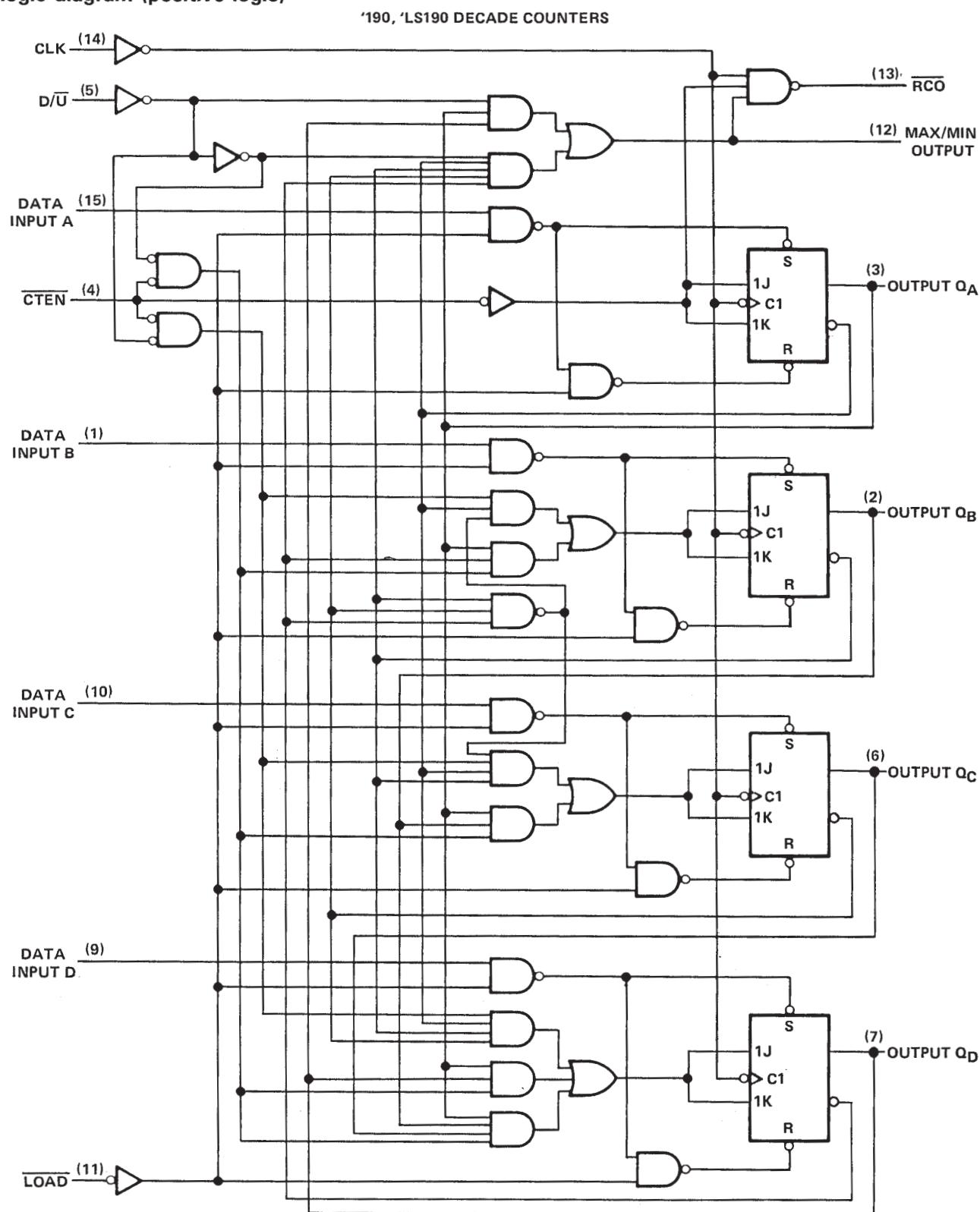
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

**SN54190, SN54LS190, SN74190, SN74LS190**  
**SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

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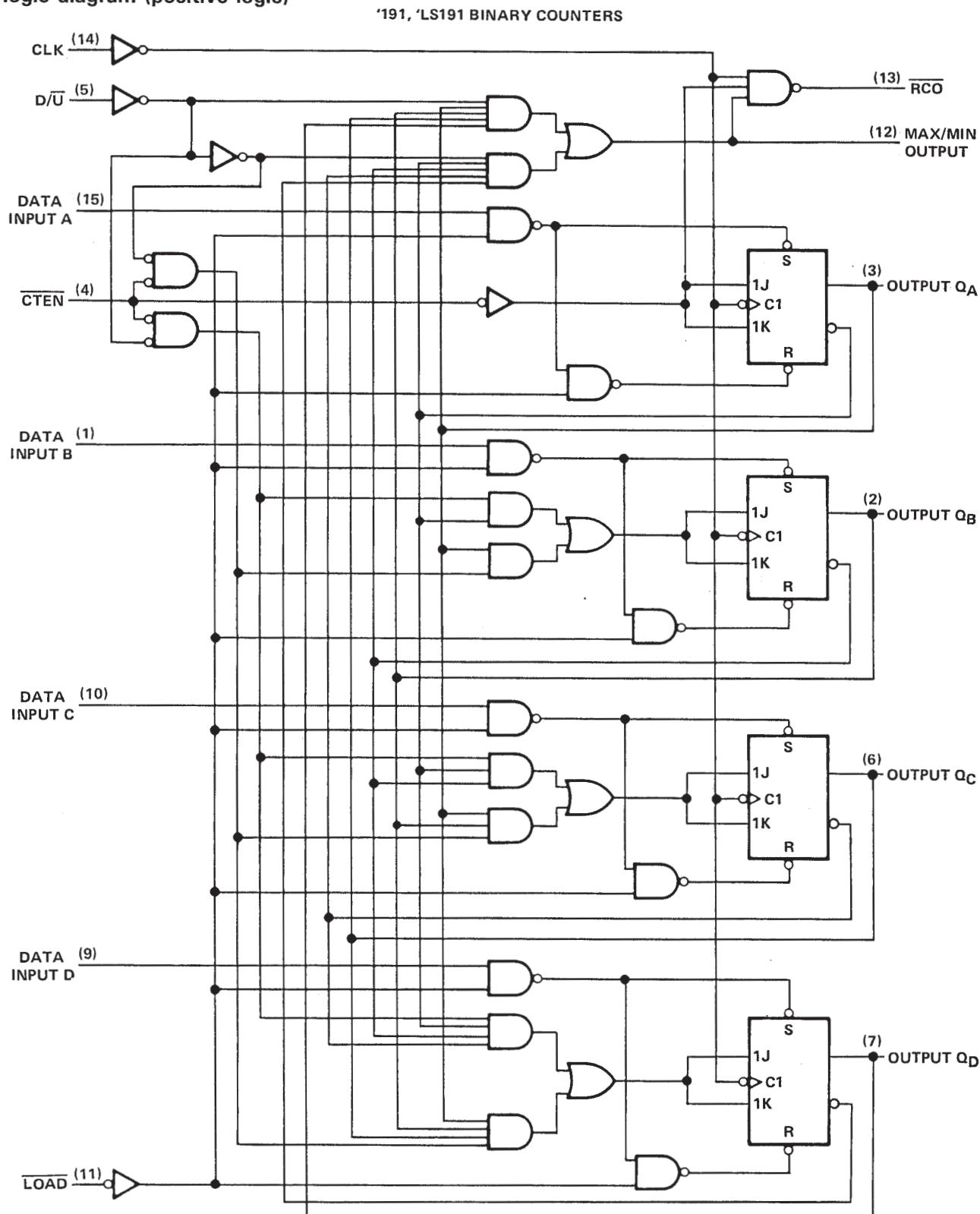
logic diagram (positive logic)



**SN54191, SN54LS191, SN74191, SN74LS191**  
**SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

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**logic diagram (positive logic)**



 **TEXAS  
INSTRUMENTS**

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SN54190, SN54LS190, SN74190, SN74LS190  
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

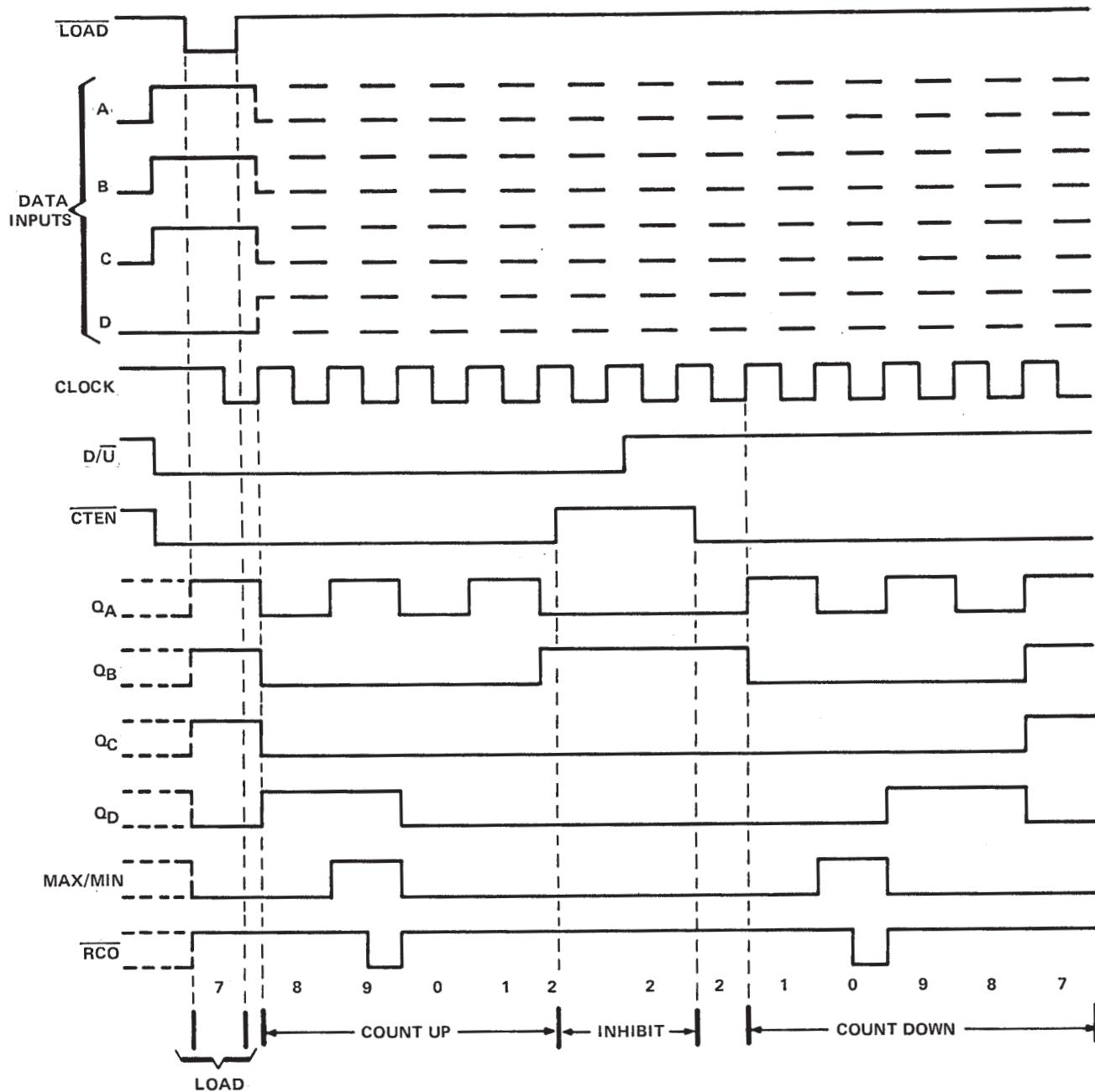
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'190, 'LS190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



# SN54191, SN54LS191, SN74191, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

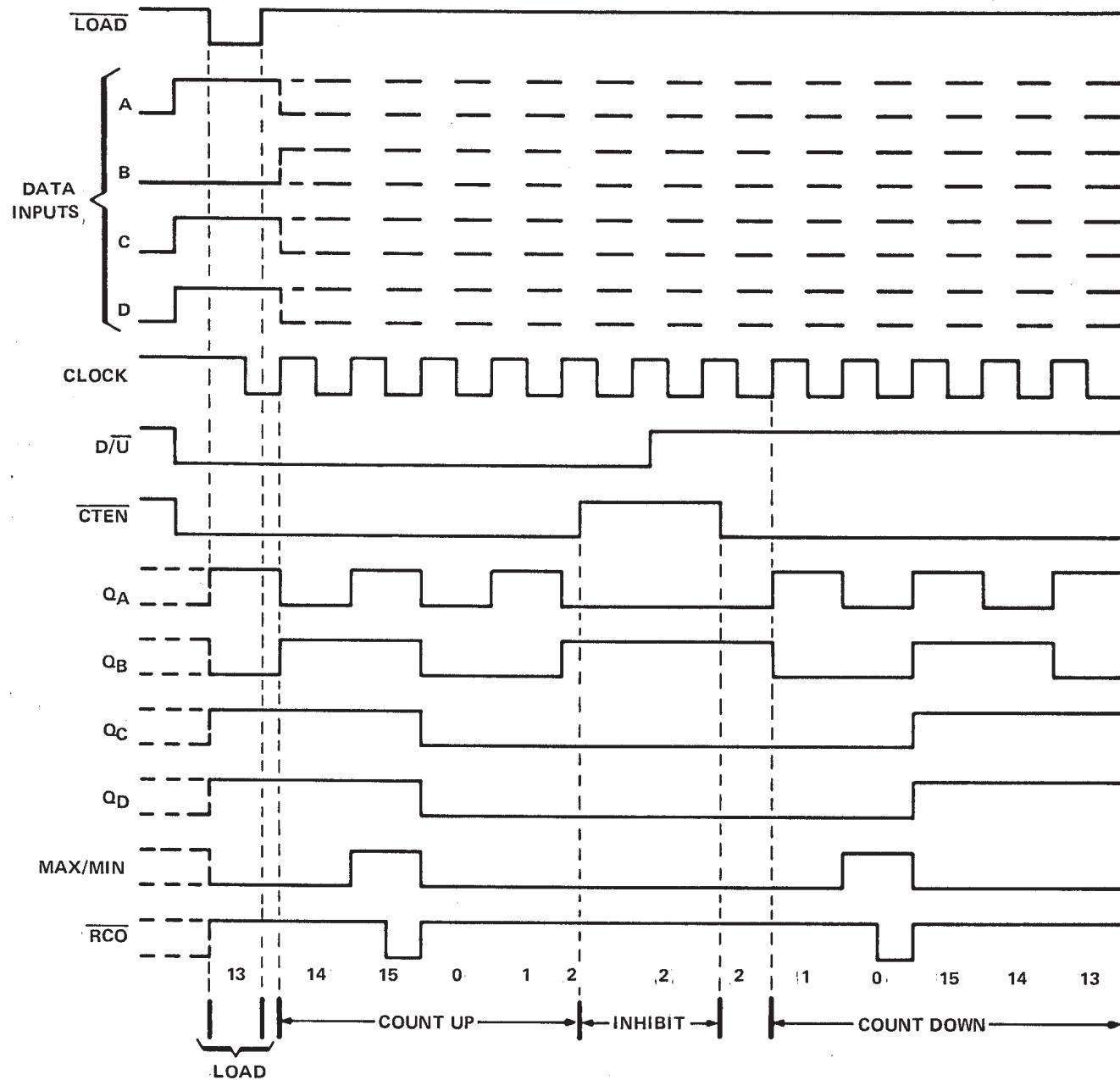
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## '191, 'LS191 BINARY COUNTERS

Typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



SN54190, SN54191, SN54LS190, SN54LS191,  
SN74190, SN74191, SN74LS190, SN74LS191  
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1) . . . . .                         | 7 V            |
| Input voltage: SN54', SN74' Circuits . . . . .                          | 5.5 V          |
| SN54LS', SN74LS' Circuits . . . . .                                     | 7 V            |
| Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . | -55°C to 125°C |
| SN74', SN74LS' Circuits . . . . .                                       | 0°C to 70°C    |
| Storage temperature range . . . . .                                     | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

|                |                                | SN54190, SN54191 |     |      | SN74190, SN74191 |     |      | UNIT |
|----------------|--------------------------------|------------------|-----|------|------------------|-----|------|------|
|                |                                | MIN              | NOM | MAX  | MIN              | NOM | MAX  |      |
| $V_{CC}$       | Supply voltage                 | 4.5              | 5   | 5.5  | 4.75             | 5   | 5.25 | V    |
| $I_{OH}$       | High-level output current      |                  |     | -0.8 |                  |     | -0.8 | mA   |
| $I_{OL}$       | Low-level output current       |                  |     | 16   |                  |     | 16   | mA   |
| $f_{clock}$    | Input clock frequency          | 0                |     | 20   | 0                |     | 20   | MHz  |
| $t_{w(clock)}$ | Width of clock input pulse     | 25               |     |      | 25               |     |      | ns   |
| $t_{w(load)}$  | Width of load input pulse      | 35               |     |      | 35               |     |      | ns   |
| $t_{su}$       | Setup time                     | 20               |     |      | 20               |     |      | ns   |
|                | Load inactive state            | 20               |     |      | 20               |     |      |      |
| $t_{hold}$     | Data hold time                 | 0                |     |      | 0                |     |      | ns   |
| $T_A$          | Operating free-air temperature | -55              |     | 125  | 0                |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS <sup>†</sup>                        | SN54190, SN54191  |                  | SN74190, SN74191 |      | UNIT             |      |               |
|-----------|---|---|------------------|------------------|------|------------------|------|---------------|
|           |   | MIN   | TYP <sup>‡</sup> | MAX              | MIN  | TYP <sup>‡</sup> | MAX  |               |
| $V_{IH}$  | High-level input voltage                            | $V_{CC} = \text{MIN}$   |                  | 2                |      | 2                |      | V             |
| $V_{IL}$  | Low-level input voltage                             | $V_{CC} = \text{MIN}$   |                  |                  | 0.8  |                  | 0.8  | V             |
| $V_{IK}$  | Input clamp voltage                                 | $V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$  |                  |                  | -1.5 |                  | -1.5 | V             |
| $V_{OH}$  | High-level output voltage                           | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -0.8 \text{ mA}$ | 2.4              | 3.4              |      | 2.4              | 3.4  | V             |
| $V_{OL}$  | Low-level output voltage                            | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 16 \text{ mA}$   | 0.2              | 0.4              |      | 0.2              | 0.4  | V             |
| $I_I$     | High-level input current at maximum input voltage   | $V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$   |                  |                  | 1    |                  | 1    | mA            |
| $I_{IH}$  | High-level input current at any input except enable | $V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$   |                  |                  | 40   |                  | 40   | $\mu\text{A}$ |
| $I_{IH}$  | High-level input current at enable input            |   |                  |                  | 120  |                  | 120  | $\mu\text{A}$ |
| $I_{IL}$  | Low-level input current at any input except enable  | $V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$   |                  |                  | -1.6 |                  | -1.6 | mA            |
| $I_{IL}$  | Low-level input current at enable input             |   |                  |                  | -4.8 |                  | -4.8 | mA            |
| $I_{OS}$  | Short-circuit output current <sup>§</sup>           | $V_{CC} = \text{MAX}$   | -20              | -65              | -18  | -65              |      | mA            |
| $I_{CC}$  | Supply current                                      | $V_{CC} = \text{MAX}$ , See Note 2  | 65               | 99               | 65   | 105              |      | mA            |

<sup>†</sup>For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with all inputs grounded and all outputs open.



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# SN54190, SN54191, SN74190, SN74191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

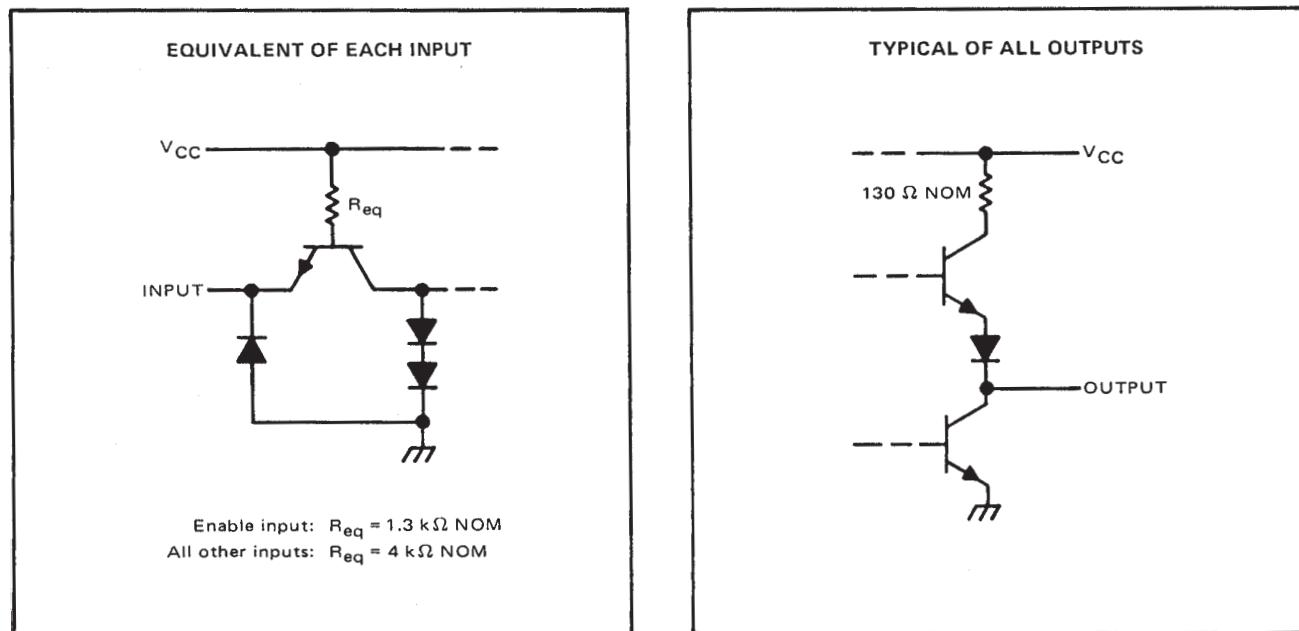
| PARAMETER <sup>†</sup> | FROM<br>(INPUT) | TO<br>(OUTPUT)       | TEST CONDITIONS  |     |     | UNIT |
|------------------------|-----------------|----------------------|--|-----|-----|------|
|                        |                 |                      | MIN  | TYP | MAX |      |
| $f_{max}$              |                 |                      | $C_L = 15 \text{ pF}$ , $R_L = 400 \Omega$ ,<br>See Figures 1 and 3 thru 7 | 20  | 25  | MHz  |
| $t_{PLH}$              | Load            | $Q_A, Q_B, Q_C, Q_D$ |  | 22  | 33  | ns   |
| $t_{PHL}$              |                 | $Q_A, Q_B, Q_C, Q_D$ |  | 33  | 50  |      |
| $t_{PLH}$              | Data A, B, C, D | $Q_A, Q_B, Q_C, Q_D$ |  | 14  | 22  | ns   |
| $t_{PHL}$              |                 | $Q_A, Q_B, Q_C, Q_D$ |  | 35  | 50  |      |
| $t_{PLH}$              | CLK             | $\overline{RCO}$     |  | 13  | 20  | ns   |
| $t_{PHL}$              |                 | $Q_A, Q_B, Q_C, Q_D$ |  | 16  | 24  |      |
| $t_{PLH}$              | CLK             | $Q_A, Q_B, Q_C, Q_D$ |  | 16  | 24  | ns   |
| $t_{PHL}$              |                 | Max/Min              |  | 24  | 36  |      |
| $t_{PLH}$              | D/ $\bar{U}$    | $\overline{RCO}$     |  | 28  | 42  | ns   |
| $t_{PHL}$              |                 | Max/Min              |  | 37  | 52  |      |
| $t_{PLH}$              | D/ $\bar{U}$    | $\overline{RCO}$     |  | 30  | 45  | ns   |
| $t_{PHL}$              |                 | Max/Min              |  | 30  | 45  |      |
| $t_{PLH}$              | D/ $\bar{U}$    | Max/Min              |  | 21  | 33  | ns   |
| $t_{PHL}$              |                 | Max/Min              |  | 22  | 33  |      |

<sup>†</sup> $f_{max}$  = maximum clock frequency

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

## schematics of inputs and outputs



**SN54LS190, SN54LS191, SN74LS190, SN74LS191**  
**SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

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**recommended operating conditions**

|                |                                       | SN54LS190 |     |      | SN74LS190 |     |      | UNIT |  |
|----------------|---------------------------------------|-----------|-----|------|-----------|-----|------|------|--|
|                |                                       | SN54LS191 |     |      | SN74LS191 |     |      |      |  |
|                |                                       | MIN       | NOM | MAX  | MIN       | NOM | MAX  |      |  |
| $V_{CC}$       | Supply voltage                        | 4.5       | 5   | 5.5  | 4.75      | 5   | 5.25 | V    |  |
| $I_{OH}$       | High-level output current             |           |     | –0.4 |           |     | –0.4 | mA   |  |
| $I_{OL}$       | Low-level output current              |           |     | 4    |           |     | 8    | mA   |  |
| $f_{clock}$    | Clock frequency                       | 0         | 20  |      | 0         | 20  |      | MHz  |  |
| $t_{w(clock)}$ | Width of clock input pulse            | 25        |     |      | 25        |     |      | ns   |  |
| $t_{w(load)}$  | Width of load input pulse             | 35        |     |      | 35        |     |      | ns   |  |
| $t_{su}$       | Data setup time (See Figures 1 and 2) | 20        |     |      | 20        |     |      | ns   |  |
| $t_{su}$       | Load inactive state setup time        | 30        |     |      | 30        |     |      | ns   |  |
| $t_h$          | Data hold time                        | 5         |     |      | 5         |     |      | ns   |  |
| $t_h$          | Enable hold time                      | 0         |     |      | 0         |     |      | ns   |  |
| $t_{enable}$   | Count enable time (see Note 3)        | 40        |     |      | 40        |     |      | ns   |  |
| $T_A$          | Operating free-air temperature        | –55       | 125 |      | 0         | 70  |      | °C   |  |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER |   | TEST CONDITIONS <sup>†</sup>  | SN54LS190               |                  |      | SN74LS190 |                  |      | UNIT          |  |
|-----------|---|---|-------------------------|------------------|------|-----------|------------------|------|---------------|--|
|           |   |   | SN54LS191               |                  |      | SN74LS191 |                  |      |               |  |
|           |   |   | MIN                     | TYP <sup>‡</sup> | MAX  | MIN       | TYP <sup>‡</sup> | MAX  |               |  |
| $V_{IH}$  | High-level input voltage                          |   | 2                       |                  |      | 2         |                  |      | V             |  |
| $V_{IL}$  | Low-level input voltage                           |   |                         | 0.7              |      |           | 0.8              |      | V             |  |
| $V_{IK}$  | Input clamp voltage                               | $V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$  |                         |                  | –1.5 |           |                  | –1.5 | V             |  |
| $V_{OH}$  | High-level output voltage                         | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = V_{IL} \text{ max}$ , $I_{OH} = -400 \mu\text{A}$ | 2.5                     | 3.4              |      | 2.7       | 3.4              |      | V             |  |
| $V_{OL}$  | Low-level output voltage                          | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = V_{IL} \text{ max}$                               | $I_{OL} = 4 \text{ mA}$ | 0.25             | 0.4  | 0.25      | 0.4              |      | V             |  |
|           |   |   | $I_{OL} = 8 \text{ mA}$ |                  |      |           | 0.35             | 0.5  |               |  |
| $I_I$     | High-level input current at maximum input voltage | $V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$   |                         | 0.3              |      | 0.3       |                  |      | mA            |  |
|           |   |   |                         | 0.1              |      | 0.1       |                  |      |               |  |
| $I_{IH}$  | High-level input current                          | $V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$   |                         | 60               |      | 60        |                  |      | $\mu\text{A}$ |  |
|           |   |   |                         | 20               |      | 20        |                  |      |               |  |
| $I_{IL}$  | Low-level input current                           | $V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$   |                         | –1.2             |      | –1.2      |                  |      | mA            |  |
|           |   |   |                         | –0.4             |      | –0.4      |                  |      |               |  |
| $I_{OS}$  | Short-circuit output current <sup>§</sup>         | $V_{CC} = \text{MAX}$ ,   |                         | –20              | –100 | –20       | –100             |      | mA            |  |
| $I_{CC}$  | Supply current                                    | $V_{CC} = \text{MAX}$ , See Note 2  |                         | 20               | 35   | 20        | 35               |      | mA            |  |

<sup>†</sup>For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 2.  $I_{CC}$  is measured with all inputs grounded and all outputs open.

3. Minimum count enable time is the interval immediately preceding the rising edge of the clock pulse during which interval the count enable input must be low to ensure counting.

# SN54LS190, SN54LS191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

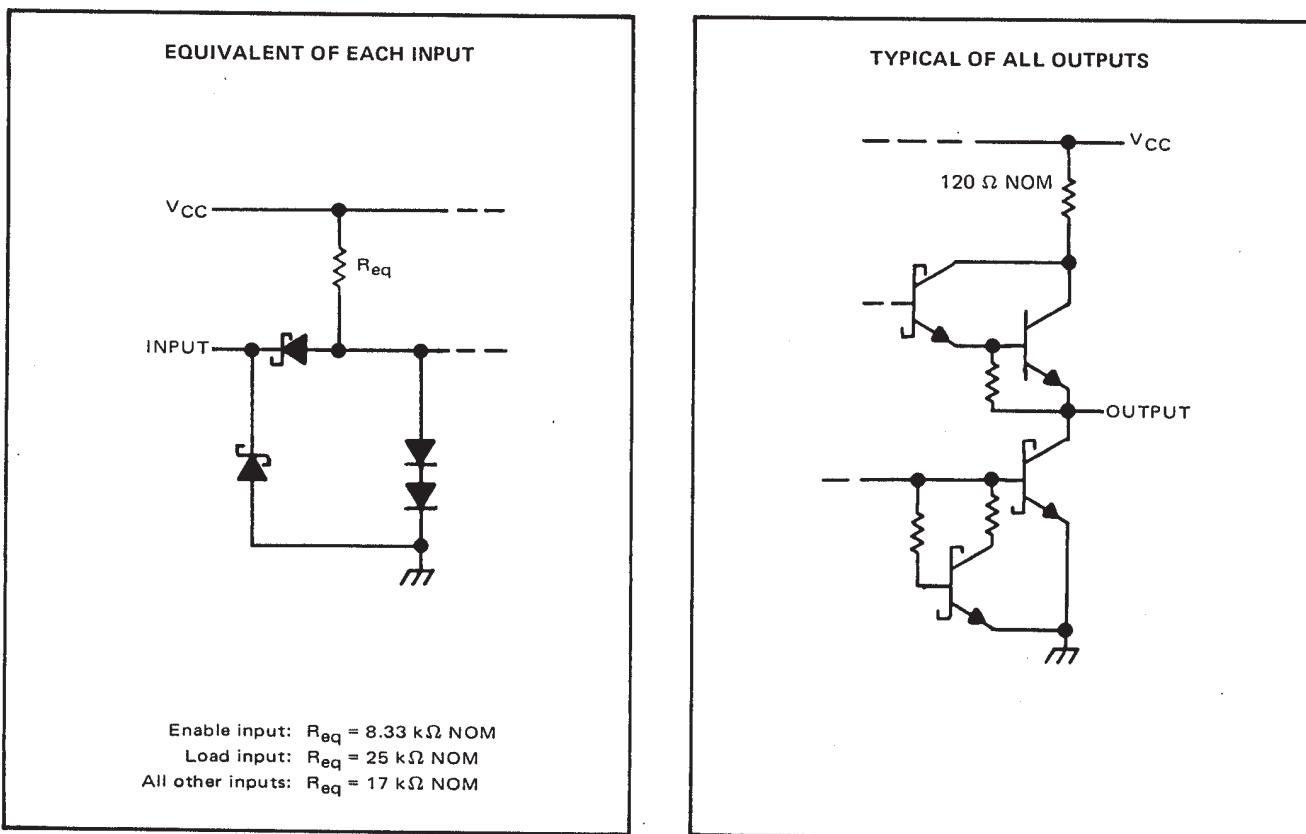
| PARAMETER <sup>†</sup> | FROM<br>(INPUT)   | TO<br>(OUTPUT)       | TEST CONDITIONS   | 'LS190, 'LS191 |     |     | UNIT |
|------------------------|-------------------|----------------------|---|----------------|-----|-----|------|
|                        |                   |                      |   | MIN            | TYP | MAX |      |
| $f_{max}$              |                   |                      | $C_L = 15 \text{ pF}$ , $R_L = 2 \text{ k}\Omega$ ,<br>See Figures 1 and 3 thru 7 | 20             | 25  |     | MHz  |
| $t_{PLH}$              | Load              | $Q_A, Q_B, Q_C, Q_D$ |   | 22             | 33  |     | ns   |
| $t_{PHL}$              |                   | $Q_A, Q_B, Q_C, Q_D$ |   | 33             | 50  |     | ns   |
| $t_{PLH}$              | Data A, B, C, D   | $Q_A, Q_B, Q_C, Q_D$ |   | 20             | 32  |     | ns   |
| $t_{PHL}$              |                   | $Q_A, Q_B, Q_C, Q_D$ |   | 27             | 40  |     | ns   |
| $t_{PLH}$              | CLK               | $\overline{RCO}$     |   | 13             | 20  |     | ns   |
| $t_{PHL}$              |                   | $Q_A, Q_B, Q_C, Q_D$ |   | 16             | 24  |     | ns   |
| $t_{PLH}$              | CLK               | Max/Min              |   | 16             | 24  |     | ns   |
| $t_{PHL}$              |                   | Max/Min              |   | 24             | 36  |     | ns   |
| $t_{PLH}$              | D/Ü               | $\overline{RCO}$     |   | 28             | 42  |     | ns   |
| $t_{PHL}$              |                   | Max/Min              |   | 37             | 52  |     | ns   |
| $t_{PLH}$              | D/Ü               | $\overline{RCO}$     |   | 30             | 45  |     | ns   |
| $t_{PHL}$              |                   | Max/Min              |   | 30             | 45  |     | ns   |
| $t_{PLH}$              | $\overline{CTEN}$ | $\overline{RCO}$     |   | 21             | 33  |     | ns   |
| $t_{PHL}$              |                   | $\overline{RCO}$     |   | 22             | 33  |     | ns   |
|                        |                   |                      |   | 21             | 33  |     | ns   |
|                        |                   |                      |   | 22             | 33  |     | ns   |

<sup>†</sup> $f_{max}$  = maximum clock frequency

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

## schematics of inputs and outputs



PARAMETER MEASUREMENT INFORMATION

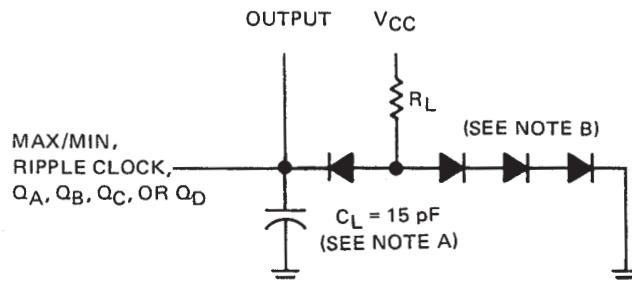


FIGURE 1—LOAD CIRCUIT  
FOR SWITCHING TIME MEASUREMENT

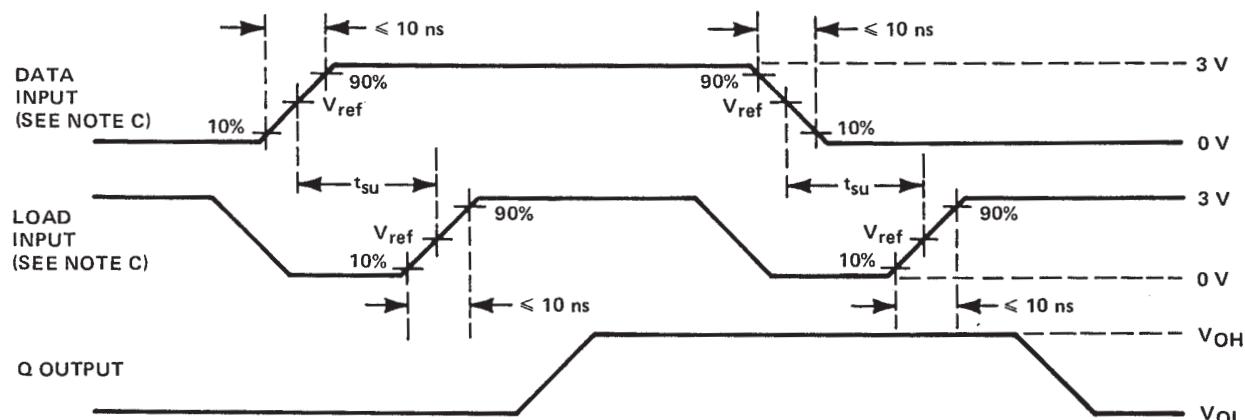
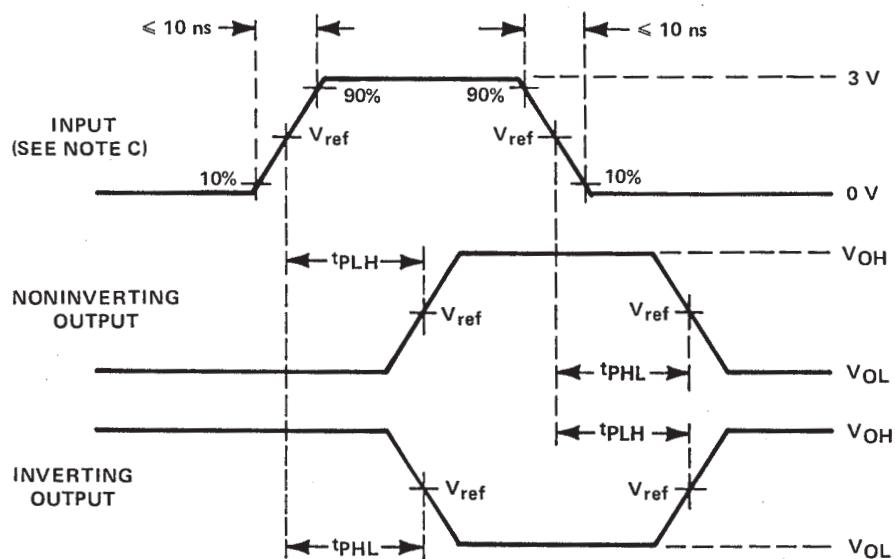


FIGURE 2—DATA SETUP TIME VOLTAGE WAVEFORMS



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

FIGURE 3—GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

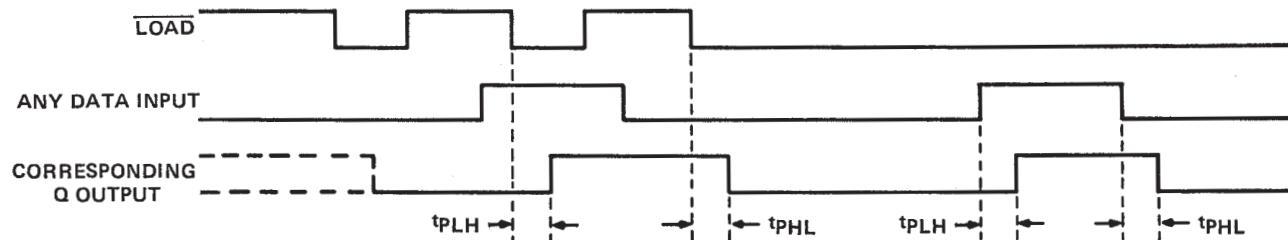
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. The input pulses are supplied by generators having the following characteristics:  $Z_{out} = 50 \Omega$ , duty cycle  $\leq 50\%$ , PRR  $\leq 1$  MHz.  
 D.  $V_{ref} = 1.5$  V for '190 and '191; 1.3 V for 'LS190 and 'LS191.

SN54190, SN54191, SN54LS190, SN54LS191,  
SN74190, SN74191, SN74LS190, SN74LS191

## SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

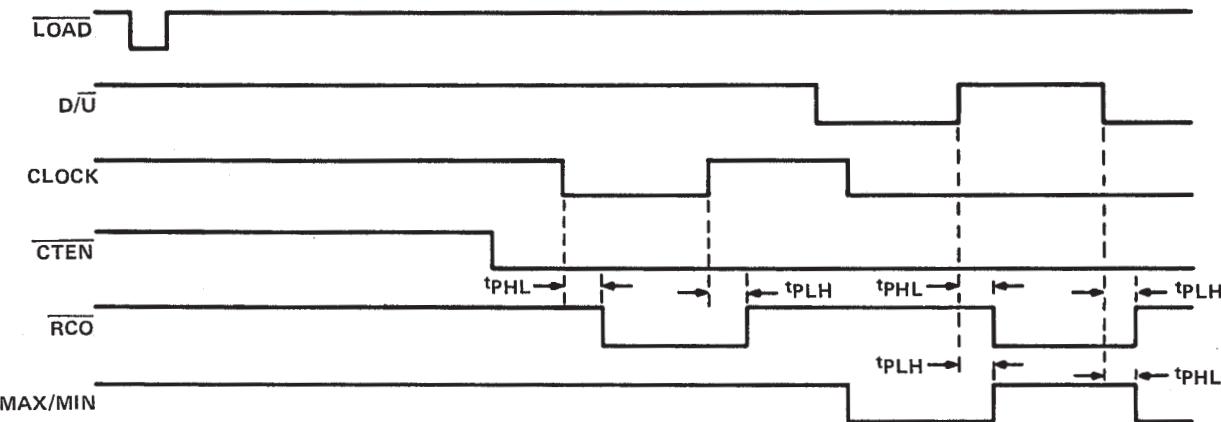
SDLS072 - DECEMBER 1972 - REVISED MARCH 1988

### PARAMETER MEASUREMENT INFORMATION (continued)



NOTE E: Conditions on other inputs are irrelevant.

FIGURE 4—LOAD TO OUTPUT AND DATA TO OUTPUT

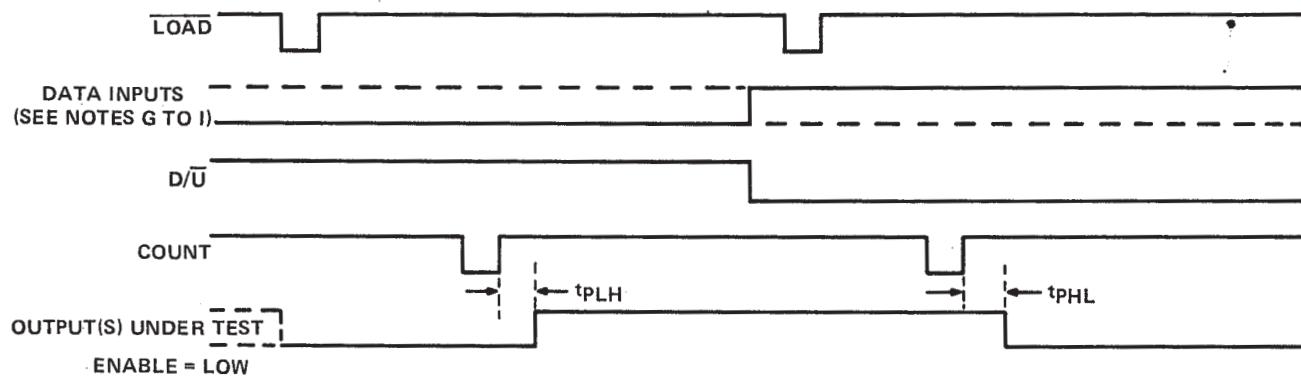


NOTE F: All data inputs are low.

FIGURE 5—ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN

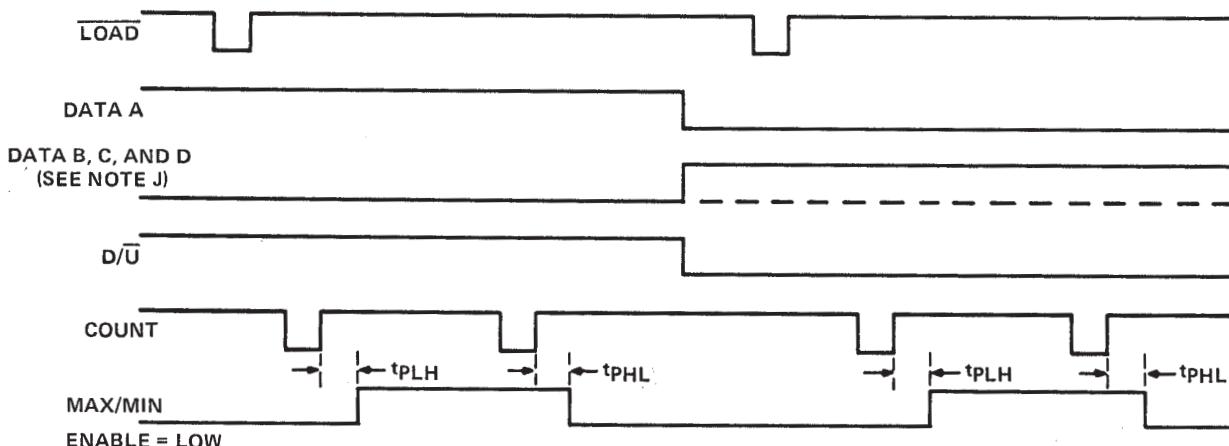
PARAMETER MEASUREMENT INFORMATION (continued)

switching characteristics (continued)



NOTES: G. To test  $Q_A$ ,  $Q_B$ , and  $Q_C$  outputs of '190 and 'LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.  
 H. To test  $Q_D$  output of '190 and 'LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.  
 I. To test  $Q_A$ ,  $Q_B$ ,  $Q_C$ , and  $Q_D$  outputs of '191 and 'LS191: All four data inputs are shown by the solid line.

FIGURE 6-CLOCK TO OUTPUT



NOTE J: Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

FIGURE 7-CLOCK TO MAX/MIN

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