Rochester Electronics®

Datasheet

# SN54265, 74265

## *Quadruple Complementary-Output Elements*

The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input.

### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

FOR REFERENCE ONLY

# SN54265, SN74265
# QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

SDLS088

DECEMBER 1983 – REVISED MARCH 1988

## FOR SYMMETRICAL GENERATION OF COMPLEMENTARY TTL SIGNALS

- **Switching Time Skew of the Complementary Outputs Is Typically 0.5 ns . . . Not More than 3 ns at Rated Loading**
- **Full Fan-Out to 20 High-Level and 10 Low-Level 54/74 Loads**
- **Active Pull-Down Provides Square Transfer Characteristics**

### description

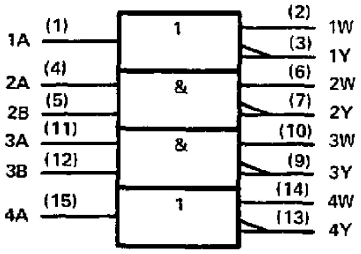
The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input. They are designed specifically for use in applications such as:

- Symmetrical clock/$\overline{\text{clock}}$ generators
- Complementary input circuit for decoders and code converters
- Switch debouncing
- Differential line driver

Examples of these four functions are illustrated in the typical application data.

The SN54265 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74265 is characterized for operation from 0°C to 70°C.

### logic symbol†




†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

### logic diagrams

**ELEMENTS 1 and 4**


**ELEMENTS 2 and 3**

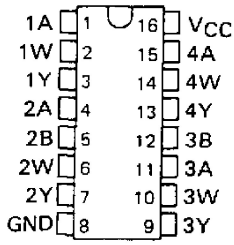

### positive logic

$Y = \overline{A}$ $W = A$

$Y = \overline{AB}$ or $Y = \overline{A} + \overline{B}$

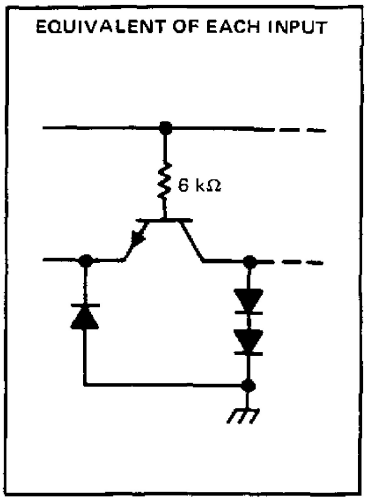
$W = AB$ or $W = \overline{\overline{A} + \overline{B}}$

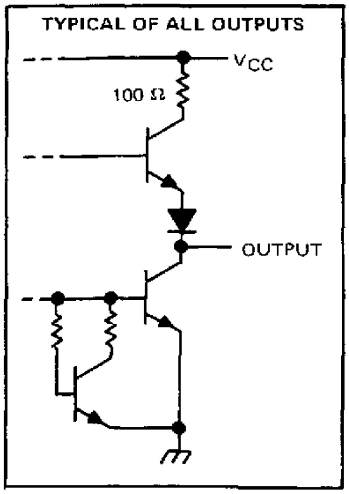
**SN54265 . . . J OR W PACKAGE**
**SN74265 . . . N PACKAGE**
**(TOP VIEW)**




NC – No internal connection

### schematics of inputs and outputs






TEXAS INSTRUMENTS
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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54265 . . . . . −55°C to 125°C
SN74265 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | SN54265 | | | SN74265 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −800 | | | −800 | μA |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, | $I_{OH}$ = −800 μA | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, | $I_{OL}$ = 16 mA | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −1.6 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX, | SN54265 | −20 | | −57 | mA |
| | | | SN74265 | −18 | | −57 | |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, | See Note 2 | | 25 | 34 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with all outputs open and all inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH(W)}$ | A or B (as applicable) | W | $R_L$ = 400 Ω, $C_L$ = 15 pF, See Note 3 | | 11.6 | 18 | ns |
| $t_{PHL(Y)}$ | | Y | | | 11.3 | 18 | |
| $t_{PHL(W)}$ | A or B (as applicable) | W | | | 9.8 | 18 | ns |
| $t_{PLH(Y)}$ | | Y | | | 10.2 | 18 | |
| $t_{PLH(W)}-t_{PHL(Y)}$ | A or B (as applicable) | W with respect to Y | | | +0.3 | ±3 | ns |
| $t_{PHL(W)}-t_{PLH(Y)}$ | | | | | −0.4 | ±3 | |

$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
$t_{PXX(W)}-t_{PXX(Y)}$ = Difference in indicated propagation delay times at the W and Y outputs, respectively.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME DIFFERENCE
vs
FREE-AIR TEMPERATURE

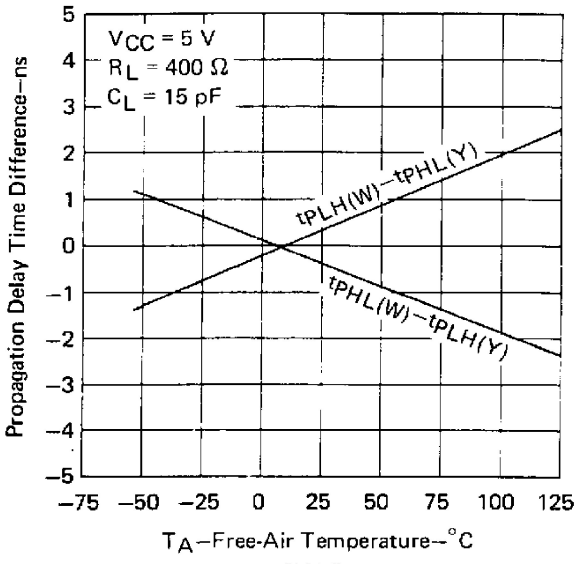



FIGURE 1

PROPAGATION DELAY TIME DIFFERENCE
vs
SUPPLY VOLTAGE

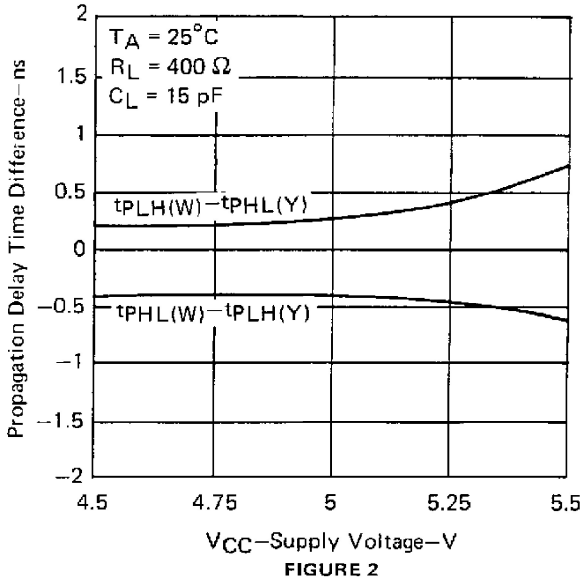



FIGURE 2

PROPAGATION DELAY TIME DIFFERENCE vs LOAD CAPACITANCE

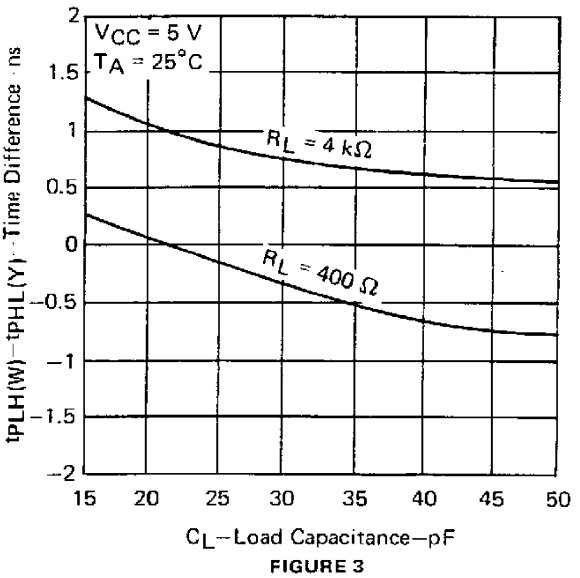



FIGURE 3

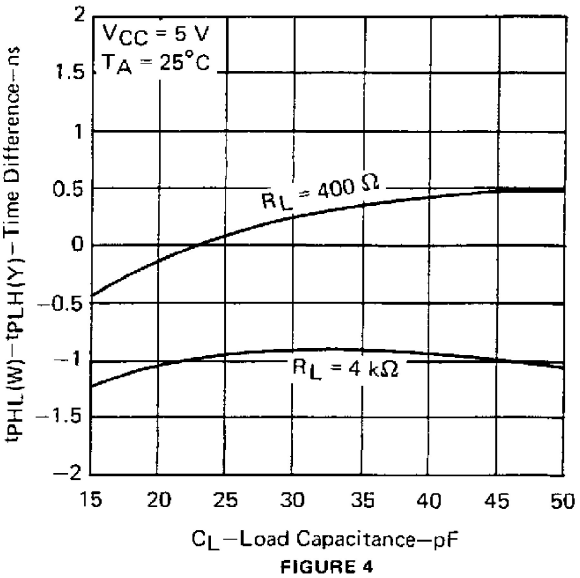



FIGURE 4

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54265 only.

## TYPICAL APPLICATION DATA

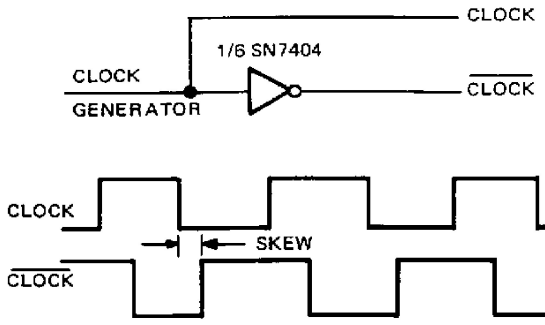



FIGURE A – TYPICAL CLOCK/$\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

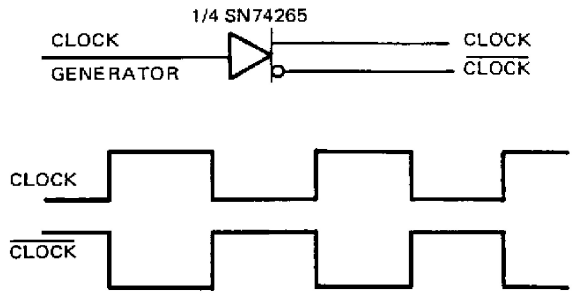



FIGURE B – SKEWLESS CLOCK/$\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

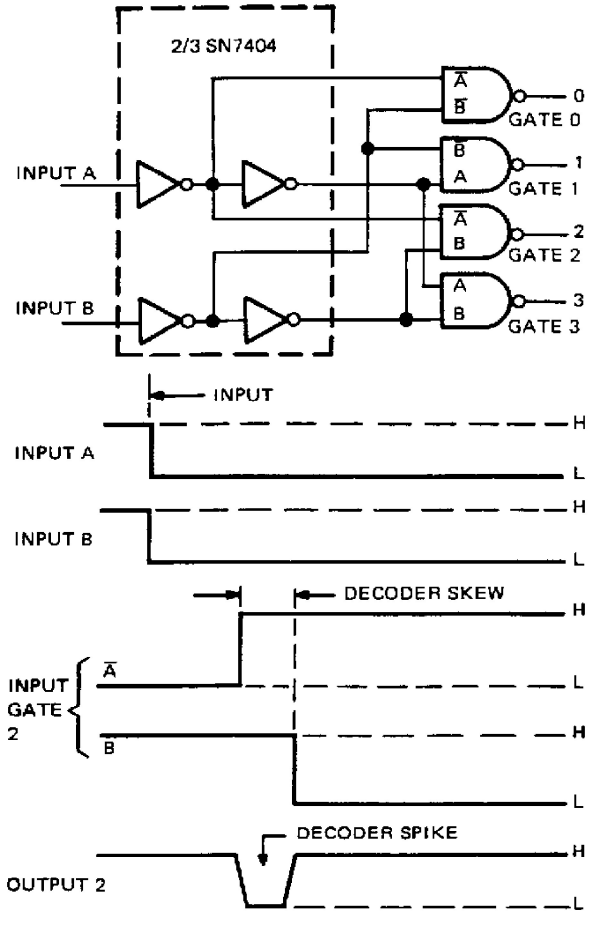



FIGURE C – TYPICAL DECODER/CODE CONVERTER

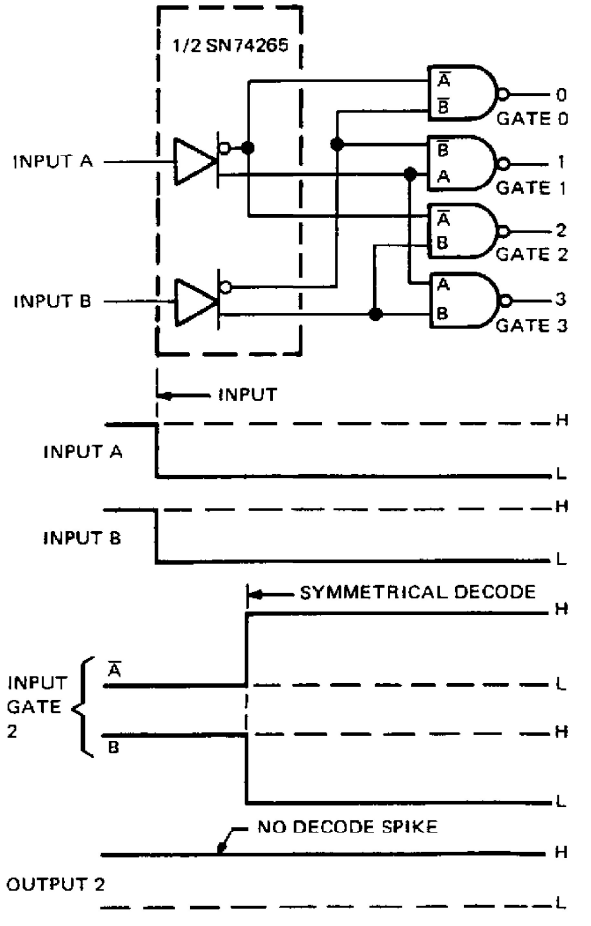



FIGURE D – SYMMETRICAL DECODER/CODE CONVERTER

## TYPICAL APPLICATION DATA

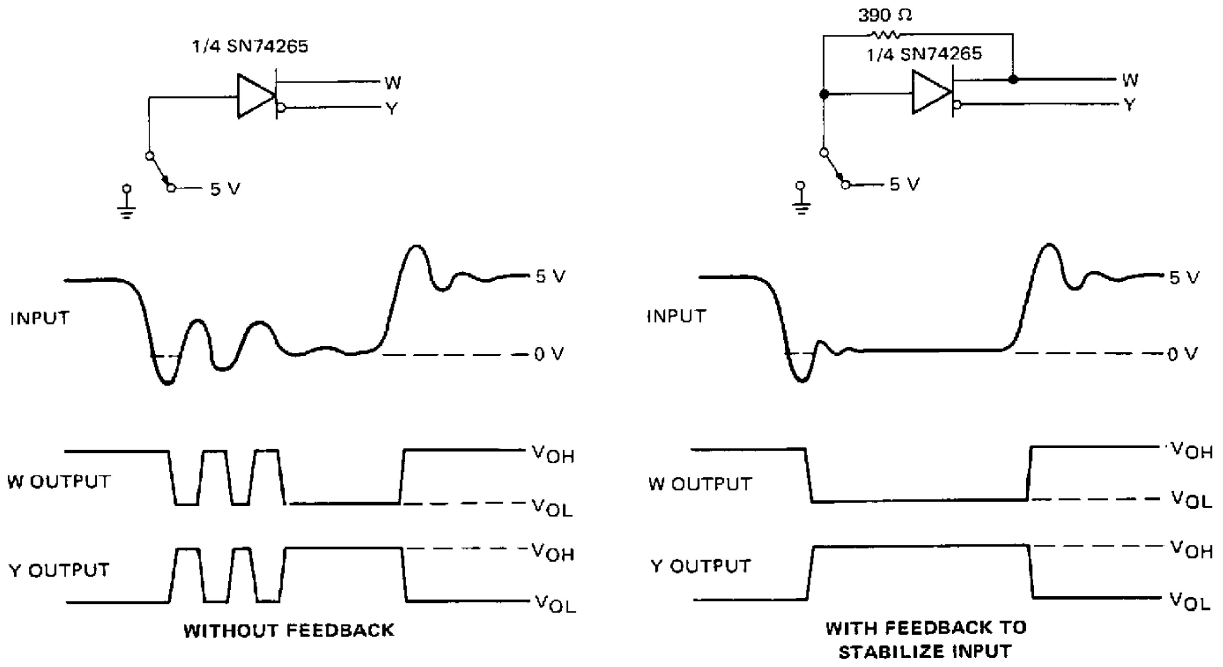



**FIGURE E – SWITCH DEBOUNCER**

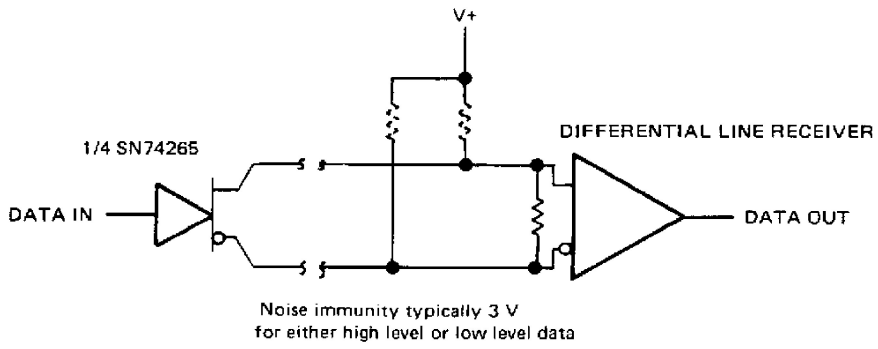



**FIGURE F – DIFFERENTIAL LINE DRIVER**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN54265J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74265N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74265N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SNJ54265J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Samples Not Available |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



**OTHER QUALIFIED VERSIONS OF SN54265, SN74265 :**

- Catalog: SN74265
- Military: SN54265

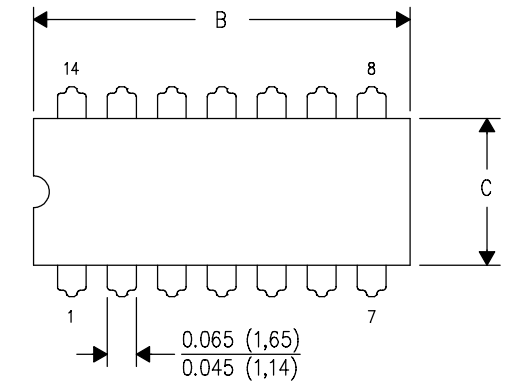
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

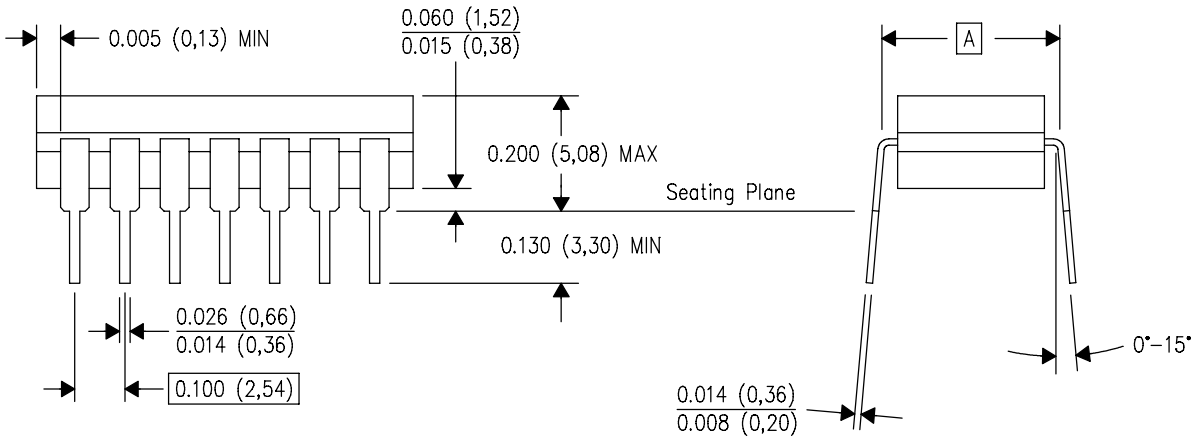
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



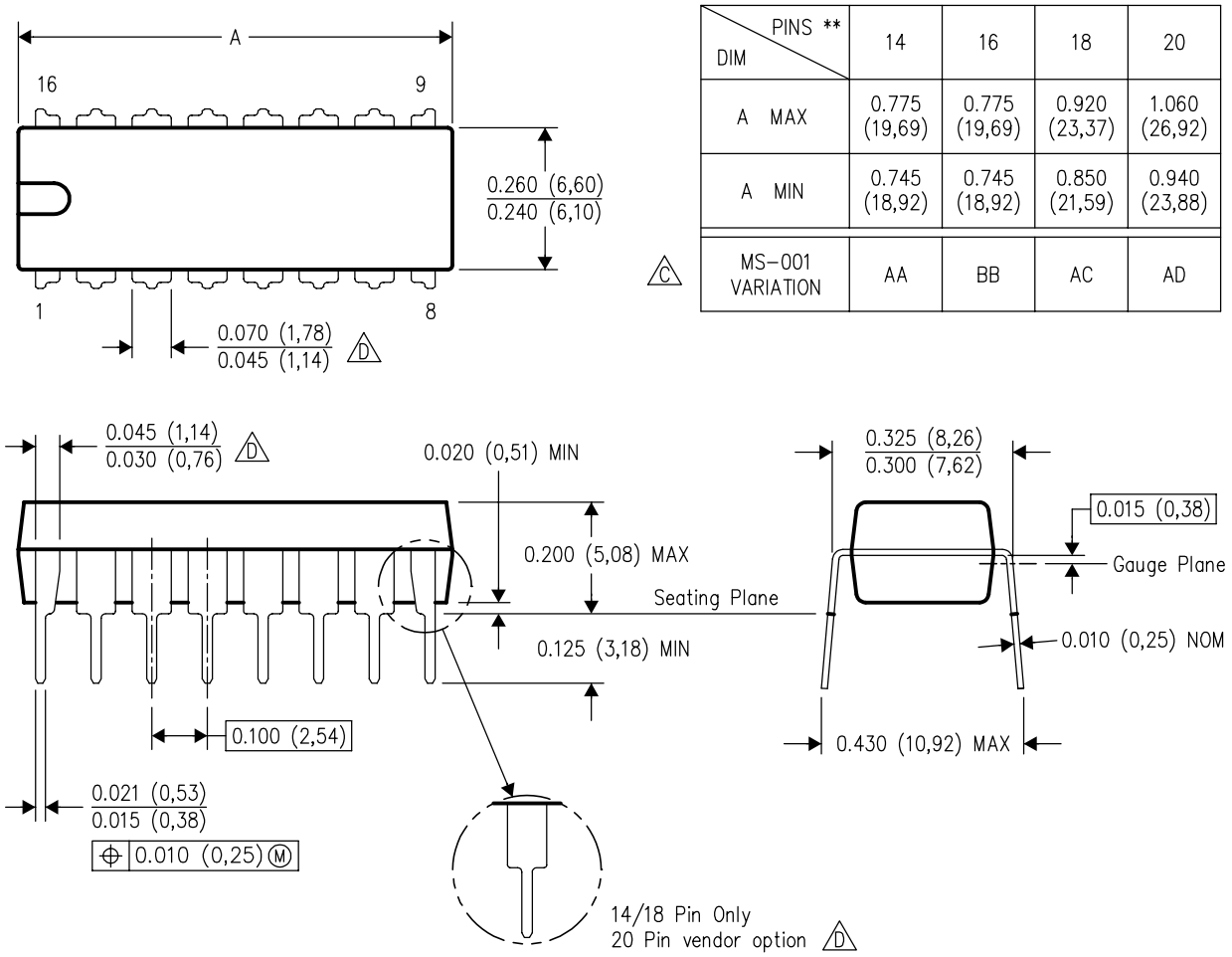

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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