APS12205, APS12215, and APS12235

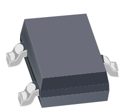
High-Temperature Hall-Effect Latches for Low Voltage Applications

FEATURES AND BENEFITS

- Optimized for applications with regulated power rails
  - □ Operation from 2.8 to 5.5 V
- AEC-Q100 automotive qualified
- Operation up to 175°C junction temperature
- Dynamic offset cancellation
  - □ Resistant to physical stress
  - □ Superior temperature stability
- Symmetrical latch switchpoints
- Output short-circuit protection
- Solid-state reliability
- Industry-standard packages and pinouts

PACKAGES:

Not to scale



3-pin SOT23W
(suffix LH)

3-pin SIP
(suffix UA)

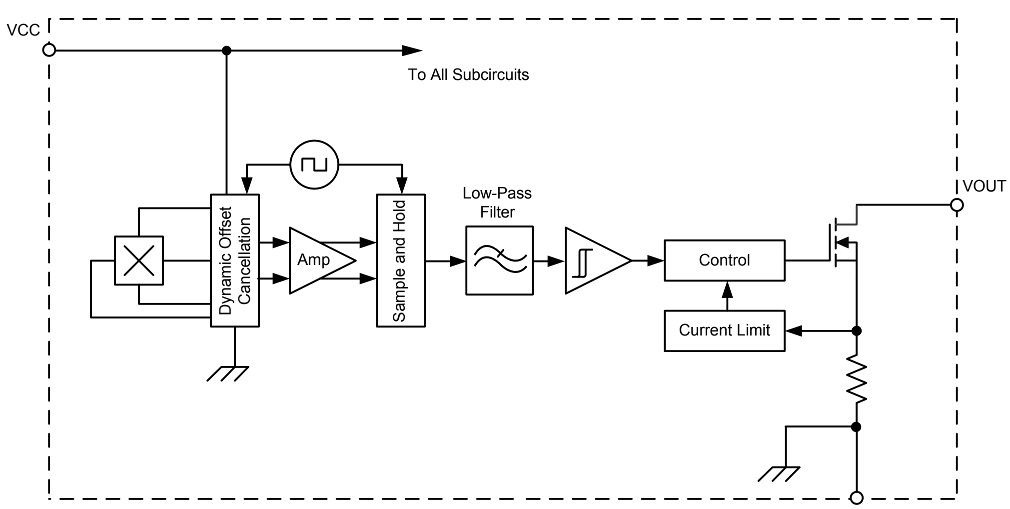
DESCRIPTION

The APS12205, APS12215, and APS12235 Hall-effect sensor ICs are extremely temperature-stable and stress-resistant devices especially suited for operation over extended junction temperature ranges up to 175°C. Superior high-temperature performance is made possible through dynamic offset cancellation, which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

The single silicon chip includes: a Hall plate, small signal amplifier, chopper stabilization, Schmitt trigger, and a short-circuit-protected open-drain output. A south pole of sufficient strength turns the output on; a north pole of sufficient strength is necessary to turn the output off. For applications requiring operation from greater than 5.5 V or operation directly from a battery, refer to the A1220, A1221, or A1223.

Two package styles provide a choice of through-hole or surface mounting. Package type LH is a modified 3-pin SOT23W surface-mount package, while UA is a three-pin ultramini SIP for through-hole mounting. Both packages are lead (Pb) free, with 100% matte-tin-plated leadframes.

Functional Block Diagram



SELECTION GUIDE

Part Number	Packing [1]	Mounting	Branding	Ambient, T_A	B_{RP} (Min)	B_{OP} (Max)
APS12205ELHALX	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	A04	–40°C to 85°C	–40 G	40 G
APS12205ELHALT [2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	A04			
APS12205LLHALX	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	A04	–40°C to 150°C		
APS12205LLHALT [2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	A04			
APS12205LUAA	Bulk, 500 pieces/bag	3-pin SIP through hole	A18			
APS12215LLHALX	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	A01	–40°C to 150°C	–90 G	90 G
APS12215LLHALT [2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	A01			
APS12215LUAA [3]	Bulk, 500 pieces/bag	3-pin SIP through hole	A03			
APS12235LLHALX [3]	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	A35	–40°C to 150°C	–180 G	180 G
APS12235LLHALT [2][3]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	A35			
APS12235LUAA [3]	Bulk, 500 pieces/bag	3-pin SIP through hole	A36			

[1] Contact Allegro for additional packing options.
[2] Available through authorized Allegro distributors only.
[3] Part variants APS12215LUAA, APS12235LUAA, APS12235LLHALT, and APS12235LLHALX are in production but have been determined to be LAST TIME BUY. This classification indicates that the part variants are obsolete and notice has been given. Sale of these devices are currently restricted to existing customer applications. These devices should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status change date: September 30, 2024. Last-time buy date: January 31, 2025.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.3	V
Output Off Voltage	V_{OUT}		6	V
Output Current	I_{OUT}	Through short-circuit current limiting device.	60	mA
Maximum Junction Temperature	T_J(max)		165	°C
		For 1000 hours.	175	°C
Storage Temperature	T_{stg}		–65 to 170	°C

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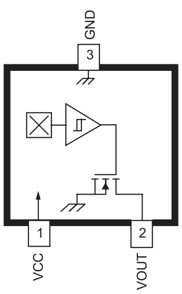
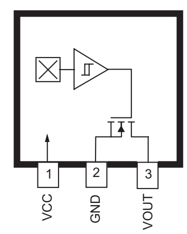
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package LH



Package UA

Terminal List

Name	Description	Number	
		Package LH	Package UA
VCC	Connects power supply to chip	1	1
VOUT	Output from circuit	2	3
GND	Ground	3	2

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ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and ambient temperature range, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit[2]
ELECTRICAL CHARACTERISTICS							
Forward Supply Voltage	V_{CC}	Operating, T_J < 175°C		2.8	–	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.5 V		–	2	3	mA
Output Leakage Current	I_{OUTOFF}	V_{OUT} = 5.5 V, B < B_{RP}		–	–	10	µA
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 5 mA, B > B_{OP}		–	50	500	mV
Output Current	I_{OUT}	Recommended value used during characterization		–	5	–	mA
Output Short-Circuit Current Limit	I_{OM}	B > B_{OP}		30	–	60	mA
Power-On Time[3]	t_{ON}	V_{CC} ≥ 2.8 V, B < B_{RP}(min) – 10 G, B > B_{OP}(max) + 10 G		–	–	25	µs
Power-On State, Output[3]	POS	V_{CC} ≥ V_{CC}(min), t < t_{ON}			Low		–
Chopping Frequency	f_C			–	800	–	kHz
Output Rise Time[3][4]	t_r	$R_{PULL-UP}$ = 1 kΩ, C_L = 20 pF		–	0.2	2	µs
Output Fall Time[3][4]	t_f	$R_{PULL-UP}$ = 1 kΩ, C_L = 20 pF		–	0.1	2	µs
MAGNETIC CHARACTERISTICS							
Operate Point	B_{OP}	APS12205		5	22	40	G
		APS12215		15	50	90	G
		APS12235		100	150	180	G
Release Point	B_{RP}	APS12205		–40	–22	–5	G
		APS12215		–90	–50	–15	G
		APS12235		–180	–150	–100	G
Hysteresis	B_{HYS}	APS12205	(B_{OP} – B_{RP})	10	45	80	G
		APS12215		30	100	180	G
		APS12235		200	300	360	G

[1] Typical data are are at T_A = 25°C and V_{CC} = 5 V, and are for initial design estimations only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] Guaranteed by device design and characterization.
[4] C_L = oscilloscope probe capacitance.

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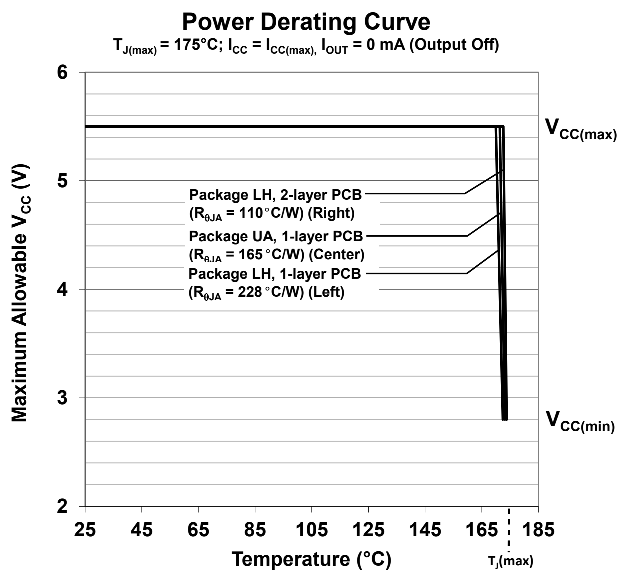
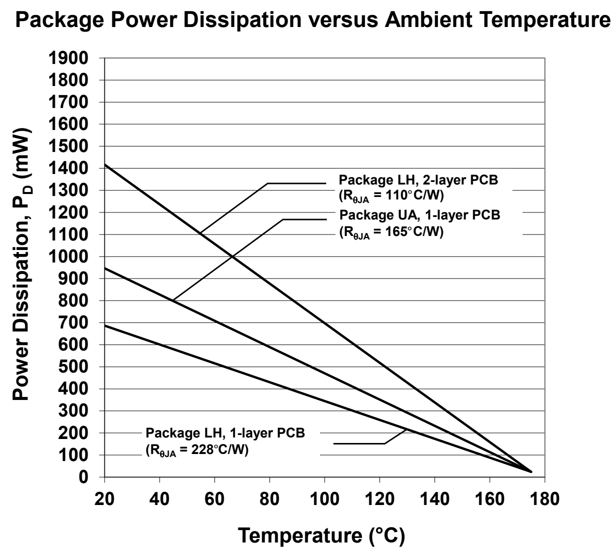
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in^2 of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W





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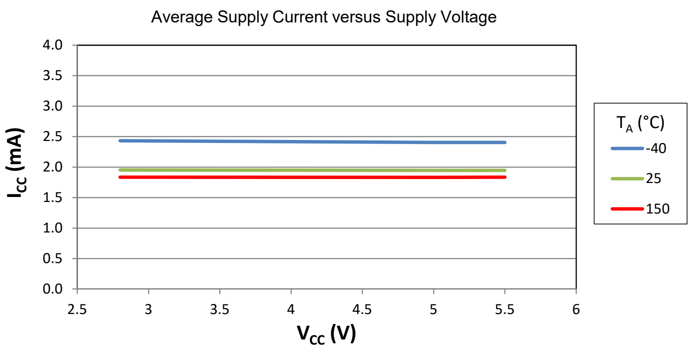
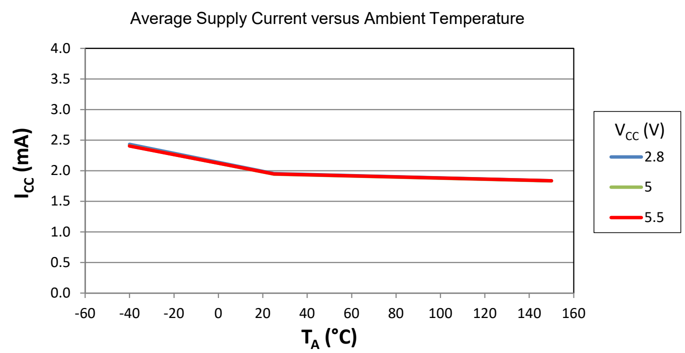
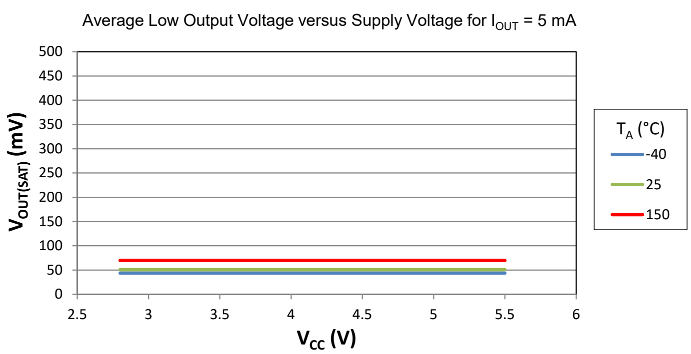
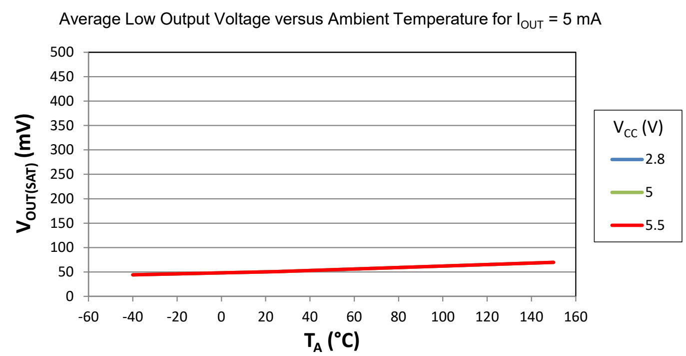
CHARACTERISTIC PERFORMANCE

Electrical Characteristics









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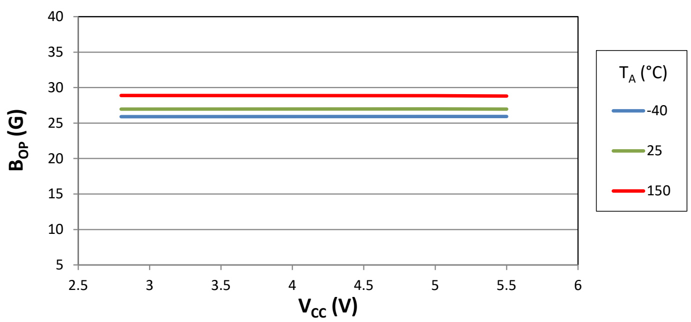
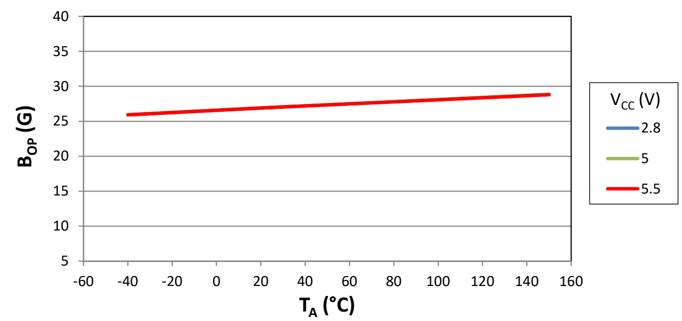
CHARACTERISTIC PERFORMANCE (continued)

APS12205 Magnetic Characteristics

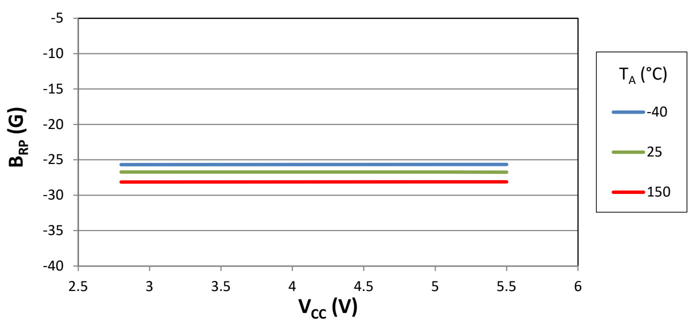
Average Operate Point versus Supply Voltage



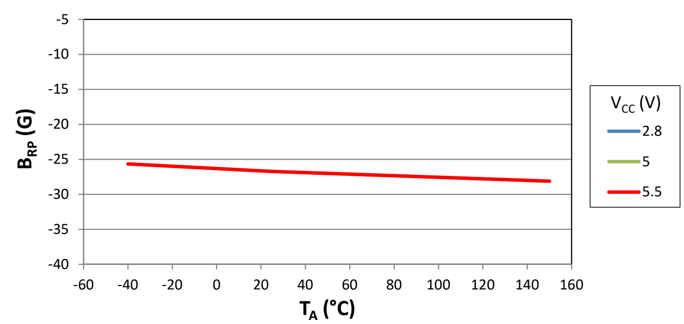
Average Operate Point versus Ambient Temperature



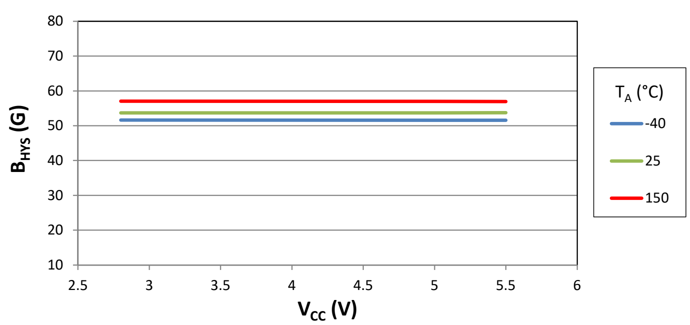
Average Release Point versus Supply Voltage



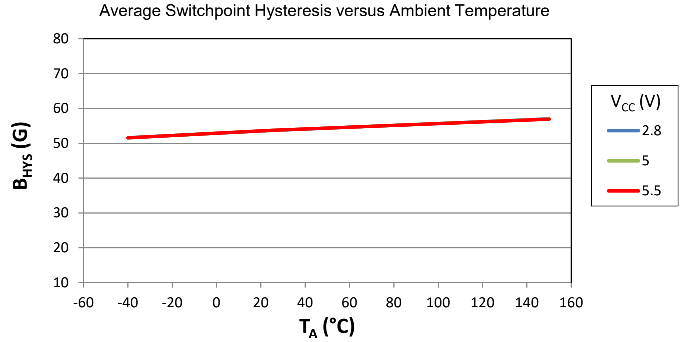
Average Release Point versus Ambient Temperature



Average Switchpoint Hysteresis versus Supply Voltage



Average Switchpoint Hysteresis versus Ambient Temperature



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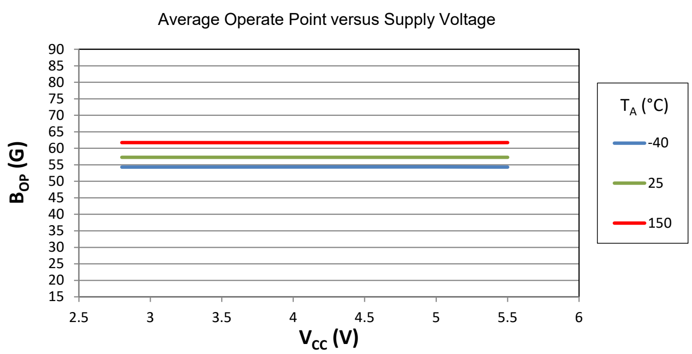
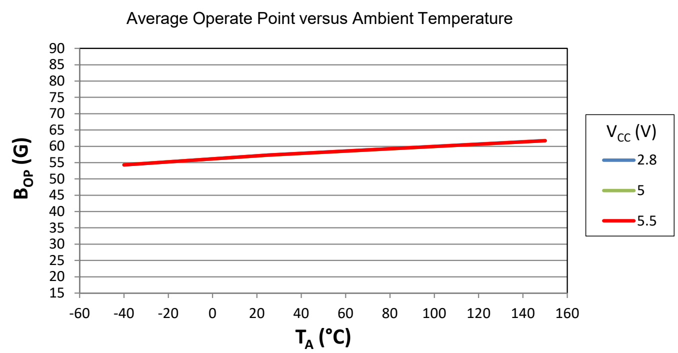
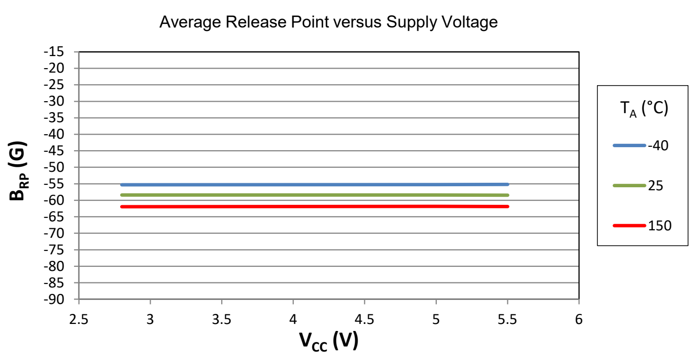
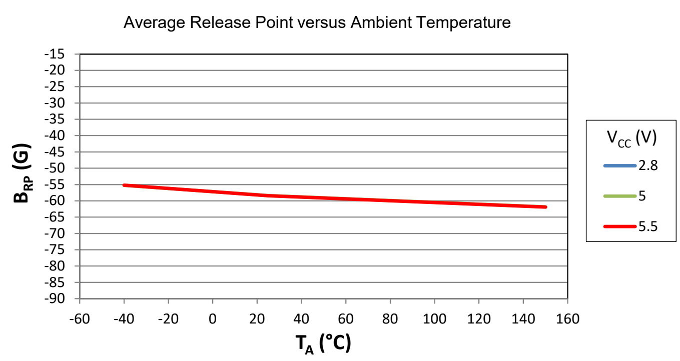
CHARACTERISTIC PERFORMANCE (continued)

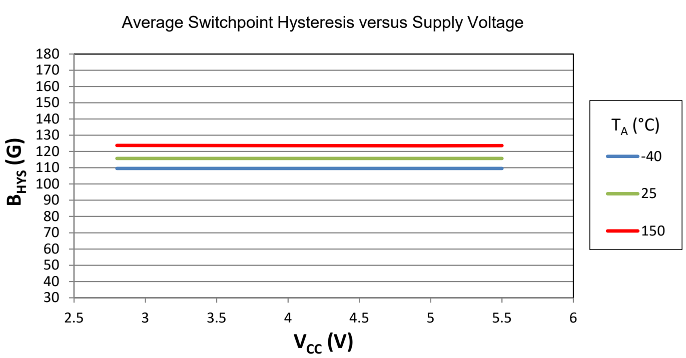
APS12215 Magnetic Characteristics

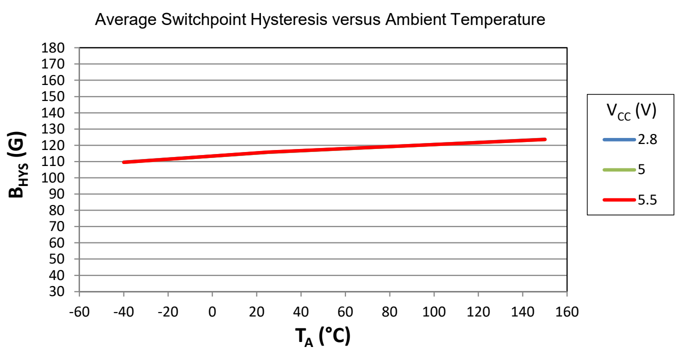












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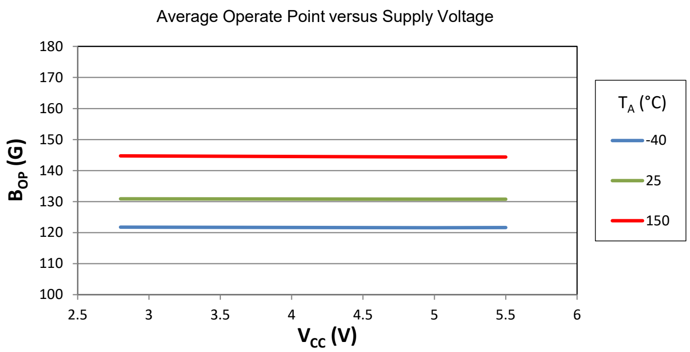
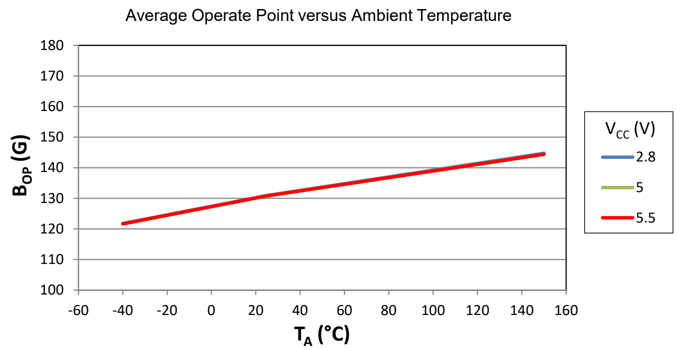
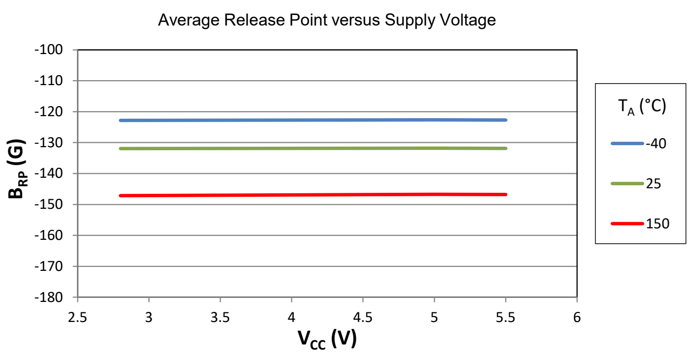
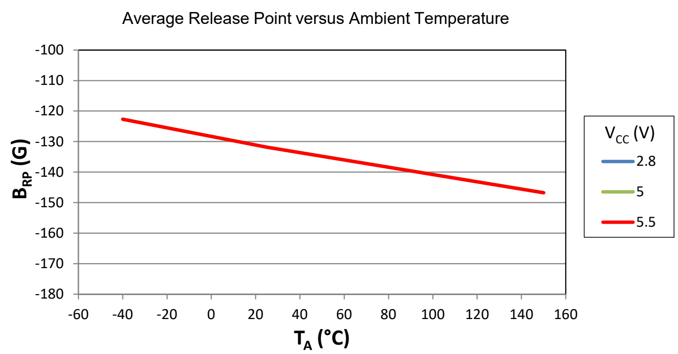
CHARACTERISTIC PERFORMANCE (continued)

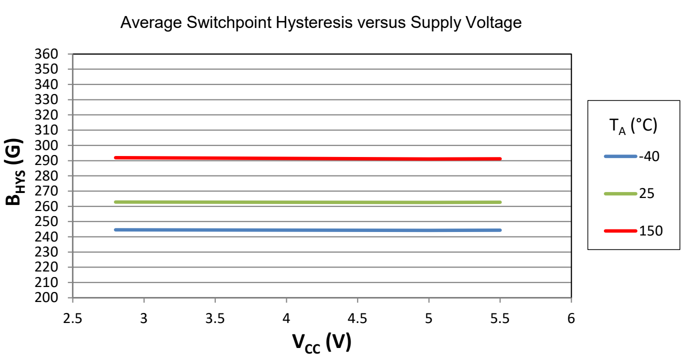
APS12235 Magnetic Characteristics

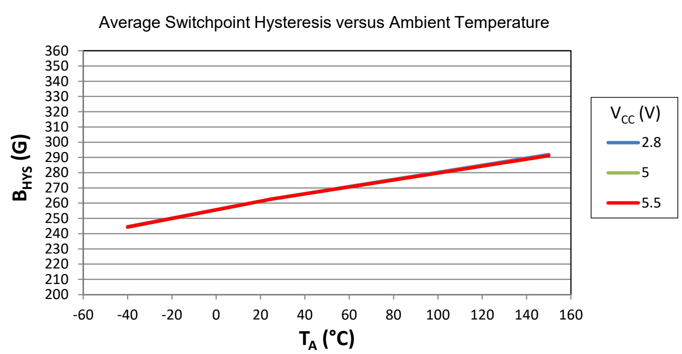












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FUNCTIONAL DESCRIPTION

OPERATION

The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP} (see Figure 1). After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of continuously sinking up to 30 mA. When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Removal of the magnetic field will leave the device output latched on if the last crossed switchpoint is B_{OP}, or latched off if the last crossed switch point is B_{RP}.

POWER-ON BEHAVIOR

Device power-on occurs once t_{ON} has elapsed. During the time prior to t_{ON}, and after $V_{CC} \geq V_{CC}(min)$, the output state is $V_{OUT(SAT)}$ (Low). After t_{ON} has elapsed, the output will correspond with the applied magnetic field for $B > B_{OP}$ or $B < B_{RP}$. See Figure 2 for an example.

Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) will give an output state of $V_{OUT(SAT)}$. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

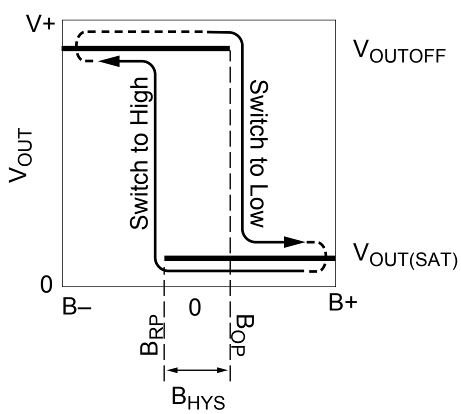

Figure 1: Switching Behavior of Latches

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity.

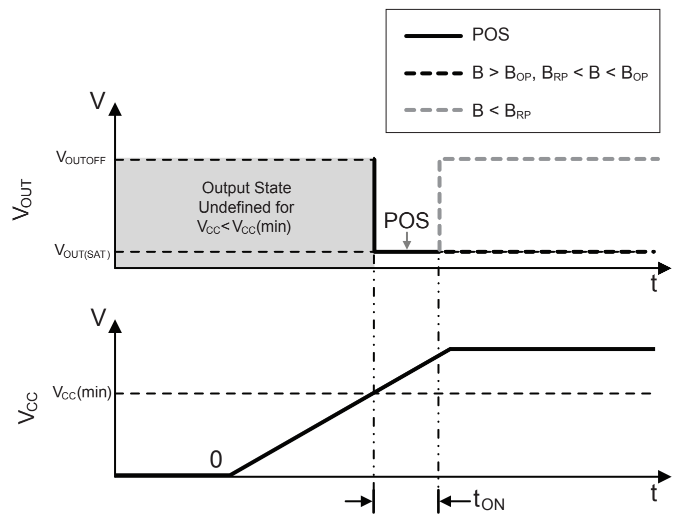

Figure 2: Power-On Timing Diagram

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APPLICATIONS

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to guarantee correct performance under harsh environmental conditions and to reduce noise from internal circuitry. As is shown in Figure 3, a 0.1 µF capacitor is typical.

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*

All are provided on the Allegro website:

www.allegromicro.com

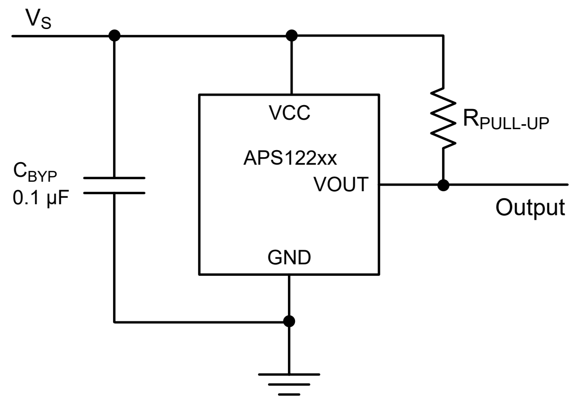

Figure 3: Typical Application Circuit

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CHOPPER STABILIZATION

A limiting factor for switchpoint accuracy when using Hall-effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The Allegro technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 4 illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro's innovative chopper stabilization technique uses a high-frequency clock. The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS12205, APS12215, and APS12235 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

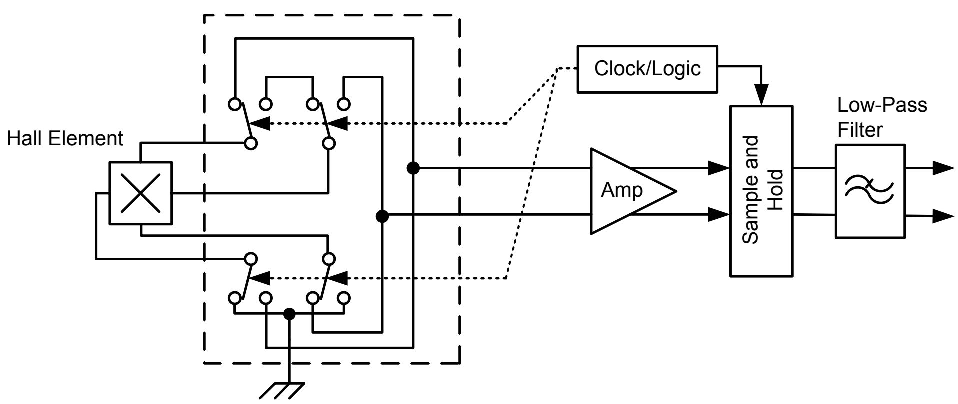

Figure 4: Model of Chopper Stabilization (Dynamic Offset Cancellation)

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The resulting power dissipation capability directly reflects upon the ability of the device to withstand extreme operating conditions. The junction temperature mission profile specified in the Absolute Maximum Ratings table designates a total operating life capability based on qualification for the most extreme conditions, where T_J may reach 175°C.

The silicon IC is heated internally when current is flowing into the VCC terminal. When the output is on, current sinking into the VOUT terminal generates additional heat. This may increase the junction temperature, T_J, above the surrounding ambient temperature. The APS12205, APS12215, and APS12235 are permitted to operate up to T_J = 175°C. As mentioned above, an operating device will increase T_J according to equations 1, 2, and 3 below. This allows an estimation of the maximum ambient operating temperature.

$$P_D = V_{IN} \times I_{IN} \tag{1}$$

$$\Delta T = P_D \times R_{\theta JA} \tag{2}$$

$$T_J = T_A + \Delta T \tag{3}$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 5 V, I_{CC} = 2.5 mA, V_{OUT} = 185 mV, I_{OUT} = 2 mA (output on), and $R_{\theta JA}$ = 165°C/W, then:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{OUT}) = (5\ V \times 2.5\ mA) + (185\ mV \times 2\ mA) = 12.5\ mW + 0.4\ mW = 12.9\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 12.9\ mW \times 165°C/W = 2.1°C$$

$$T_J = T_A + \Delta T = 25°C + 2.1°C = 27.1°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level (V_{CC}(max), I_{CC}(max)), without exceeding T_J(max), at a selected $R_{\theta JA}$.

For example, given the conditions $R_{\theta JA}$ = 228°C/W, T_J(max) = 175°C, V_{CC}(max) = 5.5 V, I_{CC}(max) = 4 mA, V_{OUT} = 500 mV, and I_{OUT} = 5 mA (output on), the maximum allowable operating ambient temperature can be determined.

The power dissipation required for the output is shown below:

$$P_D(V_{OUT}) = V_{OUT} \times I_{OUT} = 500\ mV \times 5\ mA = 2.5\ mW$$

The power dissipation required for the IC supply is shown below:

$$P_D(V_{CC}) = V_{CC} \times I_{CC} = 5.5\ V \times 4\ mA = 22\ mW$$

Next, by inverting using equation 2:

$$\Delta T = P_D \times R_{\theta JA} = [P_D(V_{OUT}) + P_D(V_{CC})] \times 228°C/W = (2.5\ mW + 22\ mW) \times 228°C/W = 24.5\ mW \times 228°C/W = 5.6°C$$

Finally, by inverting equation 3 with respect to voltage:

$$T_A(est) = T_J(max) - \Delta T = 175°C - 5.6°C = 169.4°C$$

In the above case there is only sufficient power dissipation capability to operate up to T_A(est). This particular result indicates that, at T_J(max), the application and device can only dissipate adequate amounts of heat at ambient temperatures ≤ T_A(est); the APS12205, APS12215, and APS12235 performance is not guaranteed above T_A = 150°C for the “L” temperature variant and T_A = 85°C for the “E” temperature variant.

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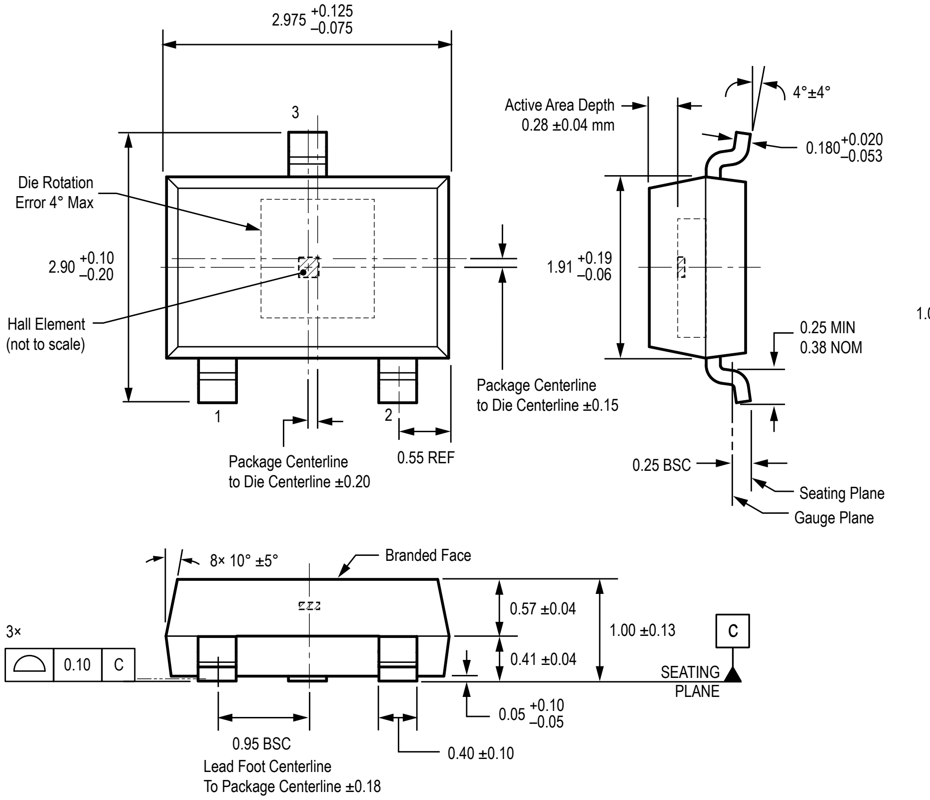
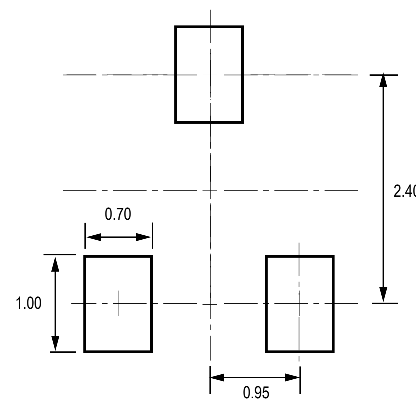
Package LH, 3-Pin (SOT-23W)

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000628, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

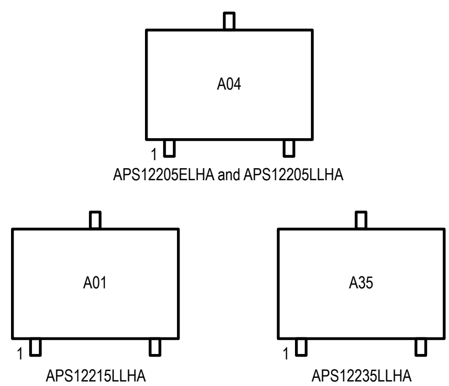




PCB Layout Reference View

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Standard Branding Reference View



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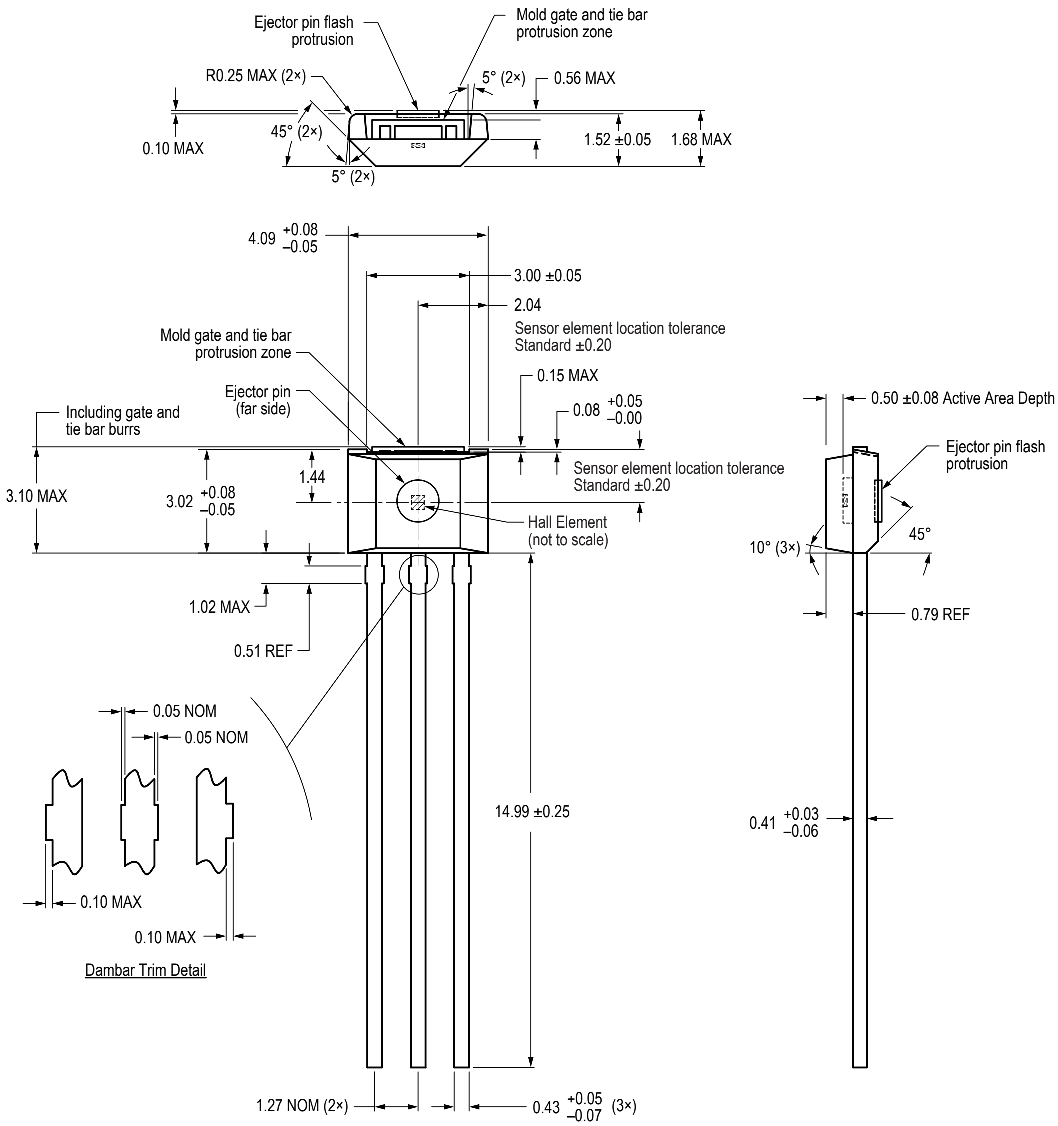
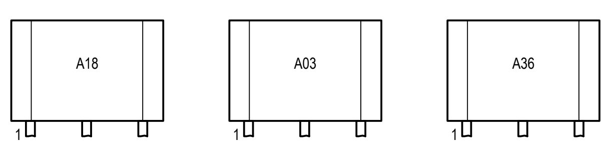
Package UA, 3-Pin SIP

For Reference Only – Not For Tooling Use

(Reference DWG-0000404, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



Standard Branding Reference View
Branding scale and appearance at supplier discretion.



APS12205LUAA APS12215LUAA APS12235LUAA

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Revision History

Number	Date	Description
–	June 3, 2016	Initial release
1	June 20, 2016	Updated Functional Block Diagram (page 1); Updated Selection Guide (page 2) and package outline drawing brand information (pages 14-15).
2	September 23, 2016	Updated Title (all pages), Selection Guide (page 2), Absolute Maximum Ratings (page 2); Electrical Characteristics (page 4); added Characteristic Performance Data (pages 6-9); updated Functional Description (page 6), Chopper Stabilization (page 12), and Power Derating sections (page 13).
3	July 5, 2018	Updated T_J(max) notes (page 2), Typical Application Circuit (page 11), Power Derating section (page 13), Package Outline Drawings (pages 14-15), and other minor editorial updates.
4	June 18, 2019	Updated Selection Guide (page 2), Power Derating section (page 13), and Package Outline Drawing branding (page 14).
5	September 10, 2021	Updated Supply Current maximum value (page 4) and package drawings (page 14-15)
6	September 30, 2024	Updated part variants APS12215LUAA, APS12235LUAA, APS12235LLHALT, and APS12235LLHALX to last-time buy status

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