

PART NUMBER

54LS76ABEA-ROCV

Rochester Electronics

Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

INCH-POUND

MIL-M-38510/301F

4 March 2004

SUPERSEDING

MIL-M-38510/301E

14 February 2003

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR LOW-POWER SCHOTTKY TTL, FLIP-FLOPS,
CASCADABLE, MONOLITHIC SILICON

Inactive for new design after 18 April 1997.

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, low-power Schottky TTL, flip-flops, bistable logic gate microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3).

1.2 Part number. The part number is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

<u>Device type</u>	<u>Circuit</u>
01	Dual J-K flip-flop with clear
02	Dual D type flip-flop with clear and preset
03	Dual J-K flip-flop with clear and preset
04	Dual J-K flip-flop with preset
05	Dual J-K flip-flop with preset and common clear and common clock
06	Hex D type flip-flop with common clear and common clock
07	Quad D type flip-flop with common clear and common clock
08	Dual, J-K flip-flop with clear
09	Dual, J-K flip-flop with clear and preset
10	Dual, J-K flip-flop with clear and preset

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
A	GDFP5-F14 or CDFP6-F14	14	Flat pack
B	GDFP4-14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
X	CQCC2-N20	20	Square leadless chip carrier
2	CQCC1-N20	20	Square leadless chip carrier

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43216-5000, or emailed to bipolar@dsccl.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at www.dodssp.daps.mil.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to 7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to 5.5 V dc
Storage temperature range	-65° to +150°C
Maximum power dissipation per flip-flop, (P_D) <u>1/</u>	25 mW
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction to case (θ_{JC}): Cases A, B, C, D, E, F, X, and 2	(See MIL-STD-1835)
Junction temperature (T_J) <u>2/</u>	175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55° to +125°C
Input set up time: Device types:	
01, 03, 04, 05, 08, 09, and 10	25 ns minimum
02, 06, and 07	20 ns minimum
Input hold time: Device types:	
01, 03, 04, 05, 08, and 10	0 ns minimum
02, 06, 07, and 09	5 ns minimum

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with MIL-PRF-38535.

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Logic diagrams. The logic diagrams shall be as specified on figure 2.

3.3.3 Truth tables. The truth tables and logic equations shall be as specified on figure 3.

3.3.4 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 10 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with, MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit	
				Min	Max		
High level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -400 μA	All	2.5		V	
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 4 mA	All		0.4	V	
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA, T _C = +25°C	All		-1.5	V	
Low level input current	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	<u>2/</u>	01, 03,	-0.030	-0.360	mA
				04	-0.010	-0.360	
				05, 08, 10			
	<u>2/</u>		06, 07	-0.075	-0.400		
	I _{IL2}		<u>3/</u>	02, 09	-0.030	-0.400	
			<u>3/</u>	06	-0.075	-0.420	
	I _{IL3}		<u>3/</u>	07	-0.075	-0.420	
			<u>4/</u>	01, 08	-0.060	-0.720	
	I _{IL4}		<u>4/</u>	03, 04, 10	-0.060	-0.760	
			<u>5/</u>	01, 02, 03, 04, 05, 08, 09, 10	-0.060	-0.800	
	I _{IL5}		<u>6/</u>	02	-0.060	-1.20	
	I _{IL6}		<u>4/</u>	05	-0.12	-1.52	
	I _{IL7}		<u>6/</u>	05	-0.120	-1.60	
			<u>6/</u>	09	-0.060	-1.60	
High level input current	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	<u>7/</u>	All		20	μA
	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	<u>7/</u>	All		100	
	I _{IH3}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	<u>8/</u>	02, 09		40	
	I _{IH4}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	<u>8/</u>	02, 09		200	
	I _{IH5}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	<u>9/</u>	01, 02, 03, 04, 05, 08, 10		60	
	I _{IH6}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	<u>9/</u>	01, 02, 03, 04, 05, 08, 10		300	
	I _{IH7}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	<u>10/</u>	01, 03, 04, 08, 09, 10		80	
	I _{IH8}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	<u>10/</u>	01, 03, 04, 08, 09, 10		400	
	I _{IH9}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	<u>6/</u>	05		120	
	I _{IH10}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	<u>6/</u>	05		600	
	I _{IH11}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	<u>4/</u>	05		160	
	I _{IH12}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	<u>4/</u>	05		800	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Short circuit output current	I _{OS}	V _{CC} = 5.5 V <u>11/</u> V _{IN} = 0 V	01, 02, 03, 05, 06, 07, 08, 09 04, 10	-15 -15	-100 -130	mA
Supply current	I _{CC}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	01, 02, 03, 04, 05, 08 09, 10 06 07	 26 18	8	mA
Maximum clock frequency	f _{MAX}	V _{CC} = 5.0 V C _L = 50 pF ± 10% R _L = 2kΩ ± 5%	01, 03, 04 05, 06, 07 08, 10 02, 09	25 20		MHz
Propagation delay to high logic level (clear or preset to output)	t _{PLH1}		01, 03, 04, 05, 08, 10 02, 09 07	5 5 5	32 39 51	ns
Propagation delay to low logic level (clear or preset to output)	t _{PHL1}		01, 03, 04, 05, 08, 10 02, 09 06 07	5 5 5 5	40 59 52 55	ns
Propagation delay to high logic level (clock to output)	t _{PLH2}		01, 03, 04, 05, 08, 10 02, 09 06 07	5 5 5 5	32 39 47 46	ns
Propagation delay to low logic level (clock to output)	t _{PHL2}		01, 03, 04, 05, 08, 10 02, 09 06 07	5 5 5 5	42 59 52 55	ns

1/ See table III for complete terminal conditions.2/ Input condition - J or K (device types 01, 03, 04, 05, 08, and 10); and D (device types 06 and 07).3/ Input condition - D (device type 02); clock or clear (device types 06 and 07); and J or $\bar{K}$ (device type 09).4/ Input condition - Clock.5/ Input condition - Clear or preset (device types 03 and 10); clear (device types 01 and 08); preset or clock (device types 02 and 09); and preset (device types 04 and 05).6/ Input condition - Clear.7/ Input condition - J or K (device types 01, 03, 04, 05, 08, and 10); D (device type 02); J or $\bar{K}$ (device type 09); and D, clear, clock (device types 06 and 07).8/ Input condition - Preset or clock.9/ Input condition - Clear or preset (device types 03 and 10); clear (device types 01, 02, and 08); and preset (device types 04 and 05).10/ Input condition - Clock (device type 01, 03, 04, 08, and 10); and clear (device type 09).11/ Not more than one output should be shorted at a time.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 9, 10, 11	1, 2, 3
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

Pin number	Pin symbols device type 01		Pin symbols device type 02		Pin symbols device type 03		Pin symbols device type 04		Pin symbols device type 05	
	Cases 2, X	Cases A, B, C, and D	Cases 2, X	Cases A, B, C, and D	Cases 2, X	Cases E, F	Cases 2, X	Cases A, B, C, and D	Cases 2, X	Cases A, B, C, and D
1	NC	CLK1	NC	CLR1	NC	CLK1	NC	CLK1	NC	CLR1
2	CLK1	CLR1	CLR1	1D	CLK1	1K	CLK1	1K	CLR	1K
3	CLR1	1K	1D	CLK1	1K	1J	1K	1J	1K	1J
4	1K	V _{CC}	CLK1	PS1	1J	PS1	1J	PS1	1J	PS1
5	NC	CLK2	NC	1Q	PS1	1Q	NC	1Q	NC	1Q
6	V _{CC}	CLR2	PS1	1 $\bar{Q}$	NC	1 $\bar{Q}$	PS1	1 $\bar{Q}$	PS1	1 $\bar{Q}$
7	NC	2J	NC	GND	1Q	2 $\bar{Q}$	NC	GND	NC	GND
8	CLK2	2 $\bar{Q}$	1Q	2 $\bar{Q}$	1 $\bar{Q}$	GND	1Q	2 $\bar{Q}$	1Q	2 $\bar{Q}$
9	CLR2	2Q	1 $\bar{Q}$	2Q	2 $\bar{Q}$	2Q	1 $\bar{Q}$	2Q	1 $\bar{Q}$	2Q
10	2J	2K	GND	PS2	GND	PS2	GND	PS2	GND	PS2
11	NC	GND	NC	CLK2	NC	2J	NC	2J	NC	2J
12	2 $\bar{Q}$	1Q	2 $\bar{Q}$	2D	2Q	2K	2 $\bar{Q}$	2K	2 $\bar{Q}$	2K
13	2Q	1 $\bar{Q}$	2Q	CLR2	PS2	CLK2	2Q	CLK2	2Q	CLK
14	2K	1J	PS2	V _{CC}	2J	CLR2	PS2	V _{CC}	PS2	V _{CC}
15	NC		NC		2K	CLR1	NC		NC	
16	GND		CLK2		NC	V _{CC}	2J		2J	
17	NC		NC		CLK2		NC		NC	
18	1Q		2D		CLR2		2K		2K	
19	1 $\bar{Q}$		CLR2		CLR1		CLK2		CLK	
20	1J		V _{CC}		V _{CC}		V _{CC}		V _{CC}	

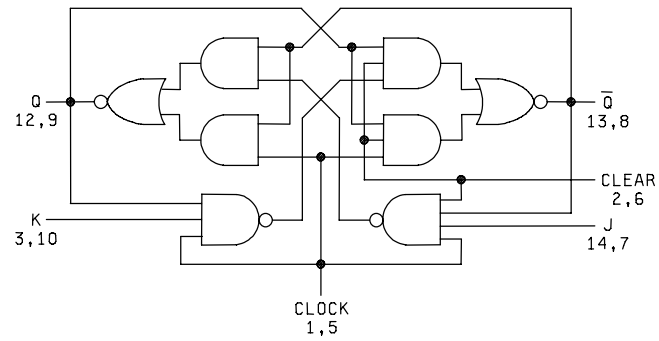
FIGURE 1. Terminal connections.

Pin number	Pin symbols device type 06		Pin symbols device type 07		Pin symbols device type 08		Pin symbols device type 09		Pin symbols device type 10	
	Cases 2, X	Cases E, F	Cases 2, X	Cases E, F	Cases 2, X	Cases A, B, C, and D	Cases 2, X	Cases E, F	Cases 2, X	Cases E, F
1	NC	CLR	NC	CLR	NC	1J	NC	1CLR	NC	1CLK
2	CLR	1Q	CLR	1Q	1J	1 $\bar{Q}$	1CLR	1J	1CLK	1PS
3	1Q	1D	1Q	1 $\bar{Q}$	1 $\bar{Q}$	1Q	1J	1 $\bar{K}$	1PS	1CLR
4	1D	2D	1 $\bar{Q}$	1D	1Q	1K	1 $\bar{K}$	1CLK	1CLR	1J
5	2D	2Q	1D	2D	NC	2Q	1CLK	1PS	1J	V _{CC}
6	NC	3D	NC	2 $\bar{Q}$	1K	2 $\bar{Q}$	NC	1Q	NC	2CLK
7	2Q	3Q	2D	2Q	NC	GND	1PS	1 $\bar{Q}$	V _{CC}	2PS
8	3D	GND	2 $\bar{Q}$	GND	2Q	2J	1Q	GND	2CLK	2CLR
9	3Q	CLK	2Q	CLK	2 $\bar{Q}$	2CLK	1 $\bar{Q}$	2 $\bar{Q}$	2PS	2J
10	GND	4Q	GND	3Q	GND	2CLR	GND	2Q	2CLR	2 $\bar{Q}$
11	NC	4D	NC	3 $\bar{Q}$	NC	2K	NC	2PS	NC	2Q
12	CLK	5Q	CLK	3D	2J	1CLK	2 $\bar{Q}$	2CLK	2J	2K
13	4Q	5D	3Q	4D	2CLK	1CLR	2Q	2 $\bar{K}$	2 $\bar{Q}$	GND
14	4D	6D	3 $\bar{Q}$	4 $\bar{Q}$	2CLR	V _{CC}	2PS	2J	2Q	1 $\bar{Q}$
15	5Q	6Q	3D	4Q	NC		2CLK	2CLR	2K	1Q
16	NC	V _{CC}	NC	V _{CC}	2K		NC	V _{CC}	NC	1K
17	5D		4D		NC		2 $\bar{K}$		GND	
18	6D		4 $\bar{Q}$		1CLK		2J		1 $\bar{Q}$	
19	6Q		4Q		1CLR		2CLR		1Q	
20	V _{CC}		V _{CC}		V _{CC}		V _{CC}		1K	

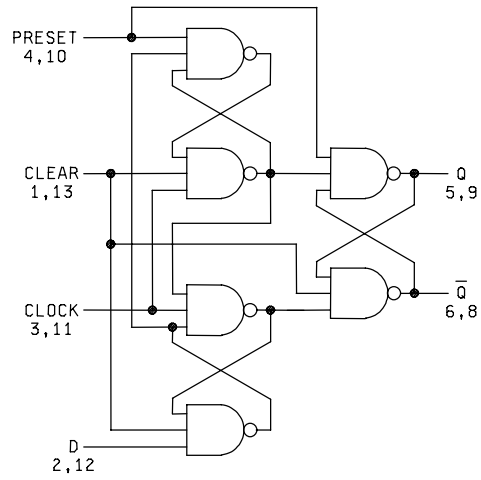
FIGURE 1. Terminal connections - Continued.

(Pin numbers shown apply to the DIP and flat packs only)

DEVICE TYPE 01



DEVICE TYPE 02



DEVICE TYPE 03

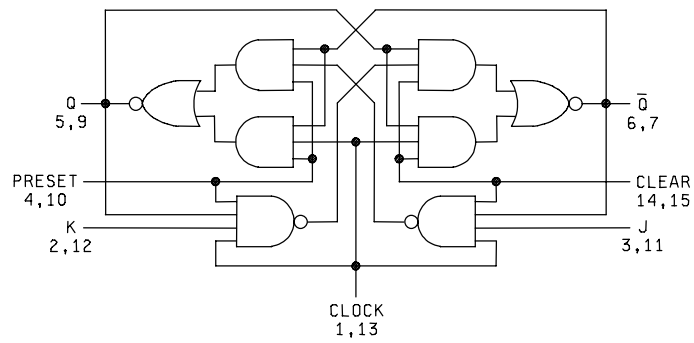
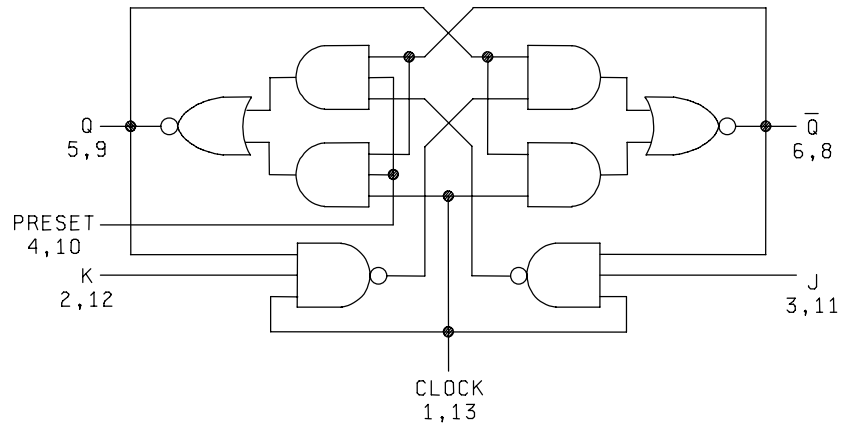


FIGURE 2. Logic Diagrams.

(Pin numbers shown apply to the DIP and flat packs only)

DEVICE TYPE 04



DEVICE TYPE 05

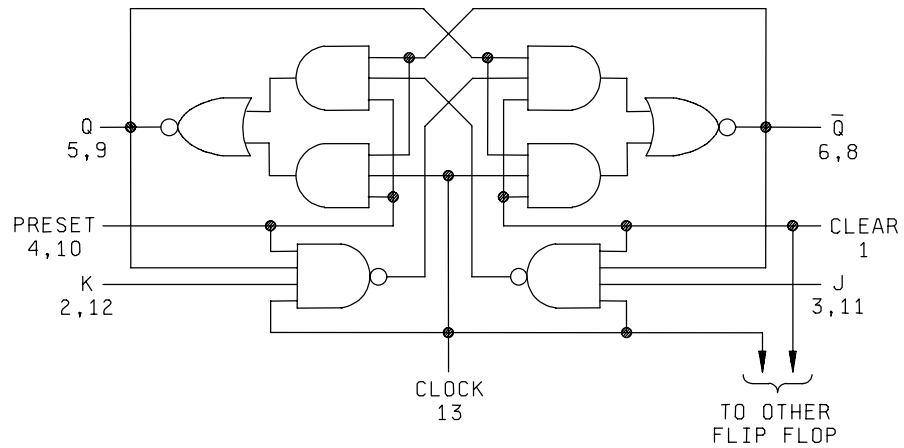


FIGURE 2. Logic Diagrams - Continued.

MIL-M-38510/301F

(Pin numbers shown apply to the DIP and flat packs only)

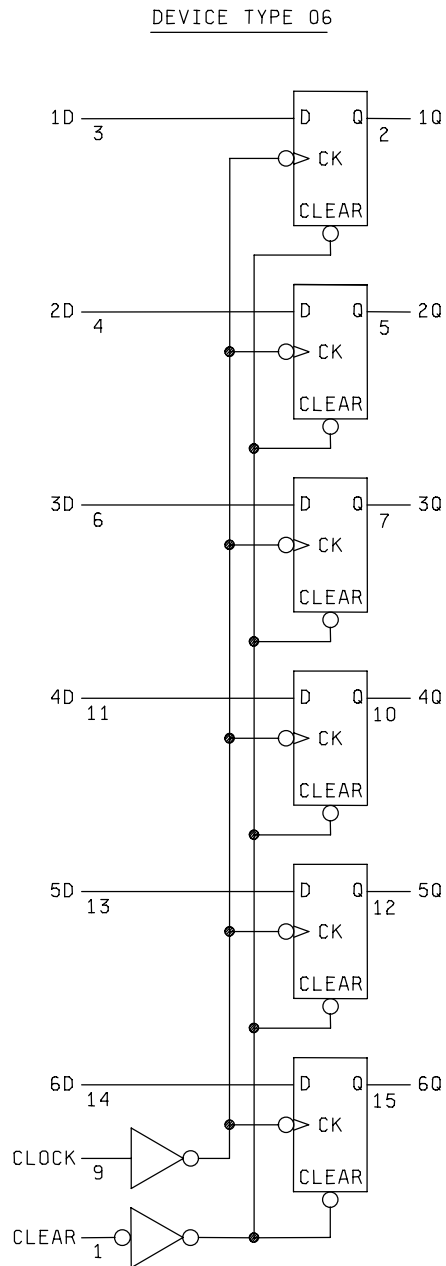
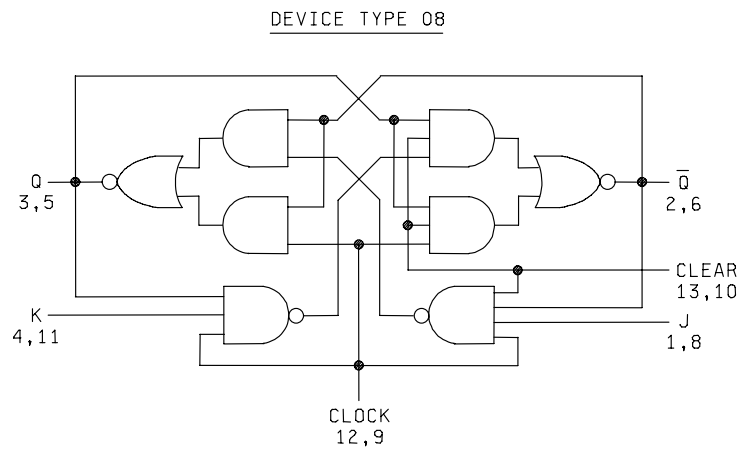
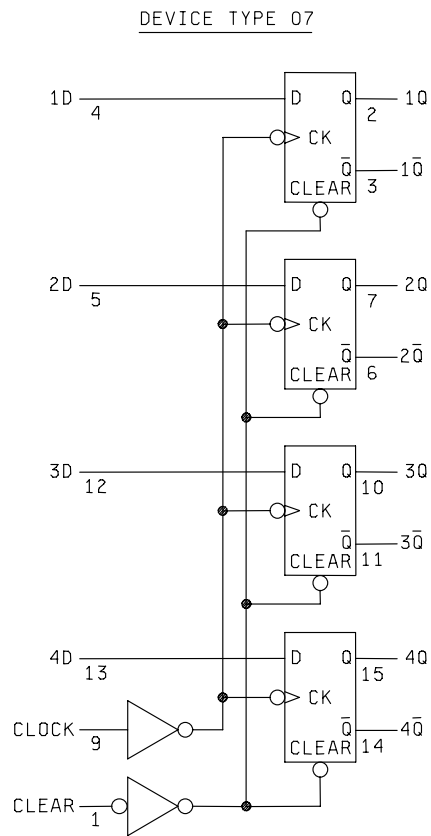


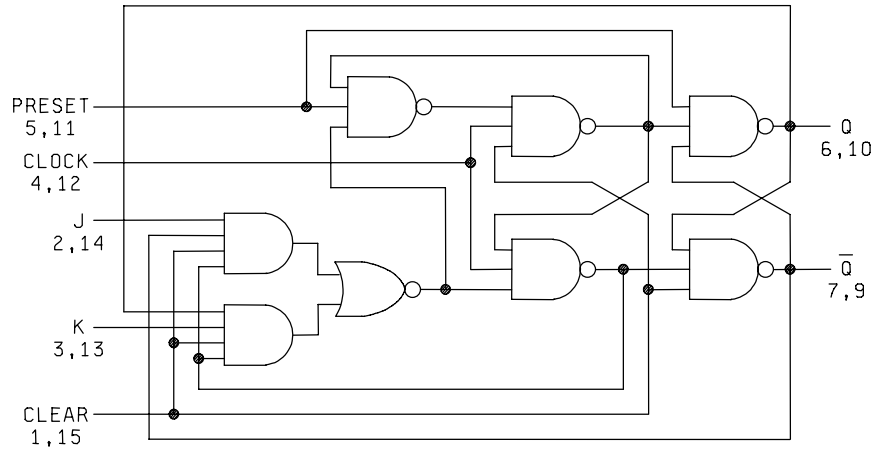
FIGURE 2. Logic Diagrams - Continued.

(Pin numbers shown apply to the DIP and flat packs only)

FIGURE 2. Logic Diagrams - Continued.

(Pin numbers shown apply to the DIP and flat packs only)

DEVICE TYPE 09



DEVICE TYPE 10

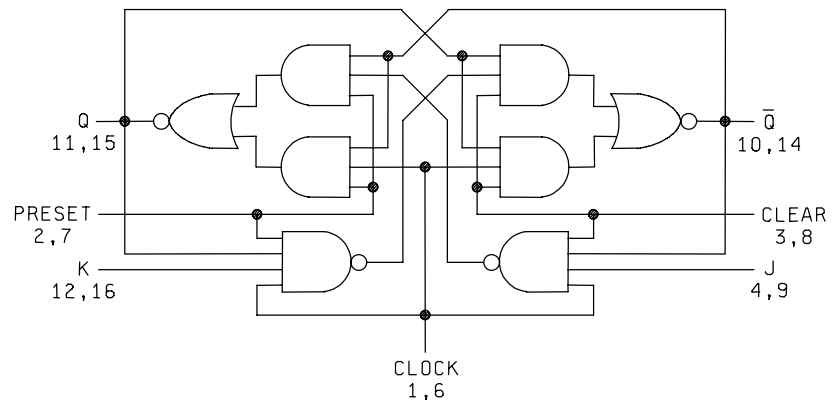


FIGURE 2. Logic Diagrams - Continued.

DEVICE TYPE 01

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↓ = transition from high to low level

Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

DEVICE TYPE 02

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↑ = transition from low to high level

Q_0 = the level of Q before the indicated steady state input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FIGURE 3. Truth tables.

DEVICE TYPES 03 AND 10

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	$\overline{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↓ = transition from high to low level

Q₀ = the level of Q before the indicated steady state input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

DEVICE TYPE 04

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	H	L
H	↓	L	L	Q ₀	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q ₀	$\overline{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↓ = transition from high to low level

Q₀ = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

FIGURE 3. Truth tables - Continued.

DEVICE TYPES 05

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	$\overline{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↓ = transition from high to low level

Q₀ = the level of Q before the indicated steady state input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

DEVICE TYPE 06

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↑ = transition from low to high level

Q₀ = the level of Q before the indicated steady state input conditions were established.

FIGURE 3. Truth tables - Continued.

DEVICE TYPE 07

INPUTS			OUTPUT	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	L
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

 $\uparrow$ = transition from low to high level Q_0 = the level of Q before the indicated steady state input conditions were established.

DEVICE TYPE 08

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	$\uparrow$	L	L	Q_0	$\overline{Q}_0$
H	$\uparrow$	H	L	H	L
H	$\uparrow$	L	H	L	H
H	$\uparrow$	H	H	TOGGLE	

H = high level (steady state)

L = low level (steady state)

X = irrelevant

 $\uparrow$ = transition from low to high level Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each clock transition.

FIGURE 3. Truth tables - Continued.

DEVICE TYPE 09

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	$\bar{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

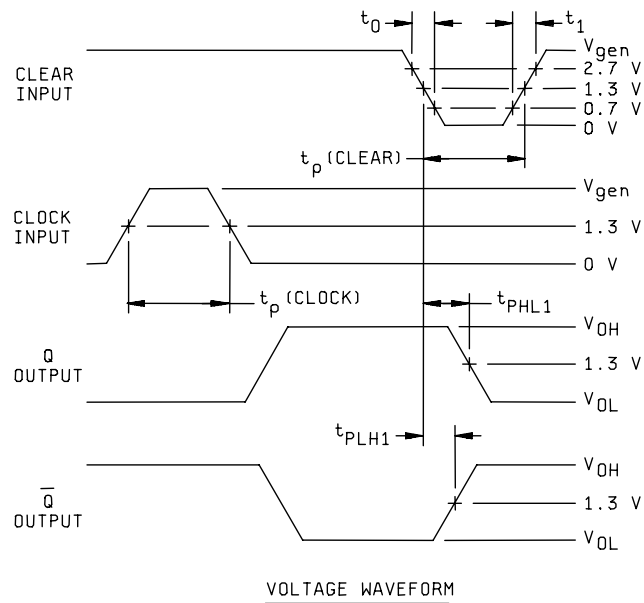
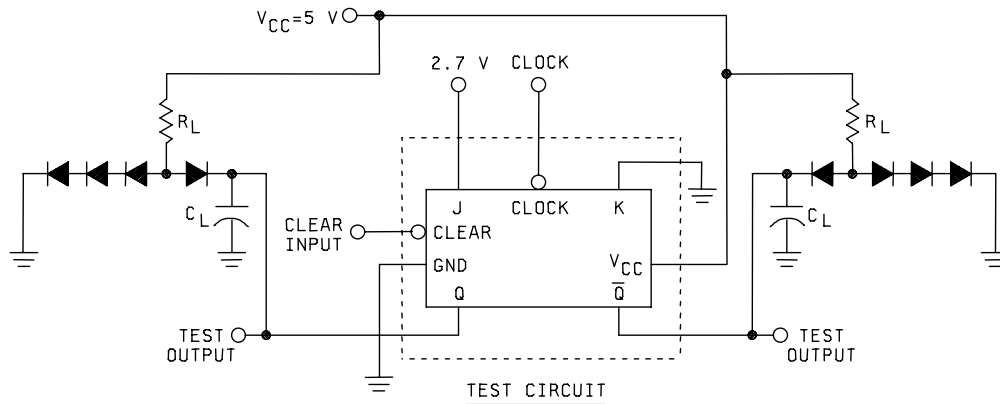
↑ = transition from low to high level

Q₀ = the level of Q before the indicated steady state input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↑ clock transition.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

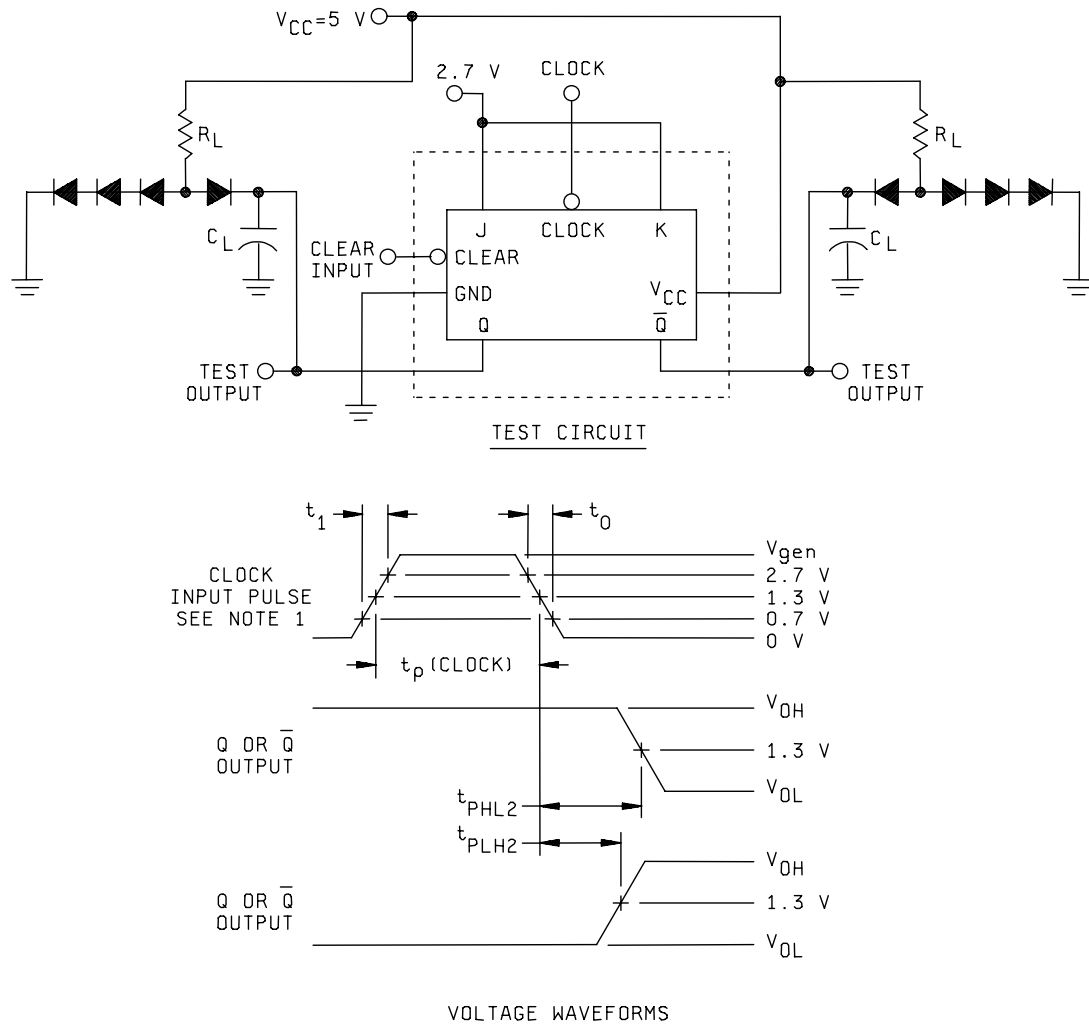
FIGURE 3. Truth tables - Continued.



NOTES:

1. Clear inputs dominate regardless of the state of clock or J-K inputs.
2. Clear input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_1 \leq 15 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $t_p(\text{clear}) = 30 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2 \text{ k}\Omega \pm 5\%$.
6. Clock input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_p(\text{clock}) = 25 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$.

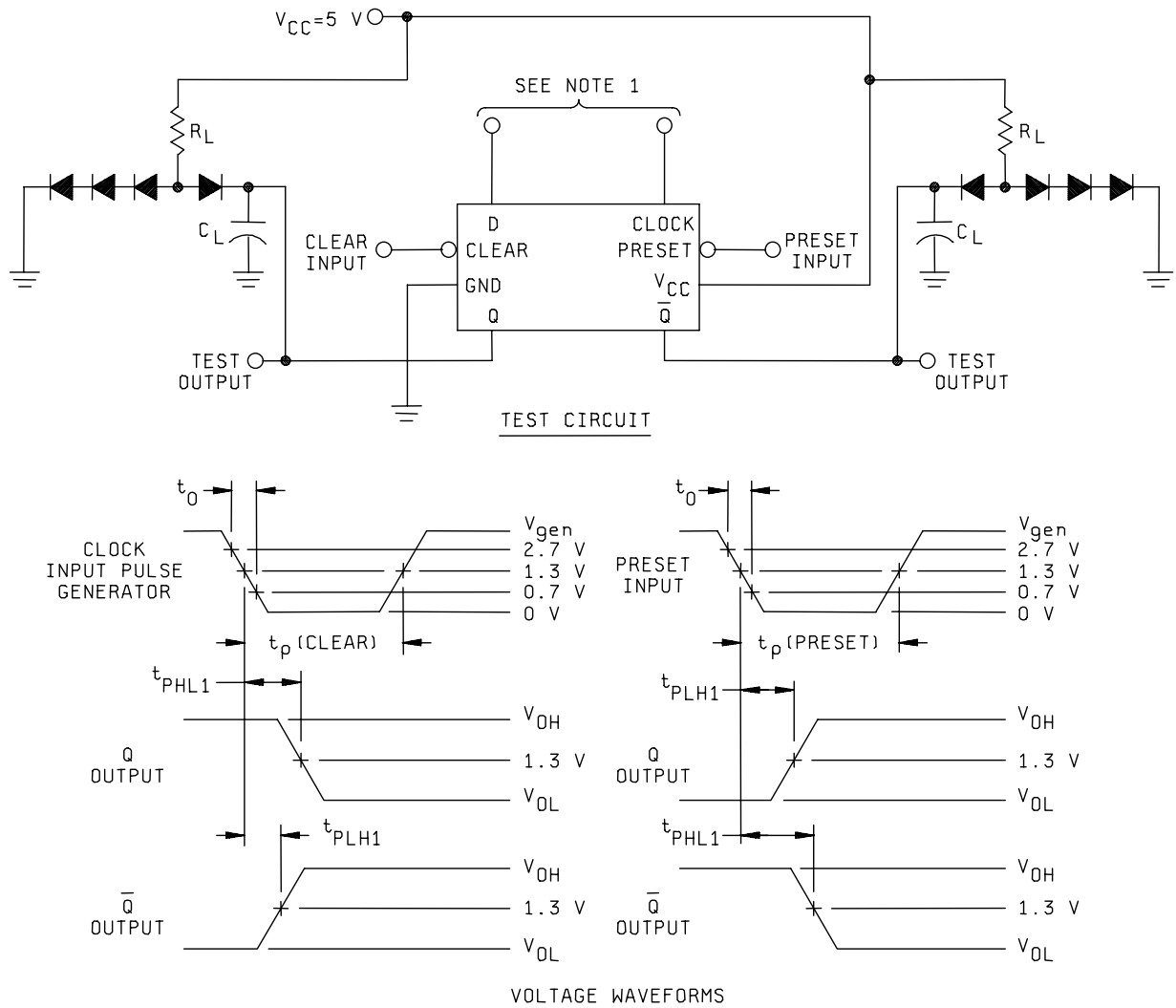
FIGURE 4. Clear switching time test circuit and waveforms for device types 01 and 08.



NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen} = 3$ V, $t_1 \leq 15$ ns, $t_0 \leq 6$ ns, t_p (clock) = 25 ns, $PRR \leq 1$ MHz. When testing f_{MAX} the clock input characteristics are $V_{gen} = 3$ V, $t_1 = t_0 \leq 6$ ns, t_p (clock) ≤ 25 ns, and $PRR =$ see table III.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50$ pF $\pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2$ k Ω $\pm 5\%$.

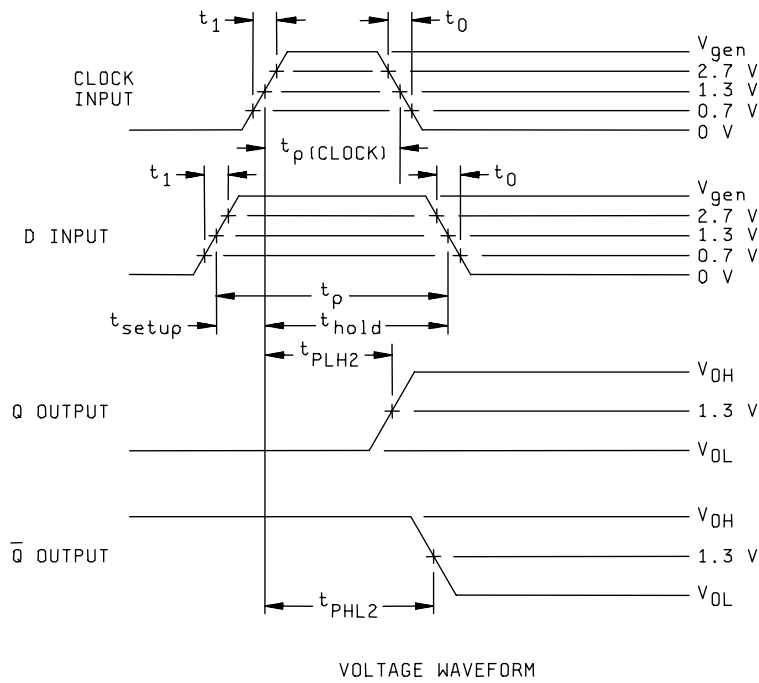
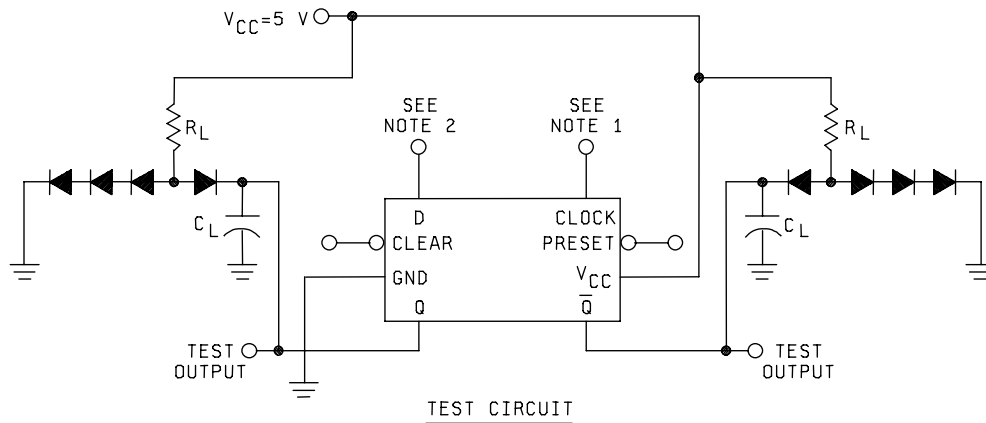
FIGURE 5. Synchronous switching test circuit for device types 01 and 08.



NOTES:

1. Clear and preset inputs dominate regardless of the state of clock or D inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear or preset input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_0 \leq 6\text{ ns}$, $t_p(\text{clear}) = t_p(\text{preset}) = 35\text{ ns}$, $\text{PRR} \leq 1\text{ MHz}$.
4. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2\text{ k}\Omega \pm 5\%$.
6. When testing clear to output switching, preset input shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table III).

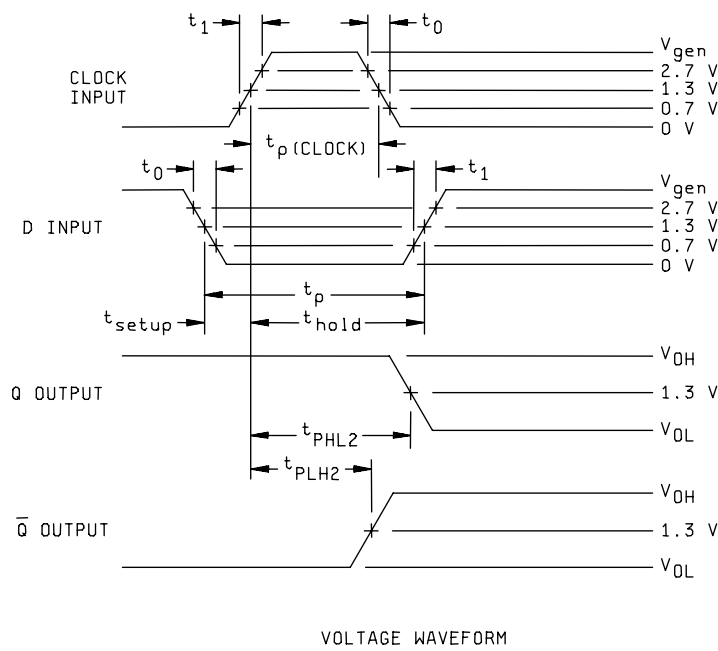
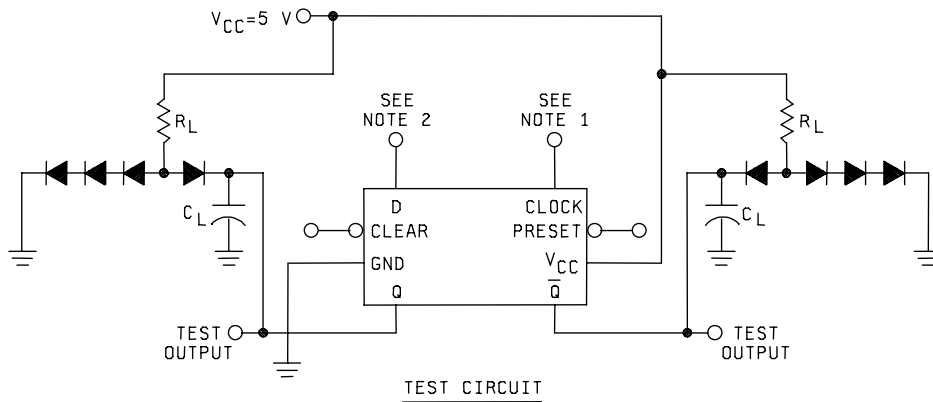
FIGURE 6. Clear and preset switching test circuit and waveforms for device type 02.



NOTES:

1. Clock input pulse has the following characteristics: $V_{\text{gen}} = 3 \text{ V}$, $t_1 \leq 15 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $t_p(\text{clock}) = 30 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$. When testing f_{MAX} , $\text{PRR} = \text{see table III}$, $t_p(\text{clock}) \leq 30 \text{ ns}$, and $t_0 = t_1 \leq 6 \text{ ns}$.
2. D input has the following characteristics: $V_{\text{gen}} = 3 \text{ V}$, $t_1 \leq 15 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $t_{\text{setup}} = 20 \text{ ns}$, $t_{\text{hold}} = 5 \text{ ns}$, $t_p = 25 \text{ ns}$, and PRR is 50% of the clock PRR . For f_{MAX} , $t_0 = t_1 \leq 6 \text{ ns}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2 \text{ k}\Omega \pm 5\%$.

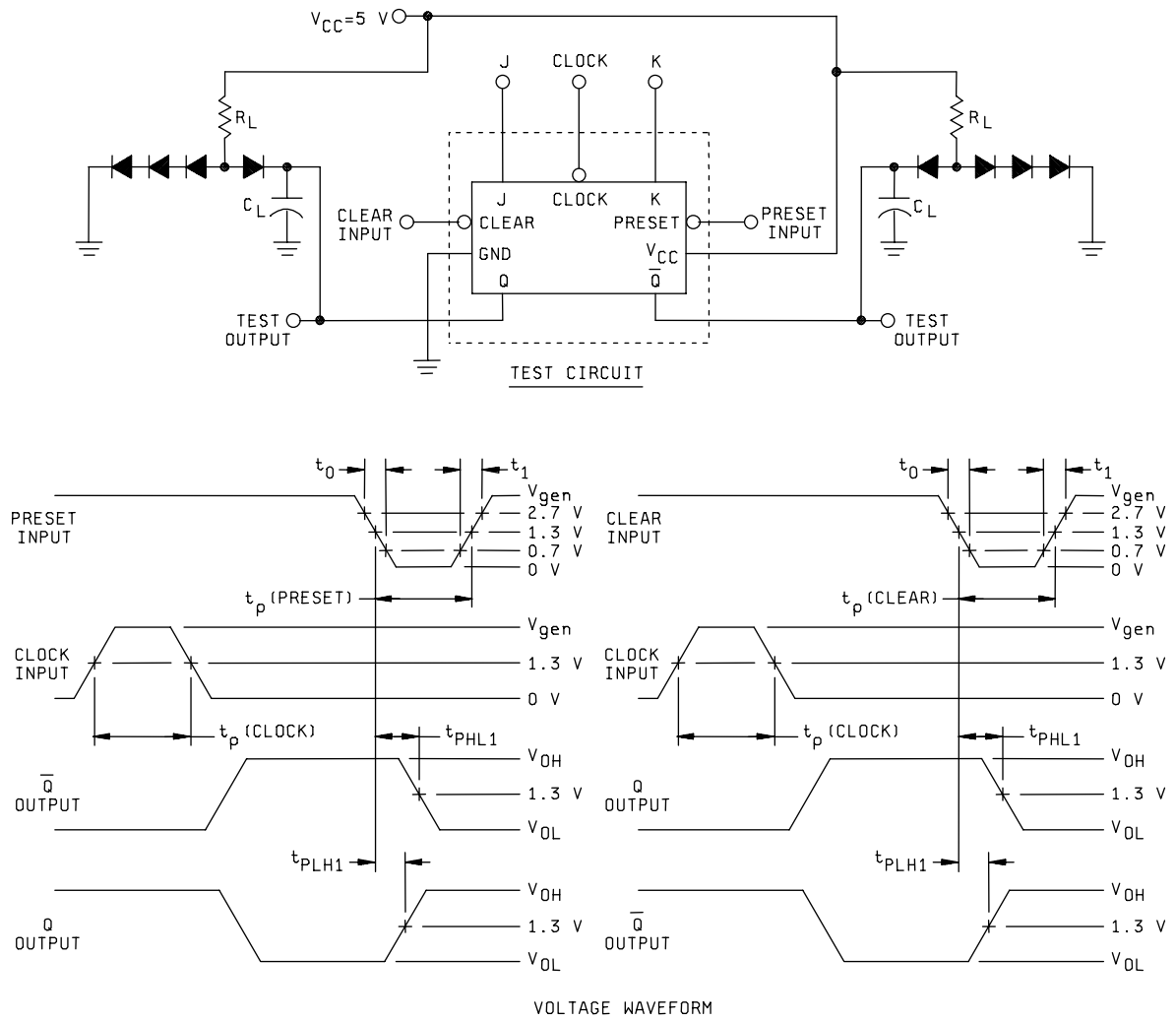
FIGURE 7. Synchronous switching test circuit (high-level data) for device type 02.



NOTES:

1. Clock input pulse has the following characteristics: $V_{gen} = 3\text{ V}$, $t_1 \leq 15\text{ ns}$, $t_0 \leq 6\text{ ns}$, $t_p(\text{clock}) = 30\text{ ns}$, $\text{PRR} \leq 1\text{ MHz}$.
2. D input has the following characteristics: $V_{gen} = 3\text{ V}$, $t_1 \leq 15\text{ ns}$, $t_0 \leq 6\text{ ns}$, $t_{setup} = 20\text{ ns}$, $t_{hold} = 5\text{ ns}$, $t_p = 25\text{ ns}$, and PRR is 50% of the clock PRR .
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2\text{ k}\Omega \pm 5\%$.

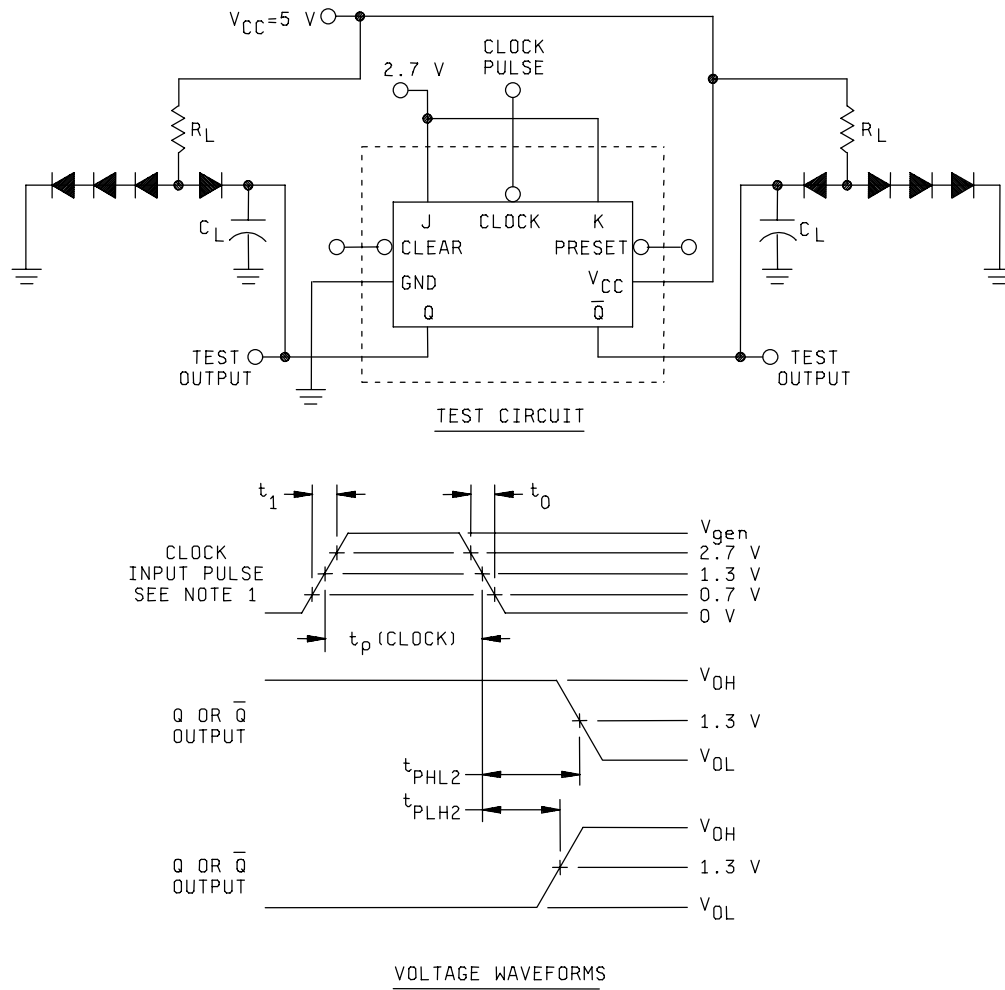
FIGURE 8. Synchronous switching test circuit (low-level data) for device type 02.



NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input has the following characteristics: $V_{gen} = 3\text{ V}$, $t_1 \leq 15\text{ ns}$, $t_0 \leq 6\text{ ns}$, $t_p(\text{clear}) = t_p(\text{preset}) = 30\text{ ns}$, $\text{PRR} \leq 1\text{ MHz}$, and $Z_{out} \approx 50\Omega$.
3. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2\text{ k}\Omega \pm 5\%$.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset input shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied. (see table III).
7. Clock input pulse characteristics: $t_p(\text{clock}) \geq 25\text{ ns}$, $V_{gen} = 3\text{ V}$, $\text{PRR} \leq 1\text{ MHz}$.

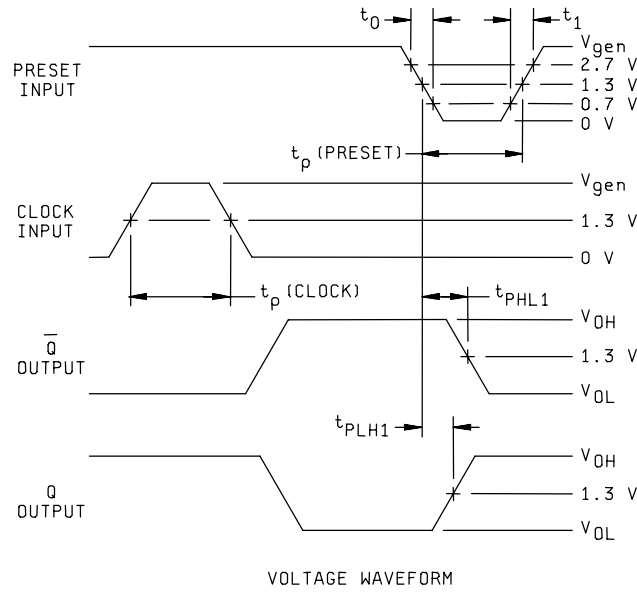
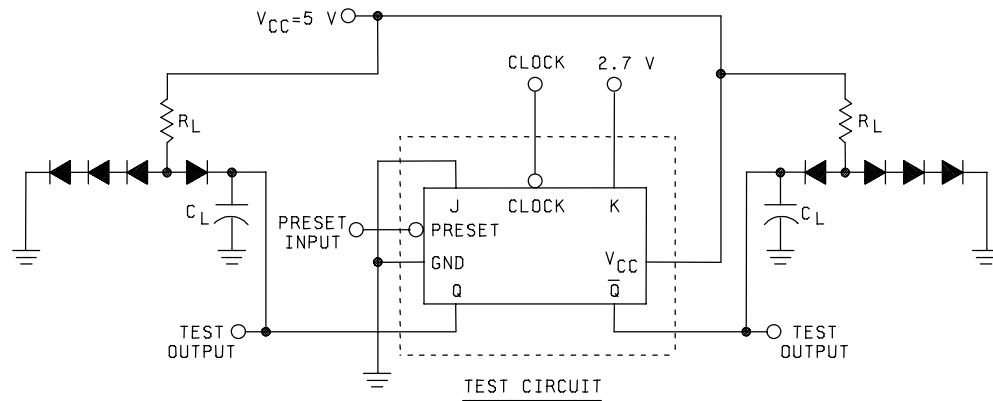
FIGURE 9. Clear and preset switching test circuit and waveforms for device types 03, 05, and 10.



NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen} = 3\text{ V}$, $t_0 \leq 6\text{ ns}$, $t_1 \leq 15\text{ ns}$, $t_p(\text{clock}) = 25\text{ ns}$, $\text{PRR} \leq 1\text{ MHz}$. When testing f_{MAX} the clock input characteristics are $V_{gen} = 3\text{ V}$, $t_1 = t_0 \leq 6\text{ ns}$, $t_p(\text{clock}) \leq 25\text{ ns}$, and $\text{PRR} = \text{see table III}$.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2\text{ k}\Omega \pm 5\%$.

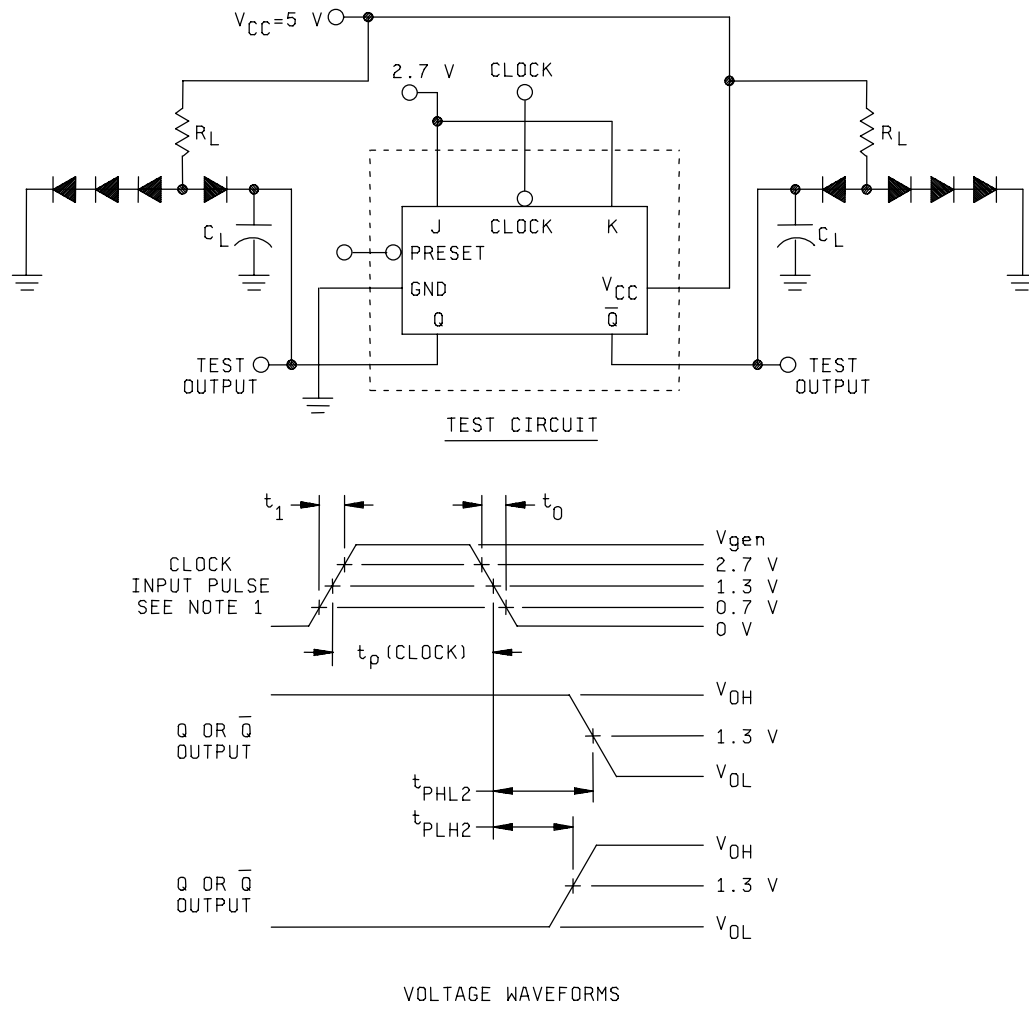
FIGURE 10. Synchronous switching test circuit for device types 03, 05, and 10.



NOTES:

1. Preset inputs dominate regardless of the state of clock or J-K inputs.
2. Preset input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_0 \leq 15\text{ ns}$, $t_1 \leq 6\text{ ns}$, $t_p(\text{preset}) = 30\text{ ns}$, $\text{PRR} \leq 1\text{ MHz}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2\text{ k}\Omega \pm 5\%$.
6. Clock input pulse characteristics: $V_{gen} = 3\text{ V}$, $t_p(\text{clock}) \geq 25\text{ ns}$, $\text{PRR} \leq 1\text{ MHz}$.

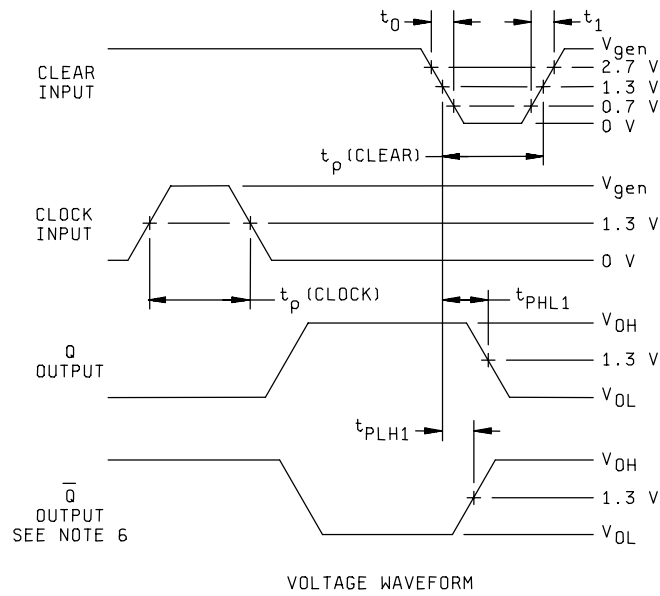
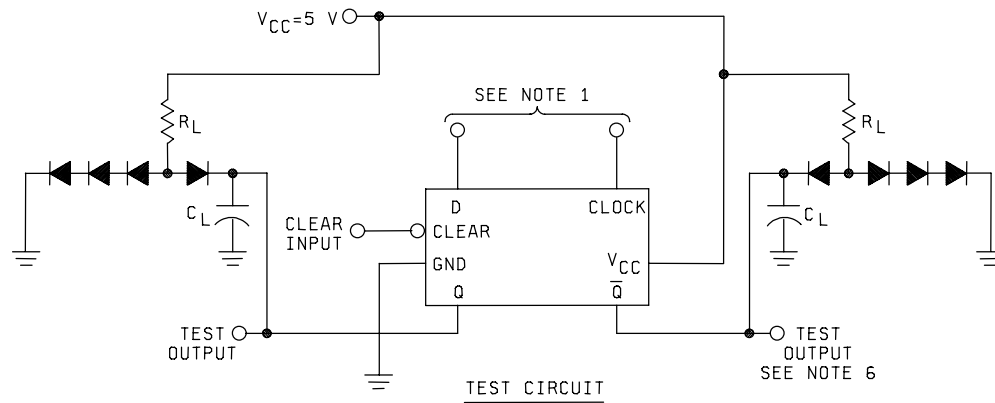
FIGURE 11. Preset switching test circuit and waveforms for device type 04.



NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen} = 3$ V, $t_0 \leq 6$ ns, $t_1 \leq 15$ ns, $t_p(\text{clock}) = 25$ ns, $PRR \leq 1$ MHz. When testing f_{MAX} the clock input characteristics are $V_{gen} = 3$ V, $t_1 = t_0 \leq 6$ ns, $t_p(\text{clock}) \leq 25$ ns, and $PRR =$ see table III.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50$ pF $\pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2$ k Ω $\pm 5\%$.

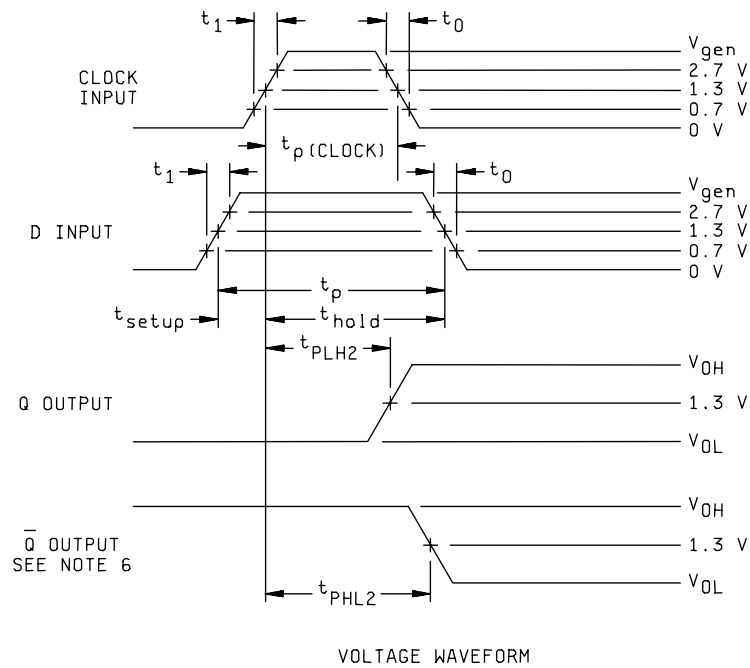
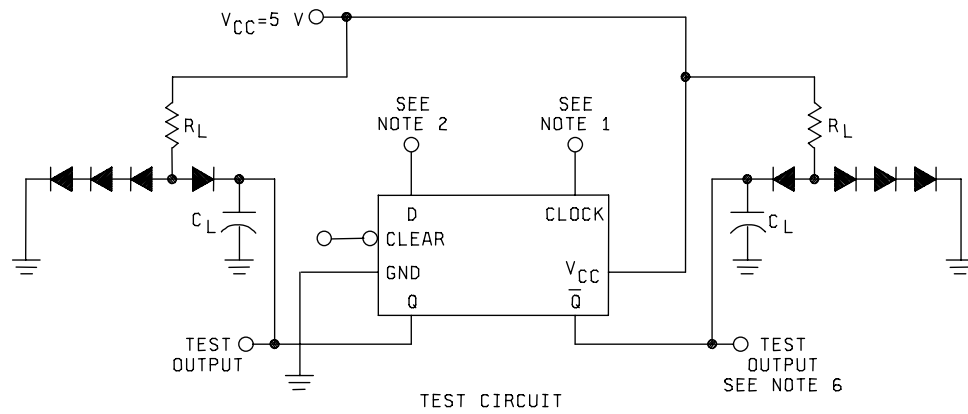
FIGURE 12. Synchronous switching test circuit for device type 04.



NOTES:

1. Clear input dominates regardless of the state of clock or D inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 \leq 6 \text{ ns}$, $t_1 \leq 15 \text{ ns}$, $t_p(\text{clear}) = 35 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2 \text{ k}\Omega \pm 5\%$.
6. $\bar{Q}$ output applies to device type 07 only.
7. Clock input pulse characteristics: $t_p(\text{clock}) \geq 25 \text{ ns}$, $V_{gen} = 3 \text{ V}$, $\text{PRR} \leq 1 \text{ MHz}$.

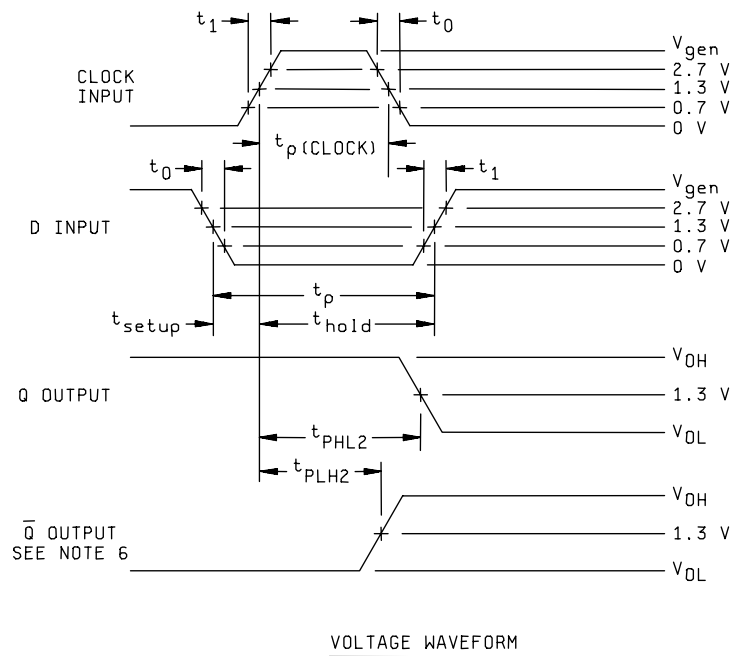
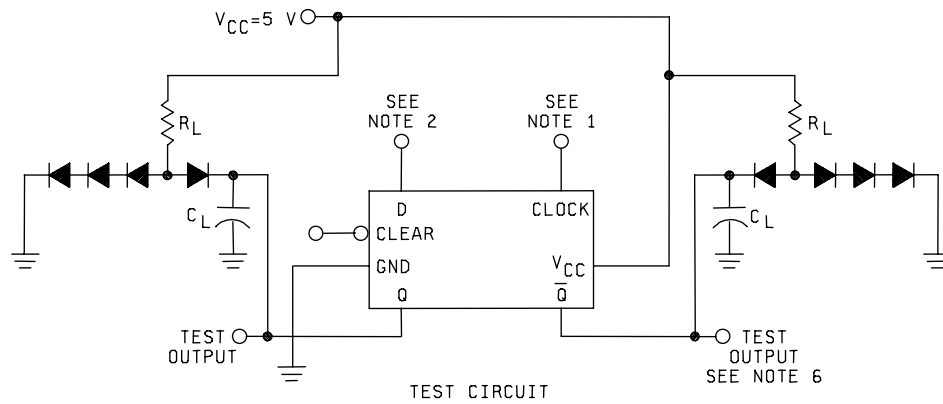
FIGURE 13. Asynchronous switching test circuit for device types 06 and 07.



NOTES:

1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_1 \leq 15 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $t_p(\text{clock}) = 30 \text{ ns}$, and $\text{PRR} \leq 1 \text{ MHz}$. When testing f_{MAX} , $\text{PRR} = \text{see table III}$, $t_p(\text{clock}) \leq 30 \text{ ns}$, and $t_0 = t_1 \leq 6 \text{ ns}$.
2. D input has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_1 \leq 15 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $t_{setup} = 20 \text{ ns}$, $t_{hold} = 5 \text{ ns}$, $t_p = 25 \text{ ns}$, and PRR is 50% of the clock PRR . For f_{MAX} , $t_0 = t_1 \leq 6 \text{ ns}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2 \text{ k}\Omega \pm 5\%$.
6. $\bar{Q}$ output applies to device type 07 only.

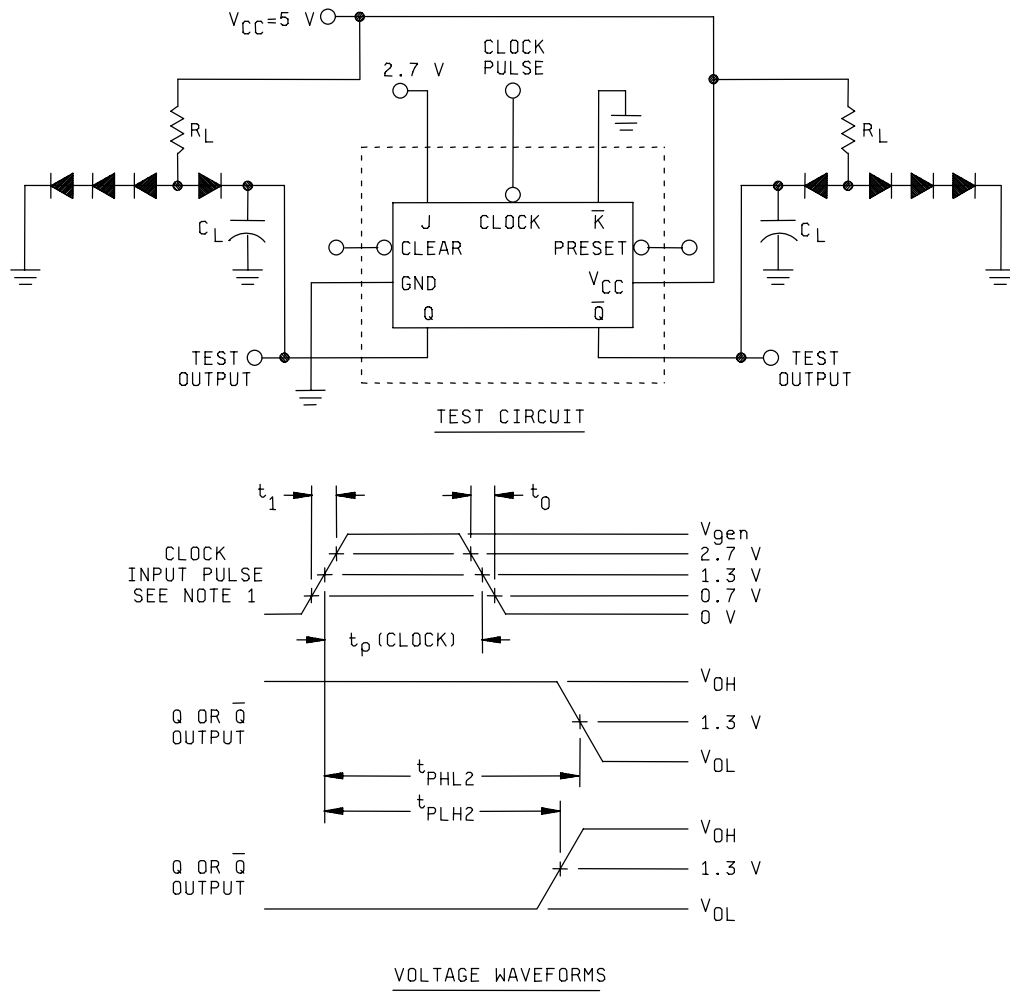
FIGURE 14. Synchronous switching test circuit (high-level data) for device types 06 and 07.



NOTES:

1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_1 \leq 15 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $t_p(\text{clock}) = 30 \text{ ns}$, and $\text{PRR} \leq 1 \text{ MHz}$.
2. D input has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_1 \leq 15 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $t_{setup} = 20 \text{ ns}$, $t_{hold} = 5 \text{ ns}$, $t_p = 25 \text{ ns}$, and PRR is 50% of the clock PRR .
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2 \text{ k}\Omega \pm 5\%$.
6. $\bar{Q}$ output applies to device type 07 only.

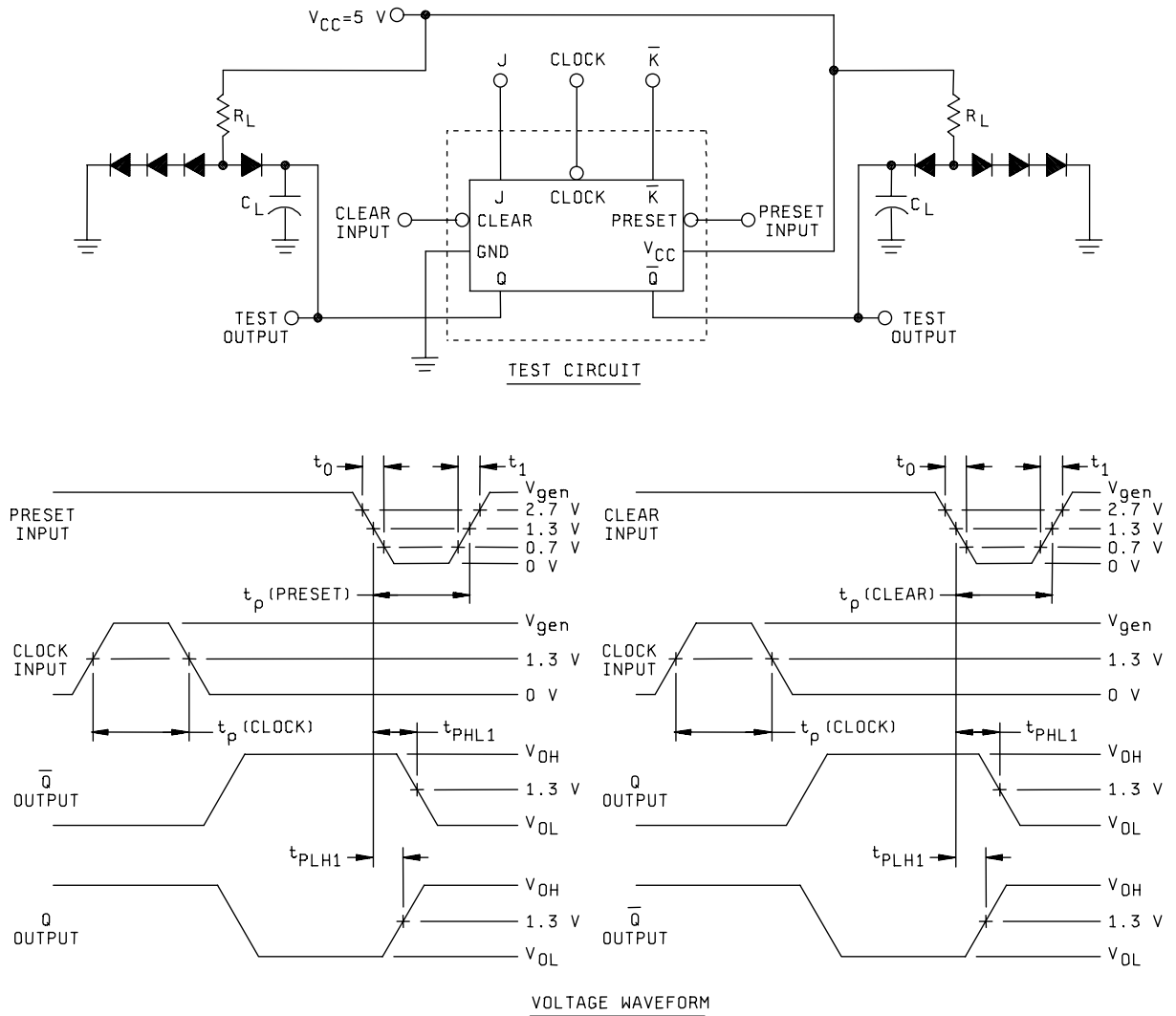
FIGURE 15. Synchronous switching test circuit (low-level data) for device types 06 and 07.



NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen} = 3$ V, $t_0 \leq 6$ ns, $t_1 \leq 15$ ns, t_p (clock) = 25 ns, and PRR ≤ 1 MHz. When testing f_{MAX} , the clock input characteristics are $V_{gen} = 3$ V, $t_0 = t_1 \leq 6$ ns, t_p (clock) ≤ 25 ns, and PRR = see table III.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50$ pF $\pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2$ k Ω $\pm 5\%$.

FIGURE 16. Synchronous switching test circuit for device type 09.



NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input has the following characteristics: $V_{gen} = 3\text{ V}$, $t_1 \leq 15\text{ ns}$, $t_0 \leq 6\text{ ns}$, $t_p(\text{clear}) = t_p(\text{preset}) = 30\text{ ns}$, $PRR \leq 1\text{ MHz}$, and $Z_{out} \approx 50\Omega$.
3. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2\text{ k}\Omega \pm 5\%$.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset input shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied. (see table III).
7. Clock input pulse characteristics: $t_p(\text{clock}) \geq 25\text{ ns}$, $V_{gen} = 3\text{ V}$, $PRR \leq 1\text{ MHz}$.

FIGURE 17, Clear and preset switching test circuit and waveforms for device type 09.

TABLE III. Group A inspection for device type 01 and 08.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X	Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).																Measured terminal	Limits		Unit
				* 2	3	4	6	8	9	10	12	13	14	16	18	19	20	Min	Max				
1	V_{OH}	3006	1	20 V	0.7 V	2.0 V	4.5 V												$\bar{Q}1$	2.5		V	
		"	2	$\underline{2/}$	2.0 V	2.0 V	"											$\bar{Q}1$	"		"		
		"	3	$\underline{2/}$	2.0 V	0.7 V	"											$\bar{Q}1$	"		"		
		"	4				"	2.0 V	0.7 V	2.0 V	-4 mA		2.0 V					$\bar{Q}2$	"		"		
		"	5				"	"	2.0 V	0.7 V	-4 mA		2.0 V					$\bar{Q}2$	"		"		
		"	6				"	"	"	2.0 V	-4 mA	-4 mA	0.7 V					$\bar{Q}2$	"		"		
		3007	7				"	"	"	2.0 V	4 mA		0.7 V					$\bar{Q}2$	0.4		"		
		"	8				"	"	"	0.7 V		4 mA	2.0 V					$\bar{Q}2$	"		"		
		"	9				"	2.0 V	0.7 V	2.0 V		4 mA	2.0 V					$\bar{Q}2$	"		"		
		"	10	2.0 V	0.7 V	2.0 V	"								4 mA		2.0 V	$\bar{Q}1$	"		"		
		"	11	$\underline{2/}$	2.0 V	2.0 V	"									4 mA	0.7 V	$\bar{Q}1$	"		"		
V	OL	"	12	$\underline{2/}$	2.0 V	0.7 V	"										4 mA	2.0 V	$\bar{Q}1$	"		"	
			13	-18 mA			"											CLK1	-1.5		"		
			14			-18 mA		"										CLR1	"		"		
			15				"	-18 mA										K1	"		"		
			16				"											CLK2	"		"		
			17				"											CLR2	"		"		
			18				"			-18 mA								J2	"		"		
			19				"							-18 mA				K2	"		"		
			20				"											J1	"		"		
		3009	21	$\underline{3/}$	4.5 V	0.4 V	5.5 V											-18 mA	K1	$\underline{4/}$	4/	mA	
		I	IL1	"	22	4.5 V	$\underline{3/}$	4.5 V	"											J1	"		"
"	23						"	4.5 V	$\underline{3/}$	0.4 V			4.5 V					J2	"		"		
"	24						"	"	$\underline{3/}$	4.5 V	4.5 V			0.4 V				K2	"		"		
"	25			0.4 V	$\underline{3/}$	4.5 V	"											4.5 V	CLK1	"		"	
"	26						"	0.4 V	$\underline{3/}$	4.5 V			4.5 V					CLK2	"		"		
"	27			4.5 V	0.4 V	4.5 V	"											4.5 V	CLR1	"		"	
"	28						"	4.5 V	0.4 V	4.5 V			4.5 V					CLR2	"		"		
3010	29			GND	GND	2.7 V	"											4.5 V	K1		20	μ A	
"	30			GND	GND	4.5 V	"											2.7 V	J1	"		"	
"	31						"	GND	GND	2.7 V			4.5 V						J2	"		"	
I	IH2			"	32				"	GND	GND	4.5 V			2.7 V					K2	"		"
		"	33				"	GND	GND	5.5 V			5.5 V					J2	"		"	"	
		"	34				"	GND	GND	5.5 V			4.5 V					K2	"	100	"	"	
		"	35	GND	GND	5.5 V	"											4.5 V	K1	"		"	
		"	36	GND	GND	4.5 V	"											5.5 V	J1	"		"	
		"	37	GND	2.7 V	4.5 V	"											GND	CLR1		60	"	
		"	38				"	GND	2.7 V	GND				4.5 V					CLR2		60	"	
		"	39				"	GND	5.5 V	GND				4.5 V					CLR2		300	"	
		"	40	GND	5.5 V	4.5 V	"											GND	CLR1		300	"	

See footnotes at end of device types 01 and 08.

Subgroup	Symbol	MIL-STD-883 method	Cases $\frac{I}{T}$	* 2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits		Unit						
				** 18	19	6	20	13	14	12	9	8	16	10	4	3	2		Min	Max							
				A,B,C,D	Case	2	3	4	5	6	7	8	9	10	11	12	13					14					
1 $T_C = 25^\circ\text{C}$			Test no.	CLK1	CLR1	K1	V _{CC}	CLK2	CLR2	J2	$\bar{Q}2$	Q2	K2	GND	Q1	$\bar{Q}1$	J1										
				41	2.7 V	GND	GND	5.5 V															CLK1	80	μA		
				42				"	2.7 V	GND	GND				GND	"							CLK2	80	"		
				43				"	5.5 V	GND	GND				GND	"							CLK2	400	"		
				44	5.5 V	GND	GND	"	"	"	"	"	"	"	"	"	"				"		GND	400	"		
				45	GND	GND	4.5 V	"	"	"	"	"	"	"	"	"	"				"	GND	GND	$\bar{Q}1$	-15	-100 mA	
				46	$\frac{2}{I}$	4.5 V	GND	"	"	"	"	"	"	"	"	"	"				"	2.25 V	GND	4.5 V	$\frac{5}{I}$	5/-100	"
				47				"	"	"	"	GND	GND	GND	GND		4.5 V				"			$\bar{Q}2$	-15	"	
				48				"	"	"	"	2/I	4.5 V	4.5 V	GND	2.25 V	GND				"			Q2	$\frac{5}{I}$	5/-100	"
				49	GND	GND	GND	"	"	"	"	GND	GND	4.5 V	GND	2.25 V	GND				"			V _{CC}	8.0	"	
	CC	3005	2/I	5.5 V	GND	"	"	2/I	5.5 V	5.5 V				GND	"			GND	5.5 V	8.0	"						
	CC	3005												GND	"			V _{CC}	5.5 V	8.0	"						

2	Same tests, terminal conditions and limits as for subgroup 1, except T _C = +125° C, and V _{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T _C = -55° C, and V _{IC} tests are omitted.																				
7 6/, 7/	Truth table tests	3014																		See g/	
51		B	A	B	B	B	4.5 V	B	B	B	H	H	L	B	GND	L	H	A	All outputs		
52		B	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
53		B	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
54		B	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
55		A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
56		B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
57		B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	H	L	"		"
58		A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B		"
59		B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	L	H	"		"
60		"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
61		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
62		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
63		"	"	"	"	"	"	"	"	"	"	"	"	L	"	"	"	"	"		"
64		"	"	"	"	"	"	"	"	"	"	"	"	H	"	"	"	"	"		"
65		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
66		"	"	"	"	"	"	"	"	"	"	"	"	L	"	"	"	"	"		"
67		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
68		"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
69		A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"
70	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
71	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A	"		
72 9/	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
73	B	"	"	"	"	"	"	"	"	"	"	"	L	"	"	H	L	"	"		
74	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B	"		
75	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
76	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
77	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A	"		
78 9/	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
79	B	"	"	"	"	"	"	"	"	"	"	"	H	"	"	L	H	"	"		
8 6/, 7/	Repeat subgroup 7 at T _C = +125° C and T _C = -55° C.																				

See footnotes at end of device types 01 and 08.

Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

111	Same tests, terminal conditions, and limits as for subgroup 10, except $T_c = -55^\circ\text{C}$
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** Terminal numbers for device type 08.

21



— 2.5 V minimum/5.5 V maximum



TABLE III. Group A inspection for device type 01 and 08 – Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

4/ I_{IL} limits in mA are as follows:

I_{IL1}	Min/Max limits for CKT				
	A	B	C	D	E
	-.075/- .250	-.03/- .30	-.11/- .25	-.12/- .36	-.12/- .36
I_{IL3}	Min/Max limits for CKT				
	A	B	C	D	E
	-.15/- .60	-.06/- .60	-.15/- .56	-.29/- .72	-.24/- .72
I_{IL4}	Min/Max limits for CKT				
	A	B	C	D	E
	-.16/- .70	-.06/- .70	-.29/- .65	-.20/- .80	-.12/- .72

5/ I_{OS} limits are as follows:

Test nos. 46 and 48: CKT's A, B, C - -7.5/-50
CKT D - -15/-100

6/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volts maximum.

7/ Tests shall be performed in sequence, attributes data only.

8/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

9/ These tests may be performed as shown in table III or alternately as follows:

Test no.	CLK1	CLR1	K1	V _{CC}	CLK2	CLR2	J2	$\bar{Q}2$	Q2	K2	GND	Q1	$\bar{Q}1$	J1
72A	A	A	A	4.5 V	B	A	A	H	L	A	GND	L	H	A
72B	B	"	"	"	B	"	"	H	L	"	"	H	L	"
72C	B	"	"	"	A	"	"	H	L	"	"	H	L	"
78A	A	"	"	"	B	"	"	L	H	"	"	H	L	"
78B	B	"	"	"	B	"	"	L	H	"	"	L	H	"
78C	B	"	"	"	A	"	"	L	H	"	"	L	H	"

10/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X Cases A,B,C,D Test no.	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
1 Tc = 25°C	V _{OH}	3006	1	0.7 V	2.0 V	GND	2.0 V	Q1	Q1	GND	Q2	Q2	PR2	CLK2	D2	CLR2	4.5 V	Q1	2.5		V
			2	2.0 V	"	GND	0.7 V	-4 mA	-4 mA	"	"	"	"	"	"	"	"	Q1	"	"	"
			3	"	"	"	2.0 V	-4 mA	-4 mA	"	"	"	"	"	"	"	"	Q1	"	"	"
			4	"	0.7 V	2.0 V	2.0 V	"	"	"	"	"	"	"	"	"	"	Q1	"	"	"
			5	"	"	"	"	"	"	"	"	-4 mA	0.7 V	GND	2.0 V	2.0 V	"	Q2	"	"	"
			6	"	"	"	"	"	"	"	"	-4 mA	2.0 V	GND	2.0 V	0.7 V	"	Q2	"	"	"
			7	"	"	"	"	"	"	"	-4 mA	"	"	2/	0.7 V	2.0 V	"	Q2	"	"	"
			8	"	"	"	"	"	"	"	"	-4 mA	"	2/	2.0 V	2.0 V	"	Q2	"	"	"
			9	2.0 V	0.7 V	2/	2.0 V	4 mA	4 mA	"	"	"	"	"	"	"	"	Q1	0.4	"	"
			10	"	2.0 V	2/	2.0 V	"	4 mA	"	"	"	"	"	"	"	"	Q1	"	"	"
			11	"	"	GND	0.7 V	4 mA	4 mA	"	"	"	"	"	"	"	"	Q1	"	"	"
			12	0.7 V	"	GND	2.0 V	4 mA	"	"	"	"	2.0 V	2/	0.7 V	2.0 V	"	Q1	"	"	"
			13	"	"	"	"	"	"	"	4 mA	4 mA	2.0 V	2/	2.0 V	"	"	Q2	"	"	"
			14	"	"	"	"	"	"	"	"	"	0.7 V	GND	"	"	"	Q2	"	"	"
V	IC	"	15	"	"	"	"	"	"	"	4 mA	4 mA	"	"	"	"	"	Q2	"	"	"
			16	"	"	"	"	"	"	"	"	4 mA	2.0 V	GND	"	0.7 V	"	Q2	"	"	"
			17	-18 mA	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR1	-1.5	"	"
			18	"	-18 mA	"	"	"	"	"	"	"	"	"	"	"	"	D1	"	"	"
			19	"	"	-18 mA	"	"	"	"	"	"	"	"	"	"	"	CLK1	"	"	"
			20	"	"	"	-18 mA	"	"	"	"	"	"	"	"	"	"	PR1	"	"	"
			21	"	"	"	"	"	"	"	"	"	-18 mA	"	"	"	"	PR2	"	"	"
			22	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK2	"	"	"
			23	"	"	"	"	"	"	"	"	"	"	-18 mA	-18 mA	"	"	D2	"	"	"
			24	"	"	"	"	"	"	"	"	"	"	"	"	-18 mA	"	CLR2	"	"	"
			25	4.5 V	0.4 V	4.5 V	GND	"	"	"	"	"	GND	4.5 V	0.4 V	4.5 V	5.5 V	D1	3/	3/	mA
			26	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D2	"	"	"
			27	4.5 V	GND	0.4 V	GND	"	"	"	"	"	"	"	"	"	"	CLK1	"	"	"
			28	GND	GND	GND	0.4 V	"	"	"	"	"	"	"	"	"	"	PR1	"	"	"
			29	"	"	"	"	"	"	"	"	"	0.4 V	GND	GND	GND	"	PR2	"	"	"
			30	"	"	"	"	"	"	"	"	"	GND	0.4 V	GND	4.5 V	"	CLK2	"	"	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X A,B,C,D Test no.	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits		Unit
				1	D1	CLK1	PR1	Q1	Q1	GND	Q2	Q2	PR2	CLK2	D2	CLR2	V _{CC}		Min	Max	
1 T _C = 25°C	I _{L5}	3009	31	0.4 V	4.5 V	4.5 V	GND			GND							5.5 V	CLR1	3/	3/	mA
	I _{H1}	"	32							"							"	CLR2	3/	3/	mA
	I _{H2}	3010	33	GND	2.7 V	4.5 V	4.5 V			"							"	D1		20	μA
		"	34							"							"	D2		20	"
		"	35							"							"	D2		100	"
	I _{H3}	"	36	GND	5.5 V	4.5 V	4.5 V			"							"	D1		100	"
		"	37	GND	4.5 V	2.7 V	4.5 V			"							"	CLK1		40	"
		"	38	4.5 V	4.5 V	4/	2.7 V			"							"	PR1		"	"
		"	39							"							"	PR2		"	"
		"	40							"							"	CLK2		"	"
	I _{H4}	"	41							"							"	CLK2		200	"
		"	42							"							"	PR2		"	"
		"	43	4.5 V	4.5 V	4/	5.5 V			"							"	PR1		"	"
	I _{H5}	"	44	GND	4.5 V	5.5 V	4.5 V			"							"	CLK1		"	"
		"	45	2.7 V	GND	4/	4.5 V			"							"	CLR1		60	"
	I _{H6}	"	46							"							"	CLR2		60	"
		"	47							"							"	CLR2		300	"
	OS	3011	48	5.5 V	GND	4/	4.5 V			"							"	CLR1		300	"
		"	49	GND						GND							"	Q1	-15	-100	mA
		"	50							"							"	Q1	"	"	"
		"	51							"							"	Q2	"	"	"
		"	52							"							"	Q2	"	"	"
2 3	CC	3005	53	5.5 V	GND	GND	GND			"							"	V _{CC}		8.0	"
		3005	54	GND	GND	GND	5.5 V			"							"	V _{CC}		8.0	"
Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C and V _{IC} tests are omitted.																					
Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																					
7 5/ 6/ T _C = 25°C	Truth table tests	3014	55	B	B	B	B	H	H	GND	H	H	B	B	B	B	4.5 V	All outputs		See 7/	
		"	56	B	"	"	"	L	"	"	"	L	A	"	"	B	"	"		"	
		"	57	A	"	"	A	L	"	"	"	L	A	"	"	A	"	"		"	
		"	58	"	"	"	B	H	L	"	"	H	B	"	"	"	"	"		"	
		"	59	"	"	"	"	"	L	"	"	L	"	A	"	"	"	"		"	
		"	60	B	"	"	"	"	H	"	"	H	"	"	"	B	"	"		"	
		"	61	B	A	"	"	"	H	"	"	H	"	"	A	B	"	"		"	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits		Unit		
			Cases A,B,C,D	1		3	4	5	6	7	8	9	10	11	12	13	14		Min	Max			
			Test no.	CLR1	D1	CLK1	PR1	Q1	Q1	GND	Q2	Q2	PR2	CLK2	D2	CLR2	V _{cc}	All outputs		See Z/			
7 5/, 6/ T _C = 25°C	Truth table tests	3014	62	B	A	A	A	L	H	GND	H	L	A	A	A	B	4.5V						
			63	A	"	"	A	L	H	"	H	"	H	L	A	"	"	A	"	"	"	"	
			64	"	"	"	B	H	"	B	L	"	L	H	B	"	"	"	"	"	"	"	"
			65	"	"	"	A	"	"	A	"	"	"	"	A	"	"	"	"	"	"	"	"
			66	"	"	"	B	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"	"
			67	"	B	B	"	"	"	"	"	"	"	"	"	B	B	"	"	"	"	"	"
			68	"	"	A	"	"	"	L	H	"	H	L	"	A	"	"	"	"	"	"	"
			69	"	"	"	"	"	B	H	L	"	L	H	B	"	"	"	"	"	"	"	"
			70	"	B	"	"	"	"	"	"	"	"	"	"	"	A	B	"	"	"	"	"
			71	"	"	B	"	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"
			72	"	"	"	"	"	A	L	"	"	"	L	A	"	"	"	"	"	"	"	"
			73	A	"	"	"	"	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"
			74	"	A	"	"	"	"	"	"	"	"	"	"	B	A	"	"	"	"	"	"
			75	"	"	"	"	"	"	H	L	"	L	H	"	A	"	"	"	"	"	"	"
			76	"	"	"	"	"	B	"	"	"	"	"	B	"	"	"	"	"	"	"	"
			77	"	"	"	"	"	A	"	"	"	"	"	A	"	"	"	"	"	"	"	"
			78	B	"	"	"	"	"	L	H	"	H	L	"	"	"	B	"	"	"	"	"
			79	A	"	"	"	"	"	"	L	H	"	H	"	"	"	A	"	"	"	"	"
			80	"	B	"	"	"	B	H	L	"	L	H	B	"	B	"	"	"	"	"	"
			81	"	B	"	"	"	A	H	L	"	L	H	A	"	B	"	"	"	"	"	"
8 4/, 5/ 9 T _C = 25°C	Repeat subgroup 7 at T _C = +125°C and T _C = -55°C	Fig. 8	82	2.7 V	IN	IN	2.7 V	OUT	OUT	GND							5.0 V	Q1	Q1	20	MHz		
T _C = 25°C	f _{max}		83	2.7 V	IN	IN	2.7 V			"							"	Q1	Q1	"	"		
			84							"	OUT		2.7 V	IN	IN	2.7 V	"	Q2	Q2	"	"		
			85							"		OUT	2.7 V	IN	IN	2.7 V	"	Q2	Q2	"	"		
	PLH1		86							"		OUT	IN			IN	"	PR2 to Q2	5	30	ns		
			87							"	OUT		IN			IN	"	CLR2 to Q2	"	"	"		
			88	IN			IN		OUT	"							"	CLR1 to Q1	"	"	"		
			89	IN			IN	OUT		"							"	PR1 TO Q1	"	"	"		
	PHL1		90	IN			IN	OUT		"							"	CLR1 to Q1	"	46	"		
			91	IN			IN		OUT	"							"	PR1 to Q1	"	"	"		
			92							"	OUT		IN			IN	"	PR2 to Q2	"	"	"		
T _C = 25°C		93								"		OUT	IN			IN	"	CLR2 to Q2	"	"	"		
		94								"		OUT	IN	IN	IN	2.7 V	"	CLK2 to Q2	"	30	"		
	PLH2	3003 Fig. 7 3003 Fig. 8	95							"		OUT	2.7 V	IN	IN	2.7 V	"	CLK2 to Q2	"	"	"		
		3003 Fig. 7 3003 Fig. 8	96	2.7 V	IN	IN	2.7 V	OUT		"			2.7 V	IN	IN	2.7 V	"	CLK2 to Q2	"	"	"		
		3003 Fig. 7 3003 Fig. 8	97	2.7 V	IN	IN	2.7 V		OUT	"							"	CLK1 to Q1	"	"	"		
		3003 Fig. 7 3003 Fig. 8	98	2.7 V	IN	IN	2.7 V		OUT	"							"	CLK1 to Q1	"	46	"		
	PHL2	3003 Fig. 8 3003 Fig. 7	99	2.7 V	IN	IN	2.7 V	OUT		"							"	CLK1 to Q1	"	"	"		
		3003 Fig. 7 3003 Fig. 8	100					OUT		"	OUT			2.7 V	IN	IN	2.7 V	CLK2 to Q2	"	"	"		
		3003 Fig. 8	101							"		OUT	2.7 V	IN	IN	2.7 V	"	CLK2 to Q2	"	"	"		

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X Cases A,B,C,D Test no.	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits		Unit
				CLR1	D1	CLK1	PR1	Q1	Q1	GND	Q2	Q2	PR2	CLK2	D2	CLR2	V _{CC}		Min	Max	
10	f _{MAX}	Fig. 8	102-105																20		MHz
	PLH1	3003 Fig.6	106-109																5	39	ns
	PHL1	3003 Fig. 6	110-113																"	59	"
	PLH2	3003 Fig. 7	114																"	39	"
		3003 Fig. 8	115																"	"	"
		3003 Fig. 7	116																"	"	"
		3003 Fig. 8	117																"	"	"
11	PHL2	3003 Fig. 7	118																"	59	"
		3003 Fig. 8	119																"	"	"
		3003 Fig. 7	120																"	"	"
		3003 Fig. 8	121																"	"	"

Same tests and terminal conditions as for subgroup 9, except T_C = +125°C

11 Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C

1/ Case X and 2 pins not referenced are NC.

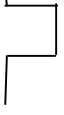
2/  --- 2.5 V minimum/5.5 V maximum
0 V

3/ I_L limits in mA are as follows:

I _L 2	Min/Max limits for CKT					
	A	B	C	D	E	F
	-075/-250	-030/-300	-095/-210	-097/-207	-135/-370	-160/-400

I _L 4	Min/Max limits for CKT					
	A	B	C	D	E	F
	-150/-500 for tests 27, 30	-060/-700	-160/-400 for tests 27, 30	-160/-400 for tests 27, 30	-120/-360 for tests 27, 30	-320/-800 (All)
	-200/-800 for tests 28, 29		-350/-760 for tests 28, 29	-355/-759 for tests 28, 29	-280/-760 for tests 28, 29	

I _L 5	Min/Max limits for CKT					
	A	B	C	D	E	F
	-200/-800	-060/-700	-350/-760	-480/-1200	-280/-760	-480/-1200

4/  --- 2.5 V minimum/5.5 V maximum
0 V

5/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volt maximum.

6/ Tests shall be performed in sequence, attributes data only.

7/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

8/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 04.

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits	Unit
1	$T_C = 25^\circ\text{C}$	3010	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	μA
				CLK1	K1	J1	PR1	Q1	$\bar{Q}1$	GND	$\bar{Q}2$	Q2	PR2	J2	K2	CLK2	V_{CC}	PR1	Max	
							2.7 V	$\bar{5}/$		GND		$\bar{5}/$	2.7 V	4.5 V	GND	GND	5.5 V		60	μA
													5.5 V	4.5 V	GND	GND		PR2	60	
							5.5 V	$\bar{5}/$								GND		PR1	300	
							GND											CLK1	300	
																2.7 V		CLK2	80	
																GND		CLK2	80	
																5.5 V		CLK2	400	
																		CLK1	400	
2	OS	3011					GND	GND										Q1	-15	mA
							4.5 V	GND	$\bar{Q}1$									$\bar{Q}1$	$\bar{6}/$	
																		Q2	-15	
																		$\bar{Q}2$	$\bar{6}/$	
																		V_{CC}	8.0	
																		V_{CC}	8.0	
3	CC	3005					5.5 V													
							GND													
7	Truth table tests	3014		51	B	A	B	H	L	GND	L	H	B	B	B	B	4.5 V	All outputs	See g/	
				52	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				53	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				54	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				55	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				56	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				57	B	B	A	"	"	"	"	"	"	"	"	"	"	"	"	"
				58	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				59	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				60	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"
8	Repeat subgroup 7 at $T_C = +125^\circ\text{C}$ and $T_C = -55^\circ\text{C}$.			61	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				62	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				63	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				64	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				65	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				66	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				67	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				68	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				69	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				70	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
9				71	B	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"
				72	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				73	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				74	B	B	B	"	"	"	"	"	"	"	"	"	"	"	"	"
				75	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				76	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				77	B	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"
				78	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				79	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits Min Max	Unit	
9 Tc = 25°C	f _{max} g/	Fig. 11 " "	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Q1 Q1 Q2	25	MHz	
			Test no.	CLK1	K1	J1	PR1	Q1	Q1	GND	Q2	PR2	J2	K2	CLK2	V _{cc}	5.0 V		"	"	
			80	IN	2.7 V	2.7 V	2.7 V	OUT	OUT	GND	"	"	"	"	"	"	"		"		
																			"	"	
																			"	"	
																			"	"	
	PLH1	3003 Fig. 11	84										OUT	IN	2.7 V	2.7 V	IN	"	Q2	"	"
													OUT						PR2 to Q2	5	21
																			PR1 to Q1	"	21
																			PR1 to Q1	"	28
																		PR2 to Q2	"	"	
																		CLK2 to Q2	"	22	
																		CLK2 to Q2	"	"	
																		CLK1 to Q1	"	"	
																		CLK1 to Q1	"	"	
																		CLK1 to Q1	"	"	
																		CLK2 to Q2	"	"	
																		CLK2 to Q2	"	"	
																		CLK2 to Q2	"	"	
																		CLK2 to Q2	"	"	
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																		CLK2 to Q2	"	"	
																		CLK2 to Q2	"	"	
																		CLK2 to Q2	"	"	
																		CLK2 to Q2	"	"	
																		CLK2 to Q2	"	"	

Same tests and terminal conditions, and limits as for subgroup 9, except $T_C = +125^\circ\text{C}$.

1/ Case X and 2 pins not referenced are NC.

2/  2.5 V minimum/5.5 V maximum

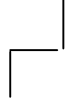
3/  2.5 V minimum/5.5 V maximum

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

4/ I_{IL} limits in mA are as follows:

Min/Max limits for CRT					
Symbol	A	B	C	D	E
I_{IL1}	-.075/- .250	-.03/- .300	-.110/- .250	-.120/- .360	-.120/- .360
I_{IL2}	-.175/- .550	-.060/- .600	-.150/- .560	-.240/- .720	-.280/- .760
I_{IL3}	-.200/- .800	-.060/- .700	-.290/- .650	-.120/- .720	-.320/- .800

5/ Momentary GND, then open.

6/ I_{OS} limits in mA are as follows:

Test no.	A	B	C	D and E	F
46, 48	-7.5/-50	-7.5/-50	-30/-130	-15/-130	-7.5/-50
46, 48 Q1, Q2	2.25 V	2.25 V	---	---	2.25 V

7/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volts maximum.

8/ Tests shall be performed in sequence, attributes data only.

9/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

10/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 05.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X A,B,C,D Test no.	Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).														Measured terminal	Limits		Unit
				2	3	4	6	8	9	10	12	13	14	16	18	19	20		Min	Max	
1 Tc = 25°C	V _{OH}	3006	1	2.0 V	0.7 V	2.0 V	0.7 V	-4 mA	Q1	Q1	Q2	Q2	PR2	J2	K2	2.0 V	4.5 V	Q1	2.5		V
			2	0.7 V	"	"	2.0 V	-4 mA	"	GND	"	"	"	"	"	2.0 V	"	Q1	"		"
			3	2.0 V	"	"	"	-4 mA	"	"	"	"	"	"	"	2/	"	Q1	"		"
			4	"	2.0 V	0.7 V	"	-4 mA	"	"	"	"	"	"	"	"	"	Q1	"		"
			5	"	"	"	"	"	"	"	-4 mA	"	2.0 V	0.7 V	2.0 V	"	"	Q2	"		"
			6	"	"	"	"	"	"	"	-4 mA	-4 mA	"	2.0 V	0.7 V	"	"	Q2	"		"
			7	0.7 V	"	"	"	"	"	"	-4 mA	"	"	"	"	2.0 V	"	Q2	"		"
			8	2.0 V	"	"	"	"	"	"	-4 mA	-4 mA	0.7 V	"	"	"	"	Q2	"		"
	OL	3007	9	2.0 V	"	"	"	"	"	"	4 mA	"	0.7 V	"	"	"	"	Q2	"	0.4	"
			10	0.7 V	"	"	"	"	"	"	4 mA	4 mA	2.0 V	"	"	"	"	Q2	"		"
			11	2.0 V	"	"	"	"	"	"	4 mA	"	"	"	"	2/	"	Q2	"		"
			12	"	"	"	"	"	"	"	"	4 mA	"	0.7 V	2.0 V	"	"	Q2	"		"
			13	"	0.7 V	2.0 V	2.0 V	"	4 mA	"	"	"	"	"	"	"	"	Q1	"		"
			14	"	"	0.7 V	2.0 V	4 mA	"	"	"	"	"	"	"	"	"	Q1	"		"
			15	"	"	"	0.7 V	4 mA	"	"	"	"	"	"	"	2.0 V	"	Q1	"		"
			16	0.7 V	"	"	2.0 V	4 mA	"	"	"	"	"	"	"	2.0 V	"	Q1	"		"
V	IC		17	-18 mA	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR	"	-1.5	"
			18	"	-18 mA	"	"	"	"	"	"	"	"	"	"	"	"	K1	"		"
			19	"	"	"	"	"	"	"	"	"	"	"	"	"	"	J1	"		"
			20	"	"	"	-18 mA	"	"	"	"	"	"	"	"	"	"	PR1	"		"
			21	"	"	"	"	"	"	"	"	-18 mA	"	"	"	"	"	PR2	"		"
			22	"	"	"	"	"	"	"	"	"	"	-18 mA	"	"	"	J2	"		"
			23	"	"	"	"	"	"	"	"	"	"	"	-18 mA	"	"	K2	"		"
			24	"	"	"	"	"	"	"	"	"	"	"	"	-18 mA	"	CLK	"		"
			25	4.5 V	0.4 V	GND	3/	"	"	"	"	"	"	"	"	4.5 V	5.5 V	K1	4/		mA
			26	3/	GND	0.4 V	4.5 V	"	"	"	"	"	"	"	"	"	"	J1	"		"
I	IL1	3009	27	3/	"	"	"	"	"	"	"	"	4.5 V	0.4 V	4.5 V	"	"	J2	"		"
			28	4.5 V	"	"	"	"	"	"	"	"	3/	4.5 V	0.4 V	"	"	K2	"		"
			29	"	"	"	"	"	"	"	"	"	0.4 V	4.5 V	4.5 V	"	"	PR2	"		"
			30	"	"	"	4.5 V	0.4 V	"	"	"	"	4.5 V	4.5 V	4.5 V	"	"	PR1	"		"
			31	3/	"	"	4.5 V	"	"	"	"	"	"	"	0.4 V	"	"	CLK	"		"
			32	4.5 V	"	"	3/	"	"	"	"	"	3/	4.5 V	4.5 V	"	"	CLK	"		"
			33	0.4 V	4.5 V	4.5 V	4.5 V	"	"	"	"	"	4.5 V	4.5 V	4.5 V	"	"	CLR	"		"
			34	GND	2.7 V	GND	GND	"	"	"	"	"	"	"	GND	"	"	K1	"	20	μ A
			35	"	"	"	GND	"	"	"	"	"	"	"	"	"	"	J1	"		"
			36	"	"	"	"	"	"	"	"	"	GND	2.7 V	GND	"	"	J2	"		"
I	IL4	3010	37	"	"	"	"	"	"	"	"	"	"	"	"	"	"	K2	"		"

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits	Unit
1 $T_c = 25^\circ\text{C}$	I _{H2}	3010	Cases A,B,C,D Test no.	CLR	K1	J1	PR1	Q1	Q1	GND	Q2	Q2	PR2	J2	K2	CLK	V _{CC}		Min	μA
				GND						GND			GND	GND	5.5 V	GND	5.5 V	K2	100	
				"						"								J2	"	
				"						"								J1	"	
				"						"								K1	"	
	I _{H5}	"	"	"						"								PR1	60	
				"						"								PR2	60	
				"						"								PR2	300	
				"						"								PR1	300	
				"						"								CLR	120	
	I _{H6}	"	"	"						"								CLR	600	
				"						"								CLK	160	
				"						"								CLK	800	
				"						"								Q1	-15	mA
				"						"								Q2	"	
2	OS	3011	"	"						"								Q2	"	
				"						"								Q1	"	
				"						"								V _{CC}	8.0	
				"						"								V _{CC}	8.0	
				"						"										
				"						"										
				"						"										
				"						"										
				"						"										
				"						"										
				"						"										
				"						"										
				"						"										
				"						"										
				"						"										
3 7 5/7, 8/7 $T_c = 25^\circ\text{C}$	Truth table tests	3014	"	B	B	A	A	L	H	GND	H	L	A	A	B	A	4.5 V	All outputs	See 7/	
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

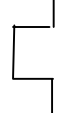
Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X	Cases 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20														Limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
7 $\bar{5}$, $\bar{6}$ / $T_C = 25^\circ\text{C}$	Truth table tests	3014	Test no.	CLR	K1	J1	PR1	Q1	$\bar{Q}1$	GND	$\bar{Q}2$	H	Q2	PR2	J2	B	A	4.5 V	See 7/	
				A	B	B	B	H	L	GND	L	"	H	"	"	"	"	"	"	
8 $\bar{4}$, $\bar{5}$ / $T_C = 25^\circ\text{C}$	Repeat subgroup 7 at $T_C = 125^\circ\text{C}$ and $T_C = -55^\circ\text{C}$	Fig. 9	95	5.0 V	2.7 V	2.7 V	2.7 V	OUT	OUT	GND	"	"	"	"	"	"	"	"	"	"
			96	"	2.7 V	2.7 V	2.7 V	"	"	"	"	"	"	"	"	"	"	"	"	"
			97	"	"	"	"	"	"	"	OUT	"	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			98	"	"	"	"	"	"	"	"	OUT	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			99	IN	GND	2.7 V	2.7 V	"	OUT	"	"	"	"	"	"	"	"	"	"	ns
			100	IN	"	"	"	"	"	"	OUT	"	"	2.7 V	2.7 V	GND	"	"	"	"
			101	2.7 V	"	"	"	"	"	"	"	OUT	"	"	GND	2.7 V	2.7 V	"	"	"
			102	"	2.7 V	GND	GND	OUT	OUT	"	"	"	"	"	"	"	"	"	"	"
			103	"	"	2.7 V	IN	"	OUT	"	"	"	"	"	"	"	"	"	"	"
			104	"	"	"	IN	"	"	"	OUT	"	"	"	"	"	"	"	"	"
			105	IN	"	"	"	"	"	"	"	"	"	IN	GND	2.7 V	2.7 V	"	"	"
			106	IN	GND	2.7 V	2.7 V	OUT	"	"	"	"	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			107	2.7 V	2.7 V	2.7 V	2.7 V	OUT	"	"	"	"	"	"	"	"	"	"	"	"
			108	"	2.7 V	2.7 V	2.7 V	"	OUT	"	"	"	"	"	"	"	"	"	"	"
t	PHL1	3003 Fig. 9	109	"	"	"	"	"	"	"	OUT	"	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			110	"	"	"	"	"	"	"	"	OUT	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			111	"	"	"	"	"	"	"	"	OUT	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			112	"	"	"	"	"	"	"	OUT	"	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			113	"	2.7 V	2.7 V	2.7 V	"	OUT	"	"	"	"	"	"	"	"	"	"	"
			114	"	2.7 V	2.7 V	2.7 V	OUT	"	"	"	"	"	"	"	"	"	"	"	"
t	PHL2	3003 Fig. 10	109	"	"	"	"	"	"	"	OUT	"	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			110	"	"	"	"	"	"	"	"	OUT	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			111	"	"	"	"	"	"	"	"	OUT	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			112	"	"	"	"	"	"	"	OUT	"	"	2.7 V	2.7 V	2.7 V	2.7 V	"	"	"
			113	"	2.7 V	2.7 V	2.7 V	"	OUT	"	"	"	"	"	"	"	"	"	"	"
			114	"	2.7 V	2.7 V	2.7 V	OUT	"	"	"	"	"	"	"	"	"	"	"	"

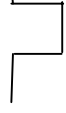
See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	2	3	4	6	8	9	10	12	13	14	16	18	19	20	Measured terminal	Limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	
10				CLR	K1	J1	PR1	Q1	$\overline{Q1}$	GND	$\overline{Q2}$	Q2	PR2	J2	K2	CLK	V _{CC}	Same tests and terminal conditions as for subgroup 9, except T _C = +125°C.	25		MHz
	f _{MAX}	Fig. 9	115-118																5	32	ns
	PLH1	3003 Fig. 9	119-122																"	40	"
	PHL1	3003 Fig. 9	123-126																"	32	"
	PLH2	3003 Fig. 10	127-130																"	42	"
	PHL2	3003 Fig. 10	131-134																"		"
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C.																				

1/ Case X and 2 pins not referenced are NC.

2/  --- 2.5 V minimum/5.5 V maximum

3/  --- 2.5 V minimum/5.5 V maximum
0 V

4/ I_{IL} limits in mA are as follows:

I_{IL1}	Min/Max limits for CKT				
	A	B	C	D	E
	-075/-250	-030/-300	-110/-250	-120/-360	-120/-360
I_{IL4}	Min/Max limits for CKT				
	A	B	C	D	E
	-200/-800	-060/-700	-290/-650	-120/-720	-320/-800
I_{IL6}	Min/Max limits for CKT				
	A	B	C	D	E
	-300/-1000	-120/-1000	-300/-1120	-240/-1440	-560/-1520
I_{IL7}	Min/Max limits for CKT				
	A	B	C	D	E
	-450/-1300	-120/-1000	-580/-1300	-120/-1500	-640/-1600

5/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volt maximum.

6/ Tests shall be performed in sequence, attributes data only.

7/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

8/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open). 1/

See footnotes at end of device types 03 and 10.

TABLE III. Group A inspection for device type 03 and 10.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open). 1/

Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X	* 2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20	Measured terminal	Limits	Unit
			Test no.	CLK1	K1	J1	PR1	Q1	Q1	Q2	GND	Q2	PR2	J2	K2	CLK2	CLR2	CLR1	V _{CC}		Min	Max
1 T _C = 25°C	I _{H2}	3010	43	GND	5.5 V	4.5 V	GND				GND							4.5 V	5.5 V	K1		100
			44	GND	4.5 V	5.5 V	4.5 V											GND		J1		"
			45								"		4.5 V	5.5 V	4.5 V					J2		"
			46								"		GND	4.5 V	5.5 V					K2		"
	I _{H5}	"	47								"		4/	GND	4.5 V					CLR2		60
			48								"		2.7 V	4.5 V	GND					PR2		"
			49	GND	4.5 V	GND	4/				"							2.7 V		CLR1		"
			50	GND	GND	4.5 V	2.7 V				"							4/		PR1		"
	I _{H6}	"	51	GND	GND	4.5 V	5.5 V				"							4/		PR1		300
			52	GND	4.5 V	GND	4/				"							5.5 V		CLR1		"
			53								"		5.5 V	4.5 V	GND					PR2		"
			54								"		4/	GND	4.5 V					CLR2		"
	I _{H7}	"	55								"		GND	GND	GND					CLR2		"
			56	2.7 V	GND	GND	GND				"									CLK1		"
			57	5.5 V	GND	GND	GND				"									CLK1		400
			58								"		GND	GND	GND					CLK2		400
2 OS	3011	"	59	GND	GND	GND	GND				"							4.5 V		Q1		-15
			60	GND	GND	GND	4.5 V		GND		"							GND		Q1		"
			61								"	GND	GND	GND	GND					Q2		"
			62							GND	"		4.5 V	"	"					Q2		"
	CC	3005	63	GND	GND	GND	GND				"		GND	"	"	"		5.5 V		V _{CC}		8.0
			64	GND	GND	GND	5.5 V				"		5.5 V	"	"	"		GND		V _{CC}		8.0
			65	B	B	A	A	L	H	H	GND	L	A	A	B	B	B	B	B	4.5 V	All outputs	See g/
			66	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
3 7 g/, Z/ table T _C = 25°C	Truth table tests	3014	67	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			68	B	A	B	B	H	L	"	"	H	B	B	A	B	A	A	A	"	"	"
			69	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			70	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			71	"	B	"	A	L	H	H	"	L	A	"	B	"	B	B	B	"	"	"
			72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A	A	"	"	"
			73	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			74	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			75	"	"	"	"	H	L	L	"	H	B	"	"	"	"	"	"	"	"	"
			76	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"	"	"
			77	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			78	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			79	"	"	"	"	L	H	H	"	L	"	"	"	"	"	B	B	"	"	"
			80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A	A	"	"	"

See footnotes at end of device types 03 and 10.

TABLE III. Group A inspection for device type 03 and 10.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open). 1/

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	4 Channels: Channel 1: 100 MHz, Channel 2: 100 MHz, Channel 3: 100 MHz, Channel 4: 100 MHz																				Limits		Unit
				* 2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20	Min	Max					
7 g, Z/ Tc = 25°C	Truth table tests	3014	81	A	B	A	A	L	H	H	GND	L	A	A	B	A	A	A	4.5 V	See g/						
			82	B	"	"	"	H	L	"	"	"	"	"	"	"	"	"	"							
			83	"	A	B	B	"	"	"	"	"	B	B	A	"	"	"	"							
			84	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"							
			85	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
			86	B	"	"	"	"	L	H	"	"	"	"	"	"	"	"	"							
			87	A	"	A	A	B	H	"	"	"	B	A	"	"	"	"	"							
			88	B	"	"	A	L	"	"	"	"	"	B	B	"	"	"	"							
			89	B	"	"	"	"	"	"	"	"	"	"	B	A	"	"	"							
			90	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
			91	B	"	"	"	H	L	L	"	"	H	"	"	"	"	"	"							
			92	A	"	"	"	H	L	L	"	"	H	"	"	"	"	"	"							
93	B	"	"	"	"	L	H	"	"	"	"	"	"	"	"	"										
8 g, Z/ 9 Tc = 25°C	Repeat subgroup 7 at Tc = +125°C and Tc = -55°C	Fig. 9	94	IN	2.7 V	2.7 V	2.7 V	2.7 V	OUT	OUT		GND						2.7 V	5.0 V	25		MHz				
			95	IN	2.7 V	2.7 V	2.7 V			OUT	"								"	"	"	"				
			96							OUT	"		2.7 V	2.7 V	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			97								"		2.7 V	2.7 V	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			3003	IN	GND	2.7 V	2.7 V	2.7 V	OUT	OUT		"						IN	"	"	5	21	ns			
			99	IN	2.7 V	GND	IN	OUT		OUT	"		2.7 V	2.7 V	GND	GND	IN	2.7 V		"	"	"	"			
			100								"		OUT	IN	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			101								"		OUT	OUT	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			102 10/								"		OUT	OUT	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			103							OUT	"		IN	GND	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			104	IN	GND	2.7 V	2.7 V	OUT										IN	"	"	"	"	"			
			105	IN	2.7 V	GND	IN		OUT				2.7 V	2.7 V	GND	GND	IN	2.7 V		"	"	"	"			
9 g, Z/ 10 Tc = 25°C	PLH1	Fig. 9	106	IN	2.7 V	2.7 V	2.7 V	2.7 V	OUT	OUT		"					2.7 V		"	"	"	"				
			107	IN	2.7 V	2.7 V	2.7 V	OUT										2.7 V		"	"	"	"			
			108							OUT	"		2.7 V	2.7 V	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			109								"		2.7 V	2.7 V	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			110								"		2.7 V	2.7 V	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			111								"		2.7 V	2.7 V	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			112	IN	2.7 V	2.7 V	2.7 V	OUT		OUT	"		2.7 V	2.7 V	2.7 V	2.7 V	IN	2.7 V		"	"	"	"			
			113	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							2.7 V	"	"	"	"	"			
			114-117							OUT	"							2.7 V	"	"	"	"	"			
			Fig. 9								"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
10	fMAX	Fig. 9	118-121																25		MHz					
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
11	Same tests and terminal conditions as for subgroup 10, except Tc = -55°C	Fig. 10	122-125																5		ns					
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			
			3003	IN	2.7 V	2.7 V	2.7 V	OUT	OUT		"							CLK1 to Q1		"	"	"	"			

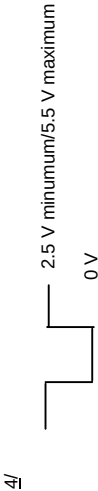
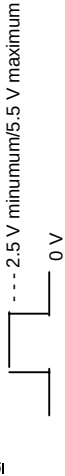
Same tests and terminal conditions as for subgroup 9, except Tc = +125°C

Same tests and terminal conditions as for subgroup 10, except Tc = -55°C

See footnotes at end of device types 03 and 10.

TABLE III. Group A inspection for device type 03 and 10.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open). 1/

- * Terminal numbers for device type 03.
** Terminal numbers for device type 10.
1/ See 6.4 for special applications note.
2/ Case X and 2 pins not referenced are NC.



5/ I_{IL} limits in mA are as follows:

I_{IL1}	Min/Max limits for CKT				
	A	B	C	D	E
	-075/-250	-030/-300	-150/-560	-120/-360	-120/-360

I_{IL3}	Min/Max limits for CKT				
	A	B	C	D	E
	-150/-500	-060/-600	-250/-560	-240/-720	-280/-760

I_{IL4}	Min/Max limits for CKT				
	A	B	C	D	E
	-200/-800	-060/-700	-290/-650	-120/-720	-320/-800

- 6/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volts maximum.
7/ Tests shall be performed in sequence, attributes data only.
8/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

9/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

10/ These tests may be performed as shown in table III or alternately as follows:

Test no.	CLK1	K1	J1	PR1	Q1	Q1	Q2	GND	Q2	PR2	J2	K2	CLK2	CLR2	CLR1	V _{CC}
98A	2.7 V	2.7 V	2.7 V	2/	OUT	OUT		GND							IN	5.0 V
99A	2.7 V	2.7 V	2.7 V	IN	OUT			"							2/	"
100A						OUT		"		2/	2.7 V	2.7 V	2.7 V	IN		"
101A							OUT	"	OUT	IN	2.7 V	2.7 V	2.7 V	2/		"
102A								"	OUT	2/	2.7 V	2.7 V	2.7 V	IN		"
103A						OUT		"		IN	2.7 V	2.7 V	2.7 V	2/		"
104A	2.7 V	2.7 V	2.7 V	2/	OUT			"							IN	"
105A	2.7 V	2.7 V	2.7 V	IN		OUT		"							2/	"

TABLE III. Group A inspection for device type 06.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open)															Measured terminal	Limits		Unit			
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17		18	19	20
1 $T_c = 25^\circ\text{C}$	V_{OH}	3006 "	Cases E, F	Test no.	CLR	Q1	D1	D2	Q2	D3	Q3	GND	CLK	Q4	D4	Q5	D5	D6	Q6	V_{CC}	4.5 V	V			
				1	2.0 V	-4 mA	2.0 V	2.0 V	-4 mA	2.0 V	-4 mA	GND	2/							Q1	2.5				
				2	"	"						"	"							Q2	"				
				3	"	"						"	"							Q3	"				
				4	"	"						"	"	-4 mA	2.0 V	-4 mA	2.0 V			Q4	"				
				5	"	"						"	"							Q5	"				
		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
	I_{OL}	"	3007 "	Cases E, F	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
I_C	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
IL1	"	3009 "	Cases E, F	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{L2}	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
IH1	"	3010 "	Cases E, F	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	
		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{H2}	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

[illegible]

See footnotes at end of device types 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	Cases 1/2, X																	Measured terminal	Limits		Unit	
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		18	19		20
10	f_{max}	Fig. 13	Test no. 95-100	CLR	Q1	D1	D2	Q2	D3	Q3	GND	CLK	Q4	D4	Q5	D5	D6	Q6	V _{CC}				25		MHz
	PHL1	3003 Fig. 13	101-106																				5	52	ns
	PLH2	3003 Fig. 14	107-112																				"	47	"
	PHL2	3003 Fig. 15	113-118																				"	52	"
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C.																								

1/ Case X and 2 pins not referenced are NC.

2/  2.5 V minimum/5.5 V maximum
0 V

3/ I_{IL} limits in mA are as follows:

I_{IL1}	Min/Max limits for CKT						
	A	B	C	D	E	F	G
	-.085/- .270	-.100/- .340	-.075/- .250	-.075/- .250	-.120/- .360	-.160/- .400	-.075/- .250

I_{IL2}	Min/Max limits for CKT						
	A	B	C	D	E	F	G
	-.115/- .350	-.150/- .420	-.125/- .275 for test 33 -.160/- .400 for test 34	-.120/- .360	-.120/- .360	-.150/- .380 for test 33 -.160/- .400 for test 34	-.075/- .250 for test 33 -.120/- .360 for test 34

4/  2.5 V minimum/5.5 V maximum
0 V

5/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volts maximum.

6/ Tests shall be performed in sequence, attributes data only.

7/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

8/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

See footnotes at end of device type 07.

[illegible]

TABLE III. Group A inspection for device type 07 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

[illegible]

See footnotes at end of device type 07.

TABLE III. Group A inspection for device type 07 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X	Cases 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20																Limits		Unit
				2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20	Measured terminal	Min	
9 T _C = 25°C	t _{PHL1}	3003 Fig. 13	83	IN															CLR to Q1	5	45	ns
			84	"															CLR to Q2	"	"	"
			85	"			2.7 V												CLR to Q3	"	"	"
			86	"															CLR to Q4	"	"	"
		3003 Fig. 14	87	2.7 V															CLK to Q4	"	35	"
			88																CLK to Q3	"	"	"
			89	"															CLK to Q2	"	"	"
			90	"															CLK to Q1	"	"	"
		3003	91	"															CLK to Q1	"	"	"
		Fig. 15	92	"															CLK to Q2	"	"	"
PHL2	93	"																CLK to Q3	"	"	"	
	94	"																CLK to Q4	"	"	"	
	3003	95	"															CLK to Q4	"	40	"	
	Fig. 14	96	"															CLK to Q3	"	"	"	
	"	97	"															CLK to Q2	"	"	"	
	"	98	"															CLK to Q1	"	"	"	
	3003	99	"															CLK to Q1	"	"	"	
	Fig. 15	100	"															CLK to Q2	"	"	"	
	"	101	"															CLK to Q3	"	"	"	
	"	102	"															CLK to Q4	"	"	"	
10	t _{MAX}	Fig. 13	103-110																25		ns	
Same tests and terminal conditions as for subgroup 9, except T _C = +125°C	PLH1	3003 Fig. 13	111-114																5	51	"	
	PHL1	3003 Fig. 13	115-118																"	55	"	
	PLH2	3003 Fig. 13	119-122																"	46	"	
	PLH2	3003 Fig. 14	123-126																"	46	"	
	PHL2	3003 Fig. 15	127-130																"	55	"	
	PHL2	3003 Fig. 14	131-134																"	55	"	
	Fig. 15	131-134																	"	55	"	
	11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C.																				

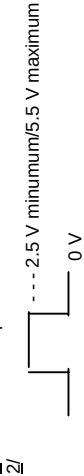
Same tests and terminal conditions as for subgroup 9, except $T_c = +125^\circ\text{C}$

Same tests, terminal conditions, and limits as for subgroup 10, except $T_c = -55^\circ\text{C}$.

See footnotes at end of device type 07.

TABLE III. Group A inspection for device type 07 - Continued.

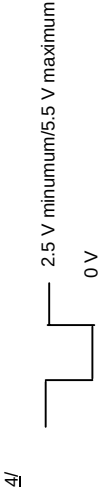
1/ Case X and 2 pins not referenced are NC.



3/ I_{IL} limits in mA are as follows:

I _{IL1}	Min/Max limits for CKT						
	A	B	C	D	E	F	G
	-075/-250	-100/-340	-075/-250	-075/-250	-120/-360	-160/-400	-075/-250

I _{IL2}	Min/Max limits for CKT						
	A	B	C	D	E	F	G
	-085/-270 for test 35 -135/-400 for test 36	-150/-420	-125/-275 for test 35 -160/-400 for test 36	-120/-400 for test 35 -120/-360 for test 36	-120/-400	-105/-380 for test 35 -160/-400 for test 36	-075/-250 for test 35 -120/-360 for test 36



5/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volts maximum.

6/ Tests shall be performed in sequence, attributes data only.

7/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

8/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

[illegible]

See footnotes at end of type 09.

TABLE III. Group A inspection for device type 09.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/2, X	Cases E, F																Measured terminal	Limits		Unit
				Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Min	Max	
1	Tc = 25°C	IH1	3010	39	GND	CLR1	J1	2.7 V	GND	Q1	Q1	GND	Q2	Q2	PR2	CLK2	K 2	J2	CLR2	Vcc	5.5 V	J1	μ A
				40	GND	GND	GND	2.7 V	4.5 V	GND	GND	GND	GND	GND	GND	4.5 V	4.5 V	GND	GND	GND	"	K 1	"
				41																	"	K 2	"
				42																	"	J2	"
				43																	"	K 2	"
				44																	"	K 2	"
				45																	"	K 1	"
				46																	"	J1	"
				47																	"	CLK1	"
				48																	"	PR1	"
				49																	"	PR2	"
				50																	"	CLK2	"
				51																	"	CLK2	"
				52																	"	PR2	"
				53																	"	PR1	"
2	Tc = 25°C	IH2	3011	54																	"	CLK1	"
				55																	"	CLK1	"
				56																	"	CLK1	"
				57																	"	CLK1	"
				58																	"	CLK1	"
				59																	"	CLK1	"
				60																	"	CLK1	"
				61																	"	CLK1	"
				62																	"	CLK1	"
				63																	"	CLK1	"
				64																	"	CLK1	"
				65																	"	CLK1	"
				66																	"	CLK1	"
				67																	"	CLK1	"
3	Tc = 25°C	IH3	3011	68																	"	CLK1	"
				69																	"	CLK1	"
				70																	"	CLK1	"
				71																	"	CLK1	"
				72																	"	CLK1	"
				73																	"	CLK1	"
				74																	"	CLK1	"
				75																	"	CLK1	"
				76																	"	CLK1	"
				77																	"	CLK1	"
				78																	"	CLK1	"
				79																	"	CLK1	"
				80																	"	CLK1	"
				81																	"	CLK1	"
				82																	"	CLK1	"
4	Tc = 25°C	IH4	3011	83																	"	CLK1	"
				84																	"	CLK1	"
				85																	"	CLK1	"
				86																	"	CLK1	"
				87																	"	CLK1	"
				88																	"	CLK1	"
				89																	"	CLK1	"
				90																	"	CLK1	"
				91																	"	CLK1	"
				92																	"	CLK1	"
				93																	"	CLK1	"
				94																	"	CLK1	"
				95																	"	CLK1	"
				96																	"	CLK1	"

See footnotes at end of device type 09.

TABLE III. Group A inspection for device type 09.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

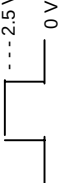
Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X Cases E, F Test no.	Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open)														Measured terminal	Limits		Unit
				3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	
7 5/, 6/ Tc = 25°C	Truth table tests	3014	87	A	A	A	A	A	A	A	A	A	A	A	A	A	A	All outputs			
			88	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			89	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			90	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			91	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			92	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			93	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			94	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			95	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			96	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			97	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			98	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			99	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
			100	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
8 Repeat subgroup 7 at T _c = +125°C and T _c = -55°C.	t _{MAX} Fig. 16 g/	3003 Fig. 17 "	105	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	Q1	20		MHz
			106	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	Q1			
			107	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q2			
			108	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Q2			
			109	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	CLR1 to Q1	5	20	ns
			110	2.7 V	GND	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	PR1 to Q1			
			111	"	"	"	"	"	"	"	"	"	"	"	"	"	"	PR2 to Q2			
			112	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR2 to Q2			
			113	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR2 to Q2			
			114	"	"	"	"	"	"	"	"	"	"	"	"	"	"	PR2 to Q2	32		
			115	2.7 V	GND	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	PR1 to Q1			
			116	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	CLR1 to Q1			
			117	2.7 V	GND	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	CLR1 to Q1	24		
			118	2.7 V	GND	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	CLR1 to Q1			
9 Tc = 25°C	t _{MAX} Fig. 16 PLH2	3003 Fig. 16 "	119	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR2 to Q2			
			120	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR2 to Q2			
			121	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR2 to Q2			
			122	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLR2 to Q2	35		
			123	2.7 V	GND	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	CLR2 to Q2			
			124	2.7 V	GND	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	IN	2.7 V	CLR2 to Q2			

See footnotes at end of device type 09.

TABLE III. Group A inspection for device type 09.
Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 1/ 2, X Cases E, F Test no.	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20	Limits		Measured terminal	Unit
				1	2	3	4	5	6	7	8	9	10	11	12	K 2	J2	CLR2	V _{CC}	Min	Max		
10	f _{MAX}	Fig. 16	125-128	CLR1	J1	K 1	CLK1	PR1	Q1	Q 1	GND	Q 2	Q2	PR2	CLK2	K 2	J2	CLR2	V _{CC}	20			MHz
	PLH1	3003 Fig. 17	129-132																	5	39		ns
	PHL1	3003 Fig. 17	133-136																	"	59		"
	PLH2	3003 Fig. 16	137-140																	"	39		"
	PHL2	3003 Fig. 16	141-144																	"	59		"
11	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and V _{CC} tests are omitted.																						

1/ Case X and 2 pins not referenced are NC.

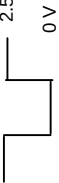
2/  - - - 2.5 V minimum/5.5 V maximum

3/ I_{IL} limits in mA are as follows:

I _{IL2}	Min/Max limits for CKT					
	A	B	C	D	E	F
	-075/-250	-030/-300	-095/-210	-160/-400	-135/-370	-160/-400

I _{IL4}	Min/Max limits for CKT					
	A	B	C	D	E	F
	-150/-500 for tests 31, 32, 35, 36	-060/-700	-160/-400 for tests 31, 32, 35, 36	-320/-800	-120/-360 for tests 31, 32, 35, 36	-320/-800
	-200/-800 for tests 33, 34		-350/-760 for tests 33, 34		-350/-760 for tests 33, 34	

I _{IL7}	Min/Max limits for CKT					
	A	B	C	D	E	F
	-200/-800	-060/-700	-350/-760	-560/-1.600	-280/-760	-560/-1.600

4/  2.5 V minimum/5.5 V maximum

5/ Input voltages shown are A = 2.0 volts minimum and B = 0.7 volts maximum.

6/ Tests shall be performed in sequence, attributes data only.

7/ Output voltages shall be H ≥ 1.5 V and L < 1.5 V.

8/ f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements (see 5.1).

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND	Ground zero voltage potential
I _{IN}	Current flowing into an input terminal
V _{IC}	Input clamp voltage
V _{IN}	Voltage level at an input terminal

MIL-M-38510/301F

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming shall not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	54LS73
02	54LS74A
03	54LS112
04	54LS113
05	54LS114
06	54LS174
07	54LS175
08	54LS107
09	54LS109
10	54LS76A

6.8 Manufacturers' designation. Manufacturers' circuits, which form a part of this specification, are designated as shown in table IV herein.

TABLE IV. Manufacturers' designation.

Manufacturers							
Device type	Texas Instruments Inc.	Signetics Corporation	National Semiconductor Corp	Raytheon Company	Motorola Inc	Fairchild Semiconductor	Advanced Micro Devices
01	A	B	C	D	E	---	---
02	A	B	C	D	E	F	---
03	A	B	C	C	D	E	---
04	A	B	C	C	F	E	D
05	A	---	C	C	D	E	---
06	A	B	C	E	F	G	D
07	A	B	C	E	F	G	D
08	A	B	C	D	E	---	---
09	A	B	C	---	E	F	---
10	A	B	C	C	D	E	---

6.9 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:

DLA - CC

(Project 5962-2038)

Review activities:

Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force - 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at www.dodssp.daps.mil.