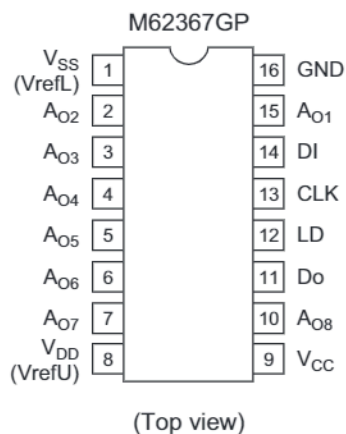


Pin Arrangement

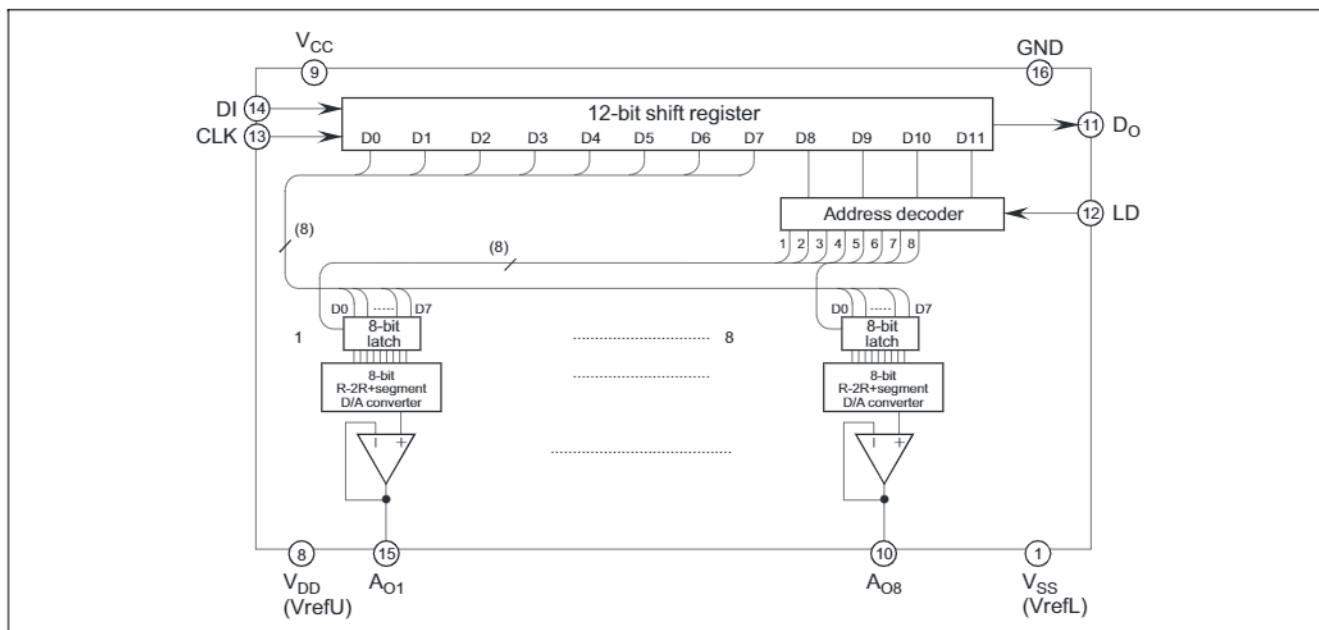


Outline: PLSP0016JA-A (16P2E-A)

Pin Description

Pin No.	Pin Name	Function
14	DI	Serial data input terminal to input 12-bit length serial data
11	Do	Terminal to output MSB data of 12-bit shift register
13	CLK	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
12	LD	When H-level signal is input to this terminal. The value stored in 12-bit shift register is loaded in decoder and D/A converter output register.
15	A ₀₁	8-bit D/A converter output terminal
2	A ₀₂	
3	A ₀₃	
4	A ₀₄	
5	A ₀₅	
6	A ₀₆	
7	A ₀₇	
10	A ₀₈	
9	V _{CC}	Power supply terminal
16	GND	GND terminal
8	V _{DD}	D/A converter upper reference voltage input terminal
1	V _{SS}	D/A converter lower reference voltage input terminal

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	-0.3 to +7.0	V
Upper reference voltage of D/A converter	V_{DD}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_O	-0.3 to $V_{CC} + 0.3$	V
Power dissipation	P_d	150	mW
Operating temperature	T_{opr}	-20 to +85	°C
Storage temperature	T_{stg}	-40 to +125	°C

Electrical Characteristics

<Digital Part>

(V_{CC} , $V_{refU} = +3\text{ V} \pm 10\%$, $V_{CC} \geq V_{refU}$, GND, $V_{refL} = 0\text{ V}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
Circuit current	I_{CC}	—	0.6	2.0	mA	CLK = 1 MHz operation, $V_{CC} = 3\text{ V}$, $I_{AO} = 0\text{ }\mu\text{A}$
Input leak current	I_{ILK}	-10	—	10	μA	$V_{IN} = 0$ to V_{CC}
Input low voltage	V_{IL}	—	—	$0.2 V_{CC}$	V	
Input high voltage	V_{IH}	$0.8 V_{CC}$	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.5\text{ mA}$
Output high voltage	V_{OH}	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$

<Analog Part>

(V_{CC} , $V_{refU} = +3\text{ V} \pm 10\%$, $V_{CC} \geq V_{refU}$, GND, $V_{refL} = 0\text{ V}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

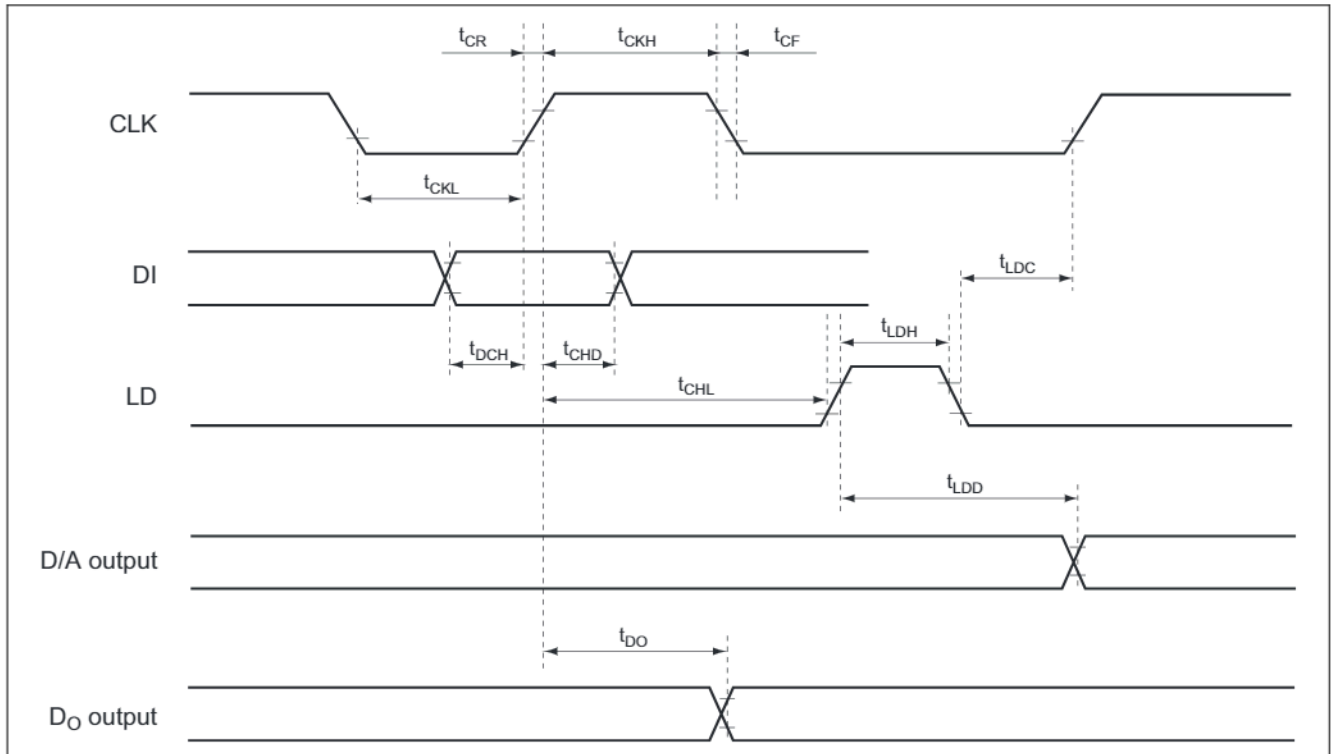
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Current dissipation	I_{refU}	—	0.6	1.5	mA	$V_{refU} = 3\text{ V}$, $V_{refL} = 0\text{ V}$ Data condition: at maximum current
D/A converter upper reference voltage range	V_{refU}	$0.7 V_{CC}$	—	V_{CC}	V	Reference voltage cannot always be set to any value in this range, because it is restricted to the buffer amplifier output voltage range.
D/A converter lower reference voltage range	V_{refL}	GND	—	$0.3 V_{CC}$	V	
Buffer amplifier output driver voltage range	V_{AO}	0.1	—	$V_{CC} - 0.1$	V	$I_{AO} = \pm 100\text{ }\mu\text{A}$
		0.2	—	$V_{CC} - 0.2$	V	$I_{AO} = +500\text{ }\mu\text{A}$ $-200\text{ }\mu\text{A}$
Buffer amplifier output voltage range	I_{AO}	-0.3	—	1	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Differential nonlinearity error	S_{DL}	-1.0	—	1.0	LSB	$V_{CC} = 2.760\text{ V}$ $V_{refU} = 2.610\text{ V}$
Nonlinearity error	S_L	-1.5	—	1.5	LSB	$V_{refL} = 0.050\text{ V}$ (10 mV/LSB)
Zero code error	S_{ZERO}	-2	—	2	LSB	Without load ($I_{AO} = \pm 0$)
Full scale error	S_{FULL}	-2	—	2	LSB	
Output capacitive load	C_O	—	—	0.1	μF	
Buffer amplifier output impedance	R_O	—	5	—	Ω	

AC Characteristics

(V_{CC} , $V_{refU} = +3\text{ V} \pm 10\%$, $V_{CC} \geq V_{refU}$, GND , $V_{refL} = 0\text{ V}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	30	—	—	ns	
Data hold time	t_{CHD}	60	—	—	ns	
LD setup time	t_{CHL}	200	—	—	ns	
LD hold time	t_{LDC}	100	—	—	ns	
LD "H" pulse duration time	t_{LDH}	100	—	—	ns	
Data output delay time	t_{DO}	70	—	350	ns	$C_L = 100\text{ pF}$
D/A output setting time	t_{LDD}	—	—	300	μs	$C_L \geq 100\text{ pF}$, $V_{AO}: 0.1 \leftrightarrow 2.6\text{ V}$ This time until the output becomes the final value of 1/2 LSB

Timing Chart



Digital Data Format



DAC Data

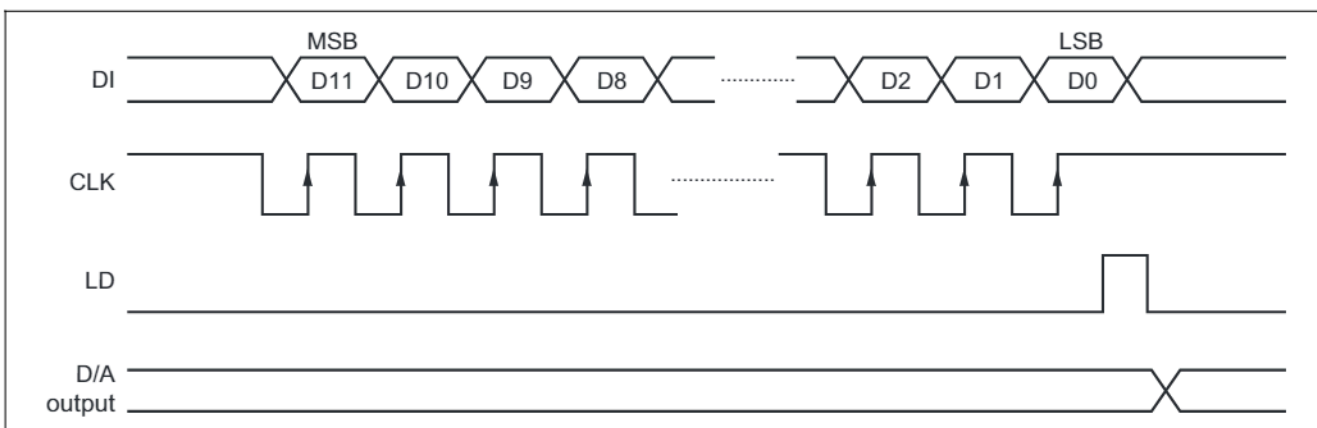
D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

Note: $V_{refU} = V_{DD}$, $V_{refL} = V_{SS}$

DAC Select Data

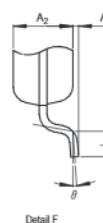
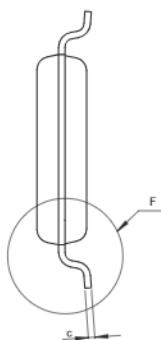
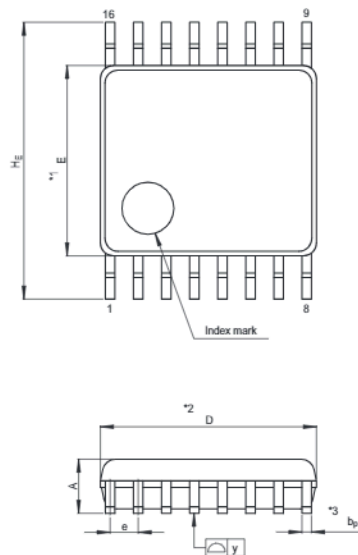
D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	A ₀₁ selection
0	0	1	0	A ₀₂ selection
0	0	1	1	A ₀₃ selection
0	1	0	0	A ₀₄ selection
0	1	0	1	A ₀₅ selection
0	1	1	0	A ₀₆ selection
0	1	1	1	A ₀₇ selection
1	0	0	0	A ₀₈ selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP16-4.4x5-0.65	PLSP0016JA-A	16P2E-A	0.06g



NOTE)

1. DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.3	4.4	4.5
A ₂	—	1.15	—
A	—	—	1.45
A ₁	0	0.1	0.2
b _p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H _E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

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Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510