Rochester Electronics®

Datasheet

PART NUMBER

DM54LS168JB-ROCS

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

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National Semiconductor

June 1989

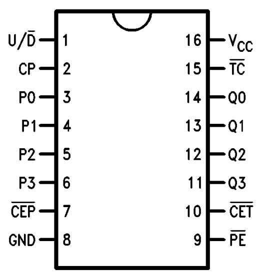
54LS168 Synchronous Bi-Directional BCD Decade Counter

General Description

The 54LS168 is a fully synchronous 4-state up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. It counts in the BCD (8421) sequence and all state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

Connection Diagram

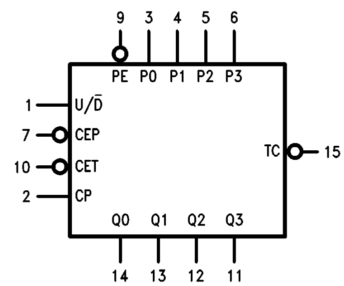
Dual-In-Line Package



TL/F/10207–1

Order Number 54LS168DMQB, 54LS168FMQB or 54LS168LMQB
See NS Package Number E20A, J16A or W16A

Logic Symbol



TL/F/10207–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$\overline{CET}$	Count Enable Trickle Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P0–P3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
U/$\overline{D}$	Up-Down Count Control Input
Q0–Q3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output (Active LOW)

  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS168			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			4	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, $\overline{CEP}$ or $\overline{CET}$ to CP	15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, $\overline{CEP}$ or $\overline{CET}$ to CP	5 5			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $U/\overline{D}$ to CP	25 25			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $U/\overline{D}$ to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10.0V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	μA
			$\overline{CET}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Data	−0.5		−400	μA
			CP, $\overline{PE}$, U/$\overline{D}$, $\overline{CEP}$	−30		−400	
			$\overline{CET}$	−60		−800	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				34	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	54LS168		Units
		C_L = 15 pF		
		Min	Max	
f_{Max}	Maximum Clock Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		20 20	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$		15 20	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$		25 25	ns

Functional Description

The 'LS168 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P0–P3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 9 in the COUNT UP mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'LS168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equation below).

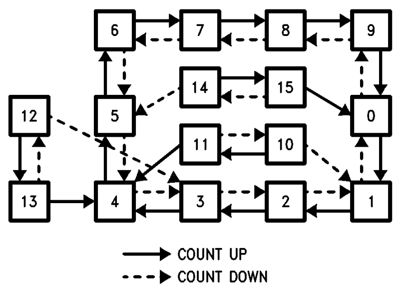
1. Count Enable $= \overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$
2. Up: $\overline{TC} = Q0 \bullet Q3 \bullet (U/\overline{D}) \bullet \overline{CET}$
3. Down: $\overline{TC} = \overline{Q0} \bullet \overline{Q1} \bullet \overline{Q2} \bullet \overline{Q3} \bullet \overline{(U/\overline{D})} \bullet \overline{CET}$

'LS168 Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

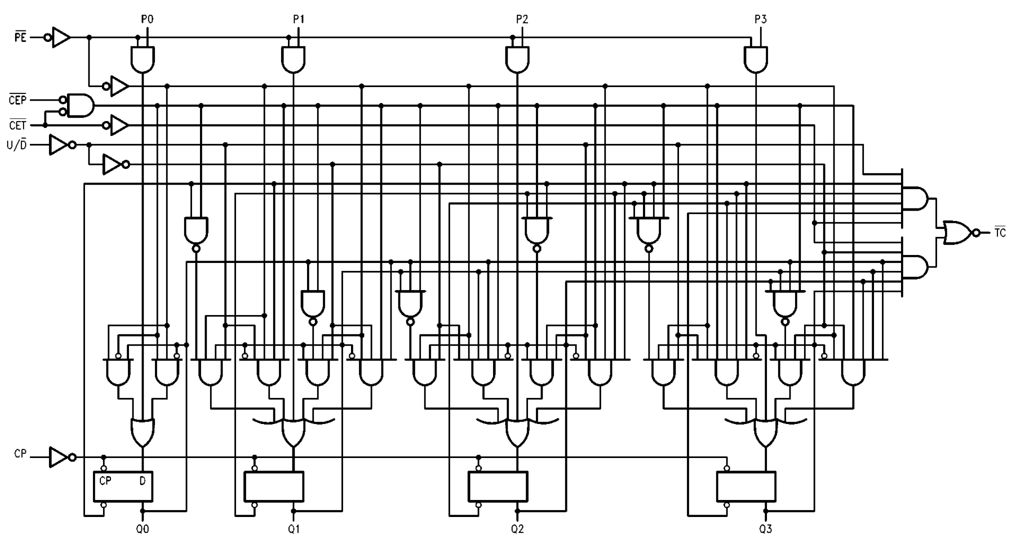
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



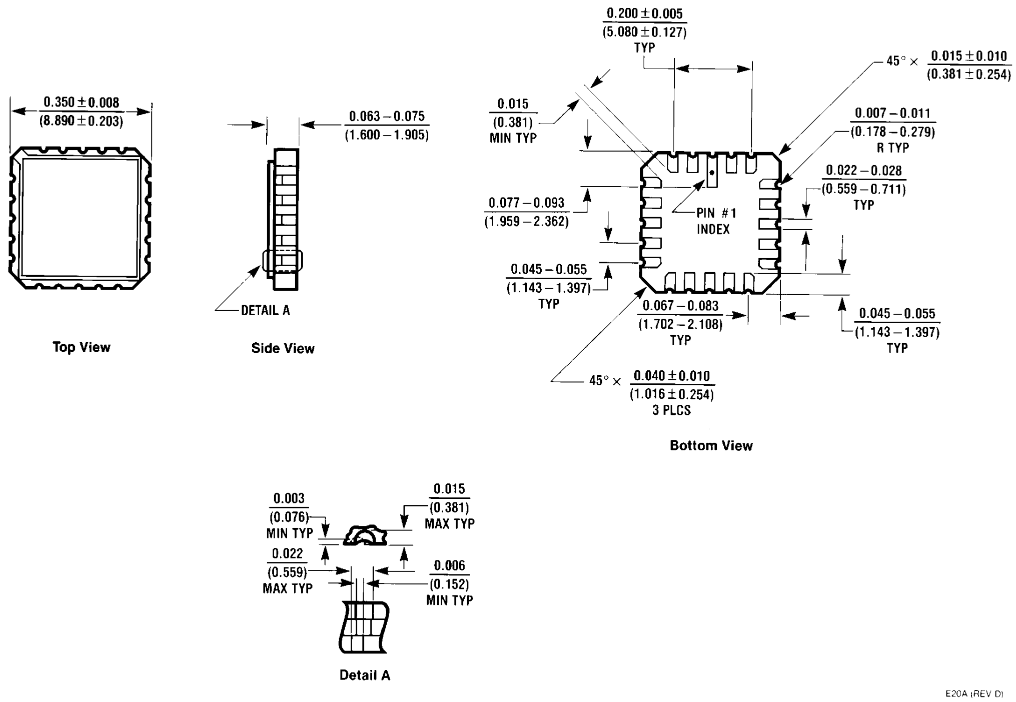
TL/F/10207–3

Logic Diagram

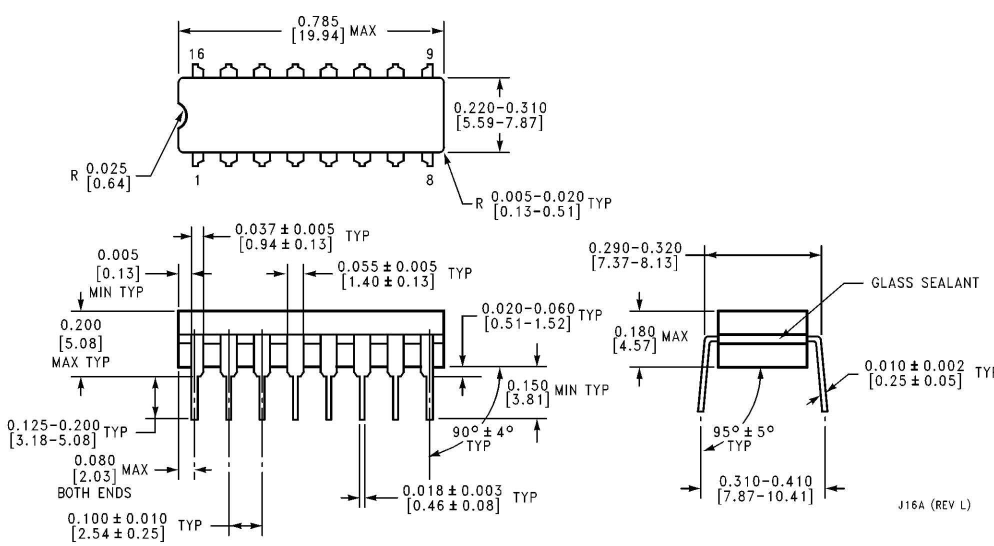


TL/F/10207–4

Physical Dimensions inches (millimeters)

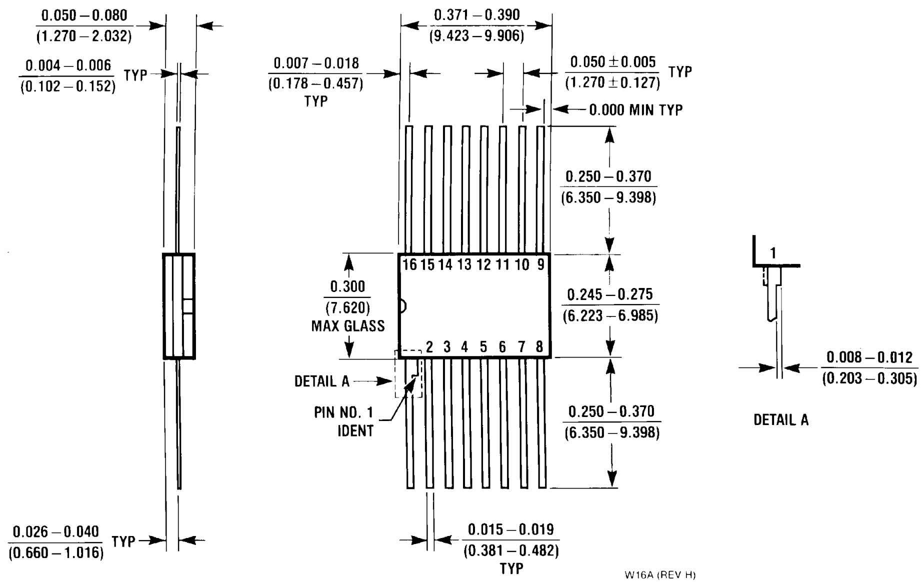


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS168LMQB
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS168DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS168FMQB
NS Package Number W16A

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